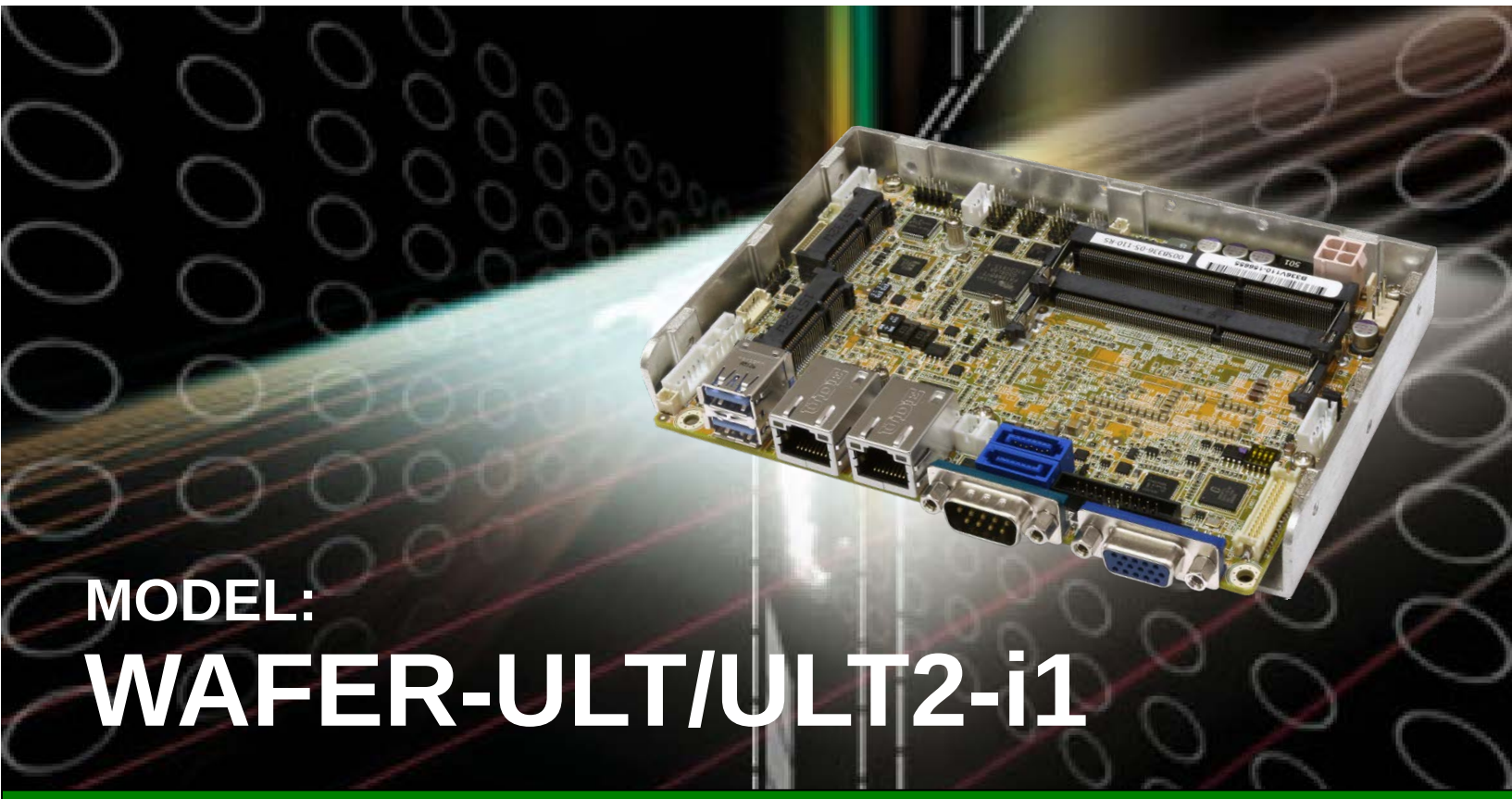
IEI Integration Corp.



MODEL:

WAFER-ULT/ULT2-i1

3.5” SBC with Intel® 4th/5th Generation Mobile Core™ i7/i5/i3 or Celeron® ULT SoC, Dual PCIe GbE, VGA, LVDS, iDP, USB 3.0, SATA 6Gb/s, PCIe Mini, iRIS-1010, HD Audio and RoHS

User Manual

Rev. 1.12 – September 28, 2018

RoHS Lead Free

Revision

Date	Version	Changes
September 28, 2018	1.12	Modified Section 4.8: Motherboard Installation
July 28, 2016	1.11	Added Figure 3-30: LAN Connector
August 31, 2015	1.10	Updated for R11 version
July 9, 2014	1.00	Initial release

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Manual Conventions

WARNING

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.

CAUTION

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.

NOTE

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

HOT SURFACE

This symbol indicates a hot surface that should not be touched without taking care.

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BIOS Menus

Chapter

1

Introduction

1.1 Introduction

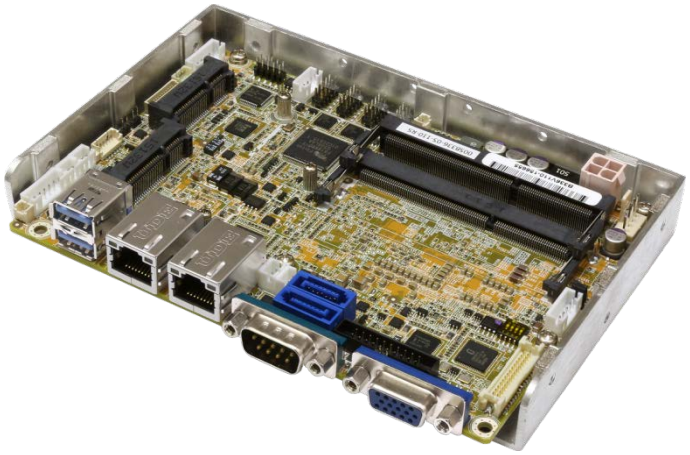


Figure 1-1: WAFER-ULT/ULT2-i1

The WAFER-ULT/ULT2-i1 3.5" SBC is an Intel® 4th/5th generation mobile ULT SoC platform that supports two 1600/1333 MHz dual-channel DDR3L SO-DIMMs up to 16 GB. The WAFER-ULT/ULT2-i1 provides two GbE interfaces through the Intel® I218-LM (with Intel® AMT 9.0 support) and the Intel® I210-AT GbE controllers. In addition, the WAFER-ULT/ULT2-i1 includes VGA, LVDS and iDP interfaces for triple independent display. Two USB 3.0 on the rear panel, two USB 2.0 by pin header, two SATA 6Gb/s, three RS-232, one RS-422/485, one PCIe Mini card slot and one audio connector provide flexible expansion options.

1.2 Benefits

Some of the WAFER-ULT/ULT2-i1 motherboard benefits include:

- Wide range temperature support
- Triple independent display support
- Heat spreader for thermal solution

1.3 Model Variations

The model variations of the WAFER-ULT/ULT2-i1 are listed below.

Model	On-board SoC
Intel® 5th Generation Mobile ULT On-Board SoC	
WAFER-ULT2-i1-i7-R11	Intel® Core™ i7-5650U (2.2 GHz, dual-core, 4 MB cache, TDP=15W)
WAFER-ULT2-i1-i5-R11	Intel® Core™ i5-5350U (1.8 GHz, dual-core, 3 MB cache, TDP=15W)
WAFER-ULT2-i1-i3-R11	Intel® Core™ i3-5010U (2.1 GHz, dual-core, 3 MB cache, TDP=15W)
WAFER-ULT2-i1-C-R11	Intel® Celeron® 3765U (1.9 GHz, dual-core, 2 MB cache, TDP=15W)
Intel® 4th Generation Mobile ULT On-Board SoC	
WAFER-ULT-i1-i7-R11	Intel® Core™ i7-4650U (1.7 GHz, dual-core, 4 MB cache, TDP=15W)
WAFER-ULT-i1-i5-R11	Intel® Core™ i5-4300U (1.9 GHz, dual-core, 3 MB cache, TDP=15W)
WAFER-ULT-i1-i3-R11	Intel® Core™ i3-4010U (1.7 GHz, dual-core, 3 MB cache, TDP=15W)
WAFER-ULT-i1-C-R11	Intel® Celeron® 2980U (1.6 GHz, dual-core, 2 MB cache, TDP=15W)

Table 1-1: Model Variations

1.4 Features

Some of the WAFER-ULT/ULT2-i1 motherboard features are listed below:

- 3.5” form factor
- Intel® 4th/5th generation mobile ULT SoC
- Two 204-pin 1600/1333 MHz dual-channel DDR3L SO-DIMMs support up to 16 GB
- Triple independent display by VGA, LVDS and iDP interfaces
- 18/24-bit dual-channel LVDS for high resolution panel
- Supports IPMI 2.0 via the optional iRIS-1010 module
- Two Intel® PCIe GbE connectors (LAN1 with Intel® AMT 9.0 support)
- One PCIe Mini card slot with mSATA support
- High Definition Audio
- RoHS compliant

1.5 Connectors

The connectors on the WAFER-ULT/ULT2-i1 are shown in the figure below.

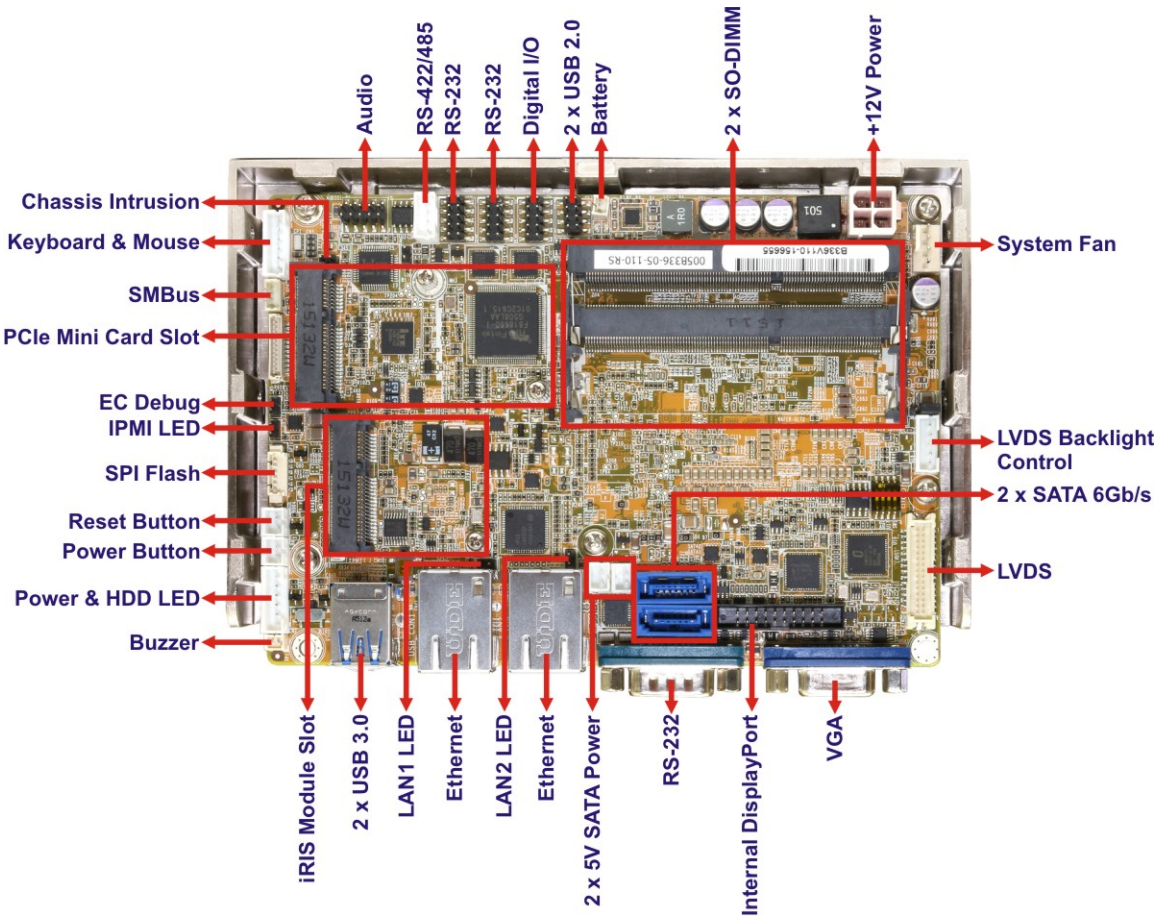


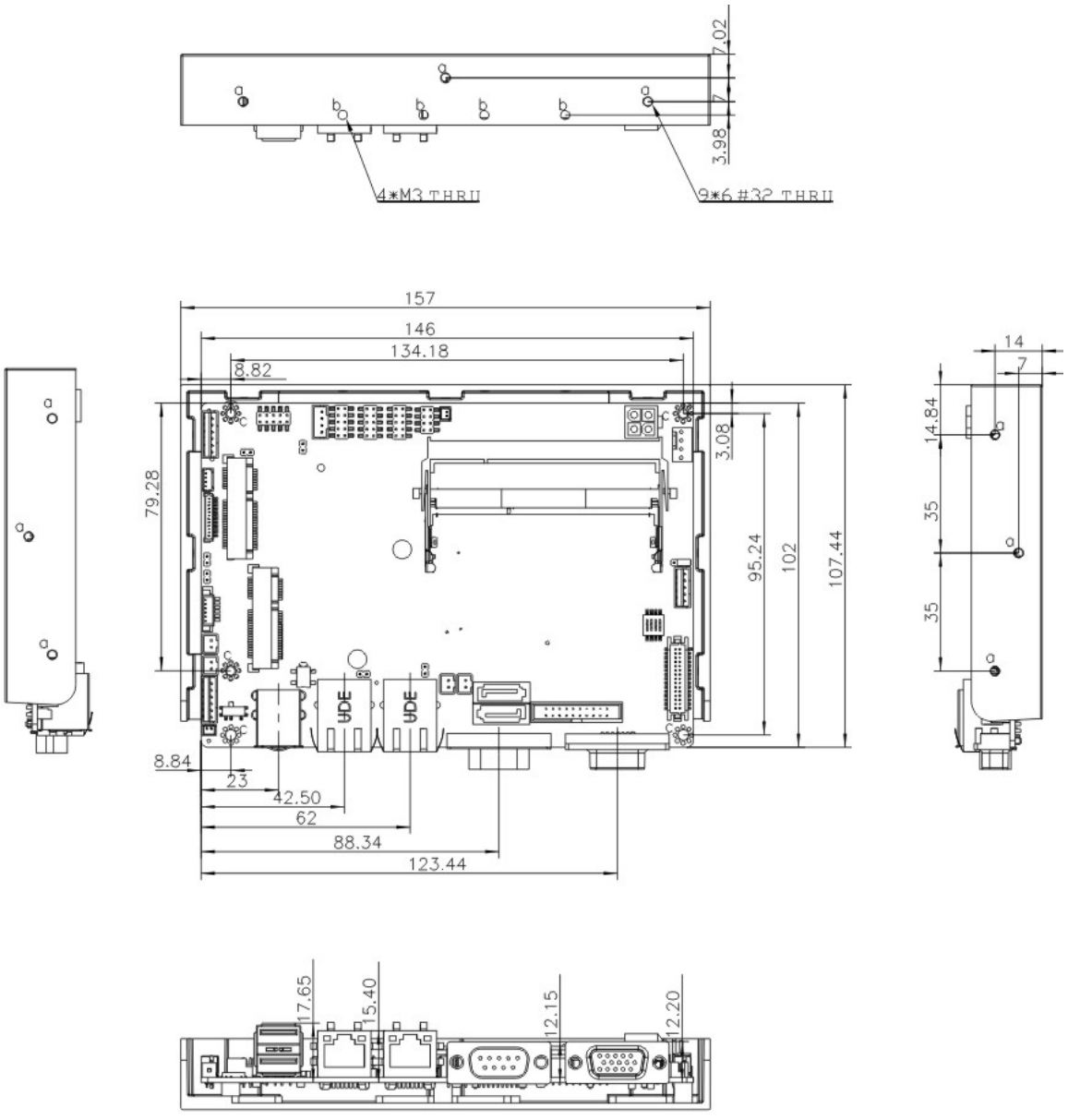
Figure 1-2: Connectors

WARNING:

The heat spreader installed on the WAFER-ULT/ULT2-i1 can only serve as a heat conductor, which needs additional heat dissipation mechanism to achieve suitable thermal condition. DO NOT put the WAFER-ULT/ULT2-i1 with the heat spreader directly on a surface that cannot dissipate system heat.

1.6 Dimensions

The main dimensions of the WAFER-ULT/ULT2-i1 are shown in the diagram below.



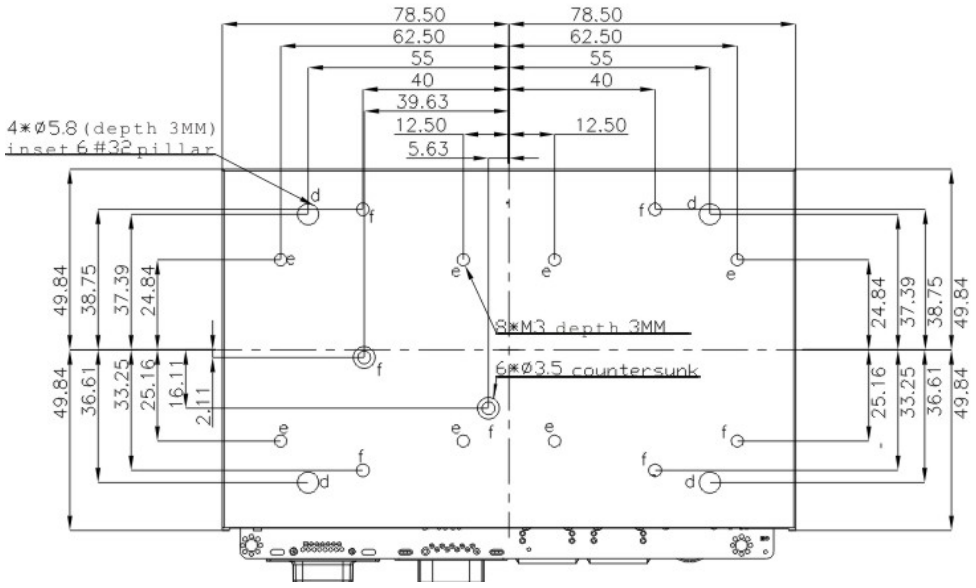


Figure 1-3: WAFER-ULT/ULT2-i1 Dimensions (mm)

1.7 Data Flow

Figure 1-4 shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

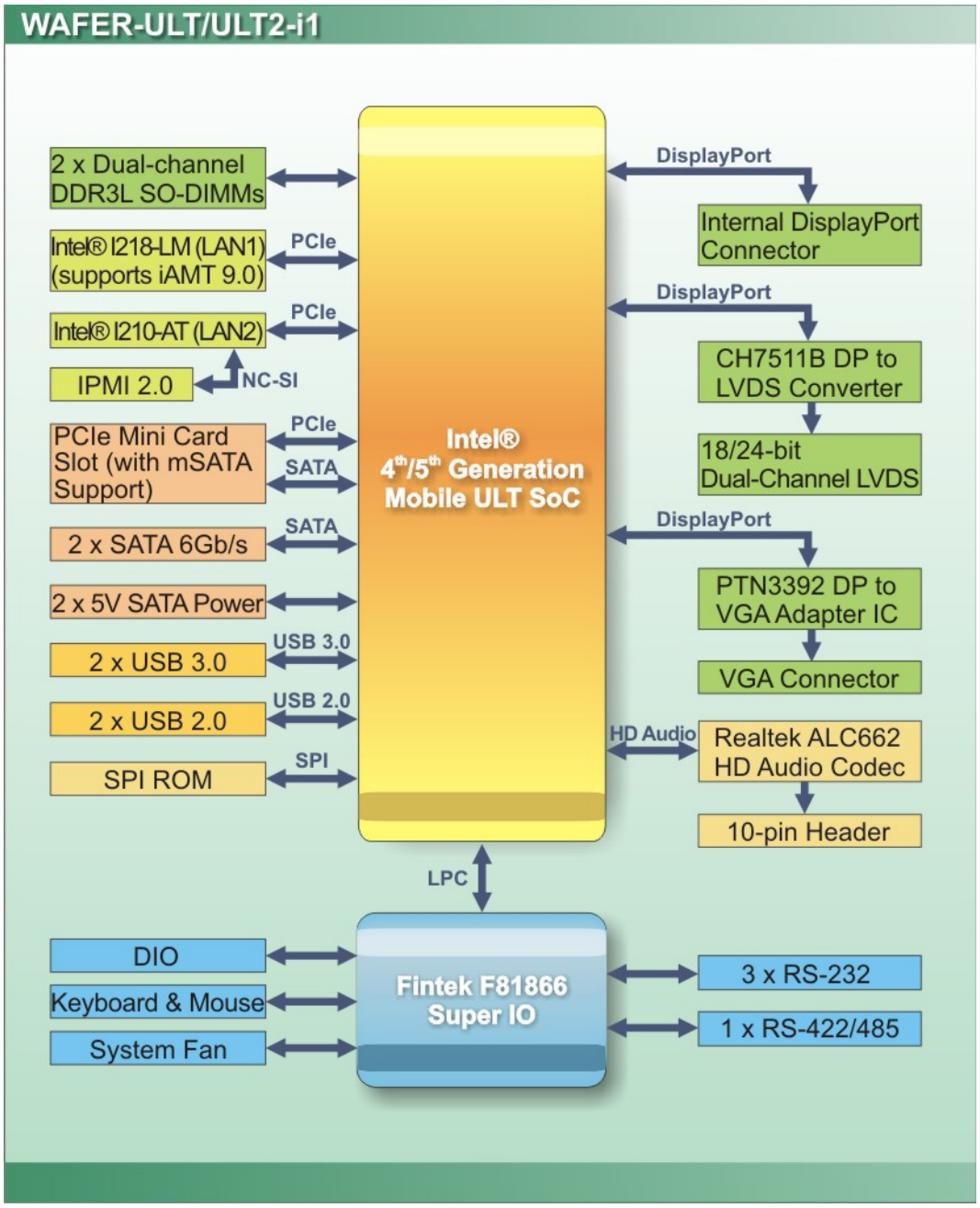


Figure 1-4: Data Flow Diagram

1.8 Technical Specifications

The WAFER-ULT/ULT2-i1 technical specifications are listed below.

Specifications/Model	WAFER-ULT/ULT2-i1
Form Factor	3.5”
SoC	**Intel® 5th generation mobile ULT on-board SoC:** Intel® Core™ i7-5650U (2.2 GHz, dual-core, 4 MB cache, TDP=15W) Intel® Core™ i5-5350U (1.8 GHz, dual-core, 3 MB cache, TDP=15W) Intel® Core™ i3-5010U (2.1 GHz, dual-core, 3 MB cache, TDP=15W) Intel® Celeron® 3765U (1.9 GHz, dual-core, 2 MB cache, TDP=15W) **Intel® 4th generation mobile ULT on-board SoC:** Intel® Core™ i7-4650U (1.7 GHz, dual-core, 4 MB cache, TDP=15W) Intel® Core™ i5-4300U (1.9 GHz, dual-core, 3 MB cache, TDP=15W) Intel® Core™ i3-4010U (1.7 GHz, dual-core, 3 MB cache, TDP=15W) Intel® Celeron® 2980U (1.6 GHz, dual-core, 2 MB cache, TDP=15W)
Memory	Two 204-pin 1600/1333 MHz dual-channel unbuffered DDR3L SDRAM SO-DIMMs supported (up to 16 GB)
Graphics Engine	Intel® HD Graphics Gen 8 supports DirectX 11.1, OpenCL 1.2 and OpenGL 4.2 (for Intel® 5th generation mobile ULT on-board SoC) Intel® HD Graphics Gen 7.5 supports DirectX 11.1, OpenCL 1.2 and OpenGL 4.2 (for Intel® 4th generation mobile ULT on-board SoC) Full MPEG2, VC1, AVC decode
Display Output	Triple independent display support One VGA (up to 2560 x 1600, 60 Hz) One 18/24-bit dual-channel LVDS by CH7511B DP to LVDS converter (up to 1920 x 1200, 60 Hz) One iDP interface for HDMI, LVDS, VGA, DVI and DisplayPort (up to 3840 x 2160, 60 Hz)
Ethernet Controllers	**LAN1**: Intel® I218-LM PCIe GbE controller with Intel® AMT 9.0 support **LAN2**: Intel® I210-AT PCIe GbE controller with NC-SI support

Specifications/Model	WAFER-ULT/ULT2-i1
Audio	Realtek ALC662 HD Audio codec One audio connector (10-pin header)
Super I/O Controller	Fintek F81866
Watchdog Timer	Software programmable, supports 1~255 sec. system reset
BIOS	UEFI BIOS
Expansion	One full-size/half-size PCIe Mini card slot with mSATA support
IPMI 2.0	One iRIS-1010 module slot
IPMI LED	One 2-pin header for IPMI LED
Chassis Intrusion	One 2-pin header
Digital I/O	8-bit digital I/O
Fan Connector	One system fan connector (4-pin wafer)
Front Panel	One power & HDD LED connector (6-pin wafer) One power button connector (2-pin wafer) One reset button connector (2-pin wafer)
Keyboard and Mouse	One 6-pin wafer connector for PS/2 keyboard and mouse
LAN LEDs	Two 2-pin headers for LAN1 LED and LAN2 LED (link signal)
Serial ATA	Two SATA 6Gb/s connectors Two 5V SATA power connectors
Serial Ports	One external RS-232 serial port Two RS-232 serial ports via internal pin headers One RS-422/485 via internal 4-pin wafer connector
SMBus	One 4-pin wafer connector
USB	Two USB 3.0 ports on rear panel Two USB 2.0 ports by pin header
Power Supply	12V only DC input AT/ATX power mode support One Internal 4-pin (2x2) power connector

Specifications/Model	WAFER-ULT/ULT2-i1
Power Consumption	+12V@2.72A (Intel® Core™ i5-4300U on-board SoC with two 8 GB 1600 MHz DDR3L SO-DIMMs)
Operating Temperature	-10ºC ~ 60ºC
Storage Temperature	-20ºC ~ 70ºC
Operating Humidity	5% ~ 95% (non-condensing)
Dimensions	146 mm x 102 mm
Weight (GW/NW)	600 g/250 g

Table 1-2: WAFER-ULT/ULT2-i1 Specifications

Chapter

2

Packing List

2.1 Anti-static Precautions

WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- ***Wear an anti-static wristband***: Wearing an anti-static wristband can prevent electrostatic discharge.
- ***Self-grounding***: Touch a grounded conductor every few minutes to discharge any excess static buildup.
- ***Use an anti-static pad***: When configuring any circuit board, place it on an anti-static mat.
- ***Only handle the edges of the PCB***: Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

2.2 Unpacking Precautions

When the WAFER-ULT/ULT2-i1 is unpacked, please do the following:

- Follow the anti-static guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

2.3 Packing List

NOTE:

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the WAFER-ULT/ULT2-i1 was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

The WAFER-ULT/ULT2-i1 is shipped with the following components:

Quantity	Item and Part Number	Image
1	WAFER-ULT/ULT2-i1 SBC with heat spreader	
2	SATA signal and power cable	
1	Audio cable	
1	Dual-port USB 2.0 cable	
1	Power cable	

Table 2-1: Packing List

2.4 Optional Items

These optional items are available.

Item and Part Number	Image
iRIS-1010 module, IPMI 2.0 adapter card with AST1010 BMC chip (without KVM over IP function) for PCIe Mini socket interface (**P/N**: iRIS-1010-R10)	
RS-232 cable (**P/N:** 19800-000300-200-RS)	
RS-422/485 cable (200 mm) (**P/N**: 32205-003800-300-RS)	
PS/2 keyboard and mouse Y cable (**P/N**: 32000-023800-RS)	
DisplayPort to 24-bit dual-channel LVDS converter board for IEI iDP connector (**P/N**: DP-LVDS-R10)	
DisplayPort to HDMI converter board for IEI iDP connector (**P/N**: DP-HDMI-R10)	
DisplayPort to VGA converter board for IEI iDP connector (**P/N**: DP-VGA-R10)	
DisplayPort to DVI-D converter board for IEI iDP connector (**P/N**: DP-DVI-R10)	

Item and Part Number	Image
DisplayPort to DisplayPort converter board for IEI iDP connector (**P/N**: DP-DP-R10)	

Table 2-2: Optional Items

Chapter

3

Connectors

3.1 Peripheral Interface Connectors

This chapter details all the peripheral interface connectors.

3.1.1 WAFER-ULT/ULT2-i1 Layout

The figure below shows all the peripheral interface connectors.

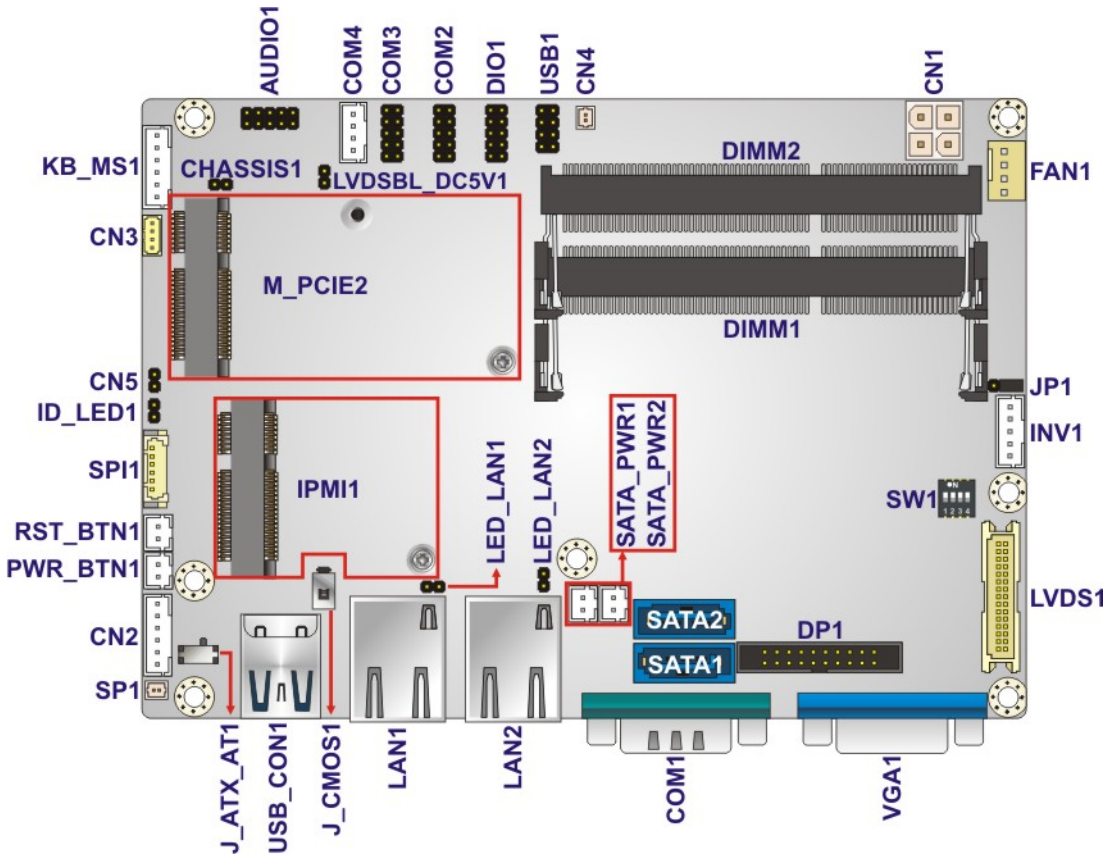


Figure 3-1: Peripheral Interface Connectors

3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
+12V power connector	4-pin Molex power connector	CN1
5 V SATA power connectors	2-pin wafer	SATA_PWR1, SATA_PWR2
Audio connector	10-pin header	AUDIO1
Battery connector	2-pin wafer	CN4
Buzzer connector	2-pin wafer	SP1
Chassis intrusion connector	2-pin header	CHASSIS1
Digital I/O connector	10-pin header	DIO1
EC debug connector	2-pin header	CN5
Internal DisplayPort connector	20-pin box header	DP1
IPMI LED connector	2-pin header	ID_LED1
iRIS module slot	iRIS module slot	IPMI1
Keyboard and mouse connector	6-pin wafer	KB_MS1
LAN1 LED connector	2-pin header	LED_LAN1
LAN2 LED connector	2-pin header	LED_LAN2
LVDS backlight control connector	5-pin wafer	INV1
LVDS connector	30-pin crimp	LVDS1
PCIe Mini card slot	PCIe Mini card slot	M_PCIE2
Power and HDD LED connector	6-pin wafer	CN2
Power button connector	2-pin wafer	PWR_BTN1
Reset button connector	2-pin wafer	RST_BTN1
SATA 6Gb/s connectors	7-pin SATA connector	SATA1, SATA2
Serial port, RS-232	10-pin header	COM2, COM3

Connector	Type	Label
Serial port, RS-422/485	4-pin wafer	COM4
SMBus connector	4-pin wafer	CN3
SO-DIMM slots	204-pin DDR3L SO-DIMM slot	DIMM1, DIMM2
SPI flash connector	6-pin wafer	SPI1
System fan connector	4-pin wafer	FAN1
USB 2.0 connector	8-pin header	USB1

Table 3-1: Peripheral Interface Connectors

3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
Ethernet connectors	RJ-45	LAN1, LAN2
USB 3.0 ports	Dual USB 3.0 port	USB_CON1
RS-232 serial port	Male DB-9	COM1
VGA connector	15-pin female	VGA1

Table 3-2: External Peripheral Connectors

3.2 Internal Peripheral Connectors

Internal peripheral connectors are found on the motherboard and are only accessible when the motherboard is outside of the chassis. This section has complete descriptions of all the internal peripheral connectors on the WAFER-ULT/ULT2-i1.

3.2.1 +12V Power Connector

CN Label:	**CN1**
CN Type:	4-pin Molex power connector, p=4.2 mm
CN Location:	See **Figure 3-2**
CN Pinouts:	See **Table 3-3**

The power connector is connected to an external power supply and supports +12V power input. Power is provided to the system, from the power supply through this connector.

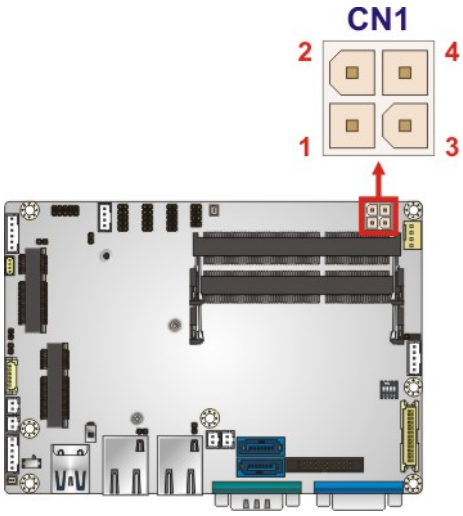


Figure 3-2: Power Connector Location

Pin	Description	Pin	Description
1	GND	2	GND
3	+12V	4	+12V

Table 3-3: Power Connector Pinouts

3.2.2 5 V SATA Power Connectors

CN Label: **SATA_PWR1, SATA_PWR2**

CN Type: 2-pin wafer, p=2 mm

CN Location: See **Figure 3-3**

CN Pinouts: See **Table 3-4**

Use the 5 V SATA power connectors to connect to SATA device power connections.

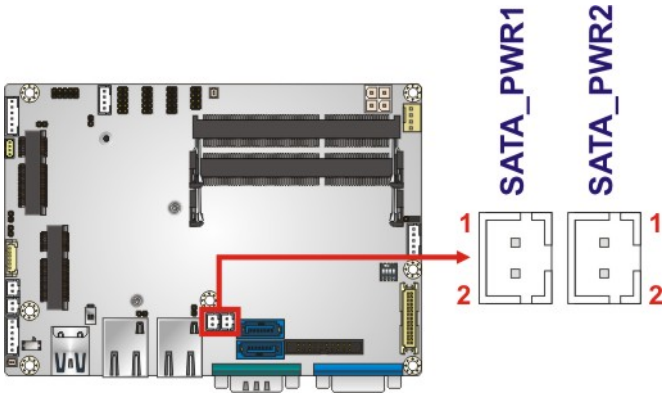


Figure 3-3: 5 V SATA Power Connector Locations

Pin	Description
1	+5V
2	GND

Table 3-4: 5 V SATA Power Connector Pinouts

3.2.3 Audio Connector

CN Label: **AUDIO1**

CN Type: 10-pin header, p=2 mm

CN Location: See **Figure 3-4**

CN Pinouts: See **Table 3-5**

This connector connects to speakers, a microphone and an audio input.

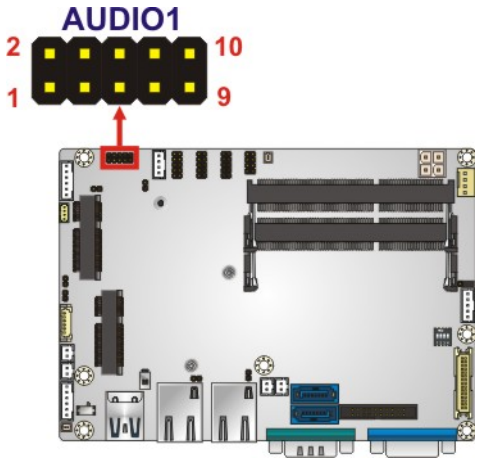


Figure 3-4: Audio Connector Location

Pin	Description	Pin	Description
1	LINEOUT1R	2	LINE1_R
3	AUD_GND	4	AUD_GND
5	LINEOUT1L	6	LINE1_L
7	AUD_GND	8	AUD_GND
9	FMIC1_R	10	FMIC1_L

Table 3-5: Audio Connector Pinouts

3.2.4 Battery Connector

CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

CN Label:	**CN4**
CN Type:	2-pin wafer, p=1.25 mm
CN Location:	See **Figure 3-5**
CN Pinouts:	See **Table 3-6**

This is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.

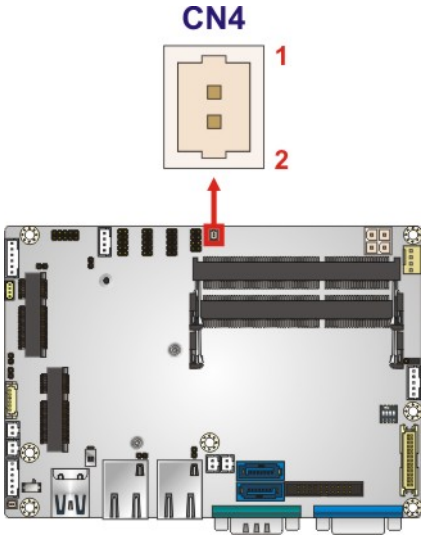


Figure 3-5: Battery Connector Location

Pin	Description
1	VBATT
2	GND

Table 3-6: Battery Connector Pinouts

3.2.5 Buzzer Connector

CN Label: **SP1**

CN Type: 2-pin wafer, p=1.25 mm

CN Location: See **Figure 3-6**

CN Pinouts: See **Table 3-7**

This is connected to the buzzer cable.

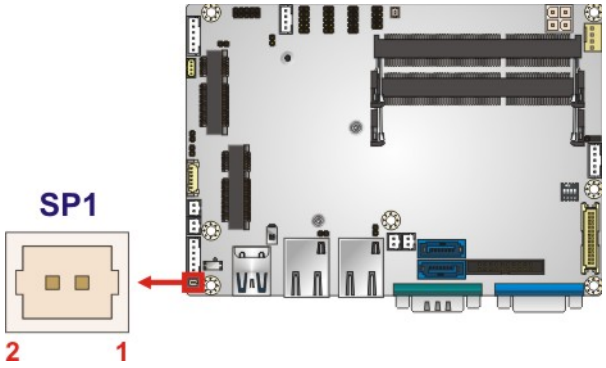


Figure 3-6: Buzzer Connector Location

Pin	Description
1	+V5S
2	GND

Table 3-7: Buzzer Connector Pinouts

3.2.6 Chassis Intrusion Connector

CN Label: **CHASSIS1**

CN Type: 2-pin header, p=2 mm

CN Location: See **Figure 3-7**

CN Pinouts: See **Table 3-8**

The chassis intrusion connector is for a chassis intrusion detection sensor or switch that detects if a chassis component is removed or replaced.

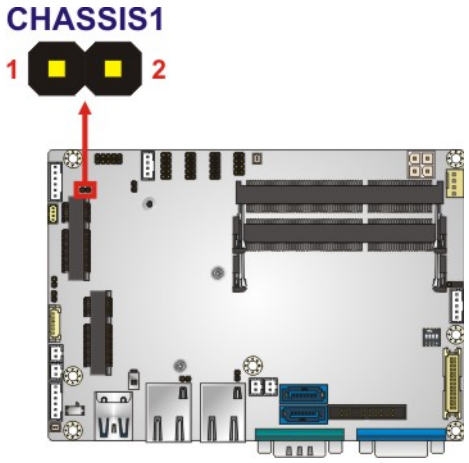


Figure 3-7: Chassis Intrusion Connector Location

Pin	Description
1	+3.3VSB
2	CHASSIS OPEN

Table 3-8: Chassis Intrusion Connector Pinouts

3.2.7 Digital I/O Connector

CN Label: **DIO1**

CN Type: 10-pin header, p=2 mm

CN Location: See **Figure 3-8**

CN Pinouts: See **Table 3-9**

The digital I/O connector provides programmable input and output for external devices. The digital I/O provides 4-bit output and 4-bit input.

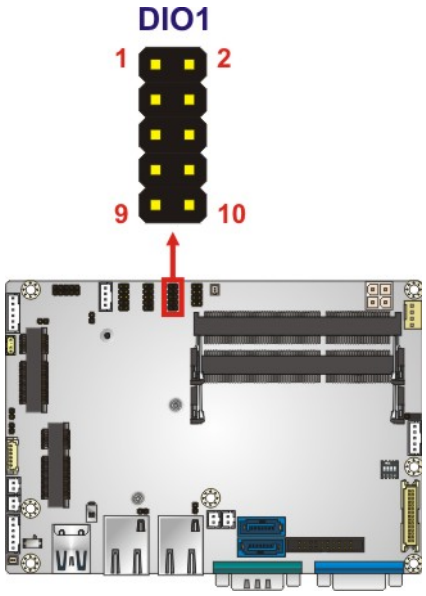


Figure 3-8: Digital I/O Connector Location

Pin	Description	Pin	Description
1	GND	2	VCC
3	Output 3	4	Output 2
5	Output 1	6	Output 0

Pin	Description	Pin	Description
7	Input 3	8	Input 2
9	Input 1	10	Input 0

Table 3-9: Digital I/O Connector Pinouts

3.2.8 EC Debug Connector

CN Label: **CN5**

CN Type: 2-pin header, p=2 mm

CN Location: See **Figure 3-9**

CN Pinouts: See **Table 3-10**

The chassis intrusion connector is for a chassis intrusion detection sensor or switch that detects if a chassis component is removed or replaced.

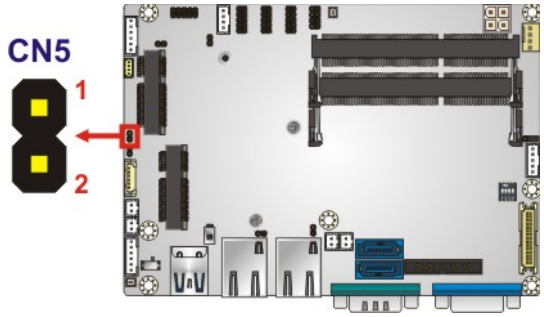


Figure 3-9: EC Debug Connector Location

Pin	Description
1	EC_SMBCLK
2	EC_SMBDAT

Table 3-10: EC Debug Connector Pinouts

3.2.9 Internal DisplayPort Connector

CN Label: **DP1**

CN Type: 20-pin box header, p=2 mm

CN Location: See **Figure 3-10**

CN Pinouts: See **Table 3-11**

The DisplayPort connector supports HDMI, LVDS, VGA, DVI and DisplayPort graphics interfaces with up to 3840x2160 resolution.

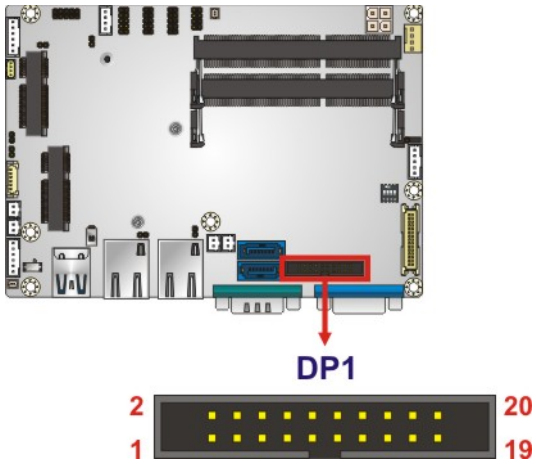


Figure 3-10: Internal DisplayPort Connector Location

Pin	Description	Pin	Description
1	+5V	11	AUXP
2	LANE1N	12	AUXN
3	LANE1P	13	GND
4	GND	14	LANE2P
5	LANE3N	15	LANE2N
6	LANE3P	16	GND
7	GND	17	LANE0P
8	AUX_CTRL_DET_D	18	LANE0N
9	GND	19	+3.3V
10	HPD	20	N/C

Table 3-11: Internal DisplayPort Connector Pinouts

3.2.10 IPMI LED Connector

CN Label: **ID_LED1**

CN Type: 2-pin wafer, p=2 mm

CN Location: See **Figure 3-11**

CN Pinouts: See **Table 3-12**

The IPMI LED connector is used to connect to the IPMI LED indicator on the chassis.

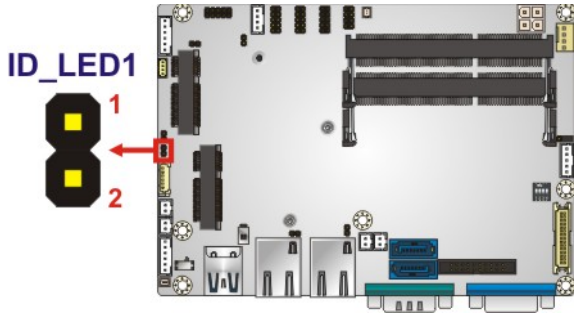


Figure 3-11: IPMI LED Connector Location

Pin	Description
1	ID_LED+
2	ID_LED-

Table 3-12: IPMI LED Connector Pinouts

3.2.11 iRIS Module Slot

CN Label: **IPMI1**

CN Type: iRIS module slot

CN Location: See **Figure 3-12**

The iRIS module slot allows installation of the iRIS-1010 module.

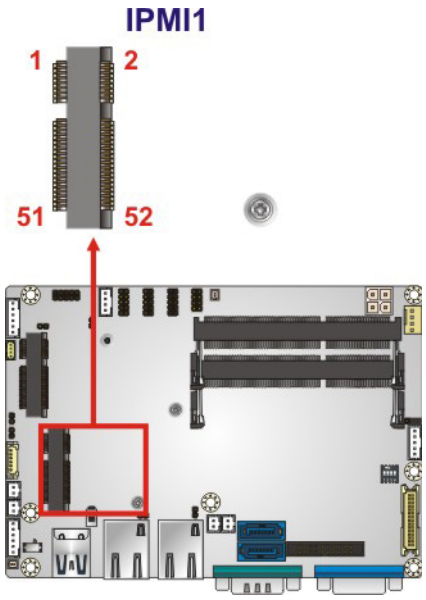


Figure 3-12: iRIS Module Slot Location

WARNING:

The iRIS module slot is designed to install the iRIS-1010 module only. DO NOT install other modules into the iRIS module slot. Doing so may cause damage to the WAFER-ULT/ULT2-i1.

3.2.12 Keyboard and Mouse Connector

CN Label:	**KB_MS1**
CN Type:	6-pin wafer, p=2 mm
CN Location:	See **Figure 3-13**
CN Pinouts:	See **Table 3-13**

The keyboard and mouse connector connects to a PS/2 Y-cable that can be connected to a PS/2 keyboard and mouse.

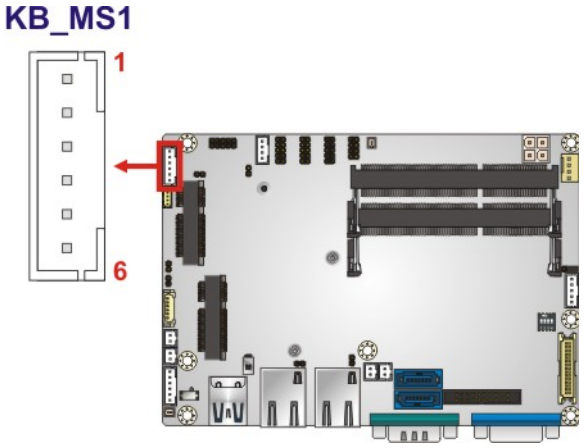


Figure 3-13: Keyboard and Mouse Connector Location

Pin	Description
1	VCC
2	Mouse Data
3	Mouse Clock
4	Keyboard Data
5	Keyboard Clock
6	GND

Table 3-13: Keyboard and Mouse Connector Pinouts

3.2.13 LAN LED Connectors

CN Label: **LED_LAN1, LED_LAN2**

CN Type: 2-pin header, p=2 mm

CN Location: See **Figure 3-14**

CN Pinouts: See **Table 3-14**

The LAN LED connectors are used to connect to the LAN LED indicators on the chassis to indicate users the link activities of the two LAN ports.

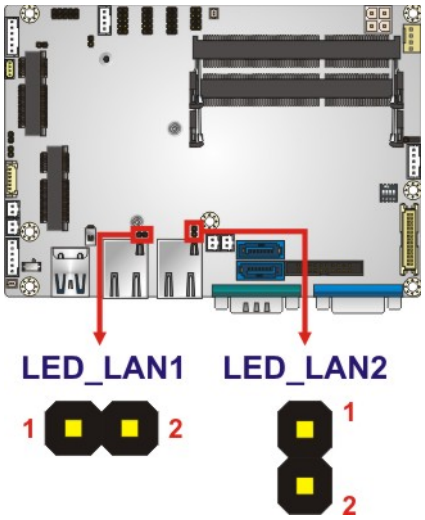


Figure 3-14: LAN LED Connector Locations

Pin	Description
1	+3.3V
2	LAN_LED_LINK#_ACT

Table 3-14: LAN LED Connector Pinouts

3.2.14 LVDS Backlight Control Connector

CN Label: **INV1**

CN Type: 5-pin wafer, p=2 mm

CN Location: See **Figure 3-15**

CN Pinouts: See **Table 3-15**

The backlight control connector provides the backlight on the LCD display connected to the WAFER-ULT/ULT2-i1 with +12V of power.

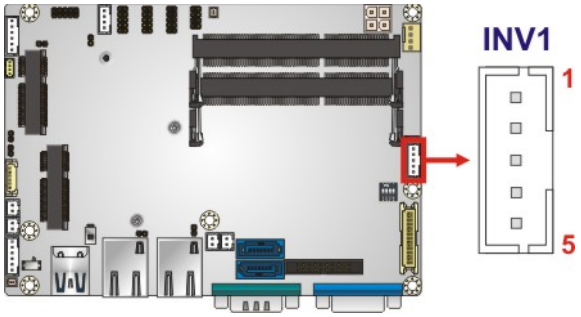


Figure 3-15: LVDS Backlight Control Connector Location

Pin	Description
1	LCD_BKLTCTL
2	GROUND
3	+12V
4	GROUND
5	BACKLIGHT ENABLE

Table 3-15: LVDS Backlight Control Connector Pinouts

3.2.15 LVDS Connector

CN Label: **LVDS1**

CN Type: 30-pin crimp, p=2 mm

CN Location: See **Figure 3-16**

CN Pinouts: See **Table 3-16**

The 30-pin LVDS LCD connector can be connected to an 18/24-bit dual-channel LVDS panel.

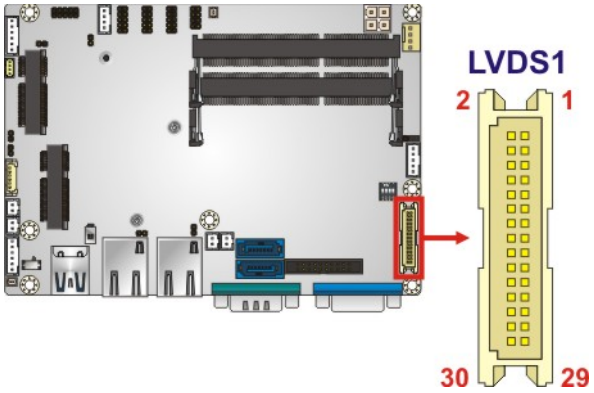


Figure 3-16: LVDS Connector Location

Pin	Description	Pin	Description
1	GND	2	GND
3	LVDS_A_TX0-P	4	LVDS_A _TX0-N
5	LVDS_A_TX1-P	6	LVDS_A _TX1-N
7	LVDS_A_TX2-P	8	LVDS_A _TX2-N
9	LVDS_A_TXCLK-P	10	LVDS_A _TXCLK-N
11	LVDS_A_TX3-P	12	LVDS_A _TX3-N
13	GND	14	GND
15	LVDS_B _TX0-P	16	LVDS_B _TX0-N
17	LVDS_B _TX1-P	18	LVDS_B _TX1-N
19	LVDS_B _TX2-P	20	LVDS_B _TX2-N
21	LVDS_B _TXCLK-P	22	LVDS_B _TXCLK-N
23	LVDS_B _TX3-P	24	LVDS_B _TX3-N
25	GND	26	GND
27	+LCD Vcc	28	+LCD Vcc
29	+LCD Vcc	30	+LCD Vcc

Table 3-16: LVDS Connector Pinouts

3.2.16 PCIe Mini Card Slot

CN Label:	**M_PCIE2**
CN Type:	PCIe Mini card slot
CN Location:	See **Figure 3-17**
CN Pinouts:	See **Table 3-17**

The PCIe Mini card slot enables a full-size/half-size PCIe Mini card expansion module to be connected to the board.

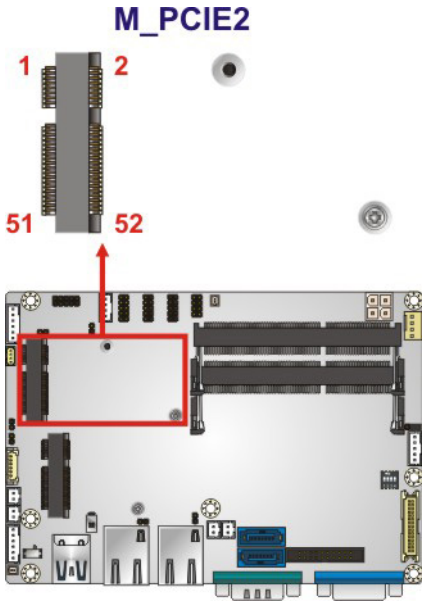


Figure 3-17: PCIe Mini Card Slot Location

Pin	Description	Pin	Description
1	PCIE_WAKE#	2	VCC3
3	N/C	4	GND
5	N/C	6	1.5V
7	N/C	8	N/C
9	GND	10	N/C
11	PCIE_CLK#	12	N/C
13	PCIE_CLK	14	N/C
15	GND	16	N/C

Pin	Description	Pin	Description
17	N/C	18	GND
19	N/C	20	N/C
21	GND	22	PCIRST#
23	PCIE_RXN	24	VCC3
25	PCIE_RXP	26	GND
27	GND	28	1.5V
29	GND	30	SMBCLK
31	PCIE_TXN	32	SMBDATA
33	PCIE_TXP	34	GND
35	GND	36	USBD-
37	GND	38	USBD+
39	VCC3	40	GND
41	VCC3	42	N/C
43	GND	44	N/C
45	N/C	46	N/C
47	N/C	48	1.5V
49	N/C	50	GND
51	M-SATA Detect	52	VCC3

Table 3-17: PCIe Mini Card Slot Pinouts

3.2.17 Power and HDD LED Connector

CN Label: **CN2**

CN Type: 6-pin wafer, p=2 mm

CN Location: See **Figure 3-18**

CN Pinouts: See **Table 3-18**

The LED connector connects to an HDD indicator LED and a power LED on the system chassis to inform the user about HDD activity and the power on/off status of the system.

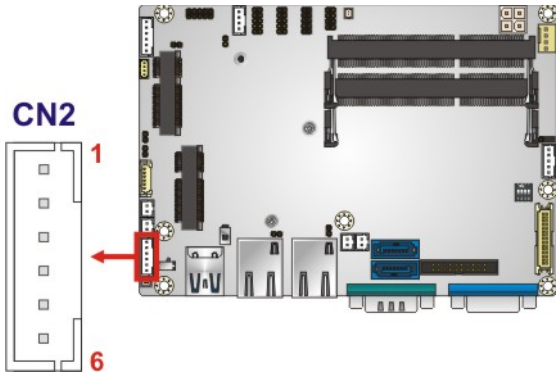


Figure 3-18: Power and HDD LED Connector Location

Function	Pin	Description
+5V	1	VCC
	2	GND
Power LED	3	PWRLED
	4	GND
HDD LED	5	VCC
	6	-HDLED

Table 3-18: Power and HDD LED Connector Pinouts

3.2.18 Power Button Connector

CN Label: **PWR_BTN1**

CN Type: 2-pin wafer, p=2 mm

CN Location: See **Figure 3-19**

CN Pinouts: See **Table 3-19**

The power button connector is connected to a power switch on the system chassis to enable users to turn the system on and off.

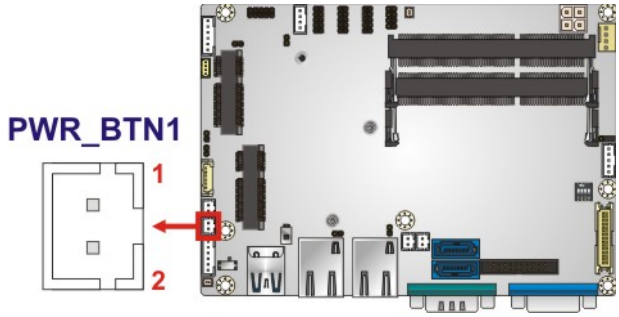


Figure 3-19: Power Button Connector Location

Pin	Description
1	PWRBTSW#
2	GND

Table 3-19: Power Button Connector Pinouts

3.2.19 Reset Button Connector

CN Label: **RST_BTN1**

CN Type: 2-pin wafer, p=2 mm

CN Location: See **Figure 3-20**

CN Pinouts: See **Table 3-20**

The reset button connector is connected to a reset switch on the system chassis to enable users to reboot the system when the system is turned on.

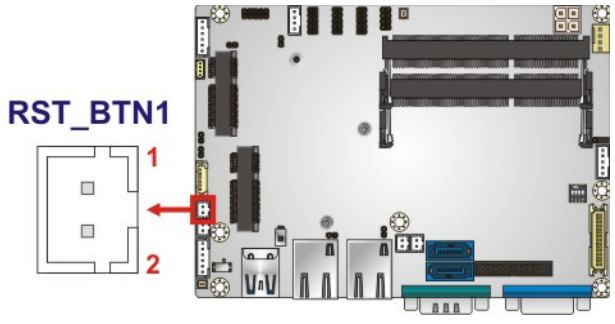


Figure 3-20: Reset Button Connector Location

Pin	Description
1	SYSRST
2	GND

Table 3-20: Reset Button Connector Pinouts

3.2.20 SATA 6Gb/s Connectors

CN Label: **SATA1, SATA2**

CN Type: 7-pin SATA drive connector

CN Location: See **Figure 3-21**

CN Pinouts: See **Table 3-21**

The SATA drive connectors can be connected to SATA drives and support up to 6Gb/s data transfer rate.

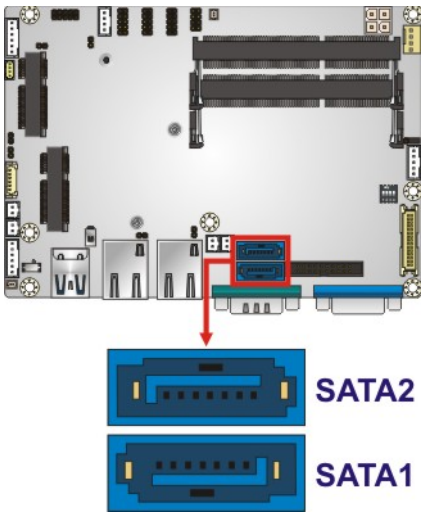


Figure 3-21: SATA 6Gb/s Connector Locations

Pin	Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-

Pin	Description
6	RX+
7	GND

Table 3-21: SATA 6Gb/s Drive Connector Pinouts

3.2.21 Serial Port Connector, RS-232

CN Label: **COM2, COM3**

CN Type: 10-pin header, p=2 mm

CN Location: See **Figure 3-22**

CN Pinouts: See **Table 3-22**

The 10-pin serial port connector provides one RS-232 serial communications channel. The COM serial port connector can be connected to an external RS-232 serial port device.

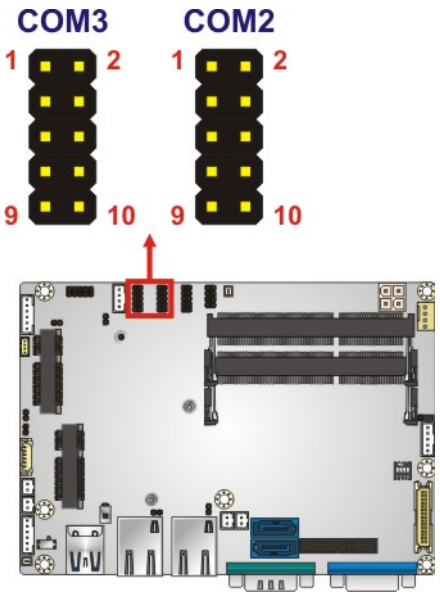


Figure 3-22: RS-232 Serial Port Connector Locations

Pin	Description	Pin	Description
1	DATA CARRIER DETECT (DCD)	2	DATA SET READY (DSR)
3	RECEIVE DATA (RXD)	4	REQUEST TO SEND (RTS)
5	TRANSMIT DATA (TXD)	6	CLEAR TO SEND (CTS)

Pin	Description	Pin	Description
7	DATA TERMINAL READY (DTR)	8	RING INDICATOR (RI)
9	GND	10	GND

Table 3-22: RS-232 Serial Port Connector Pinouts

3.2.22 Serial Port Connector, RS-422/485

CN Label: **COM4**

CN Type: 4-pin wafer, p=2 mm

CN Location: See **Figure 3-23**

CN Pinouts: See **Table 3-23**

This connector provides RS-422 or RS-485 communications.

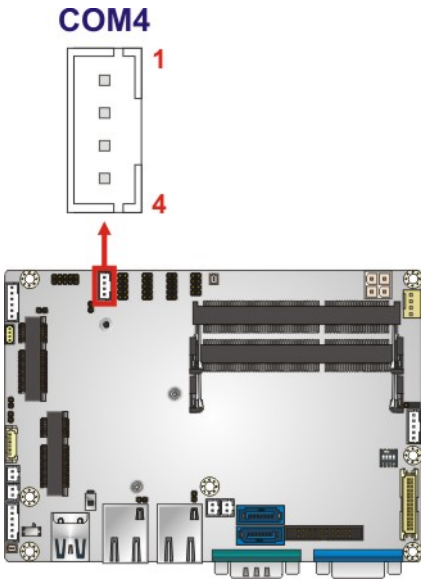


Figure 3-23: RS-422/485 Serial Port Connector Location

Pin	Description
1	RXD422-
2	RXD422+
3	TXD422+/TXD485+
4	TXD422-/TXD485-

Table 3-23: RS-422/485 Serial Port Connector Pinouts

Use the optional RS-422/485 cable to connect to a serial device. The pinouts of the DB-9 connector are listed below.

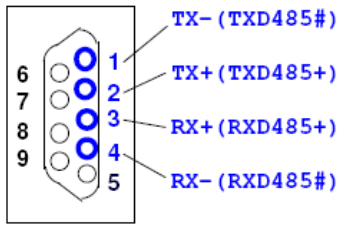
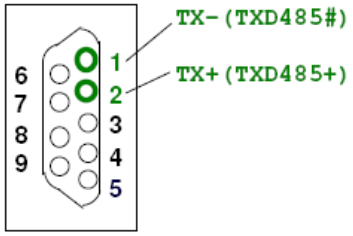
RS-422 Pinouts	RS-485 Pinouts
	

Table 3-24: DB-9 RS-422/485 Pinouts

3.2.23 SMBus Connector

CN Label: **CN3**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-24**

CN Pinouts: See **Table 3-25**

The SMBus (System Management Bus) connector provides low-speed system management communications.

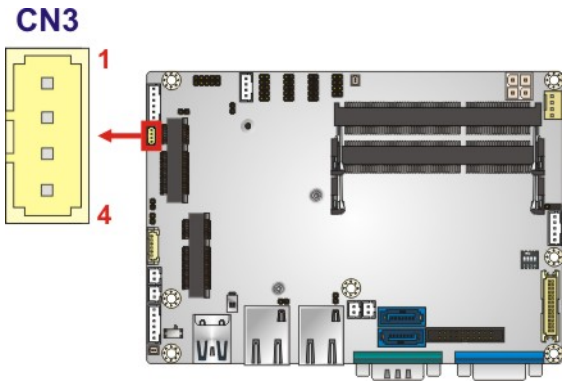


Figure 3-24: SMBus Connector Location

Pin	Description
1	GND
2	SMB_DATA

Pin	Description
3	SMB_CLK
4	+5V

Table 3-25: SMBus Connector Pinouts

3.2.24 SO-DIMM Slots

CN Label: **DIMM1, DIMM2**

CN Type: 204-pin DDR3L SO-DIMM slot

CN Location: See **Figure 3-25**

The SO-DIMM slots are for installing the SO-DIMMs on the system.

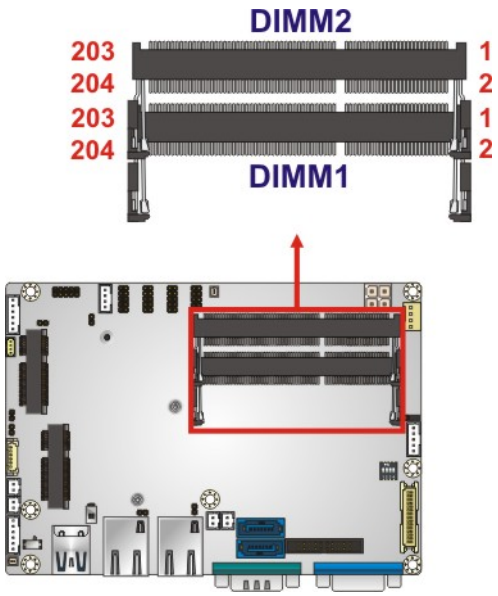


Figure 3-25: SO-DIMM Slot Locations

3.2.25 SPI Flash Connector

CN Label: **SPI1**

CN Type: 6-pin wafer, p=1.25 mm

CN Location: See **Figure 3-26**

CN Pinouts: See **Table 3-26**

The SPI flash connector is used to flash the SPI ROM.

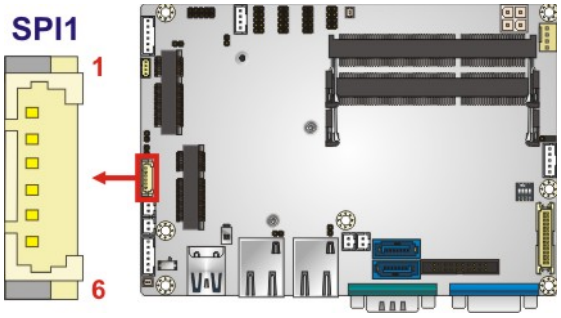


Figure 3-26: SPI Flash Connector Location

Pin	Description
1	SPI_VCC
2	SPI_2N_CS#
3	SPI_2N_MISO
4	SPI_2N_CLK
5	SPI_2N_MOSI
6	GND

Table 3-26: SPI Flash Connector Pinouts

3.2.26 System Fan Connector

CN Label: **FAN1**

CN Type: 4-pin wafer, p=2.54 mm

CN Location: See **Figure 3-27**

CN Pinouts: See **Table 3-27**

The fan connector attaches to a system cooling fan.

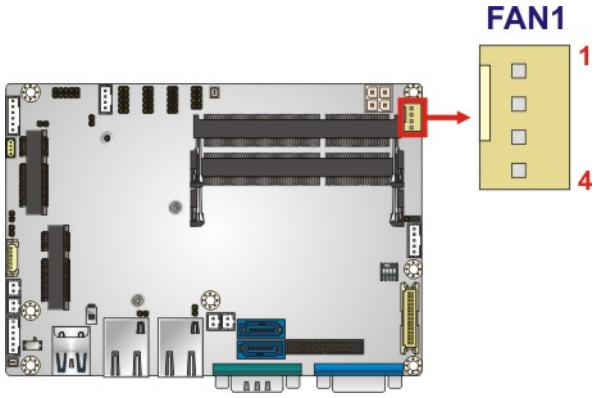


Figure 3-27: System Fan Connector Location

Pin	Description
1	GND
2	+12V
3	FANIO
4	PWM

Table 3-27: System Fan Connector Pinouts

3.2.27 USB 2.0 Connector

CN Label: **USB1**

CN Type: 8-pin header, p=2 mm

CN Location: See **Figure 3-28**

CN Pinouts: See **Table 3-28**

The USB header can connect to two USB 2.0/1.1 devices.

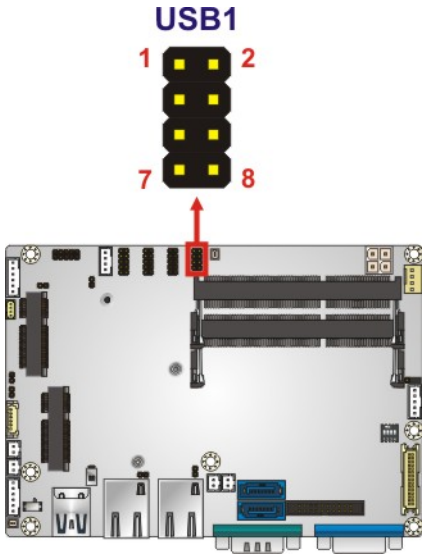


Figure 3-28: USB 2.0 Connector Location

Pin	Description	Pin	Description
1	USB_VCC	2	GND
3	DATA-	4	DATA+
5	DATA+	6	DATA-
7	GND	8	USB_VCC

Table 3-28: USB 2.0 Connector Pinouts

3.3 External Interface Connectors

The figure below shows the external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

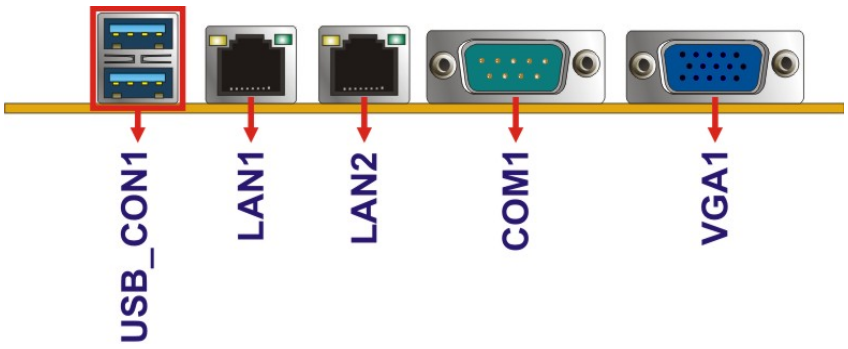


Figure 3-29: External Interface Connectors

3.3.1 Ethernet Connectors

CN Label: **LAN1, LAN2**

CN Type: RJ-45

CN Location: See **Figure 3-29**

CN Pinouts: See **Table 3-29**

Each LAN connector connects to a local network.

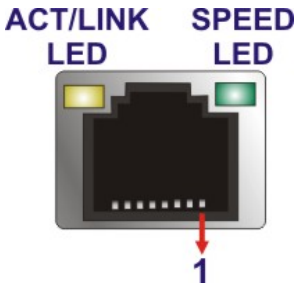


Figure 3-30: LAN Connector

Pin	Description	Pin	Description
1	LAN_MDI0+	7	LAN_MDI2+
2	LAN_MDI0-	8	LAN_MDI2-
3	LAN_MDI1+	9	LAN_MDI3+
4	LAN_MDI1-	10	LAN_MDI3-

Table 3-29: LAN Pinouts

3.3.2 USB 3.0 Ports

CN Label: **USB_CON1**

CN Type: Dual USB 3.0 port

CN Location: See **Figure 3-29**

CN Pinouts: See **Table 3-30**

The WAFER-ULT/ULT2-i1 has two external USB 3.0 ports.

Pin	Description	Pin	Description
1	VCC	10	VCC
2	D-	11	D-
3	D+	12	D+
4	GND	13	GND
5	RX-	14	RX-
6	RX+	15	RX+
7	GND	16	GND
8	TX-	17	TX-
9	TX+	18	TX+

Table 3-30: USB 3.0 Port Pinouts

3.3.3 Serial Port Connector (COM1)

CN Label: **COM1**

CN Type: DB-9

CN Location: See **Figure 3-29**

CN Pinouts: See **Table 3-31**

The serial port connects to an RS-232 serial communications device.

Pin	Description	Pin	Description
1	DATA CARRIER DETECT (DCD)	6	DATA SET READY (DSR)
2	RECEIVE DATA (RXD)	7	REQUEST TO SEND (RTS)
3	TRANSMIT DATA (TXD)	8	CLEAR TO SEND (CTS)
4	DATA TERMINAL READY (DTR)	9	RING INDICATOR (RI)
5	GND		

Table 3-31: Serial Port Pinouts

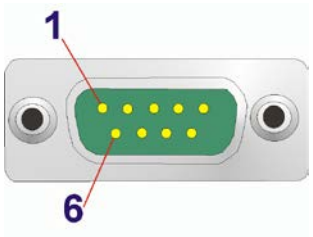


Figure 3-31: Serial Port

3.3.4 VGA Connector

CN Label: **VGA1**

CN Type: 15-pin female

CN Location: See **Figure 3-29**

CN Pinouts: See **Figure 3-32** and **Table 3-32**

The VGA connector connects to a monitor that accepts a standard VGA input.

Pin	Description	Pin	Description
1	RED	2	GREEN
3	BLUE	4	NC
5	GND	6	GND
7	GND	8	GND
9	VCC	10	GND
11	NC	12	DDCDAT
13	HSYNC	14	VSYNC
15	DDCCLK		

Table 3-32: VGA Connector Pinouts

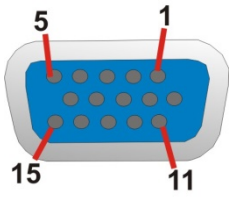


Figure 3-32: VGA Connector

Chapter

4

Installation

4.1 Anti-static Precautions

WARNING:

Failure to take ESD precautions during the installation of the WAFER-ULT/ULT2-i1 may result in permanent damage to the WAFER-ULT/ULT2-i1 and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the WAFER-ULT/ULT2-i1. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the WAFER-ULT/ULT2-i1 or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband***: - Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding***:- Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad***: When configuring the WAFER-ULT/ULT2-i1, place it on an anti-static pad. This reduces the possibility of ESD damaging the WAFER-ULT/ULT2-i1.
- ***Only handle the edges of the PCB***:-: When handling the PCB, hold the PCB by the edges.

4.2 Installation Considerations

NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

WARNING:

The installation instructions described in this manual should be carefully followed in order to prevent damage to the components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  The user manual provides a complete description of the WAFER-ULT/ULT2-i1 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the WAFER-ULT/ULT2-i1 on an anti-static pad:
  When installing or configuring the motherboard, place it on an anti-static pad. This helps to prevent potential ESD damage.
- Turn all power to the WAFER-ULT/ULT2-i1 off:
  When working with the WAFER-ULT/ULT2-i1, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the WAFER-ULT/ULT2-i1, **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

4.3 SO-DIMM Installation

To install a SO-DIMM, please follow the steps below and refer to **Figure 4-1**.

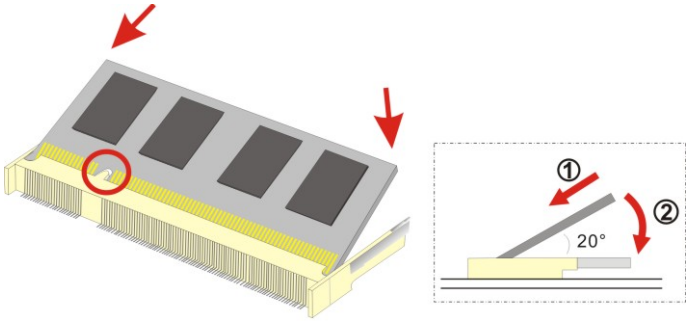


Figure 4-1: SO-DIMM Installation

Step 1: **Locate the SO-DIMM socket**. Place the board on an anti-static mat.

Step 2: **Align the SO-DIMM with the socket**. Align the notch on the memory with the notch on the memory socket.

Step 3: **Insert the SO-DIMM**. Push the memory in at a 20º angle. (See **Figure 4-1**)

Step 4: **Seat the SO-DIMM**. Gently push downwards and the arms clip into place. (See **Figure 4-1**)

4.4 iRIS-1010 Module Installation

WARNING:

The iRIS module slot is designed to install the iRIS-1010 module only. DO NOT install other modules into the iRIS module slot. Doing so may cause damage to the WAFER-ULT/ULT2-i1.

To install the iRIS-1010 module, please follow the steps below.

Step 1: **Locate the iRIS module slot**. See **Figure 3-12**.

Step 2: **Remove the retention screw**. Remove the retention screw as shown in **Figure 4-2**.

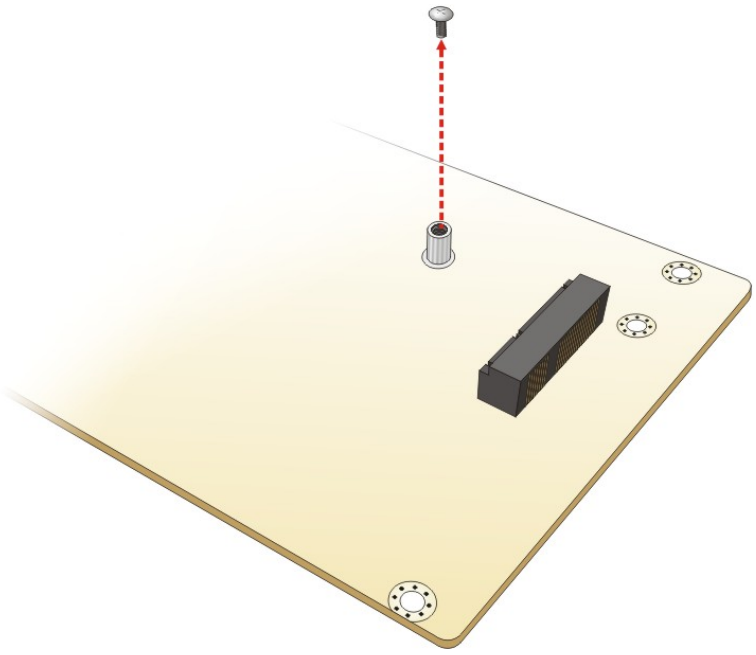


Figure 4-2: Removing the Retention Screw for the iRIS-1010 Module

Step 3: **Insert into the slot at an angle**. Line up the notch on the module with the notch on the slot. Slide the iRIS-1010 module into the slot at an angle of about 20º (**Figure 4-3**).

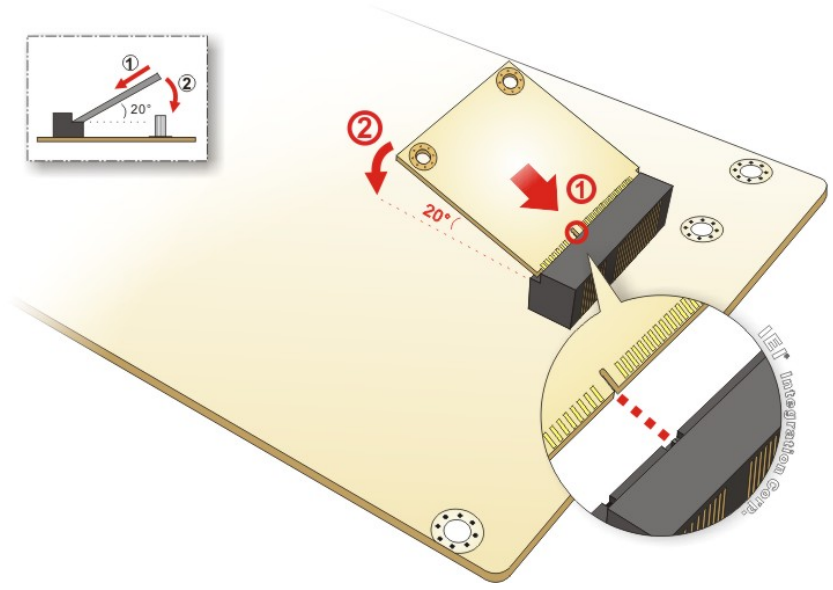


Figure 4-3: Inserting the iRIS-1010 Module into the Slot at an Angle

Step 4: **Secure the iRIS-1010 module**. Secure the iRIS-1010 module with the retention screw previously removed (**Figure 4-4**).

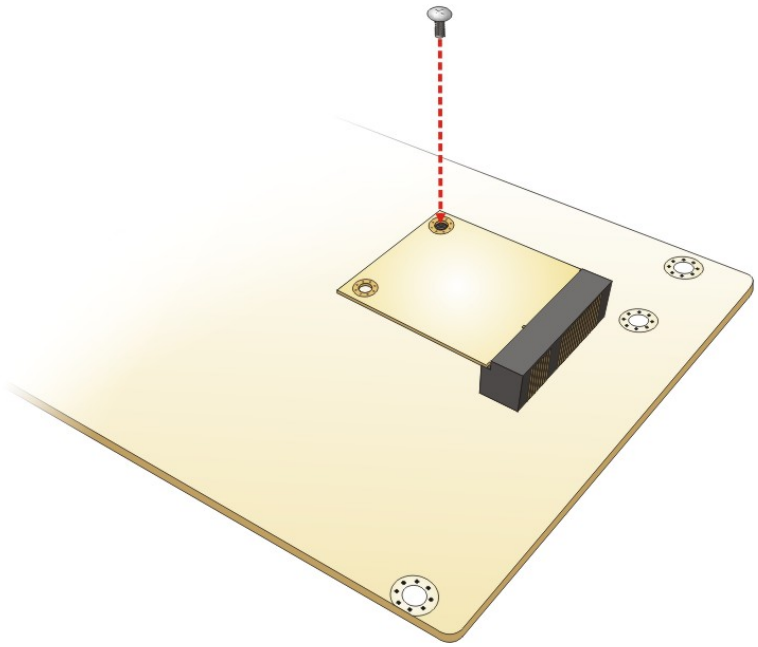


Figure 4-4: Securing the iRIS-1010 Module

NOTE:

After installing the iRIS-1010 module, use **LAN2** port to establish a network connection. Please refer to **Section 4.11** for IPMI setup procedures.

4.5 Full-size PCIe Mini Card Installation

The PCIe Mini card slot allows installation of either a full-size or half-size PCIe Mini card. To install a full-size PCIe Mini card, please follow the steps below.

Step 1: **Locate the PCIe Mini card slot**. See **Figure 3-17**.

Step 2: **Remove the retention screw**. Remove the retention screw as shown in **Figure 4-5**.

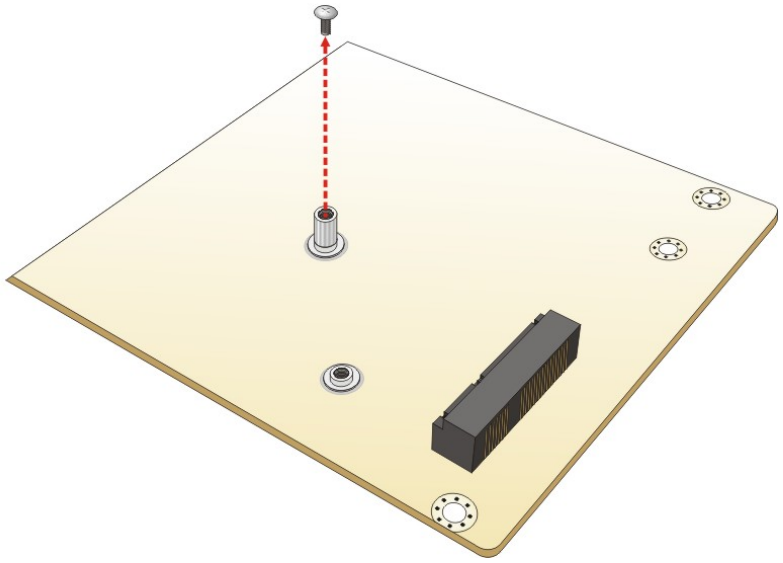


Figure 4-5: Removing the Retention Screw

Step 3: **Insert into the socket at an angle**. Line up the notch on the card with the notch on the slot. Slide the PCIe Mini card into the socket at an angle of about 20º (**Figure 4-6**).

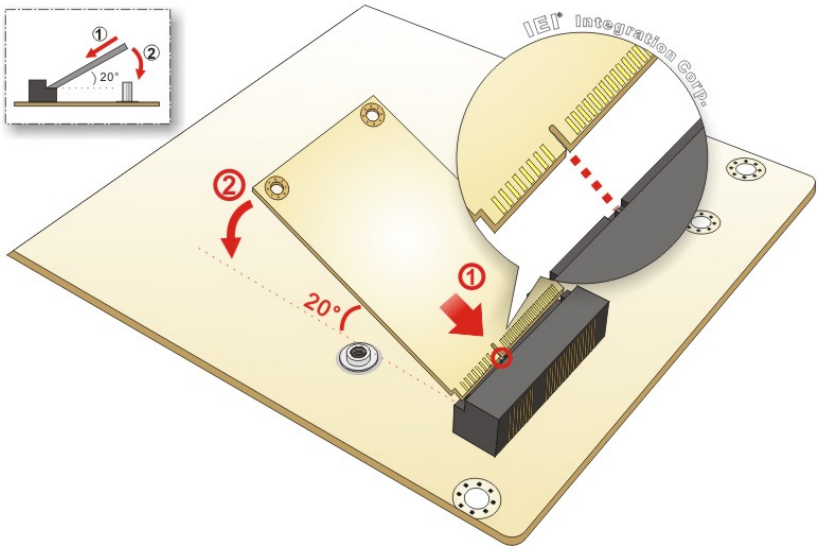


Figure 4-6: Inserting the Full-size PCIe Mini Card into the Slot at an Angle

Step 4: **Secure the full-size PCIe Mini card**. Secure the full-size PCIe Mini card with the retention screw previously removed (**Figure 4-7**).

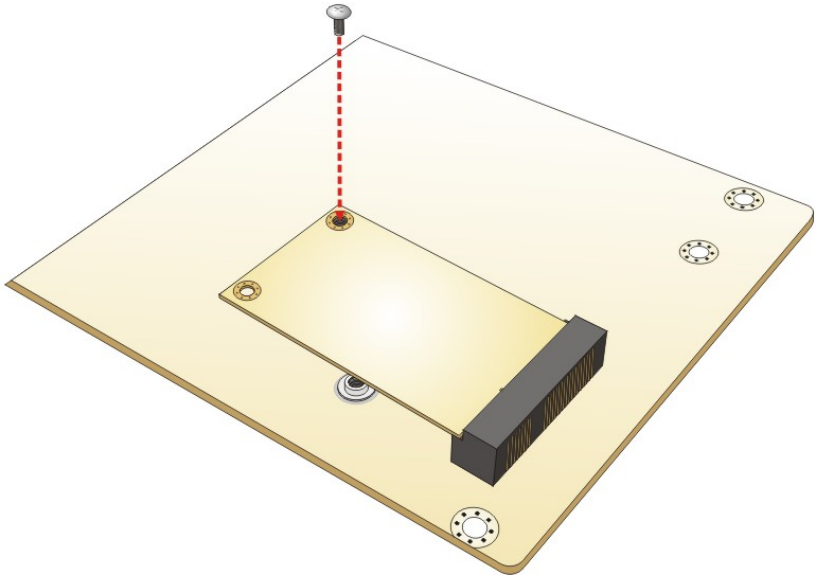


Figure 4-7: Securing the Full-size PCIe Mini Card

4.6 Half-size PCIe Mini Card Installation

The PCIe Mini card slot allows installation of either a full-size or half-size PCIe Mini card. To install a half-size PCIe Mini card, please follow the steps below.

Step 1: **Locate the PCIe Mini card slot**. See **Figure 3-17**.

Step 2: **Remove the retention screw**. Remove the retention screw as shown in **Figure 4-5**.

Step 3: **Remove the standoff**. Unscrew and remove the standoff secured on the motherboard as shown in **Figure 4-8**.

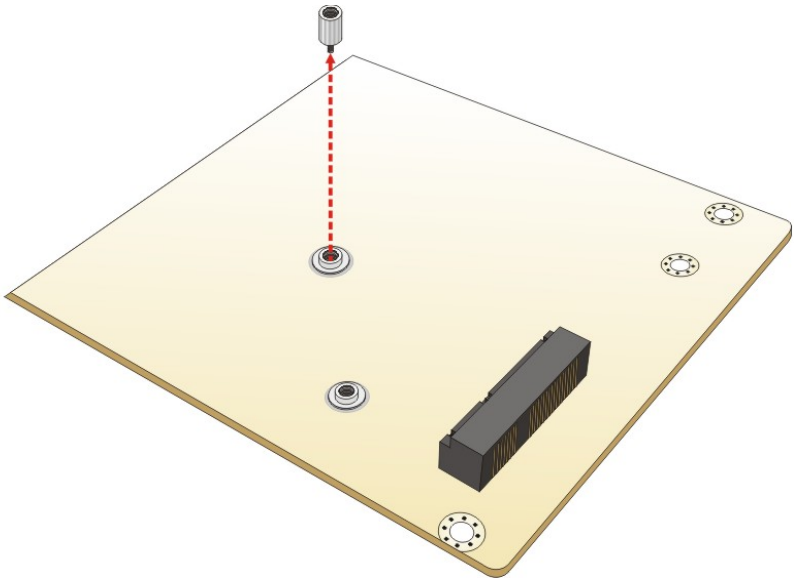


Figure 4-8: Removing the Standoff

Step 4: **Install the standoff to the screw hole for the half-size PCIe Mini card**. Install the previously removed standoff to the screw hole for the half-size PCIe Mini card (**Figure 4-9**).

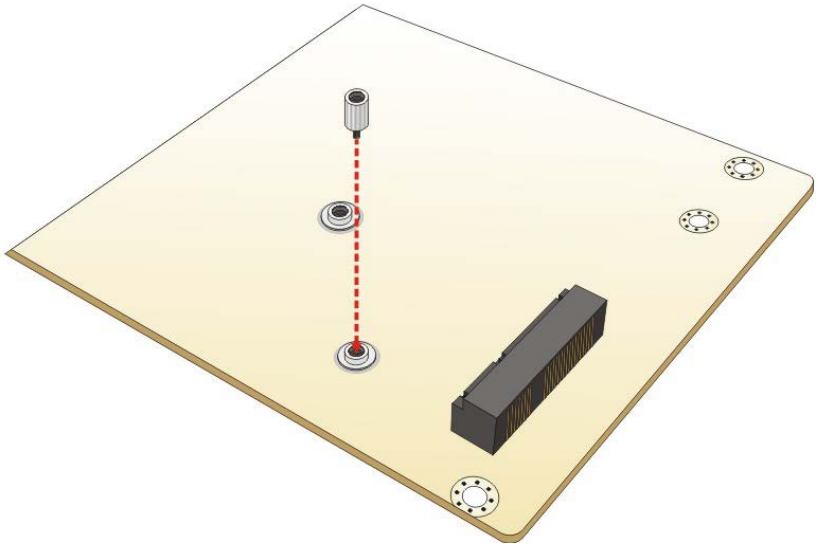


Figure 4-9: Installing the Standoff

Step 5: **Insert into the socket at an angle**. Line up the notch on the card with the notch on the slot. Slide the PCIe Mini card into the slot at an angle of about 20º (**Figure 4-10**).

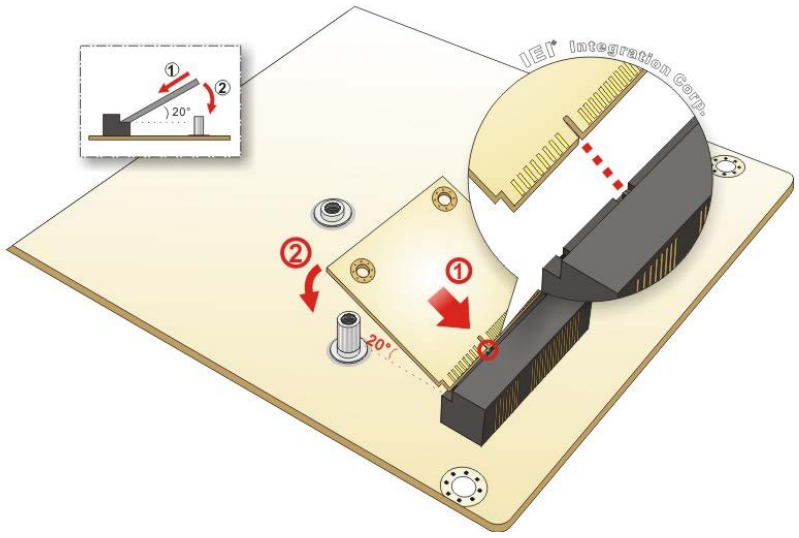


Figure 4-10: Inserting the Half-size PCIe Mini Card into the Slot at an Angle

Step 6: **Secure the half-size PCIe Mini card**. Secure the half-size PCIe Mini card with the retention screw previously removed (**Figure 4-11**).

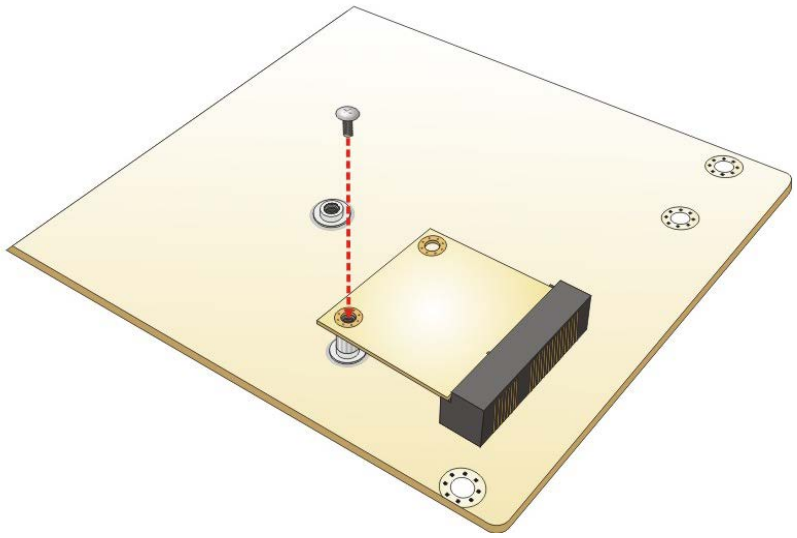


Figure 4-11: Securing the Half-size PCIe Mini Card

4.7 System Configuration

The system configuration is controlled by buttons, jumpers and switches. The system configuration should be performed before installation.

4.7.1 DC 5V Jumper for LVDS Backlight Dimming

Jumper Label: **LVDSBL_DC5V1**

Jumper Type: 2-pin header, p=2 mm

Jumper Settings: See **Table 4-1**

Jumper Location: See **Figure 4-12**

The DC 5V jumper can be used to lock the LVDS backlight dimming voltage level at DC 5V. When the jumper is being closed, the **Backlight Voltage Level** BIOS option in "Chipset → System Agent (SA) Configuration → PCH-IO Configuration → Graphics Configuration → LCD Control" menu will be locked at **5V**. Refer to **Section 5.4.1.1.1** for detailed information.

Setting	Description
Open	By BIOS setting (Default)
Short 1-2	Locked to DC 5V for CCFL

Table 4-1: DC 5V Jumper Settings

Pin	Description
1	EC_BKLT_DC5V
2	GND

Table 4-2: DC 5V Jumper Pinouts

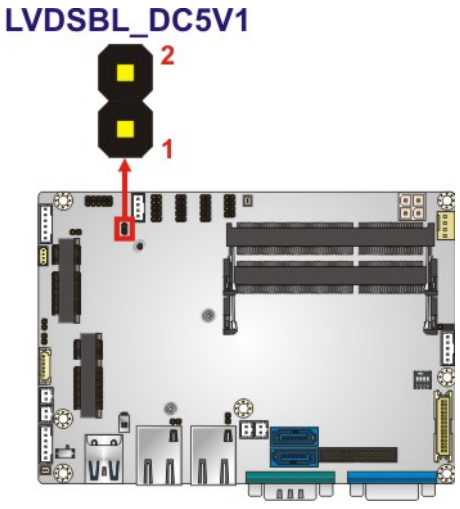


Figure 4-12: DC 5V Jumper Location

4.7.2 AT/ATX Power Mode Selection

The AT and ATX power mode selection is made through the AT/ATX power mode switch which is shown in **Figure 4-13**.

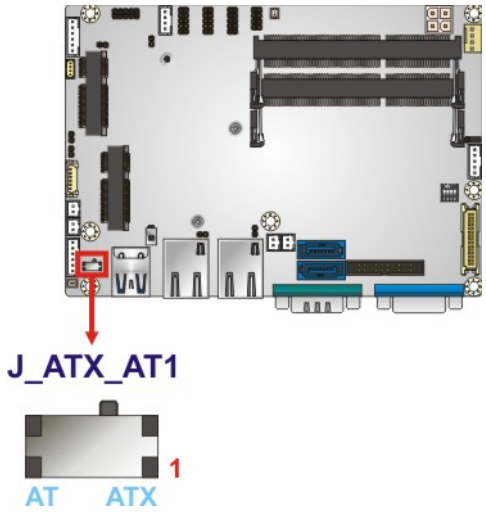


Figure 4-13: AT/ATX Power Mode Switch Location

Setting	Description
1-2	ATX power mode (default)
2-3	AT power mode

Table 4-3: AT/ATX Power Mode Switch Settings

4.7.3 Clear CMOS Button

To reset the BIOS, remove the on-board battery and press the clear CMOS button for three seconds or more. The clear CMOS button location is shown in **Figure 4-14**.

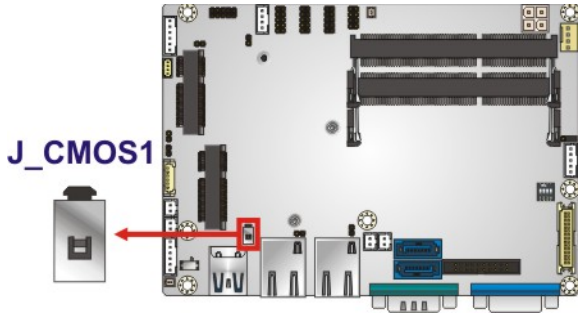


Figure 4-14: Clear CMOS Button Location

4.7.4 LVDS Panel Type Selection

Jumper Label: **SW1**

Jumper Type: DIP switch

Jumper Settings: See **Table 4-4**

Jumper Location: See **Figure 4-15**

Selects the resolution of the LCD panel connected to the LVDS connector.

* ON=0, OFF=1

SW1 (4-3-2-1)	EDID Resolution	Color Depth	Channel
0000 (default)	800 x 600 @ 60 Hz	18-bit	Single
0001	1024 x 768 @ 60 Hz	18-bit	Single
0010	1024 x 768 @ 60 Hz	24-bit	Single
0011	1280 x 768 @ 60 Hz	18-bit	Single
0100	1280 x 800 @ 60 Hz	18-bit	Single
0101	1280 x 960 @ 60 Hz	18-bit	Single
0110	1280 x 1024 @ 60 Hz	24-bit	Dual
0111	1366 x 768 @ 60 Hz	18-bit	Single
1000	1366 x 768 @ 60 Hz	24-bit	Single
1001	1440 x 900 @ 60 Hz	24-bit	Dual
1010	1440 x 1050 @ 60 Hz	24-bit	Dual
1011	1600 x 900 @ 60 Hz	24-bit	Dual
1100	1680 x 1050 @ 60 Hz	24-bit	Dual
1101	1600 x 1200 @ 60 Hz	24-bit	Dual
1110	1920 x 1080 @ 60 Hz	24-bit	Dual
1111	1920 x 1200 @ 60 Hz	24-bit	Dual

Table 4-4: LVDS Panel Type Selection

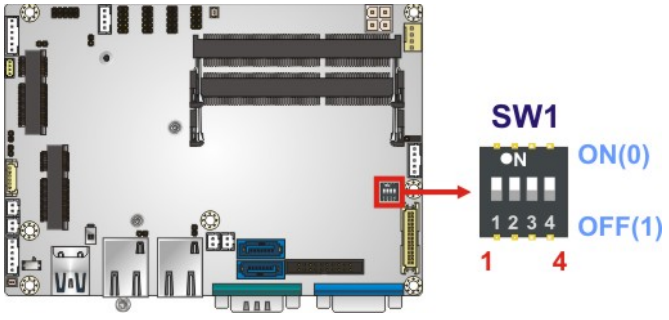


Figure 4-15: LVDS Panel Type Selection Switch Location

4.7.5 LVDS Voltage Selection

WARNING:

Permanent damage to the screen and WAFER-ULT/ULT2-i1 may occur if the wrong voltage is selected with this jumper. Please refer to the user guide that came with the monitor to select the correct voltage.

Jumper Label:	**JP1**
Jumper Type:	3-pin header, p=2 mm
Jumper Settings:	See **Table 4-5**
Jumper Location:	See **Figure 4-16**

The LVDS voltage selection jumper allows setting the voltage provided to the monitor connected to the LVDS connector.

Setting	Description
Short 1-2	+3.3V LVDS (Default)
Short 2-3	+5V LVDS

Table 4-5: LVDS Voltage Selection Jumper Settings

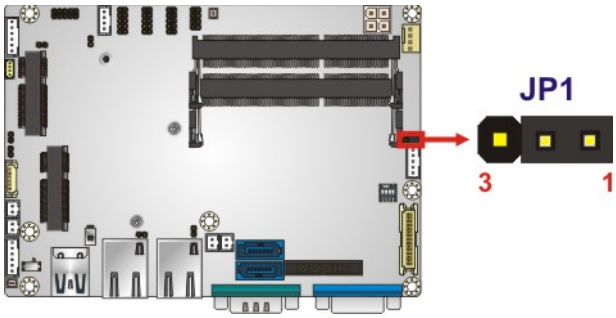


Figure 4-16: LVDS Voltage Selection Jumper Location

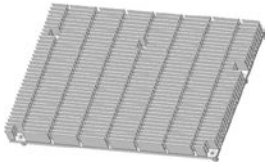
4.8 Motherboard Installation

4.8.1 Heat Spreader

WARNING:

The heat spreader installed on the WAFER-ULT/ULT2-i1 can only serve as a heat conductor, which needs additional heat dissipation mechanism to achieve suitable thermal condition. DO NOT put the WAFER-ULT/ULT2-i1 with the heat spreader directly on a surface that cannot dissipate system heat, and never run the WAFER-ULT/ULT2-i1 without the heat spreader secured to the board.

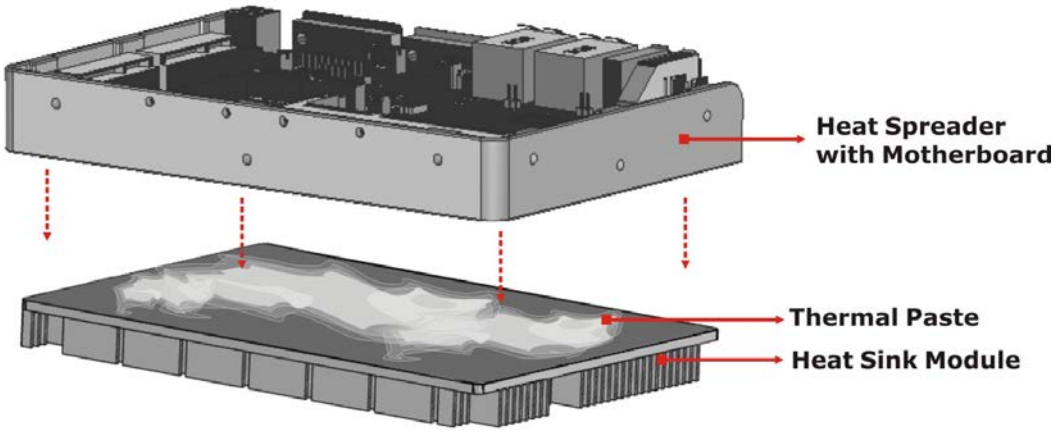
When the WAFER-ULT/ULT2-i1 is shipped, it is secured to a heat spreader with five retention screws. The heat spreader must have a direct contact with a heat dissipation surface to ensure stable operation. In addition, a thin layer of thermal paste has to be applied onto the heat dissipation surface where it contacts the heat spreader. The following diagrams show an example of a heat sink module and how it can be installed for dissipating the heat generated from the motherboard:



Heat sink module:

Material: Aluminum

Size: 146 mm x 102 mm x 12 mm



If the WAFER-ULT/ULT2-i1 must be removed from the heat spreader, the five retention screws must be removed.

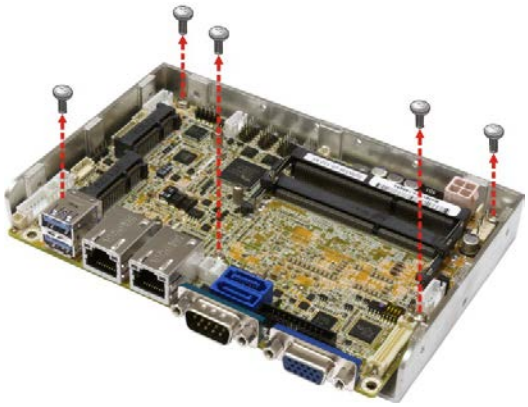


Figure 4-17: Heat Spreader Retention Screws

4.8.2 Motherboard Installation Example

Each side of the heat spreader has several screw holes allowing the WAFER-ULT/ULT2-i1 to be mounted into a chassis or a heat sink enclosure (please refer to **Figure 1-3** for the detailed dimensions). The user has to design or select a chassis or a heat sink enclosure that has screw holes matching up with the holes on the heat spreader for installing the WAFER-ULT/ULT2-i1. The following diagram shows an example of motherboard installation.

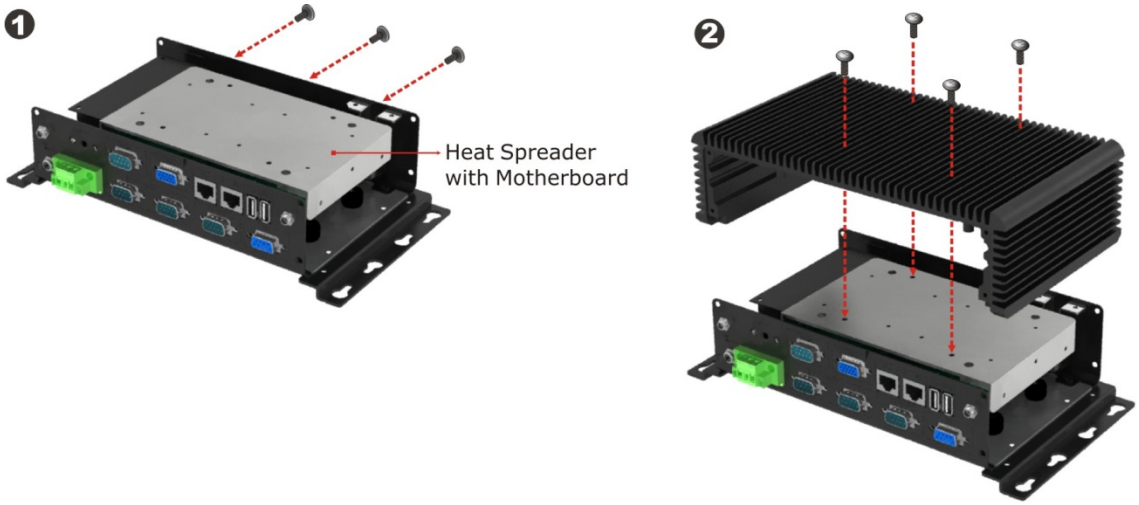


Figure 4-18: Motherboard Installation Example

4.9 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the on-board connectors.

4.9.1 AT/ATX Power Connection

Follow the instructions below to connect the WAFER-ULT/ULT2-i1 to an AT or ATX power supply.

WARNING:

Disconnect the power supply power cord from its AC power source to prevent a sudden power surge to the WAFER-ULT/ULT2-i1.

Step 1: **Locate the power cable**. The power cable is shown in the packing list in **Chapter 2**.

Step 2: **Connect the Power Cable to the Motherboard**. Connect the 4-pin (2x2) Molex type power cable connector to the power connector on the motherboard. See **Figure 4-19**.

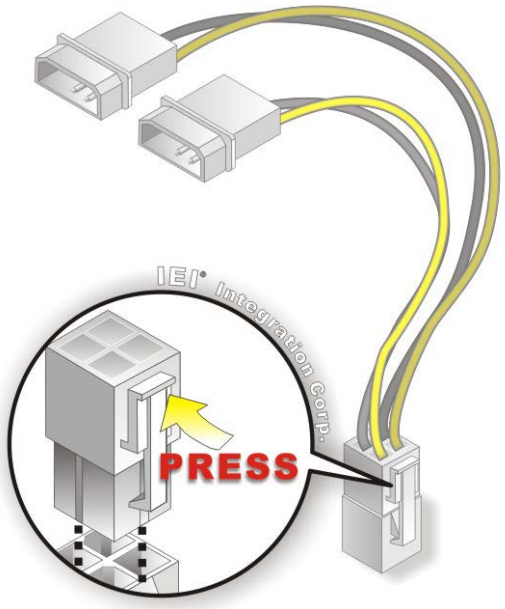


Figure 4-19: Power Cable to Motherboard Connection

Step 3: **Connect Power Cable to Power Supply**. Connect one of the 4-pin (1x4) Molex type power cable connectors to an AT/ATX power supply. See **Figure 4-20**.

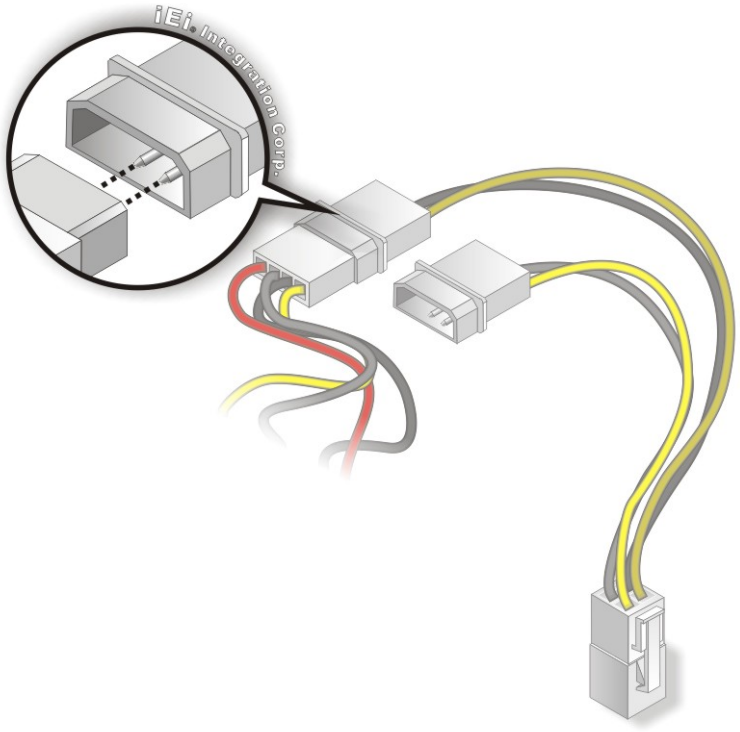


Figure 4-20: Connect Power Cable to Power Supply

4.9.2 Audio Kit Installation

The Audio Kit that came with the WAFER-ULT/ULT2-i1 connects to the 10-pin audio connector on the WAFER-ULT/ULT2-i1. The audio kit consists of three audio jacks. One audio jack, Mic In, connects to a microphone. The remaining two audio jacks, Line-In and Line-Out, connect to two speakers. To install the audio kit, please refer to the steps below:

Step 1: **Locate the audio connector**. The location of the 10-pin audio connector is shown in **Chapter 3**.

Step 2: **Align pin 1**. Align pin 1 on the on-board connector with pin 1 on the audio kit connector. Pin 1 on the audio kit connector is indicated with a white dot. See **Figure 4-21**.

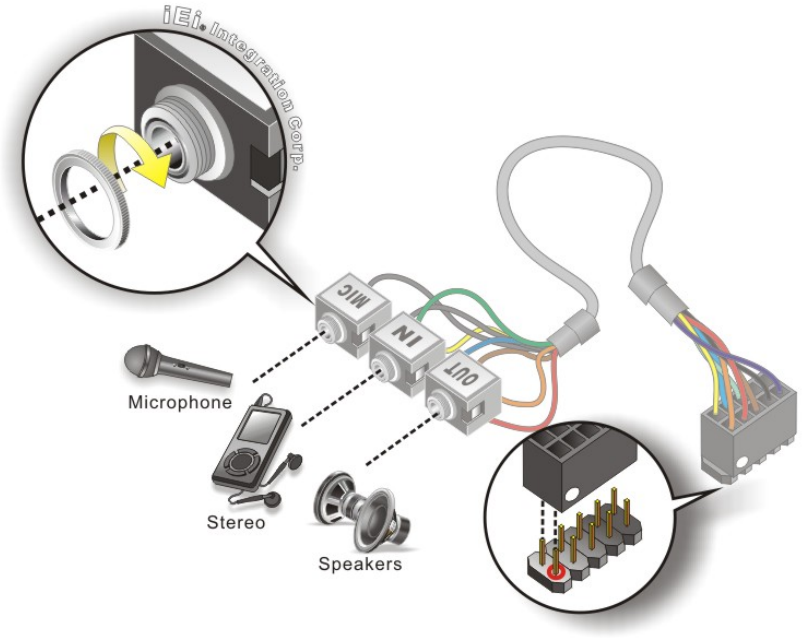


Figure 4-21: Audio Kit Cable Connection

Step 3: **Connect the audio devices**. Connect speakers to the line-out audio jack. Connect the output of an audio device to the line-in audio jack. Connect a microphone to the mic-in audio jack.

4.9.3 LVDS LCD Installation

The WAFER-ULT/ULT2-i1 can be connected to a TFT LCD screen through the LVDS crimp connectors on the board. To connect a TFT LCD to the WAFER-ULT/ULT2-i1, please follow the steps below.

Step 1: **Locate the connector**. The location of the LVDS connector is shown in **Chapter 3**.

Step 2: **Insert the cable connector**. Insert the connector from the LVDS PCB driving board to the LVDS connector as shown in **Figure 4-22**. When connecting the connectors, make sure the pins are properly aligned.

WARNING:

The diagram below is merely for illustration. The configuration and connection of the cables from the TFT LCD screen being installed may be different. Please refer to the installation manual that came with the TFT LCD screen.

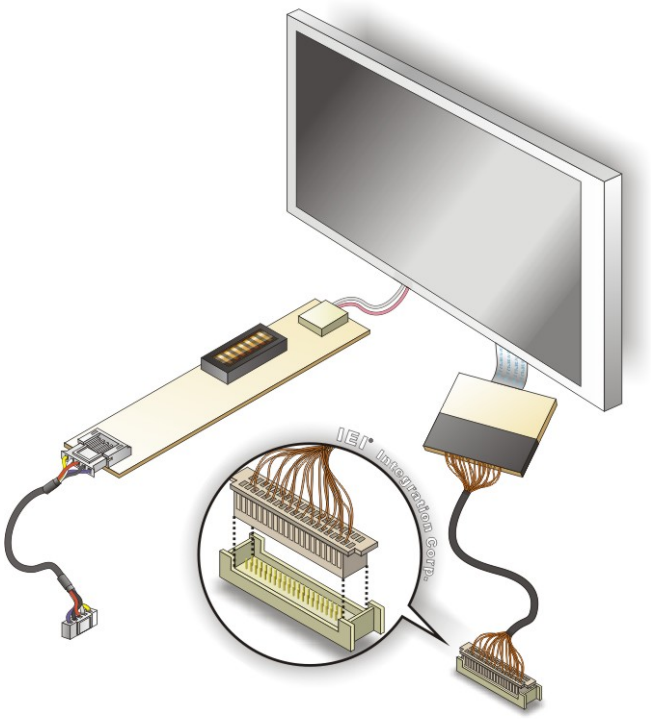


Figure 4-22: LVDS Connector

Step 3: **Locate the backlight inverter connector.** The location of the backlight inverter connector is shown in **Chapter 3**.

Step 4: **Connect backlight connector**. Connect the backlight connector to the driver TFT LCD PCB as shown in **Figure 4-23**. When inserting the cable connector, make sure the pins are properly aligned.

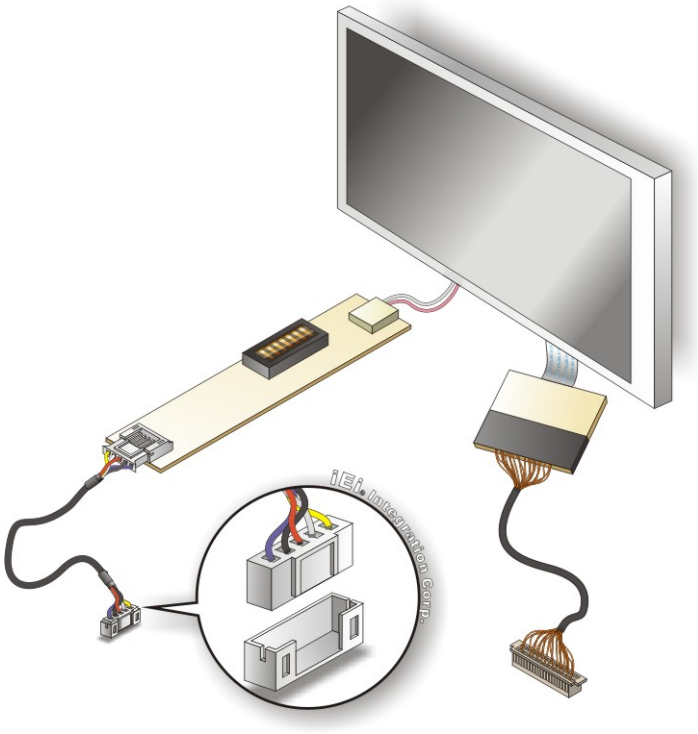


Figure 4-23: Backlight Inverter Connection

4.9.4 SATA Drive Connection

The WAFER-ULT/ULT2-i1 is shipped with two SATA signal and power cables. To connect the SATA drive to the connectors, please follow the steps below.

Step 1: **Locate the SATA connector and the SATA power connector**. The locations of the connectors are shown in **Chapter 3**.

Step 2: **Insert the cable connectors**. Insert the cable connectors into the on-board SATA drive connector and the SATA power connector. See **Figure 4-24**.

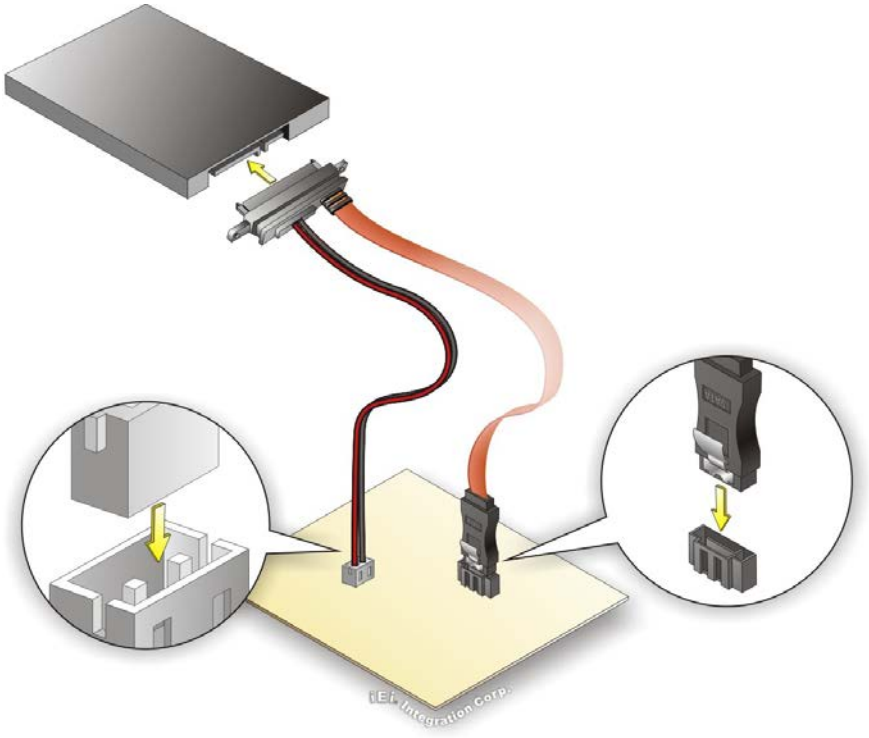


Figure 4-24: SATA Drive Cable Connection

Step 3: **Connect the cable to the SATA disk**. Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 4-24**.

Step 4: To remove the SATA cable from the SATA connector, press the clip on the connector at the end of the cable.

4.9.5 USB Cable Installation

The WAFER-ULT/ULT2-i1 is shipped with a dual-port USB 2.0 cable. To connect the USB cable connector, please follow the steps below.

Step 1: **Locate the connector**. The location of the USB connector is shown in **Chapter 3**.

WARNING:

If the USB pins are not properly aligned, the USB device can burn out.

Step 2: **Align the connectors**. Correctly align pin 1on the cable connector with pin 1 on the WAFER-ULT/ULT2-i1 USB connector.

Step 3: **Insert the cable connectors**. Once the cable connector is properly aligned with the USB connector on the WAFER-ULT/ULT2-i1, connect the cable connector to the on-board connector. See **Figure 4-25**.

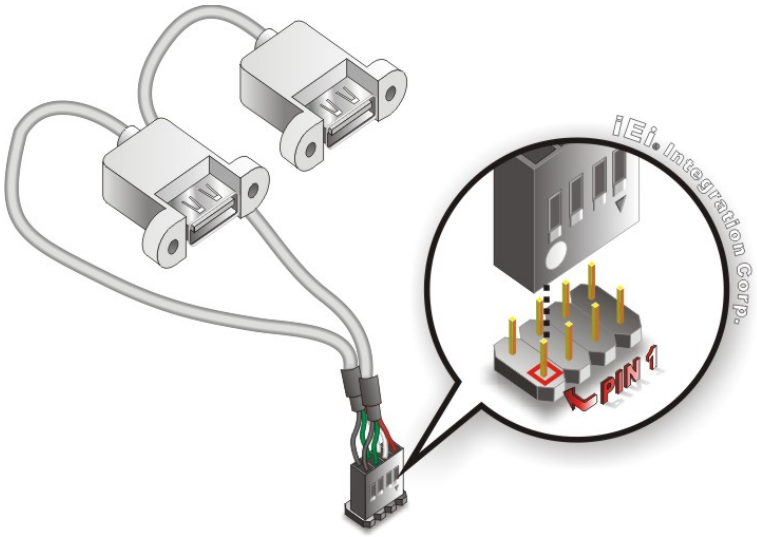


Figure 4-25: Dual-port USB Cable Connection

Step 4: **Attach the USB connectors to the chassis**. Each of the USB 2.0 connectors has two retention screw holes. To secure the connectors to the chassis, please refer to the installation instructions that came with the chassis.

4.10 Intel® AMT Setup Procedure

The WAFER-ULT/ULT2-i1 is featured with the Intel® Active Management Technology (AMT). To enable the Intel® AMT function, follow the steps below.

Step 1: Make sure at least one of the memory sockets is installed with a DDR3L SO-DIMM.

Step 2: Connect an Ethernet cable to the RJ-45 connector labeled **LAN1**.

Step 3: The AMI BIOS options regarding the Intel® ME or Intel® AMT must be enabled,

Step 4: Properly install the Intel® Management Engine Components drivers from the iAMT Driver & Utility directory in the driver CD. See **Section** Error! Reference source not found..

Step 5: Configure the Intel® Management Engine BIOS extension (MEBx). To get into the Intel® MEBx settings, press <Ctrl+P> after a single beep during boot-up process. Enter the Intel® current ME password as it requires (the Intel® default password is **admin**).

NOTE:

To change the password, enter a new password following the strong password rule (containing at least one upper case letter, one lower case letter, one digit and one special character, and be at least eight characters).

4.11 IPMI Setup Procedure

The WAFER-ULT/ULT2-i1 features Intelligent Platform Management Interface (IPMI) that helps lower the overall costs of server management by enabling users to maximize IT resources, save time and manage multiple systems. The WAFER-ULT/ULT2-i1 supports IPMI 2.0 through the optional iRIS-1010 module. Follow the steps below to setup IPMI.

4.11.1 Managed System Hardware Setup

The hardware configuration of the managed system (WAFER-ULT/ULT2-i1) is described below.

Step 1: Install an iRIS-1010 module to the iRIS module slot (refer to **Section 4.4**).

Step 2: Make sure a DDR3L SO-DIMM is installed in the SO-DIMM socket.

Step 3: Connect an Ethernet cable to the RJ-45 connector labeled **LAN2** (**Figure 3-29**).

Chapter

5

BIOS

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.

NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

Press the **DEL** or **F2** key as soon as the system is turned on or

Press the **DEL** or **F2** key when the "**Press DEL or F2 to enter SETUP**" message appears on the screen.

If the message disappears before the **DEL or F2** key is pressed, restart the computer and try again.

5.1.2 Using Setup

Use the arrow keys to highlight items, press **ENTER** to select, use the PageUp and PageDown keys to change entries, press **F1** for help and press **ESC** to quit. Navigation keys are shown in the following table.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes
-	Decrease the numeric value or make changes

Key	Function
Page Up	Move to the previous page
Page Dn	Move to the next page
Esc	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2	Load previous values
F3	Load optimized defaults
F4	Save changes and Exit BIOS

Table 5-1: BIOS Navigation Keys

5.1.3 Getting Help

When **F1** is pressed, a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window, press **Esc**.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the clear CMOS button described in **Chapter 4**.

5.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

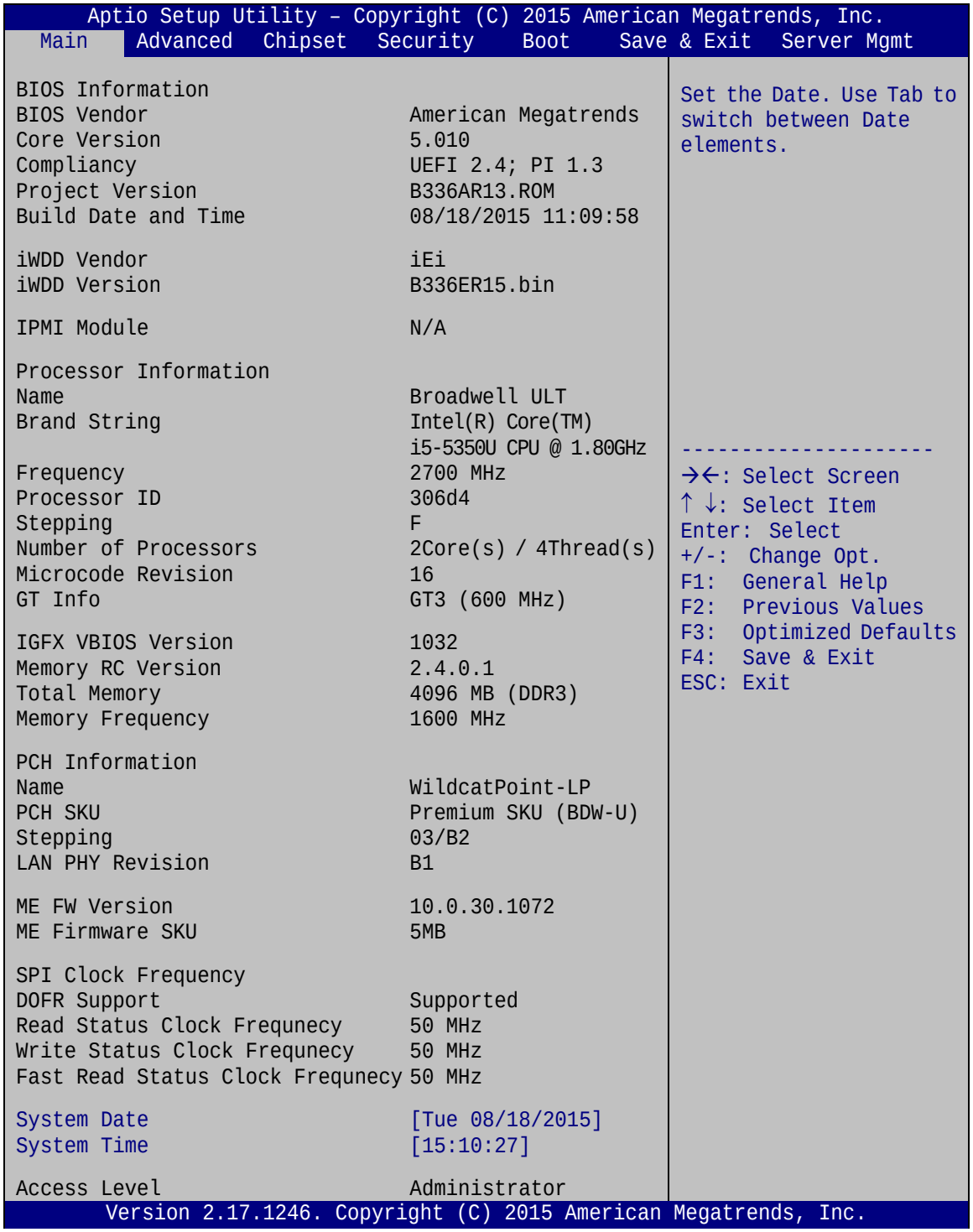
- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Boot – Changes the system boot configuration.
- Security – Sets User and Supervisor Passwords.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

5.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered.

The **Main** menu gives an overview of the basic system information.



BIOS Menu 1: Main

The Main menu has two user configurable fields:

System Date [xx/xx/xx]

Use the **System Date** option to set the system date. Manually enter the day, month and year.

System Time [xx:xx:xx]

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 2**) to configure the CPU and peripheral devices through the following sub-menus:

WARNING:

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.

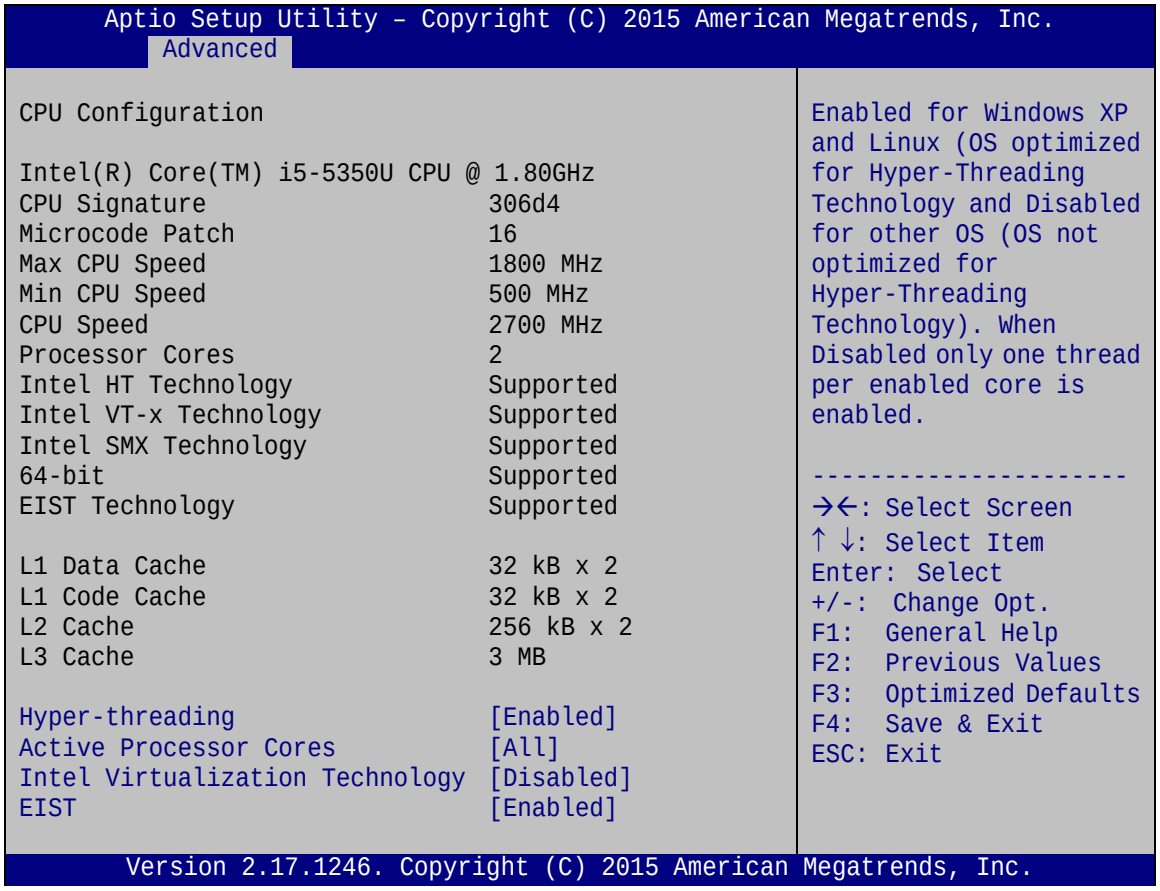
```
      Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
  Main    Advanced   Chipset   Security    Boot    Save & Exit   Server Mgmt

> CPU Configuration                                CPU Configuration
> ACPI Settings                                    Parameters
> AMT Configuration
> F81866 Super IO Configuration                    ----------------------
> iWDD H/W Monitor                                 →←: Select Screen
> RTC Wake Settings                                ↑ ↓: Select Item
> Serial Port Console Redirection                  Enter: Select
> SATA Configuration                               +/-: Change Opt.
> Intel(R) Rapid Start Technology                  F1:  General Help
> USB Configuration                                F2:  Previous Values
> iEi Feature                                      F3:  Optimized Defaults
                                                   F4:  Save & Exit
                                                   ESC: Exit
      Version 2.17.1246. Copyright (C) 2015 American Megatrends, Inc.
```

BIOS Menu 2: Advanced

5.3.1 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 3**) to view detailed CPU specifications.



BIOS Menu 3: CPU Configuration

Hyper-threading [Enabled]

Use the **Hyper-threading** BIOS option to enable or disable the Intel Hyper-Threading Technology.

- ➔ **Disabled** Disables the Intel Hyper-Threading Technology.
- ➔ **Enabled** **DEFAULT** Enables the Intel Hyper-Threading Technology.

Active Processor Cores [All]

Use the **Active Processor Cores** BIOS option to enable numbers of cores in the processor package.

- ➔ **All** **DEFAULT** Enable all cores in the processor package.
- ➔ **1** Enable one core in the processor package.

Intel Virtualization Technology [Disabled]

Use the **Intel Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel® Virtualization technology allows several OSs to run on the same system at the same time.

- ➔ **Disabled** **DEFAULT** Disables Intel Virtualization Technology.
- ➔ **Enabled** Enables Intel Virtualization Technology.

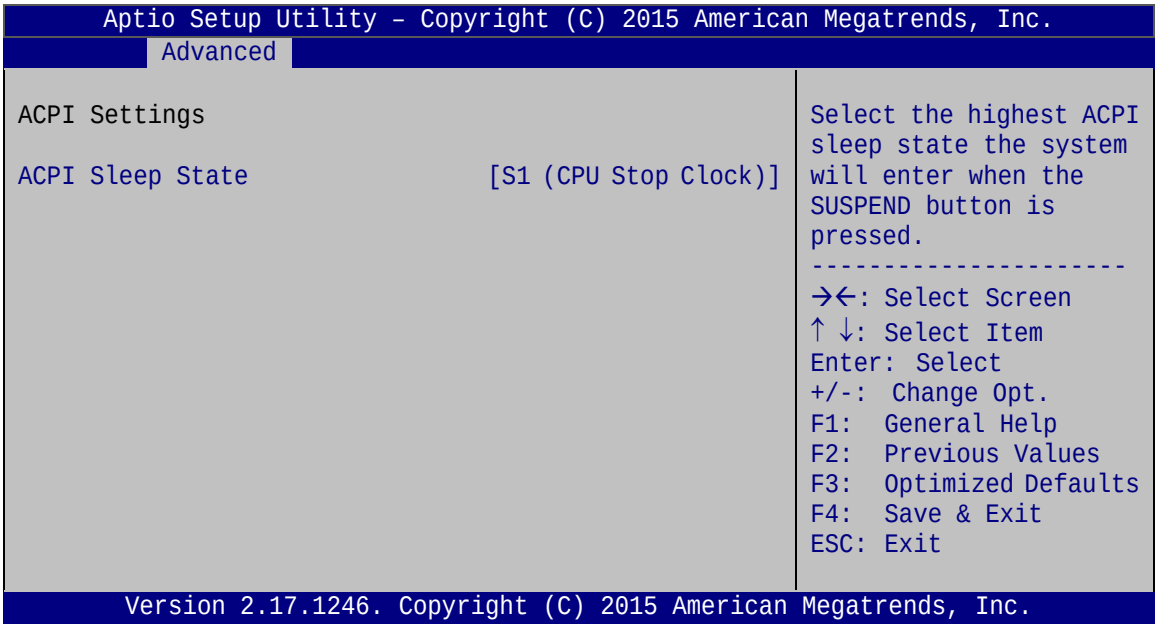
EIST [Enabled]

Use the **EIST** option to enable or disable the Enhanced Intel® SpeedStep Technology (EIST).

- ➔ **Disabled** Disables Enhanced Intel® SpeedStep Technology
- ➔ **Enabled** **DEFAULT** Enables Enhanced Intel® SpeedStep Technology

5.3.2 ACPI Settings

The **ACPI Settings** menu (**BIOS Menu 4**) configures the Advanced Configuration and Power Interface (ACPI) options.



BIOS Menu 4: ACPI Settings

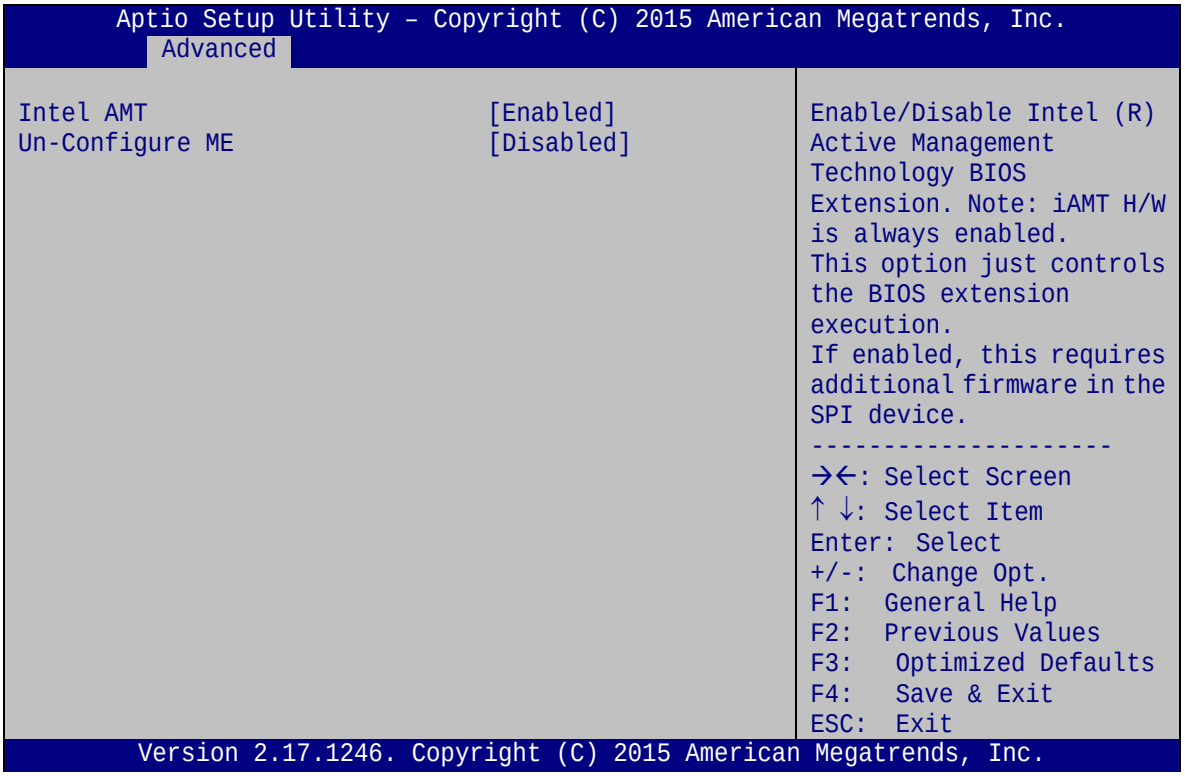
ACPI Sleep State [S1 (CPU Stop Clock)]

Use the **ACPI Sleep State** option to specify the sleep state the system enters when it is not being used.

➔ **S1 (CPU Stop Clock)**	**DEFAULT**	The system enters S1 (POS) sleep state. The system appears off. The CPU is stopped; RAM is refreshed; the system is running in a low power mode.
➔ **S3 (Suspend to RAM)**		The caches are flushed and the CPU is powered off. Power to the RAM is maintained. The computer returns slower to a working state, but more power is saved.

5.3.3 AMT Configuration

The **AMT Configuration** menu (**BIOS Menu 5**) allows the Intel® AMT options to be configured.



BIOS Menu 5: AMT Configuration

Intel AMT [Enabled]

Use **Intel AMT** option to enable or disable the Intel® AMT function.

- ➔ **Disabled** Intel® AMT is disabled
- ➔ **Enabled** **DEFAULT** Intel® AMT is enabled

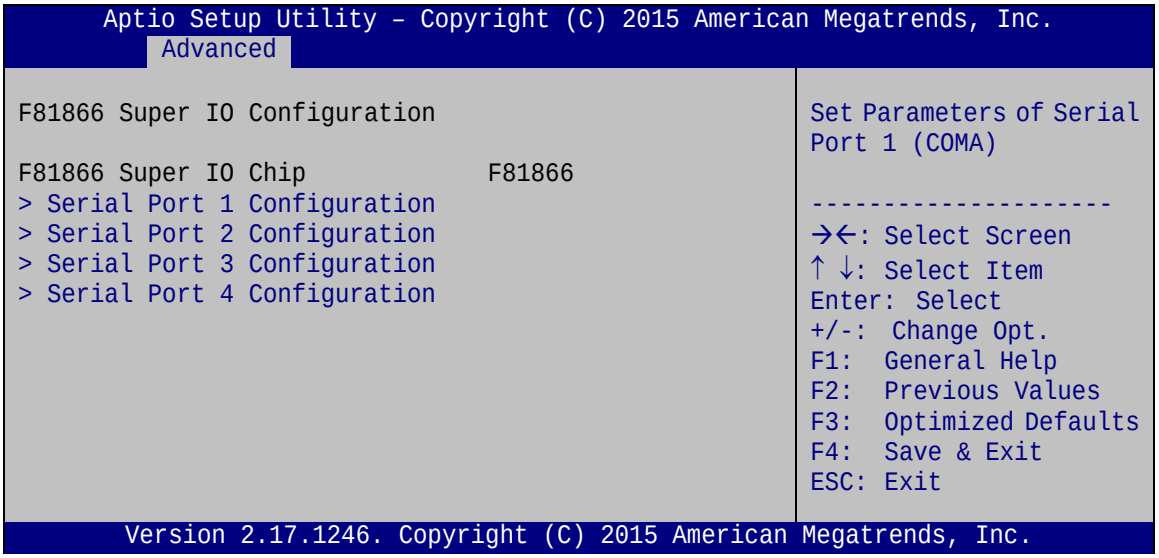
Un-Configure ME [Disabled]

Use the **Un-Configure ME** option to perform ME unconfigure without password operation.

- ➔ **Disabled** **DEFAULT** Not perform ME unconfigure
- ➔ **Enabled** To perform ME unconfigure

5.3.4 F81866 Super IO Configuration

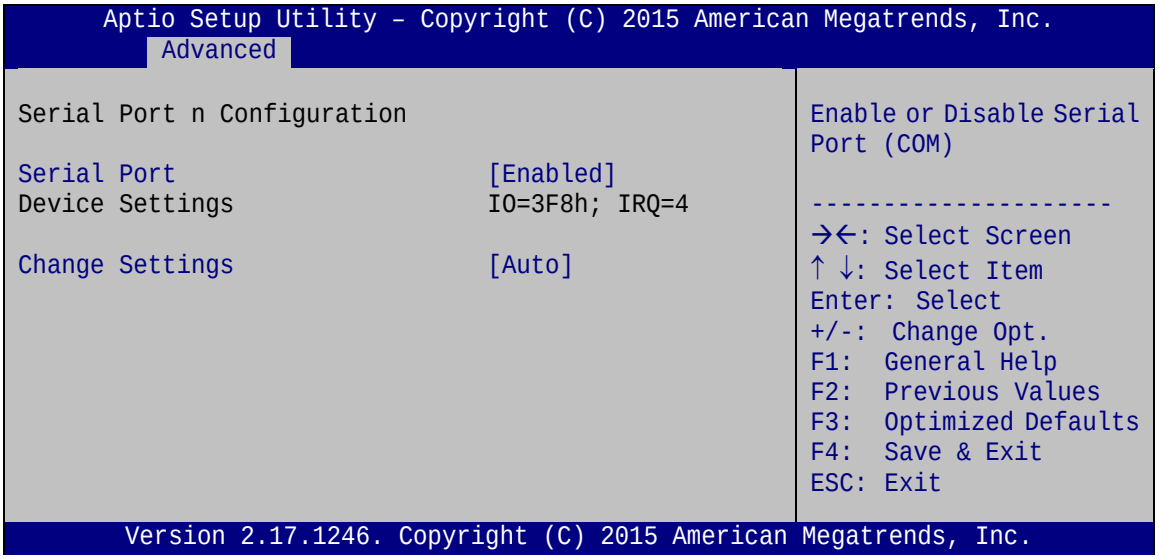
Use the **F81866 Super IO Configuration** menu (**BIOS Menu 6**) to set or change the configurations for the serial ports.



BIOS Menu 6: F81866 Super IO Configuration

5.3.4.1 Serial Port n Configuration

Use the **Serial Port n Configuration** menu (**BIOS Menu 7**) to configure the serial port n.



BIOS Menu 7: Serial Port n Configuration Menu

5.3.4.1.1 Serial Port 1 Configuration

Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

➔	**Disabled**		Disable the serial port
➔	**Enabled**	**DEFAULT**	Enable the serial port

Change Settings [Auto]

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔	**Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔	**IO=3F8h; IRQ=4**		Serial Port I/O port address is 3F8h and the interrupt address is IRQ4
➔	**IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 3F8h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12
➔	**IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 2F8h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12
➔	**IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 3E8h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12
➔	**IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 2E8h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12

5.3.4.1.2 Serial Port 2 Configuration

Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

➔	**Disabled**		Disable the serial port
➔	**Enabled**	**DEFAULT**	Enable the serial port

Change Settings [Auto]

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔	**Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔	**IO=2F8h; IRQ=3**		Serial Port I/O port address is 2F8h and the interrupt address is IRQ3
➔	**IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 3F8h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12
➔	**IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 2F8h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12
➔	**IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 3E8h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12
➔	**IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 2E8h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12

5.3.4.1.3 Serial Port 3 Configuration

Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

➔	**Disabled**		Disable the serial port
➔	**Enabled**	**DEFAULT**	Enable the serial port

Change Settings [Auto]

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔	**Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔	**IO=3E8h; IRQ=11**		Serial Port I/O port address is 3E8h and the interrupt address is IRQ11
➔	**IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 3E8h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12
➔	**IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 2E8h and the interrupt address is IRQ3, 4, 5, 6, 7, 10, 11, 12
➔	**IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 2F0h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12
➔	**IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 2E0h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12

5.3.4.1.4 Serial Port 4 Configuration

Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

➔	**Disabled**		Disable the serial port
➔	**Enabled**	**DEFAULT**	Enable the serial port

Change Settings [Auto]

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔	**Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔	**IO=2E8h; IRQ=11**		Serial Port I/O port address is 2E8h and the interrupt address is IRQ11
➔	**IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 3E8h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12
➔	**IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 2E8h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12
➔	**IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 2F0h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12
➔	**IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**		Serial Port I/O port address is 2E0h and the interrupt address is IRQ3, 4, 5, 6, 7, 9, 10, 11, 12

5.3.5 iWDD H/W Monitor

The **iWDD H/W Monitor** menu (**BIOS Menu 8**) contains the fan configuration submenu and displays the system temperatures and voltages.

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
        Advanced
PC Health Status                                Smart Fan Mode Select

CPU temperature                 : +45C
System temperature              : +40 C

CPU_FAN1 Speed                  : N/A           ---------------------
                                                →←: Select Screen
CPU_CORE                        : +1.772 V      ↑ ↓: Select Item
+5V                             : +5.051 V      Enter: Select
+12V                            : +11.101 V     +/-: Change Opt.
+DDR                            : +1.334 V      F1: General Help
+5VSB                           : +5.034 V      F2: Previous Values
+3.3V                           : +3.265 V      F3: Optimized Defaults
+3.3VSB                         : +3.213 V      F4: Save & Exit
                                                ESC: Exit
> Smart Fan Mode Configuration
        Version 2.17.1246. Copyright (C) 2015 American Megatrends, Inc.
```

BIOS Menu 8: iWDD H/W Monitor

5.3.5.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 9**) to configure the smart fan temperature and speed settings.

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
        Advanced
Smart Fan Mode Configuration                    SYS Smart Fan control
                                                settings
CPU_FAN1 Smart Fan Control      [Auto Mode]
Auto mode fan start temperature 50              ---------------------
Auto mode fan off temperature   40              →←: Select Screen
Auto mode fan start PWM         30              ↑ ↓: Select Item
Auto mode fan slope PWM         1               Enter: Select
                                                +/-: Change Opt.
                                                F1: General Help
                                                F2: Previous Values
                                                F3: Optimized Defaults
                                                F4: Save & Exit
                                                ESC: Exit
        Version 2.17.1246. Copyright (C) 2015 American Megatrends, Inc.
```

BIOS Menu 9: Smart Fan Mode Configuration

CPU_FAN1 Smart Fan Control [Auto Mode]

Use the **CPU_FAN1 Smart Fan Control** option to configure the system fan.

➔	**Manual Mode**		The fan spins at the speed set in Manual PWM Setting settings.
➔	**Auto Mode**	**DEFAULT**	The fan adjusts its speed using Auto PWM Mode settings.

Auto mode fan start/off temperature

Use the + or – key to change the **Auto mode fan start/off temperature** value. Enter a decimal number between 1 and 100.

Auto mode fan start PWM

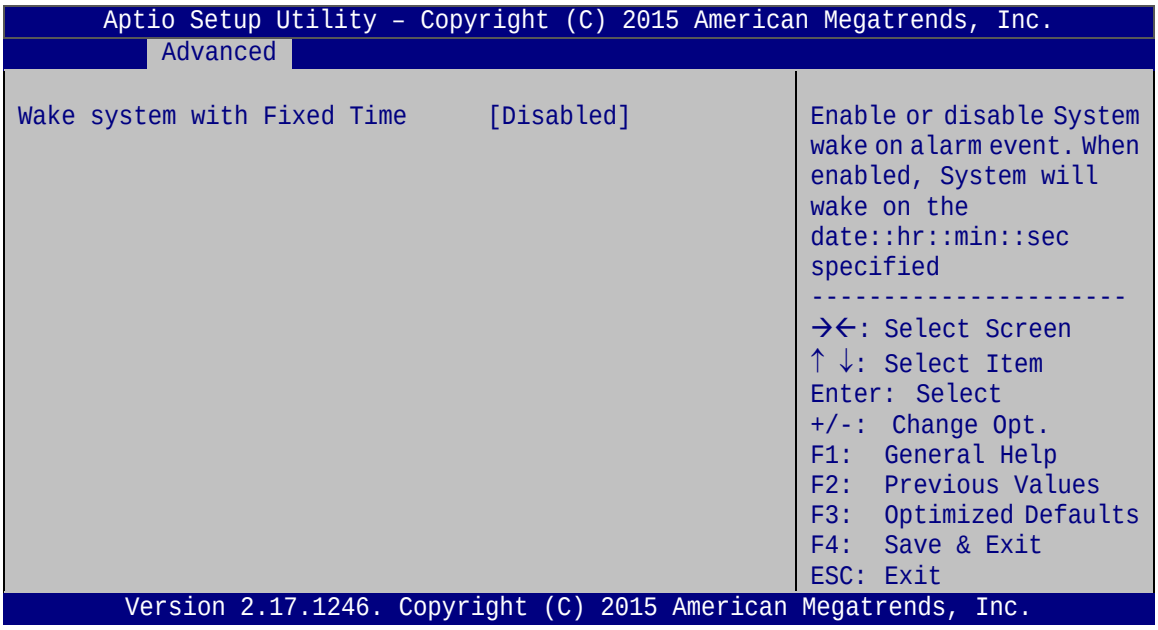
Use the + or – key to change the **Auto mode fan start PWM** value. Enter a decimal number between 1 and 100.

Auto mode fan slope PWM

Use the + or – key to change the **Auto mode fan slope PWM** value. Enter a decimal number between 1 and 8.

5.3.6 RTC Wake Settings

The **RTC Wake Settings** menu (**BIOS Menu 10**) enables the system to wake at the specified time.



BIOS Menu 10: RTC Wake Settings

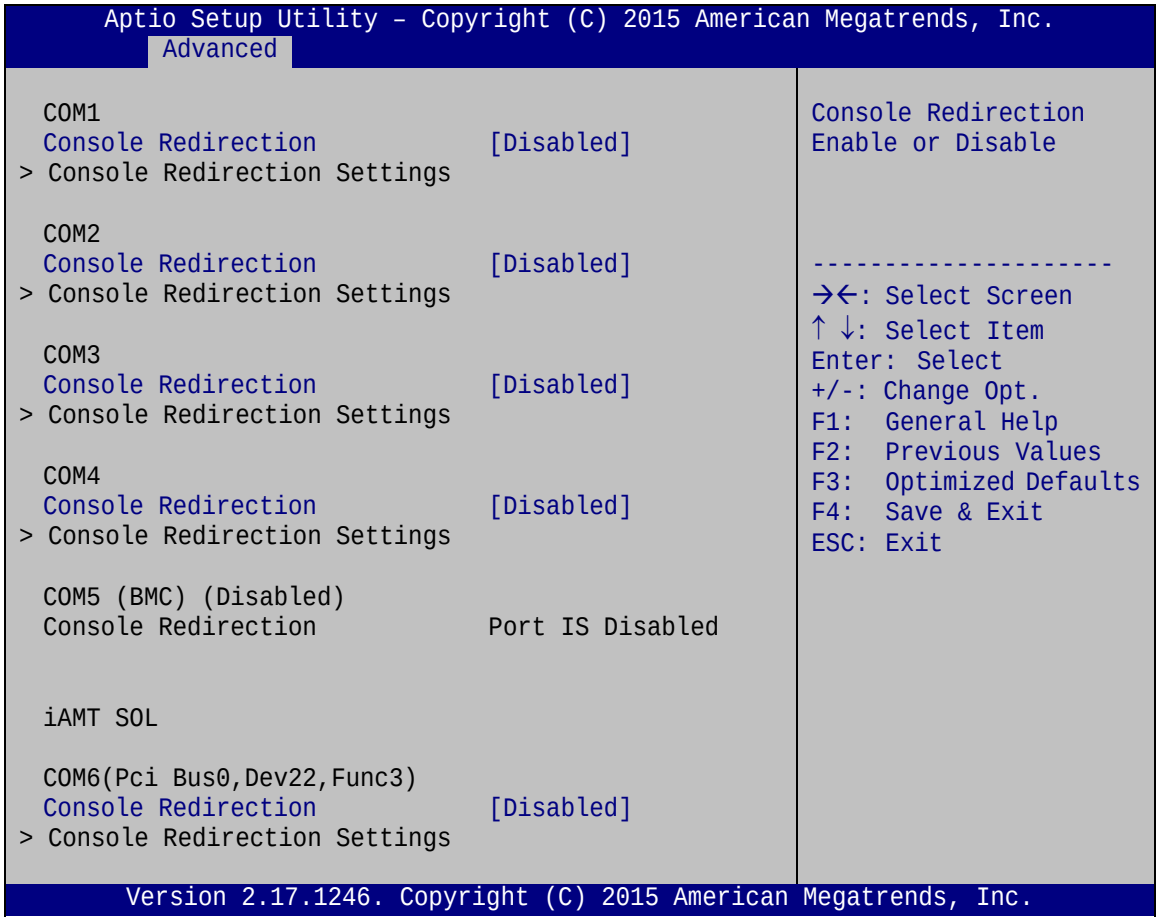
Wake system with Fixed Time [Disabled]

Use the **Wake system with Fixed Time** option to enable or disable the system wake on alarm event.

➔ **Disabled**	**DEFAULT**	The real time clock (RTC) cannot generate a wake event
➔ **Enabled**		If selected, the **Wake up every day** option appears allowing you to enable to disable the system to wake every day at the specified time. Besides, the following options appear with values that can be selected: Wake up every day Wake up date Wake up hour Wake up minute Wake up second After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

5.3.7 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 11**) allows the console redirection options to be configured. Console redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



BIOS Menu 11: Serial Port Console Redirection

Console Redirection [Disabled]

Use **Console Redirection** option to enable or disable the console redirection function.

- ➔ **Disabled** **DEFAULT** Disabled the console redirection function
- ➔ **Enabled** Enabled the console redirection function

NOTE:

The following options are available in the **Console Redirection Settings** submenu when the **Console Redirection** option is enabled.

Terminal Type [ANSI]

Use the **Terminal Type** option to specify the remote terminal type.

➔	**VT100**		The target terminal type is VT100
➔	**VT100+**		The target terminal type is VT100+
➔	**VT-UTF8**		The target terminal type is VT-UTF8
➔	**ANSI**	**DEFAULT**	The target terminal type is ANSI

Bits per second [115200]

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match the other side. Long or noisy lines may require lower speeds.

➔	**9600**		Sets the serial port transmission speed at 9600.
➔	**19200**		Sets the serial port transmission speed at 19200.
➔	**57600**		Sets the serial port transmission speed at 57600.
➔	**115200**	**DEFAULT**	Sets the serial port transmission speed at 115200.

Data Bits [8]

Use the **Data Bits** option to specify the number of data bits.

➔	**7**		Sets the data bits at 7.
➔	**8**	**DEFAULT**	Sets the data bits at 8.

Parity [None]

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

➔	**None**	**DEFAULT**	No parity bit is sent with the data bits.
➔	**Even**		The parity bit is 0 if the number of ones in the data bits is even.
➔	**Odd**		The parity bit is 0 if the number of ones in the data bits is odd.
➔	**Mark**		The parity bit is always 1. This option does not provide error detection.
➔	**Space**		The parity bit is always 0. This option does not provide error detection.

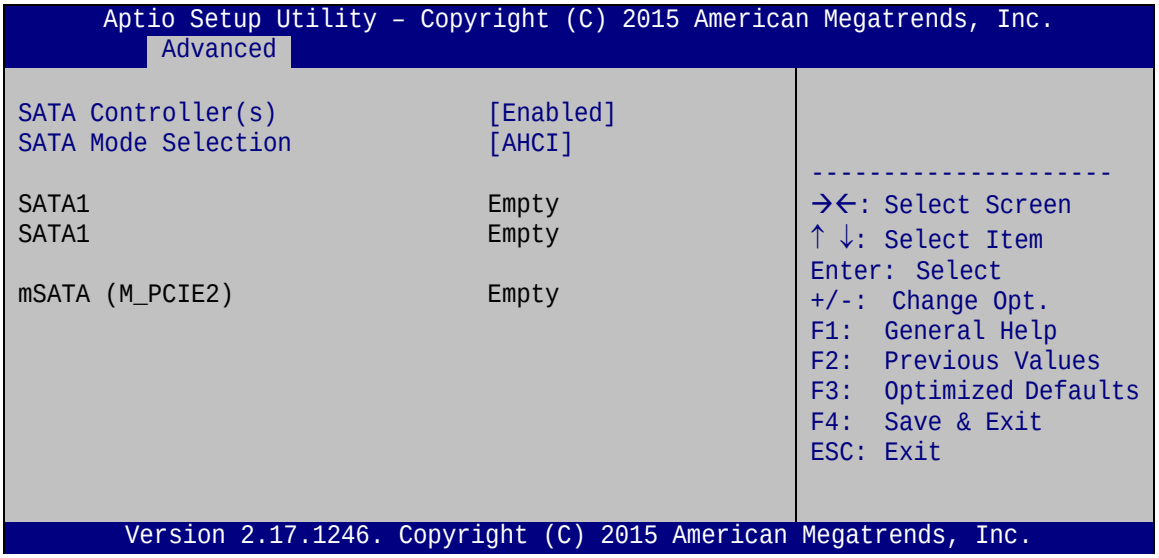
Stop Bits [1]

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

➔	**1**	**DEFAULT**	Sets the number of stop bits at 1.
➔	**2**		Sets the number of stop bits at 2.

5.3.8 SATA Configuration

Use the **SATA Configuration** menu (**BIOS Menu 12**) to change and/or set the configuration of the SATA devices installed in the system.



BIOS Menu 12: SATA Configuration

SATA Controller(s) [Enabled]

Use the **SATA Controller(s)** option to configure the SATA controller.

- **Enabled** **DEFAULT** Enable SATA controller.
- **Disabled** Disable SATA controller.

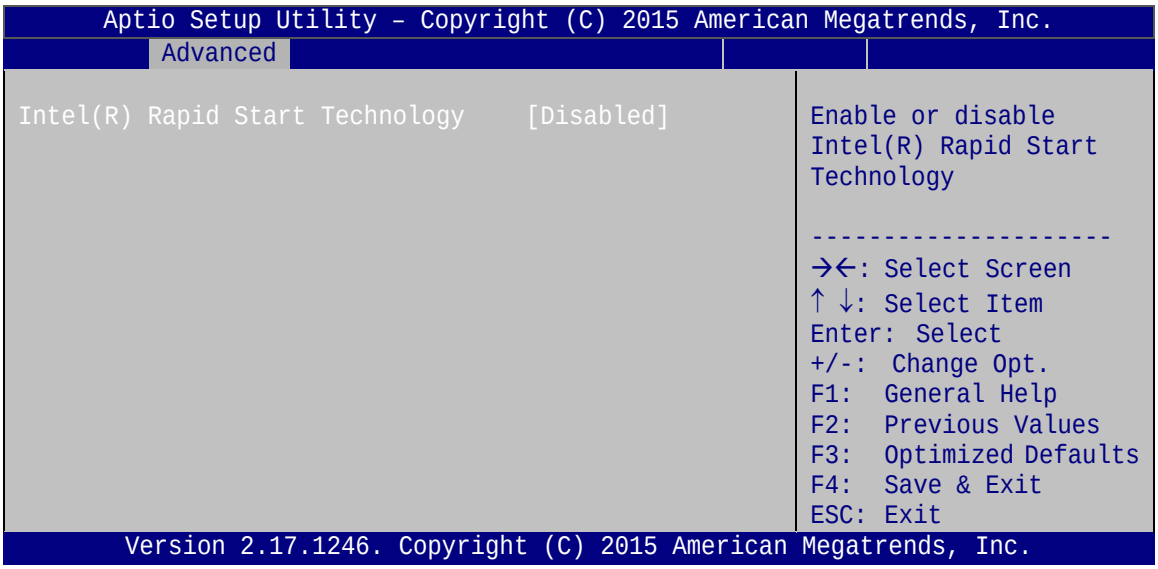
SATA Mode Selection [AHCI]

Use the **SATA Mode Selection** option to configure SATA devices.

- **AHCI** **DEFAULT** Configures SATA devices as AHCI device.
- **RAID** Configures SATA devices as RAID device.

5.3.9 Intel(R) Rapid Start Technology

Use the **Intel(R) Rapid Start Technology** (**BIOS Menu 13**) menu to configure Intel® Rapid Start Technology support.



BIOS Menu 13: Intel(R) Rapid Start Technology

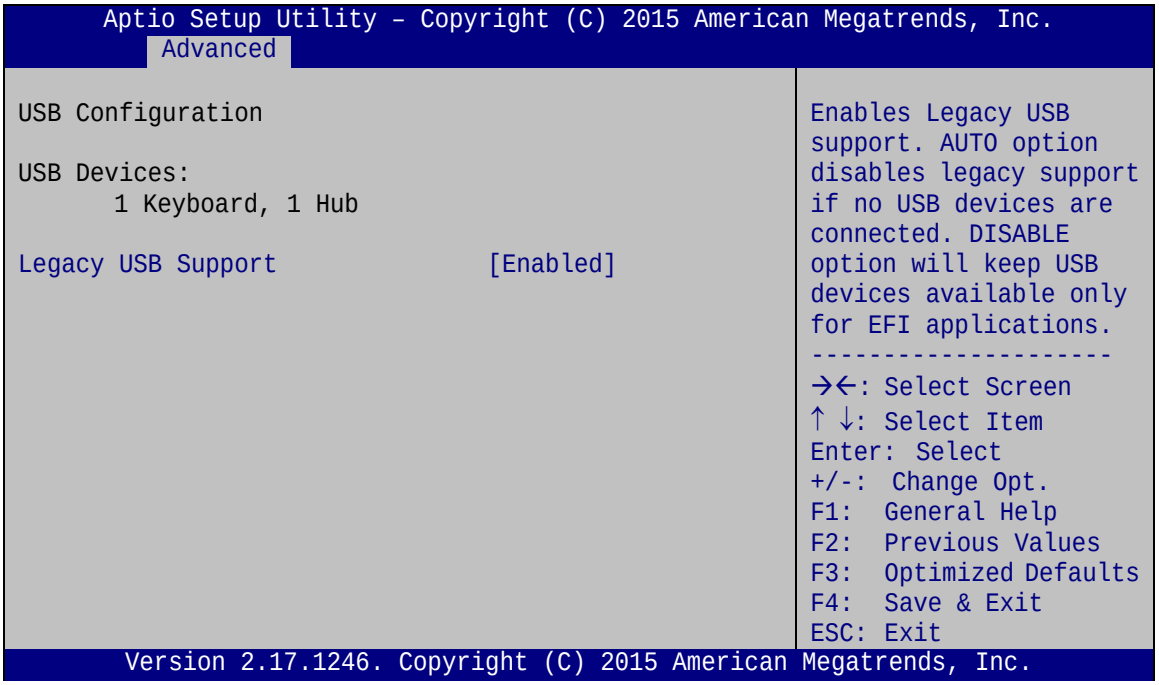
Intel(R) Rapid Start Technology [Disabled]

Use **Intel(R) Rapid Start Technology** option to enable or disable the Intel® Rapid Start Technology function.

➔	**Disabled**	**DEFAULT**	Intel® Rapid Start Technology is disabled
➔	**Enabled**		Intel® Rapid Start Technology is enabled

5.3.10 USB Configuration

Use the **USB Configuration** menu (**BIOS Menu 14**) to read USB configuration information and configure the USB settings.



BIOS Menu 14: USB Configuration

USB Devices

The **USB Devices** field lists the USB devices that are enabled on the system

Legacy USB Support [Enabled]

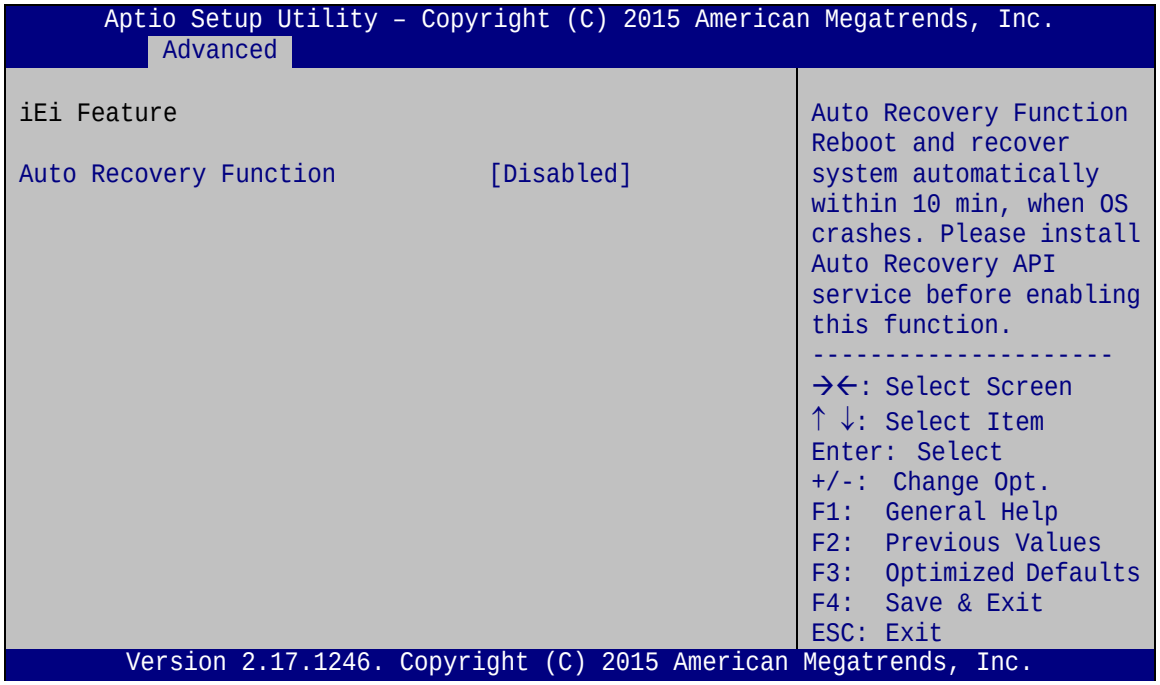
Use the **Legacy USB Support** BIOS option to enable USB mouse and USB keyboard support.

Normally if this option is not enabled, any attached USB mouse or USB keyboard does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.

➔	**Enabled**	**DEFAULT**	Legacy USB support enabled
➔	**Disabled**		Legacy USB support disabled
➔	**Auto**		Legacy USB support disabled if no USB devices are connected

5.3.11 iEi Feature

Use the **iEi Feature** menu (**BIOS Menu 15**) to configure One Key Recovery function.



BIOS Menu 15: iEi Feature

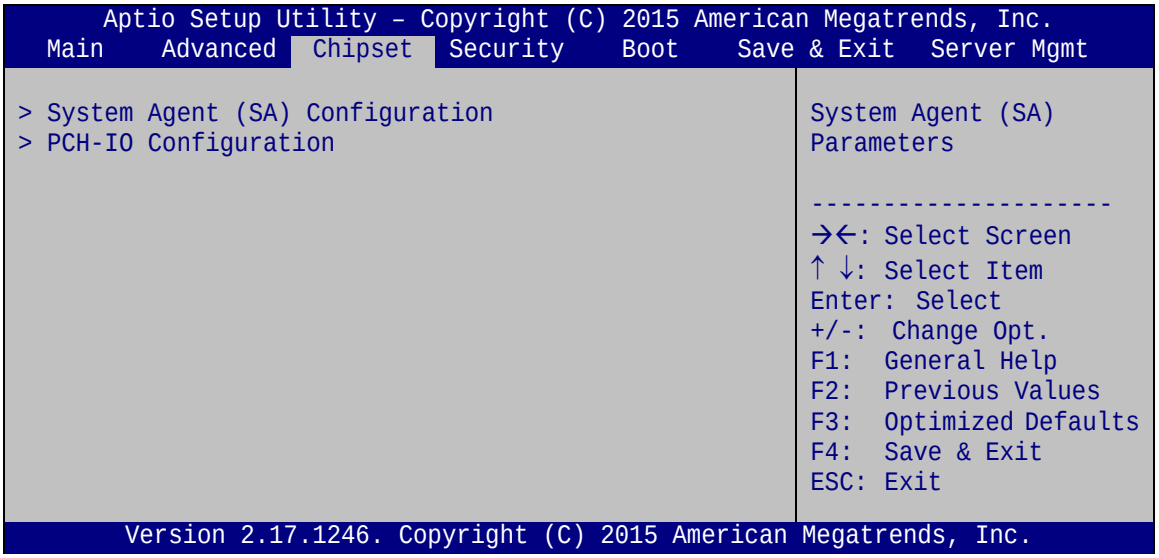
Auto Recovery Function [Disabled]

Use the **Auto Recovery Function** BIOS option to enable or disable the auto recovery function of the IEI One Key Recovery.

➔	**Disabled**	**DEFAULT**	Auto recovery function disabled
➔	**Enabled**		Auto recovery function enabled

5.4 Chipset

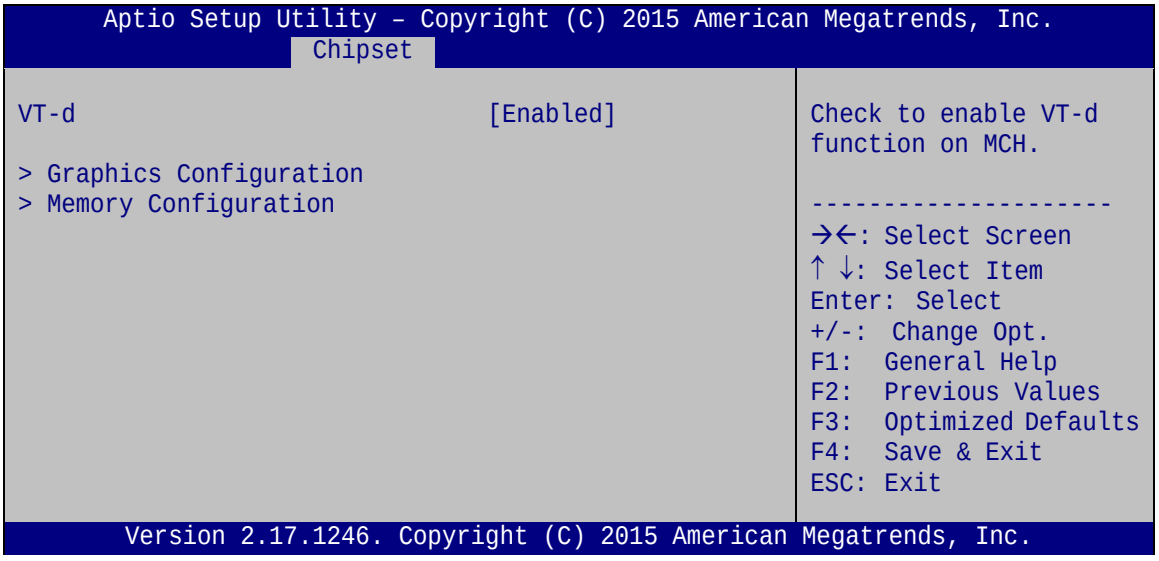
Use the **Chipset** menu (**BIOS Menu 16**) to access the PCH-IO and System Agent (SA) configuration menus.



BIOS Menu 16: Chipset

5.4.1 System Agent (SA) Configuration

Use the **System Agent (SA) Configuration** menu (**BIOS Menu 17**) to display the memory information.



BIOS Menu 17: System Agent (SA) Configuration

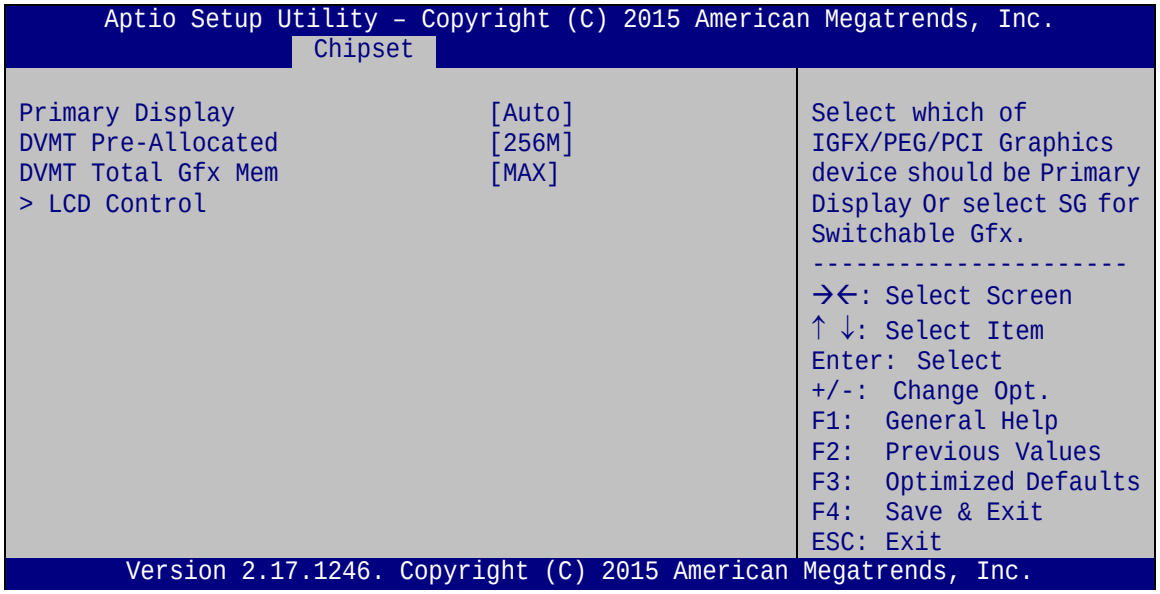
VT-d [Enabled]

Use the **VT-d** option to enable or disable VT-d support.

➔	**Disabled**		Disables VT-d support.
➔	**Enabled**	**DEFAULT**	Enables VT-d support.

5.4.1.1 Graphics Configuration

Use the **Graphics Configuration** (**BIOS Menu 18**) menu to configure the video device connected to the system.



BIOS Menu 18: Graphics Configuration

Primary Display [Auto]

Use the **Primary Display** option to select the display device used by the system when it boots. Configuration options are listed below.

- Auto **DEFAULT**
- IGFX
- PCIE

DVMT Pre-Allocated [256M]

Use the **DVMT Pre-Allocated** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

- 32M
- 64M
- 128M
- 256M **Default**
- 512M

DVMT Total Gfx Mem [MAX]

Use the **DVMT Total Gfx Mem** option to select DVMT5.0 total graphic memory size used by the internal graphic device. The following options are available:

- 128M
- 256M
- MAX **Default**

5.4.1.1.1 LCD Control

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
                    Chipset

LCD Control                                  | Select the video Device
                                             | which will be activated
Primary IGFX Boot Display       [VBIOS Default] | during POST. This has no
Backlight Control Type          [LED(PWM)]   | effect if external
                                             | graphics present.
                                             | Secondary boot display
                                             | selection will appear
                                             | based on your selection.
                                             | VGA modes will be
                                             | supported only on
                                             | primary display.
                                             | ----------------------
                                             | →←: Select Screen
                                             | ↑ ↓: Select Item
                                             | Enter: Select
                                             | +/-: Change Opt.
                                             | F1: General Help
                                             | F2: Previous Values
                                             | F3: Optimized Defaults
                                             | F4: Save & Exit
                                             | ESC: Exit
Version 2.17.1246. Copyright (C) 2015 American Megatrends, Inc.
```

BIOS Menu 19: LCD Control

Primary IGFX Boot Display [VBIOS Default]

Use the **Primary IGFX Boot Display** option to select the display device used by the system when it boots. Configuration options are listed below.

- VBIOS Default **DEFAULT**
- CRT
- LVDS
- DP

Backlight Control Type [LED(PWM)]

Use the **Backlight Control Type** BIOS option to select the LCD backlight control type. Configuration options are listed below.

- LED(PWM) **DEFAULT**
- CCFL(Linear)

Backlight Voltage Level

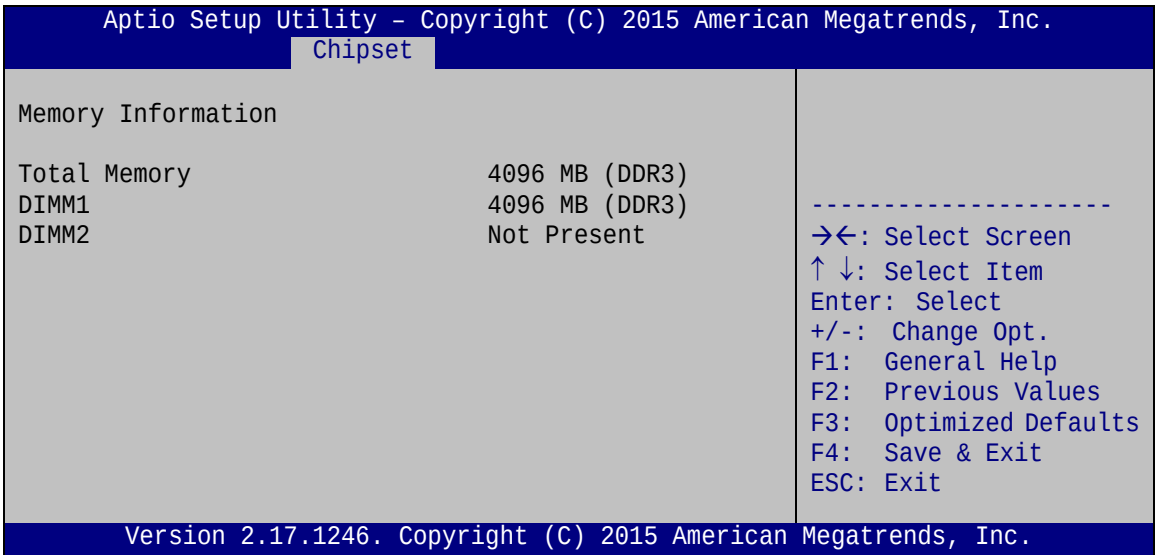
The **Backlight Voltage Level** option is available only when the **Backlight Control Type** option is set to **CCFL(Linear)**. Use this BIOS option to select the LCD backlight dimming voltage level from **5V** or **3.3V**.

NOTE:

The **Backlight Voltage Level** BIOS setting will be fixed to **5V** when the DC 5V jumper for LVDS backlight dimming is being closed. Refer to **Section 4.7.1** for detailed information.

5.4.1.2 Memory Configuration

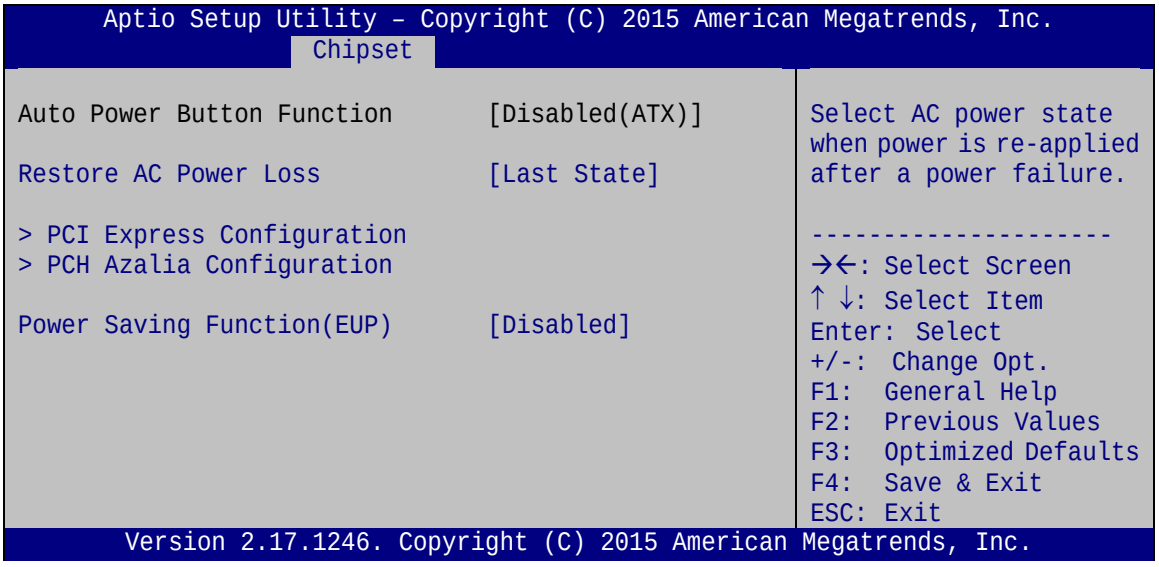
Use the **Memory Configuration** submenu (**BIOS Menu 20**) to view memory information.



BIOS Menu 20: Memory Configuration

5.4.2 PCH-IO Configuration

Use the **PCH-IO Configuration** menu (**BIOS Menu 21**) to configure the PCH parameters.



BIOS Menu 21: PCH-IO Configuration

Restore AC Power Loss [Last State]

Use the **Restore AC Power Loss** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system.

➔ **Power Off**		The system remains turned off
➔ **Power On**		The system turns on
➔ **Last State**	**DEFAULT**	The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

Power Saving Function(EUP) [Disabled]

Use the **Power Saving Function(EUP)** BIOS option to enable or disable the power saving function.

➔ **Disabled**	**DEFAULT**	Power saving function is disabled.
➔ **Enabled**		Power saving function is enabled. It will reduce power consumption when the system is off.

5.4.2.1 PCI Express Configuration

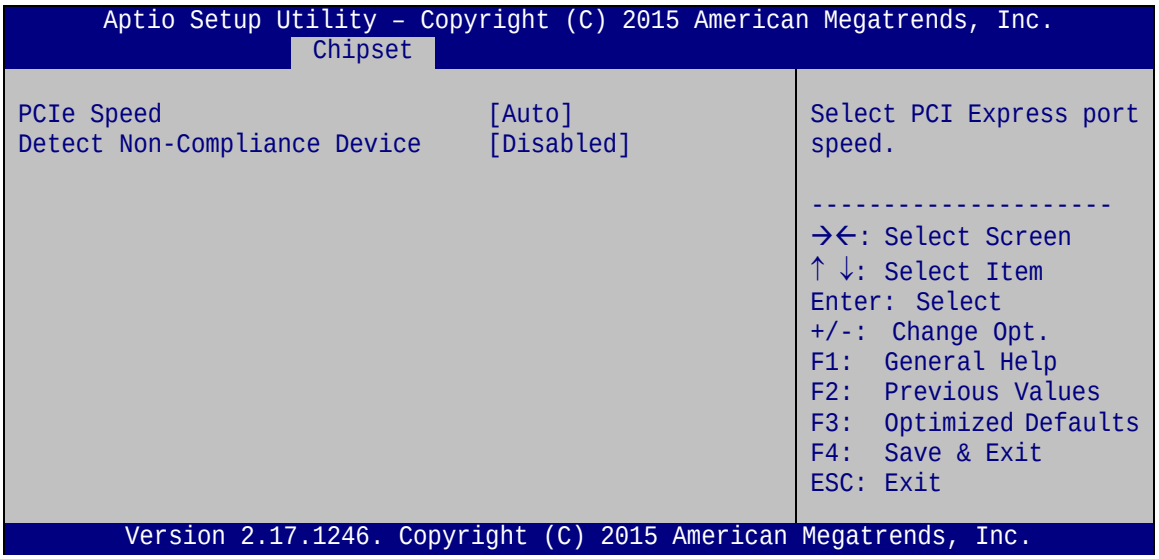
Use the **PCI Express Configuration** menu (**BIOS Menu 22**) to configure the PCIe Mini slot.

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
                    Chipset
PCI Express Configuration                  | M_PCIE2 Settings.
                                           |
> M_PCIE2                                  | ----------------------
                                           | →←: Select Screen
                                           | ↑ ↓: Select Item
                                           | Enter: Select
                                           | +/-: Change Opt.
                                           | F1: General Help
                                           | F2: Previous Values
                                           | F3: Optimized Defaults
                                           | F4: Save & Exit
                                           | ESC: Exit
Version 2.17.1246. Copyright (C) 2015 American Megatrends, Inc.
```

BIOS Menu 22: PCI Express Configuration

5.4.2.1.1 M_PCIE2

Use the **M_PCIE2** menu (**BIOS Menu 23**) to configure the **M_PCIE2** slot settings.



BIOS Menu 23: M_PCIE2 Configuration Menu

PCIe Speed [Auto]

Use this option to select the support type of the PCIe Mini slot. The following options are available:

- Auto **Default**
- Gen1
- Gen2

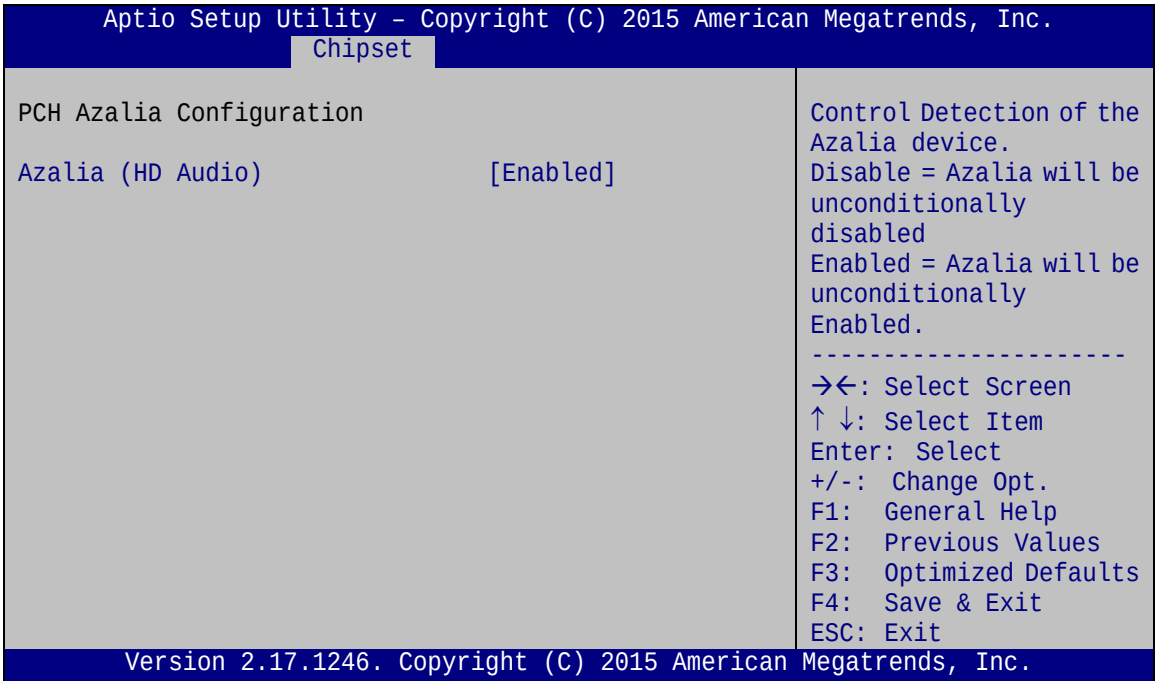
Detect Non-Compliance Device [Disabled]

Use the **Detect Non-Compliance Device** option to enable or disable detecting if a non-compliance PCI Express device is connected to the PCI Express slot.

➔	**Disabled**	**DEFAULT**	Disables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.
➔	**Enabled**		Enables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.

5.4.2.2 PCH Azalia Configuration

Use the **PCH Azalia Configuration** menu (**BIOS Menu 24**) to configure the PCH Azalia settings.



BIOS Menu 24: PCH Azalia Configuration

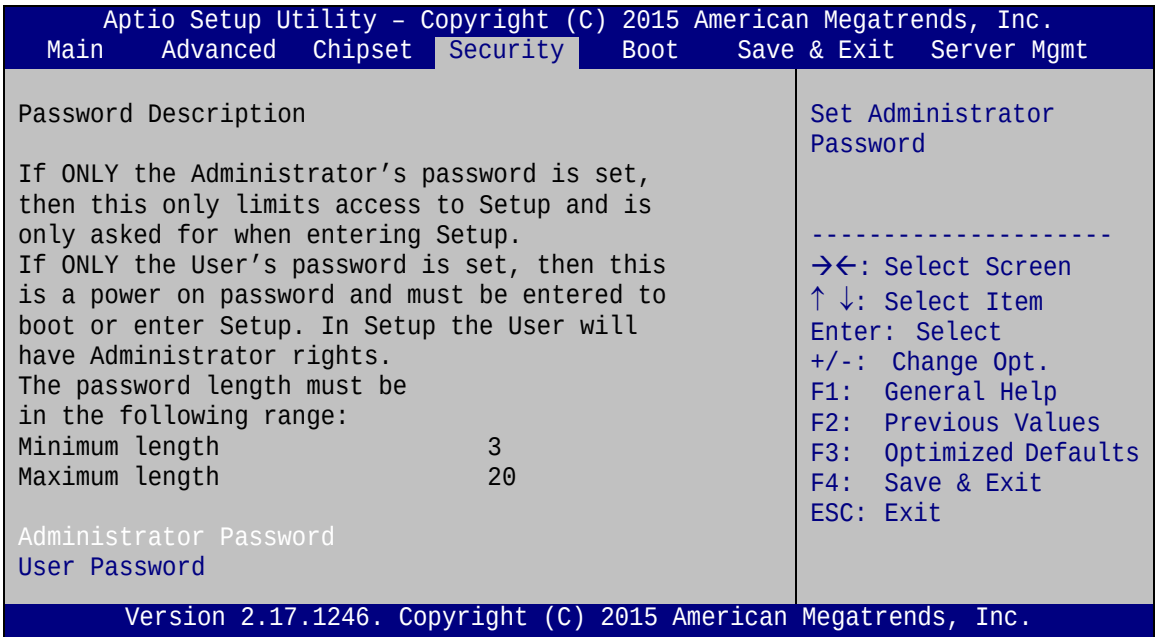
Azalia (HD Audio) [Enabled]

Use the **Azalia (HD Audio)** option to enable or disable the High Definition Audio controller.

- ➔ **Disabled** The onboard High Definition Audio controller is disabled
- ➔ **Enabled** **DEFAULT** The onboard High Definition Audio controller automatically detected and enabled

5.5 Security

Use the **Security** menu (**BIOS Menu 25**) to set system and user passwords.



BIOS Menu 25: Security

Administrator Password

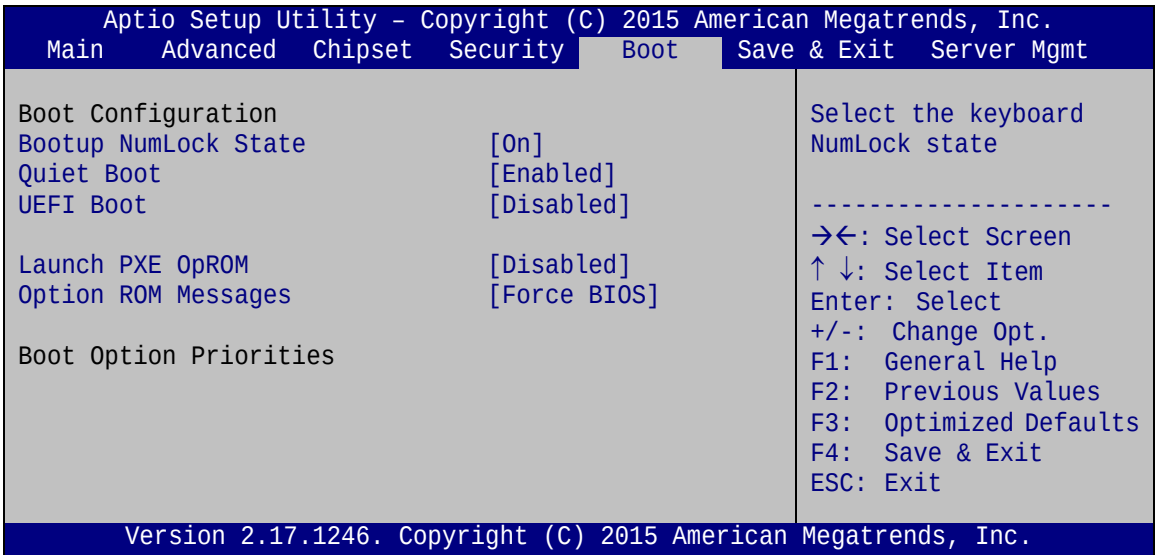
Use the **Administrator Password** to set or change an administrator password.

User Password

Use the **User Password** to set or change a user password.

5.6 Boot

Use the **Boot menu** (**BIOS Menu 26**) to configure system boot options.



BIOS Menu 26: Boot

Bootup NumLock State [On]

Use the **Bootup NumLock State** BIOS option to specify if the number lock setting must be modified during boot up.

- ➔ **On** **DEFAULT** Allows the Number Lock on the keyboard to be enabled automatically when the computer system boots up. This allows the immediate use of the 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard is lit.
- ➔ **Off** Does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard lights up when the Number Lock is engaged.

Quiet Boot [Enabled]

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

➔	**Disabled**		Normal POST messages displayed
➔	**Enabled**	**DEFAULT**	OEM Logo displayed instead of POST messages

UEFI Boot [Disabled]

Use the **UEFI Boot** option to enable or disable to boot from the UEFI devices.

➔	**Enabled**		Boot from UEFI devices is enabled.
➔	**Disabled**	**DEFAULT**	Boot from UEFI devices is disabled.

Launch PXE OpROM [Disabled]

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

➔	**Disabled**	**DEFAULT**	Ignore all PXE Option ROMs
➔	**Enabled**		Load PXE Option ROMs.

Option ROM Messages [Force BIOS]

Use the **Option ROM Messages** option to set the Option ROM display mode.

➔	**Force BIOS**	**DEFAULT**	Sets display mode to force BIOS.
➔	**Keep Current**		Sets display mode to current.

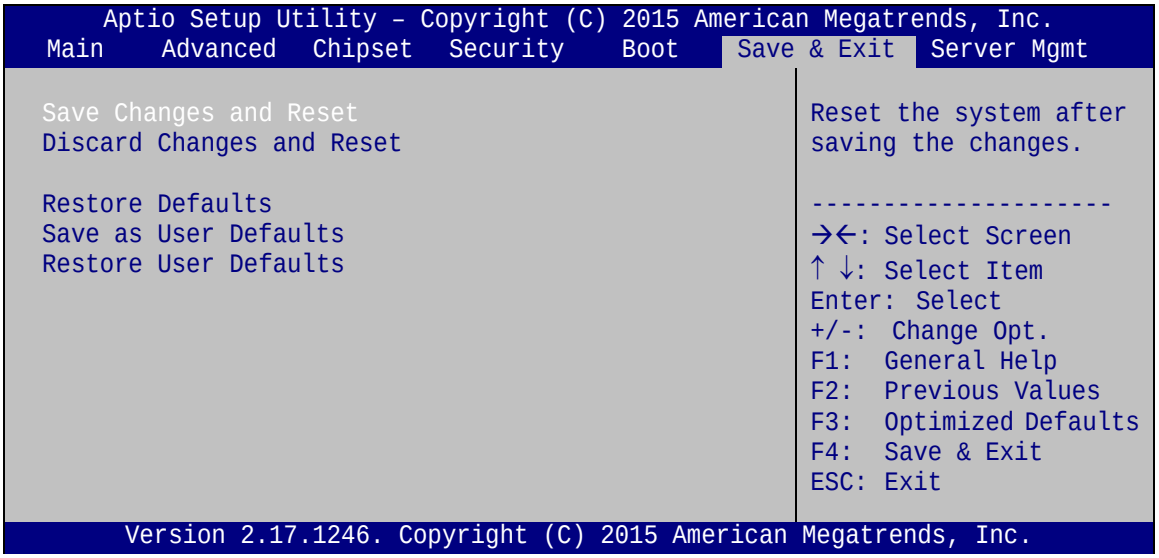
Boot option filter [Legacy only]

Use the **Boot option filter** option to control what devices the system can boot to.

- UEFI and Legacy
- Legacy only **DEFAULT**
- UEFI only

5.7 Save & Exit

Use the **Save & Exit** menu (**BIOS Menu 27**) to load default BIOS values, optimal failsafe values and to save configuration changes.



BIOS Menu 27: Save & Exit

Save Changes and Reset

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and reset the system.

Discard Changes and Reset

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

Restore Defaults

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

Save as User Defaults

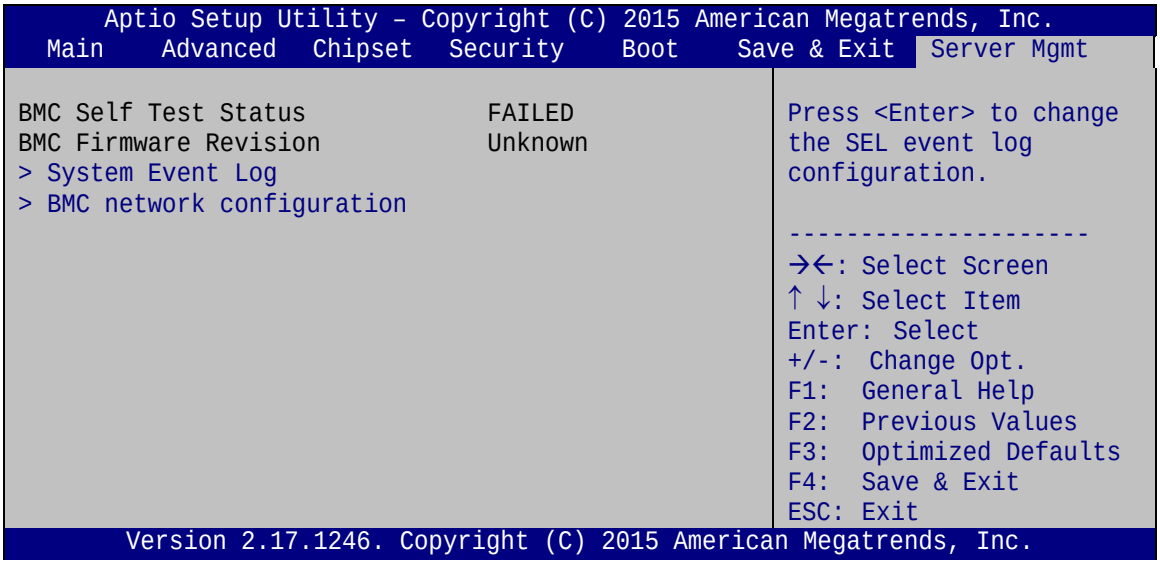
Use the **Save as User Defaults** option to save the changes done so far as user defaults.

Restore User Defaults

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

5.8 Server Mgmt

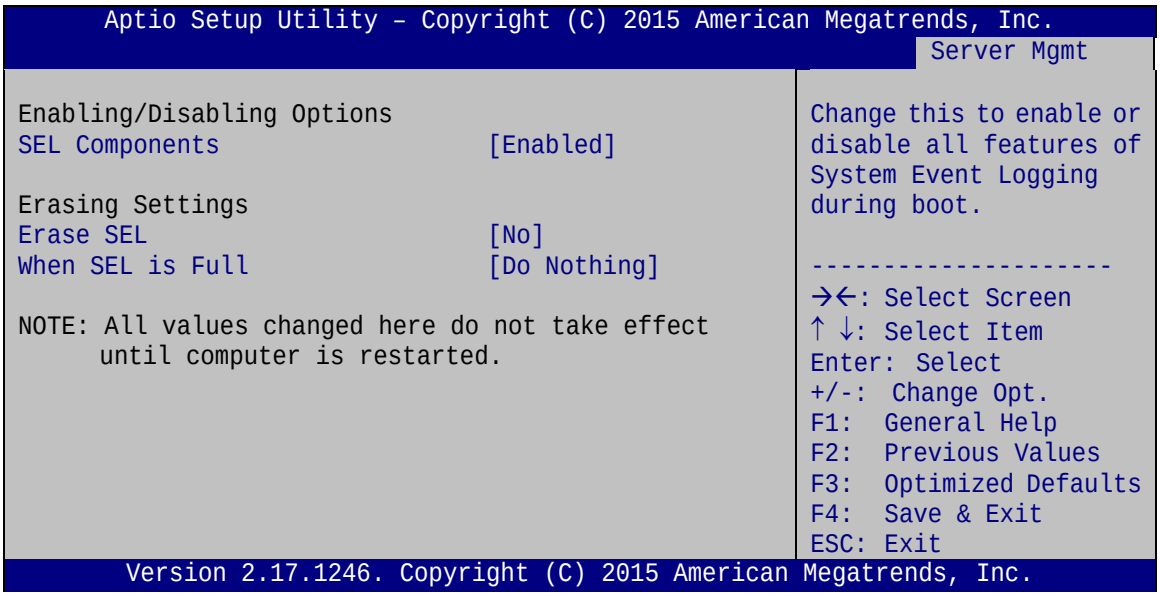
Use the **Server Mgmt** menu (**BIOS Menu 28**) to configure system event log and BMC network parameters.



BIOS Menu 28: Server Mgmt

5.8.1 System Event Log

Use the **System Event Log** menu (**BIOS Menu 29**) to configure system event log options.



BIOS Menu 29: System Event Log

SEL Components [Enabled]

Use the **SEL Components** option to enable or disable all features of System Event Log during boot.

➔	**Disabled**		System Event Log features disabled.
➔	**Enabled**	**DEFAULT**	System Event Log features enabled.

Erase SEL [No]

Use the **Erase SEL** option to select an option for erasing SEL (system event log).

➔	**No**	**DEFAULT**	Do not erase SEL
➔	**Yes, On next reset**		Erase SEL on next reset
➔	**Yes, On every reset**		Erase SEL on every reset

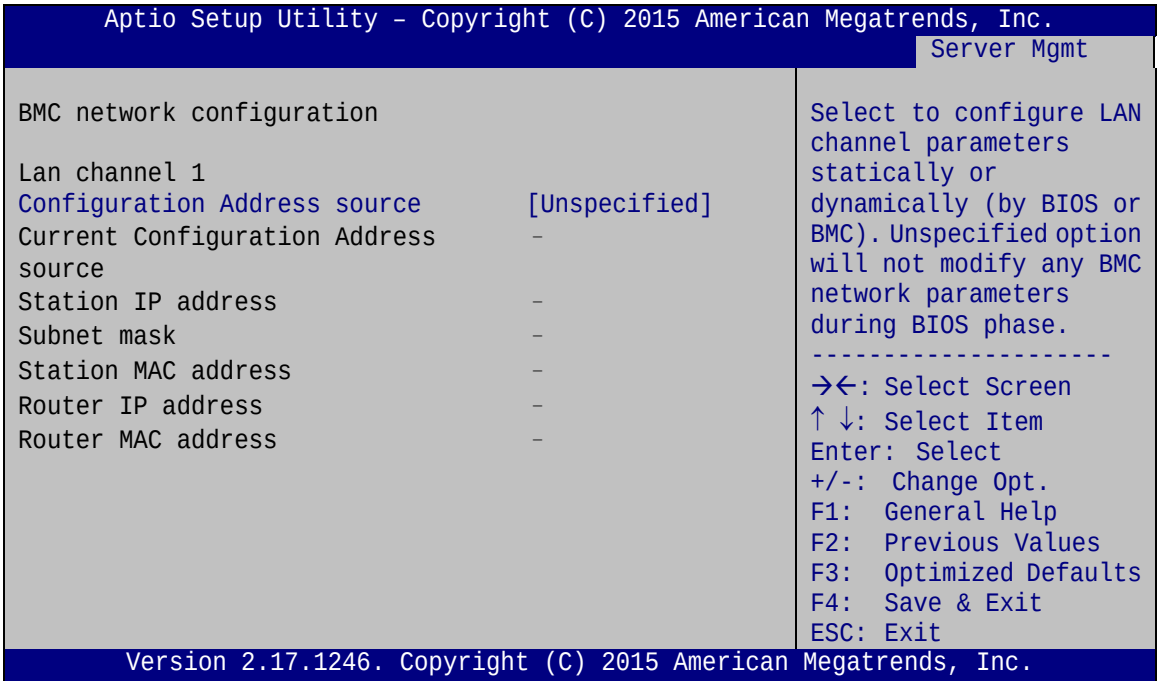
When SEL is Full [Do Nothing]

Use the **When SEL is Full** option to select an option for reaction to a full SEL.

➔	**Do Nothing**	**DEFAULT**	Do nothing when SEL is full
➔	**Erase Immediately**		Erase SEL immediately when SEL is full

5.8.2 BMC Network Configuration

Use the **BMC Network Configuration** menu (**BIOS Menu 30**) to configure BMC network parameters.



BIOS Menu 30: System Event Log

Configuration Address source [Unspecified]

Use the **Configuration Address source** option to configure LAN channel parameters statically or dynamically (by BIOS or BMC). Choosing the **Unspecified** option will not modify any BMC network parameters during BIOS phase. The following options are available:

- Unspecified **DEFAULT**
- Static
- DynamicBmcDhcp
- DynamicBmcNonDhcp

Chapter

6

Software Drivers

6.1 Available Drivers

All the drivers for the WAFER-ULT/ULT2-i1 are available on IEI Resource Download Center (https://download.ieiworld.com). Type WAFER-ULT/ULT2-i1 and press Enter to find all the relevant software, utilities, and documentation.

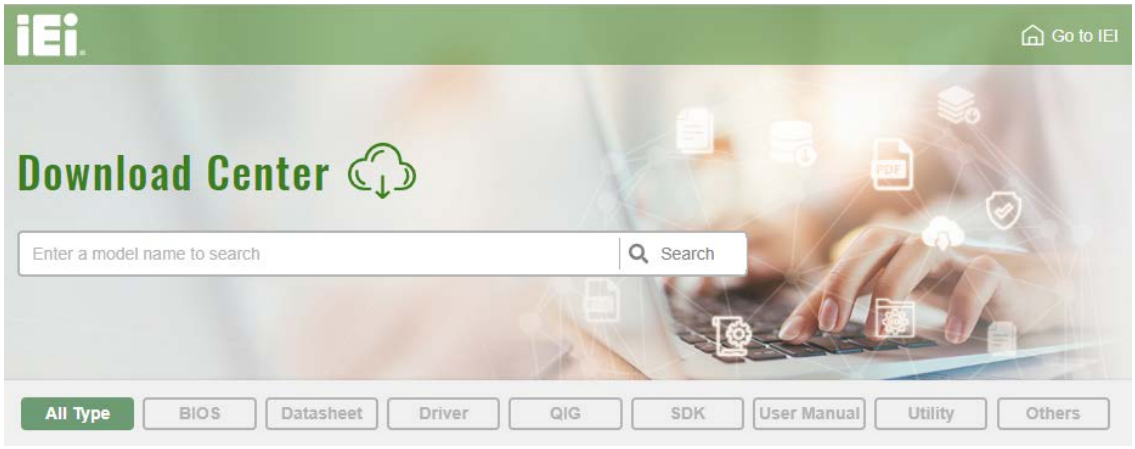
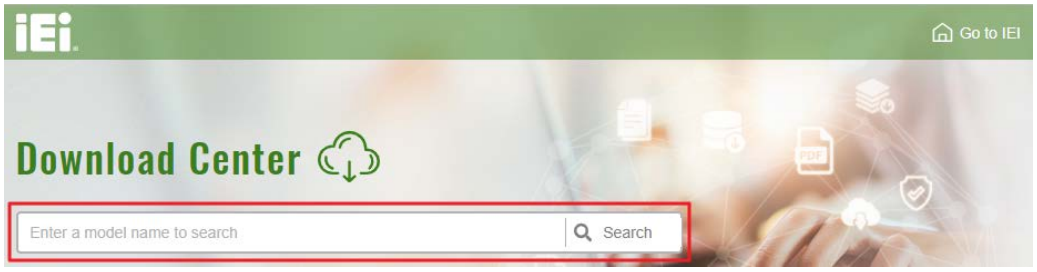


Figure 6-1: IEI Resource Download Center

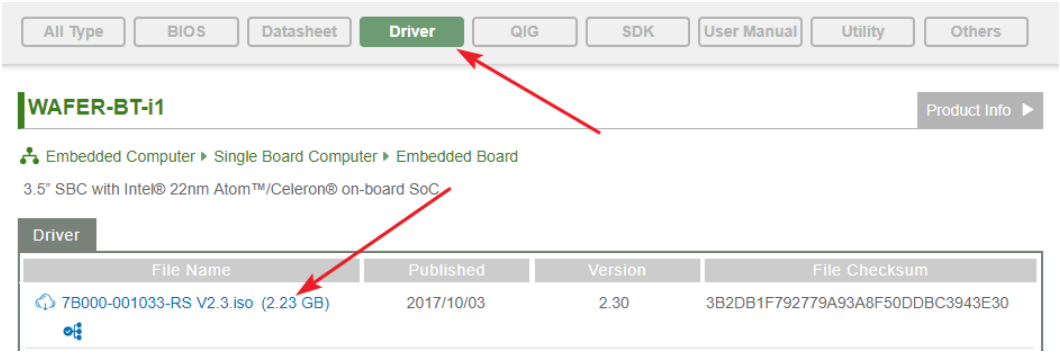
6.2 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

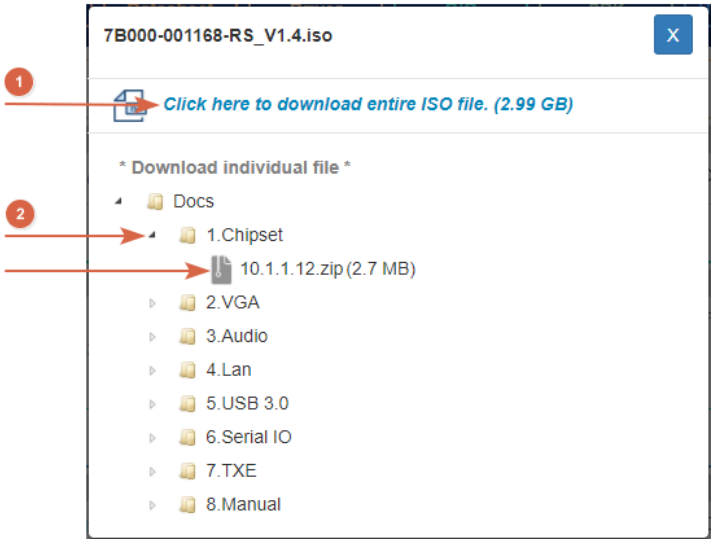
Step 1: Go to https://download.ieiworld.com. Type WAFER-ULT/ULT2-i1 and press Enter.



Step 2: All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.



Step 3: Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (❶), or click the small arrow to find an individual driver and click the file name to download (❷).



NOTE:

To install software from the downloaded ISO image file in Windows 8, 8.1 or 10, double-click the ISO file to mount it as a virtual drive to view its content. On Windows 7 system, an additional tool (such as Virtual CD-ROM Control Panel from Microsoft) is needed to mount the file.

Appendix

A

Regulatory Compliance

DECLARATION OF CONFORMITY

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

BIOS Options

Below is a list of BIOS configuration options in the BIOS chapter.

Appendix

C

Terminology

AC '97	Audio Codec 97 (AC'97) refers to a codec standard developed by Intel® in 1997.
ACPI	Advanced Configuration and Power Interface (ACPI) is an OS-directed configuration, power management, and thermal management interface.
AHCI	Advanced Host Controller Interface (AHCI) is a SATA Host controller register-level interface.
ATA	The Advanced Technology Attachment (ATA) interface connects storage devices including hard disks and CD-ROM drives to a computer.
ARMD	An ATAPI Removable Media Device (ARMD) is any ATAPI device that supports removable media, besides CD and DVD drives.
ASKIR	Amplitude Shift Keyed Infrared (ASKIR) is a form of modulation that represents a digital signal by varying the amplitude ("volume") of the signal. A low amplitude signal represents a binary 0, while a high amplitude signal represents a binary 1.
BIOS	The Basic Input/Output System (BIOS) is firmware that is first run when the computer is turned on and can be configured by the end user
CODEC	The Compressor-Decompressor (CODEC) encodes and decodes digital audio data on the system.
CMOS	Complimentary metal-oxide-conductor is an integrated circuit used in chips like static RAM and microprocessors.
COM	COM refers to serial ports. Serial ports offer serial communication to expansion devices. The serial port on a personal computer is usually a male DB-9 connector.
DAC	The Digital-to-Analog Converter (DAC) converts digital signals to analog signals.
DDR	Double Data Rate refers to a data bus transferring data on both the rising and falling edges of the clock signal.
DMA	Direct Memory Access (DMA) enables some peripheral devices to bypass the system processor and communicate directly with the system memory.

DIMM	Dual Inline Memory Modules are a type of RAM that offer a 64-bit data bus and have separate electrical contacts on each side of the module.
DIO	The digital inputs and digital outputs are general control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.
EHCI	The Enhanced Host Controller Interface (EHCI) specification is a register-level interface description for USB 2.0 Host Controllers.
EIDE	Enhanced IDE (EIDE) is a newer IDE interface standard that has data transfer rates between 4.0 MBps and 16.6 MBps.
EIST	Enhanced Intel® SpeedStep Technology (EIST) allows users to modify the power consumption levels and processor performance through application software. The application software changes the bus-to-core frequency ratio and the processor core voltage.
FSB	The Front Side Bus (FSB) is the bi-directional communication channel between the processor and the Northbridge chipset.
GbE	Gigabit Ethernet (GbE) is an Ethernet version that transfers data at 1.0 Gbps and complies with the IEEE 802.3-2005 standard.
GPIO	General purpose input
HDD	Hard disk drive (HDD) is a type of magnetic, non-volatile computer storage device that stores digitally encoded data.
ICH	The Input/Output Control Hub (ICH) is an Intel® Southbridge chipset.
IrDA	Infrared Data Association (IrDA) specify infrared data transmission protocols used to enable electronic devices to wirelessly communicate with each other.
L1 Cache	The Level 1 Cache (L1 Cache) is a small memory cache built into the system processor.
L2 Cache	The Level 2 Cache (L2 Cache) is an external processor memory cache.
LCD	Liquid crystal display (LCD) is a flat, low-power display device that consists of two polarizing plates with a liquid crystal panel in between.

LVDS	Low-voltage differential signaling (LVDS) is a dual-wire, high-speed differential electrical signaling system commonly used to connect LCD displays to a computer.
POST	The Power-on Self Test (POST) is the pre-boot actions the system performs when the system is turned-on.
RAM	Random Access Memory (RAM) is volatile memory that loses data when power is lost. RAM has very fast data transfer rates compared to other storage like hard drives.
SATA	Serial ATA (SATA) is a serial communications bus designed for data transfers between storage devices and the computer chipsets. The SATA bus has transfer speeds up to 1.5 Gbps and the SATA II bus has data transfer speeds of up to 3.0 Gbps.
S.M.A.R.T	Self Monitoring Analysis and Reporting Technology (S.M.A.R.T) refers to automatic status checking technology implemented on hard disk drives.
UART	Universal Asynchronous Receiver-transmitter (UART) is responsible for asynchronous communications on the system and manages the system's serial communication (COM) ports.
UHCI	The Universal Host Controller Interface (UHCI) specification is a register-level interface description for USB 1.1 Host Controllers.
USB	The Universal Serial Bus (USB) is an external bus standard for interfacing devices. USB 1.1 supports 12Mbps data transfer rates and USB 2.0 supports 480Mbps data transfer rates.
VGA	The Video Graphics Array (VGA) is a graphics display system developed by IBM.

Appendix

D

Digital I/O Interface

D.1 Introduction

The DIO connector on the WAFER-ULT/ULT2-i1 is interfaced to GPIO ports on the Super I/O chipset. The DIO has both 4-bit digital inputs and 4-bit digital outputs. The digital inputs and digital outputs are generally control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.

NOTE:

For further information, please refer to the datasheet for the Super I/O chipset.

The BIOS interrupt call **INT 15H** controls the digital I/O.

INT 15H:

AH – 6FH	
Sub-function:	
AL – 8	:Set the digital port as INPUT
AL	:Digital I/O input value

D.2 Assembly Language Sample 1

```
MOV     AX, 6F08H       ;setting the digital port as input
INT     15H             ;
```

AL low byte = value

AH – 6FH	
Sub-function:	
AL – 9	:Set the digital port as OUTPUT
BL	:Digital I/O input value

D.3 Assembly Language Sample 2

```
MOV     AX, 6F09H       ;setting the digital port as output
MOV     BL, 09H         ;digital value is 09H
INT     15H             ;
```

Digital Output is 1001b

Appendix

E

Watchdog Timer

NOTE:

The following discussion applies to DOS environment. Contact IEI support or visit the IEI website for specific drivers for other operating systems.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMIs or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table E-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

NOTE:

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

EXAMPLE PROGRAM:

```
; INITIAL TIMER PERIOD COUNTER

;
W_LOOP:
;

        MOV     AX, 6F02H       ;setting the time-out value
        MOV     BL, 30          ;time-out value is 48 seconds
        INT     15H

;
; ADD THE APPLICATION PROGRAM HERE
;

        CMP     EXIT_AP, 1      ;is the application over?
        JNE     W_LOOP          ;No, restart the application

        MOV     AX, 6F02H       ;disable Watchdog Timer
        MOV     BL, 0           ;
        INT     15H

;
; EXIT ;
```

Appendix

F

Hazardous Materials Disclosure

The details provided in this appendix are to ensure that the product is compliant with the Peoples Republic of China (China) RoHS standards. The table below acknowledges the presences of small quantities of certain materials in the product, and is applicable to China RoHS only.

A label will be placed on each product to indicate the estimated "Environmentally Friendly Use Period" (EFUP). This is an estimate of the number of years that these substances would "not leak out or undergo abrupt change." This product may contain replaceable sub-assemblies/components which have a shorter EFUP such as batteries and lamps. These components will be separately marked.

Please refer to below table.

Part Name	Toxic or Hazardous Substances and Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
Housing	O	O	O	O	O	O
Display	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O
Battery	O	O	O	O	O	O

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in SJ/T11363-2006 (now replaced by GB/T 26572-2011).

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in SJ/T11363-2006 (now replaced by GB/T 26572-2011).

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有"环境友好使用期限"的标签，此期限是估算这些物质"不会有泄漏或突变"的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	O	O	O	O	O	O
显示	O	O	O	O	O	O
印刷电路板	O	O	O	O	O	O
金属螺帽	O	O	O	O	O	O
电缆组装	O	O	O	O	O	O
风扇组装	O	O	O	O	O	O
电力供应组装	O	O	O	O	O	O
电池	O	O	O	O	O	O
O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11363-2006 (现由 GB/T 26572-2011 取代) 标准规定的限量要求以下。 X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11363-2006 (现由 GB/T 26572-2011 取代) 标准规定的限量要求。						