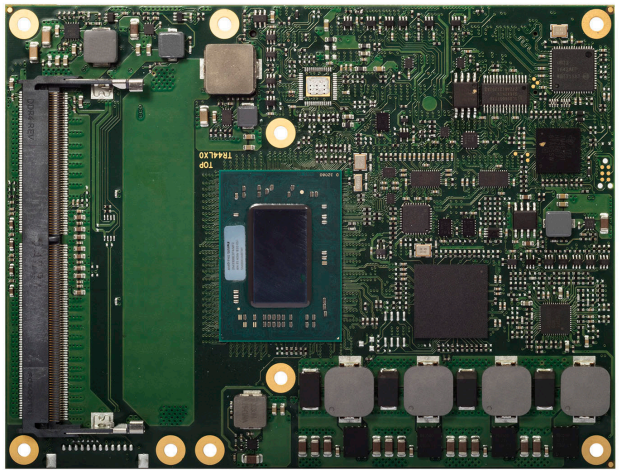

COM Express™ conga-TR4

COM Express Type 6 Basic module based on 4th Generation AMD Embedded V- and R-Series SoC

User's Guide

Revision 1.5

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2018.01.15	BEU	• Preliminary release
1.0	2018.10.15	BEU	• Updated "Electrostatic Sensitive Device" information on page 3 • Corrected single/dual channel MT/s rates for two variants in table 2 • Updated section 2.2 "Supported Operating Systems" • Added values for four variants in section 2.5 "Power Consumption" • Added values in section 2.6 "Supply Voltage Battery Power" • Updated images in section 4 "Cooling Solutions" • Added note about requiring a re-driver on carrier for USB 3.1 Gen 2 in section 5.1.2 "USB" and 7.4 "USB Host Controller" • Added Intel® Ethernet Controller i211 as assembly option in table 4 "Feature Summary" and section 5.1.4 "Ethernet" • Corrected section 7.4 "USB Host Controller" • Added section 9 "System Resources"
1.1	2019.03.19	BEU	• Corrected image in section 2.4 "Supply Voltage Standard Power" • Updated section 10.4 "Supported Flash Devices"
1.2	2019.04.02	BEU	• Corrected supported memory in table 2, 3, and added information about supported memory in table 4 • Added information about the new industrial variant in table 3 and 7
1.3	2019.07.30	BEU	• Updated note in section 4 "Cooling Solutions" • Changed number of supported USB 3.1 Gen 2 interfaces to two throughout the document • Added note regarding USB 3.1 Gen 2 in section 7.4 "USB Host Controller"
1.4	2020.01.07	BEU	• Updated title page • Updated CPU clock speed of variant 041603 in table 2 • Added variants 041620 and 041621 to table 3 and 7 • Updated section 4 "Cooling Solutions" • Updated references for power supply implementation guidelines in section 5.1.12 "Power Control" • Added reference to BIOS Setup Description application note in section 10 "BIOS Setup Description" • Updated section 10.3 "Updating the BIOS" • Updated supported flash device in section 10.4 "Supported Flash Devices" • Added note to several button signals in table 24 • Updated section 11 "Industry Specifications"
1.5	2020.03.04	BEU	• Added power consumption values and updated existing ones in table 7

Preface

This user's guide provides information about the components, features and interfaces available on the conga-TR4. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide
COM Express™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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Caution

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Note

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Terminology

Term	Description
GB	Gigabyte
GHz	Gigahertz
kB	Kilobyte
MB	Megabyte
Mbit	Megabit
kHz	Kilohertz
MHz	Megahertz
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PEG	PCI Express Graphics
PCH	Platform Controller Hub
SM	System Management
N.C	Not connected
N/A	Not available
TBD	To be determined

Contents

List of Tables

1 Introduction

COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express™ modules are available in following form factors:

- Mini 84mm x 55mm
- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x 110mm

Table 1 COM Express™ 3.0 Pinout Types

Types	Connector Rows	PCIe Lanes	PCI	IDE	SATA Ports	LAN ports	USB 2.0 / USB 3.0	Display Interfaces
Type 1	A-B	Up to 6		-	4	1	8 / 0	VGA, LVDS
Type 2	A-B C-D	Up to 22	32 bit	1	4	1	8 / 0	VGA, LVDS, PEG
Type 3	A-B C-D	Up to 22	32 bit	-	4	3	8 / 0	VGA,LVDS, PEG
Type 4	A-B C-D	Up to 32		1	4	1	8 / 0	VGA,LVDS, PEG
Type 5	A-B C-D	Up to 32		-	4	3	8 / 0	VGA,LVDS, PEG
Type 6	A-B C-D	Up to 24		-	4	1	8 / 4*	VGA,LVDS/eDP, PEG, 3x DDI
Type 7	A-B C-D	Up to 32		-	2	5 (1x 1 G, 4x 10 G)	4 / 4*	-
Type 10	A-B	Up to 4		-	2	1	8 / 2*	LVDS/eDP, 1xDDI

** The SuperSpeed USB ports (USB 3.0) are not in addition to the USB 2.0 ports. Up to 4 of the USB 2.0 ports can support SuperSpeed USB.*

The conga-TR4 modules use the Type 6 pinout definition and comply with COM Express 3.0 specification. They are equipped with two high performance connectors that ensure stable data throughput and support high bandwidth networking.

The COM (computer on module) integrates all the core components of a common PC and is mounted onto an application specific carrier board. COM modules are legacy-free (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 3.0/2.0, and 10 Gigabit Ethernet.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

conga-TR4 Options Information

The conga-TR4 is available in five variants. This user's guide describes these variants. The table below shows the different configurations available. Check the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Table 2 conga-TR4 Commercial Options

Part-No.	041600	041601	041602	041603
SoC	V1807B	V1756B	V1605B	V1202B
CPU Clock Speed	3.35 GHz (3.8 GHz Turbo)	3.25 GHz (3.6 GHz Turbo)	2.0 GHz (3.6 GHz Turbo)	2.3 GHz (3.2 GHz Turbo)
L2 Shared Cache	2 MB	2 MB	2 MB	1 MB
Memory (DDR4)	2400 MT/s dual channel, single/dual rank 3200 MT/s dual channel, single rank only	2400 MT/s dual channel, single/dual rank 3200 MT/s dual channel, single rank only	2400 MT/s dual channel, single/dual rank	2400 MT/s dual channel, single/dual rank
Graphics Engine	AMD Radeon™ Vega 11	AMD Radeon™ Vega 8	AMD Radeon™ Vega 8	AMD Radeon™ Vega 3
GPU Clock Speed	1300 MHz (11 Compute Units)	1300 MHz (8 Compute Units)	1100 MHz (8 Compute Units)	1000 MHz (3 Compute Units)
PCIe	1x PCIe Gen 3 (x8/x4) 4x PCIe Gen 3 (x4/x2/x1) 4x PCIe Gen 2 (x1)	1x PCIe Gen 3 (x8/x4) 4x PCIe Gen 3 (x4/x2/x1) 4x PCIe Gen 2 (x1)	1x PCIe Gen 3 (x8/x4) 4x PCIe Gen 3 (x4/x2/x1) 4x PCIe Gen 2 (x1)	1x PCIe Gen 3 (x8/x4) 4x PCIe Gen 3 (x4/x2/x1) 4x PCIe Gen 2 (x1)
USB	Up to: 2x USB 3.1 Gen 2 2x USB 3.1 Gen 1 4x USB 2.0	Up to: 2x USB 3.1 Gen 2 2x USB 3.1 Gen 1 4x USB 2.0	Up to: 2x USB 3.1 Gen 2 2x USB 3.1 Gen 1 4x USB 2.0	Up to: 2x USB 3.1 Gen 2 2x USB 3.1 Gen 1 4x USB 2.0
DDI	2x Dedicated DDI 1x DDI multiplexed with USB port	2x Dedicated DDI 1x DDI multiplexed with USB port	2x Dedicated DDI 1x DDI multiplexed with USB port	2x Dedicated DDI 1x DDI multiplexed with USB port
LVDS	1x LVDS (default) or 1x eDP (optional)	1x LVDS (default) or 1x eDP (optional)	1x LVDS (default) or 1x eDP (optional)	1x LVDS (default) or 1x eDP (optional)
SoC TDP	35-54W	35-54W	12-25W	12-25W

Table 3 conga-TR4 Industrial Options

Part-No.	041610	041620	041621
SoC	V1404I	R1606G	R1505G
CPU Clock Speed	2.0 GHz (3.6 GHz Turbo)	2.6 GHz (3.5 GHz Turbo)	2.4 GHz (3.3 GHz Turbo)
L2 Shared Cache	2 MB	1 MB	1 MB
Memory (DDR4)	2400 MT/s dual channel, single/dual rank	2400 MT/s dual channel, single/dual rank	2400 MT/s dual channel, single/dual rank
Graphics Engine	AMD Radeon™ Vega 8	AMD Radeon™ Vega 3	AMD Radeon™ Vega 3
GPU Clock Speed	1300 MHz (8 Compute Units)	1200 MHz (3 Compute Units)	1000 MHz (3 Compute Units)
PCIe	1x PCIe Gen 3 (x8/x4) 4x PCIe Gen 3 (x4/x2/x1) 4x PCIe Gen 2 (x1)	1x PCIe Gen 3 (x4) 3x PCIe Gen 3 (x1) 4x PCIe Gen 2 (x1)	1x PCIe Gen 3 (x4) 3x PCIe Gen 3 (x1) 4x PCIe Gen 2 (x1)
USB	Up to: 2x USB 3.1 Gen 2 2x USB 3.1 Gen 1 4x USB 2.0	Up to: 2x USB 3.1 Gen 2 1x USB 3.1 Gen 1 4x USB 2.0	Up to: 2x USB 3.1 Gen 2 1x USB 3.1 Gen 1 4x USB 2.0
DDI	2x Dedicated DDI 1x DDI multiplexed with USB port	2x Dedicated DDI	2x Dedicated DDI
LVDS/eDP	1x LVDS (default) or 1x eDP (optional)	1x LVDS (default) or 1x eDP (optional)	1x LVDS (default) or 1x eDP (optional)
SoC TDP	12-25W	12-25W	12-25W

2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 6 (Basic size 95 x 125 mm)	
SoC	4th Generation AMD Embedded V- and R-Series (FP5) SoC. **NOTE:** R-Series is not available yet.	
Memory	Two memory sockets (located on the top and bottom side of the conga-TR4). Supports: - SO-DIMM ECC and non-ECC DDR4 memory modules - Data rates up to 3200 MT/s with single rank memory - Maximum 32 GB capacity (16 GB on each socket)	
Chipset	Integrated in the SoC	
Audio	High Definition Audio (HDA) interface with support for up to three codecs.	
Ethernet	1x Gigabit Ethernet PHY or via the onboard Intel® Ethernet i210 Controller (i211 available as assembly option).	
Graphics Options	AMD Radeon™ Vega Graphics Core (GFX9). Supports: - DirectX® 12, EGL 1.4, OpenCL® 2.1, OpenGL® ES (1.1, 2.x and 3.x), OpenGL® Next, OpenGL® 4.6 - Video Core Next (VCN): H.265/HEVC HW encode and decode, 10b HEVC and VP9 decode, MS compliant JPEG encode and decode - Up to four independent displays (three in R-Series)	
	1x PCIe Gen 3 (x8/x4) (Only x4 in R-Series) 1x LVDS (default) or 1x eDP (optional) 2x Dedicated DDI (DP/HDMI/DVI) 1x DDI (DP/HDMI/DVI) (N/A in R-Series) multiplexed with USB 3.1 Gen 2	**NOTE:** HDMI/DVI requires an external level shifter on carrier board.
Peripheral Interfaces	USB up to: - 2x USB 3.1 Gen 2 - 2x USB 3.1 Gen 1 (Only 1x in R-Series) - 4x USB 2.0 2x SATA® 6 Gb/s ports 4x PCIe Gen 3 (x4/x2/x1) (Only 3x PCIe Gen3 (x1) in R-Series) 4x PCIe Gen 2 (x1) 2x UART	Fan control GPIOs Buses: - SPI - LPC - SM - I²C
BIOS	AMI Aptio® UEFI 5.x firmware; 8 MByte serial SPI with congatec Embedded BIOS features	
Security	Infineon LPC TPM 2.0 on module. Integrated TPM 2.0 in SoC.	
Power Management	ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).	
cBC	Multi-stage watchdog, manufacturing and board information, board statistics, I2C bus, Power loss control.	

Note

Some of the features mentioned in the table above are optional. See Table 2 and Table 3 for available features on each module variant.

2.2 Supported Operating Systems

The conga-TR4 supports the following operating systems.

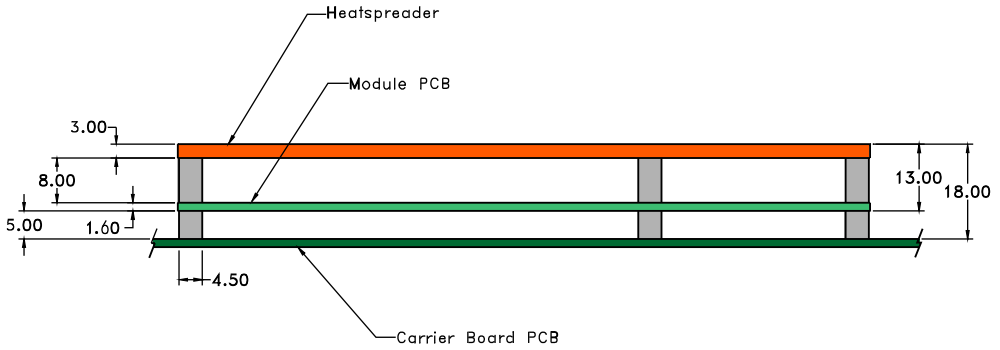
- Microsoft® Windows® 10 (64-bit)
- Microsoft® Windows® 10 IoT Enterprise (64-bit)
- Linux (32/64-bit)

Note

To improve the graphic performance of conga-TR4 after installing Microsoft® Windows® Operating System, congatec AG recommends the installation of AMD catalyst driver.

2.3 Mechanical Dimensions

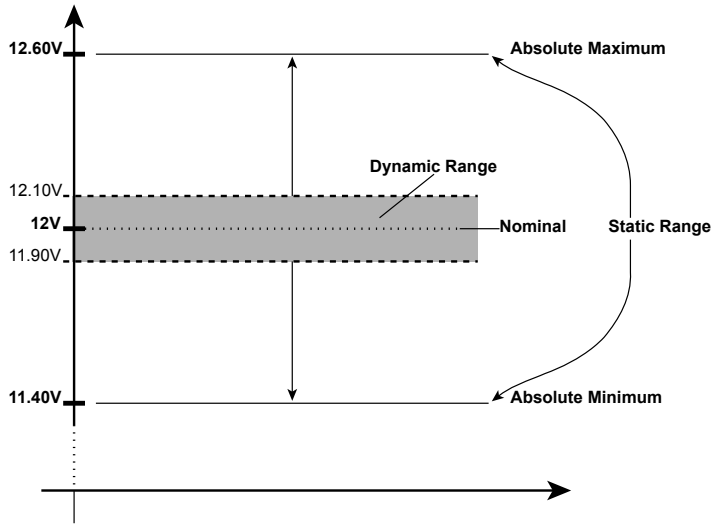
- 95.0 mm x 125.0 mm (3.74" x 4.92")
- Height approximately 18 or 21 mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18 mm. If the 8 mm (height) carrier board connector is used then approximate overall height is 21 mm.



2.4 Supply Voltage Standard Power

- 12V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Table 5 Electrical Characteristics

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-TR4 module
- modified congatec carrier board
- conga-TR4 cooling solution
- Microsoft Windows® 10 (64-bit)

Note

The SoC was stressed to its maximum workload with the AMD APU Validation Toolkit (AVT).

Table 6 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle.	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency.
S0: Peak value	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime.	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.
S3	COM is powered by VCC_5V_SBY.	
S5	COM is powered by VCC_5V_SBY.	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

The tables below provide additional information about the power consumption data for each of the conga-TR4 variants offered. The values are recorded at various operating modes.

Table 7 Power Consumption Values

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64-bit)	CPU			Current (Amp.) S0 @12V and S3/S5 @5V				
					Variant	Cores	Clock Speed (Turbo) in GHz	S0: Min	S0: Max	S0: Peak	S3	S5
041600	2x2 GB DDR4-2400	B.1	TR44R010	Windows 10	V1807B	4	3.35 (3.75)	0.35	4.25	6.43	0.16	0.08
041601	2x2 GB DDR4-2400	B.1	TR44R010	Windows 10	V1756B	4	3.25 (3.6)	0.34	4.08	7.02	0.16	0.08
041602	2x2 GB DDR4-2400	B.1	TR44R010	Windows 10	V1605B	4	2.0 (3.6)	0.37	2.17	3.29	0.16	0.08
041603	2x2 GB DDR4-2400	B.1	TR44R010	Windows 10	V1202B	2	2.5 (3.4)	0.35	2.18	2.58	0.16	0.08
041610	2x4 GB DDR4-2400	C.0	TR44R205	Windows 10	V1404B	4	2.0 (3.6)	0.42	2.29	3.47	0.17	0.08
041620	2x4 GB DDR4-2400	C.0	TR44R205	Windows 10	R1606G	2	2.6 (3.5)	0.38	2.22	2.57	0.16	0.08
041621	2x4 GB DDR4-2400	C.0	TR44R205	Windows 10	R1505G	2	2.4 (3.3)	0.37	2.09	2.19	0.16	0.08

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 8 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	2.25 µA
20°C	3V DC	2.41 µA
70°C	3V DC	3.08 µA

Note

Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.

Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).

Consider also the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec AG website at www.congatec.com/support/application-notes.

We recommend to always have a CMOS battery present when operating the conga-TR4.

2.7 Environmental Specifications

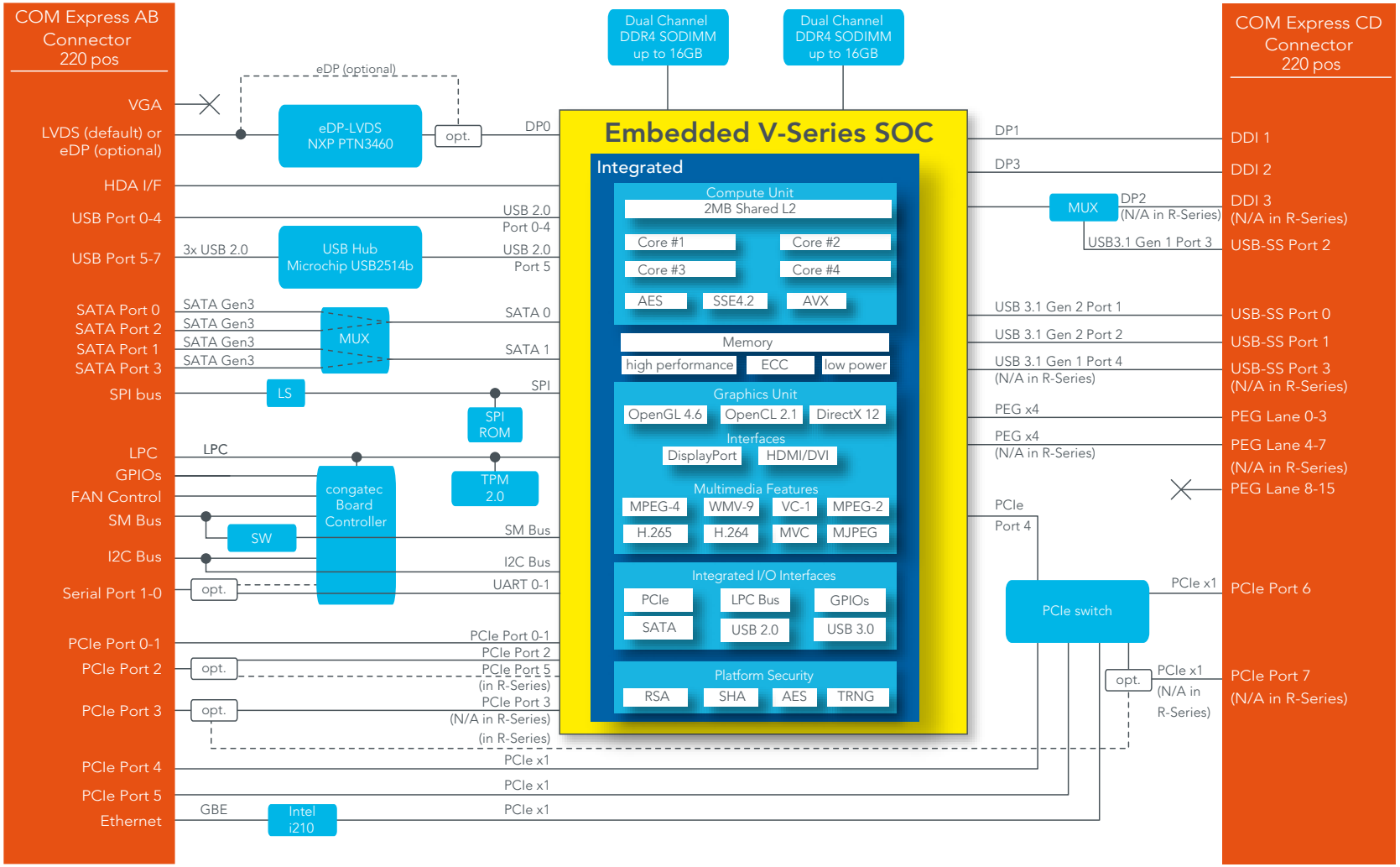
Temperature (commercial variants)	Operation:	0° to 60°C	Storage: -40° to +85°C
Temperature (industrial variants)	Operation:	-40° to 85°C	Storage: -40° to +85°C
Humidity	Operation:	10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



4 Cooling Solutions

congatec AG offers the cooling solutions listed in Table 9 for conga-TCA5. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants

	Cooling Solution	Part No	Description
1	HSP	041651	Heatspreader with 2.7 mm bore-hole standoffs.
		041652	Heatspreader with M2.5 mm threaded standoffs.
2	CSP	041653	Passive cooling with 2.7 mm bore-hole standoffs.
		041654	Passive cooling with M2.5 mm threaded standoffs.
3	CSA	048555	Active cooling with 2.7 mm bore-hole standoffs.
		048556	Active cooling with M2.5 mm threaded standoffs.

Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*

2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

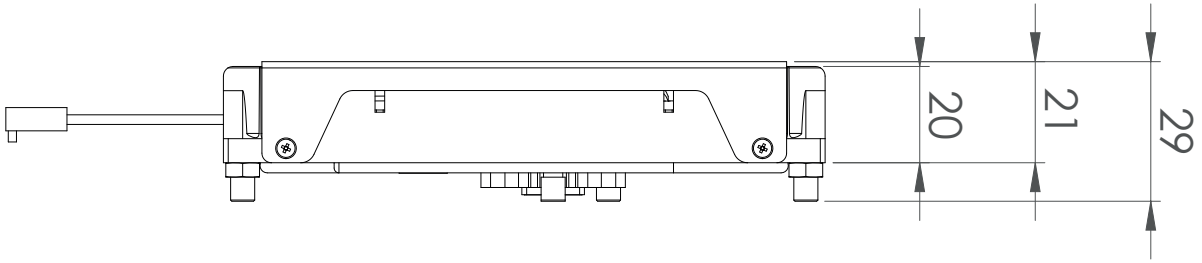
Caution

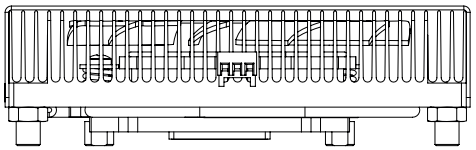
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

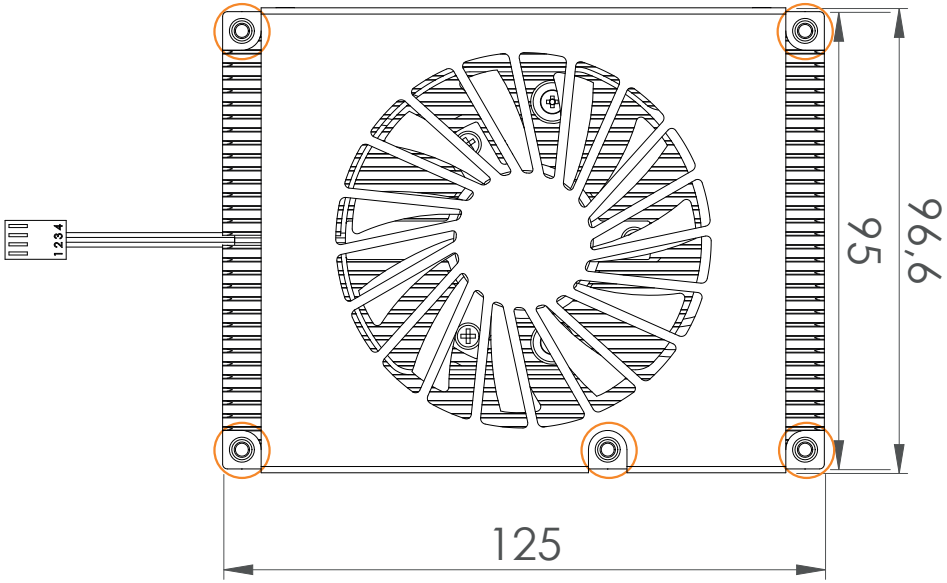
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

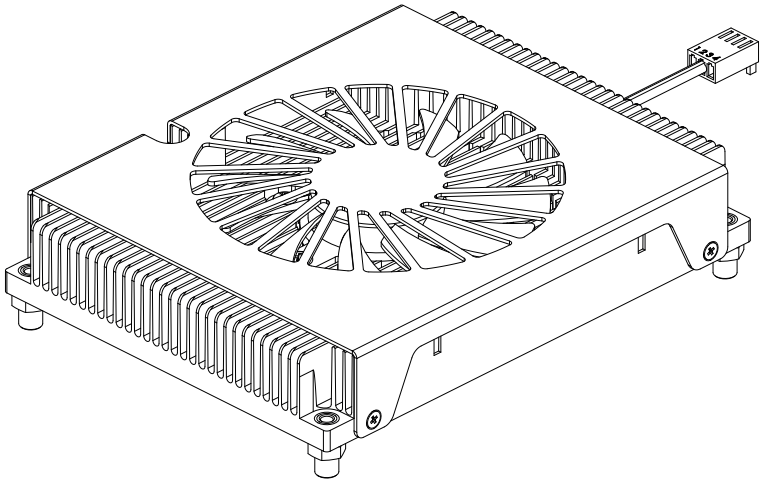
4.1 CSA Dimensions



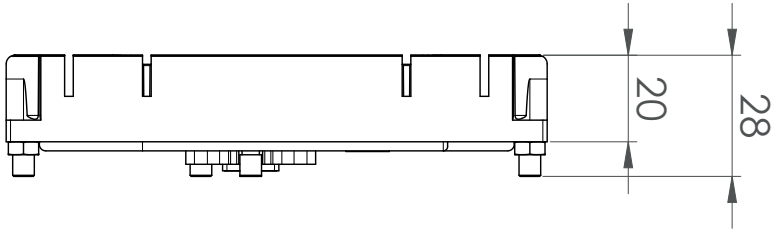


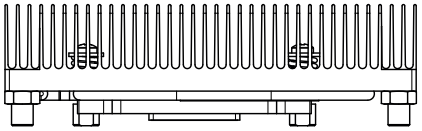
Threaded standoff for threaded version
or
non-threaded standoff for borehole version



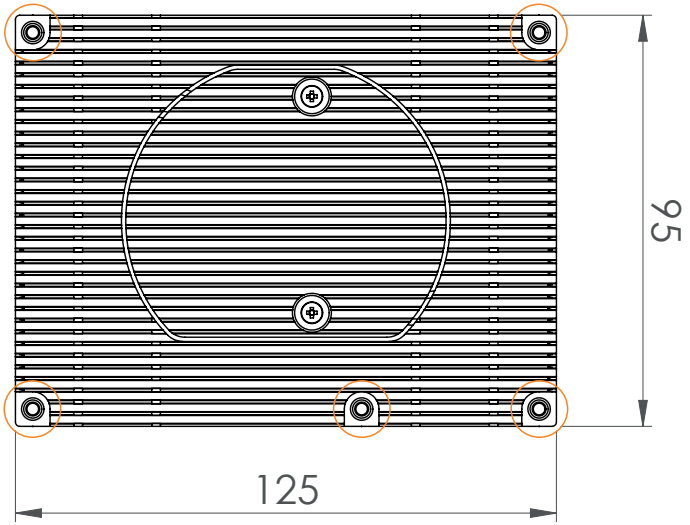


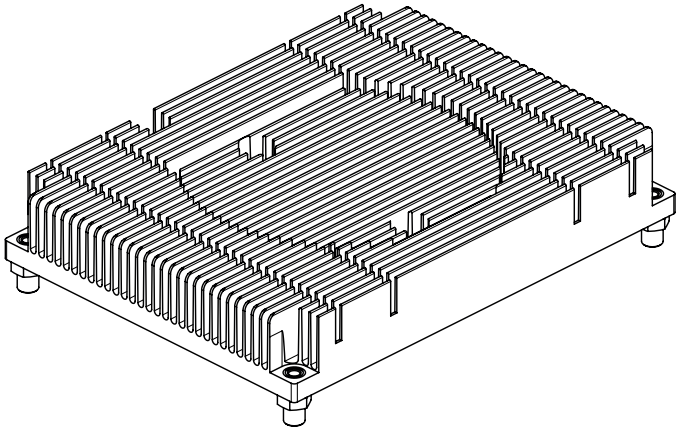
4.2 CSP Dimensions



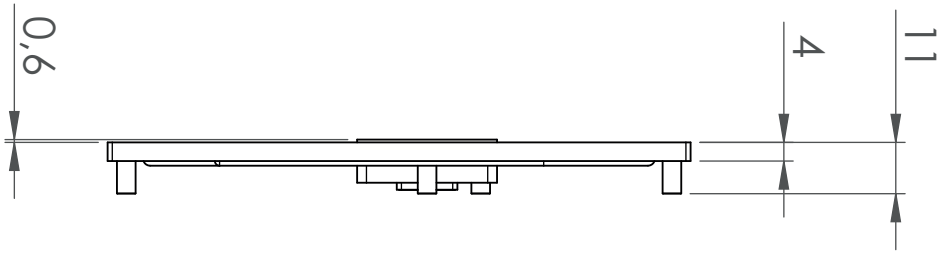


Threaded standoff for threaded version
or
non-threaded standoff for borehole version

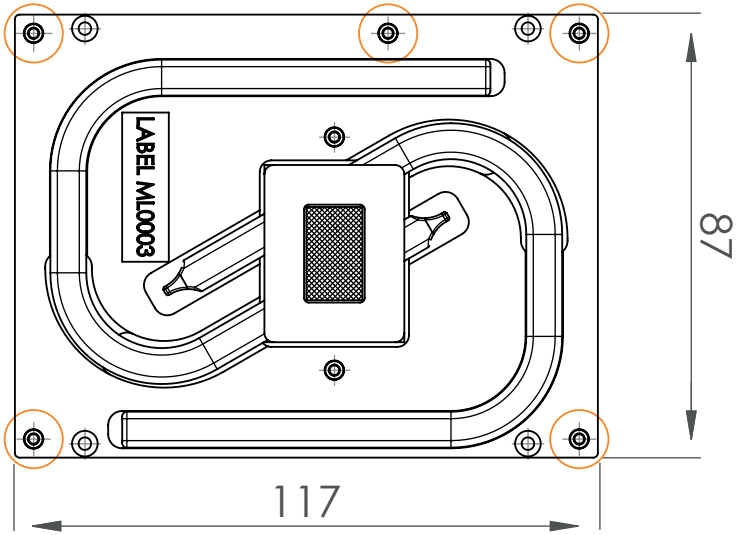


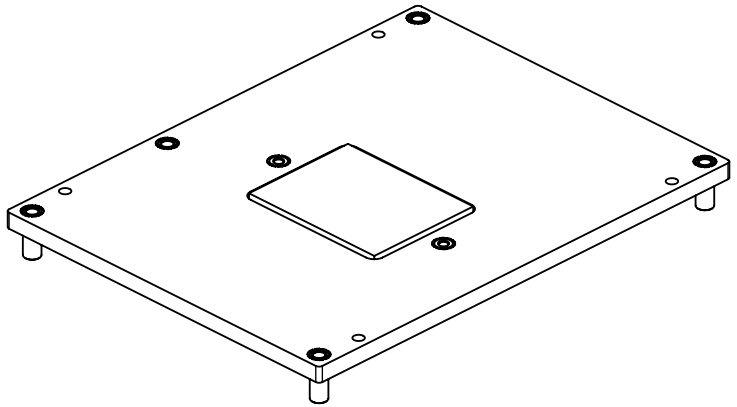


4.3 Heatspreader Dimensions



Threaded standoff for threaded version
or
non-threaded standoff for borehole version





5 Connector Rows

The conga-TR4 is connected to the carrier board via two 220-pin connectors (COM Express Type 6 pinout). These connectors are broken down into four rows (rows A-B and C-D).

5.1 Primary Connector Rows A and B

The following subsystems can be found on the primary connector rows A and B.

5.1.1 Serial ATA™ (SATA)

The conga-TR4 offers two 6Gb/s SATA ports. A switch on the module routes them to the four ports of the COM Express connector. You can set the two active ports via BIOS setup.

5.1.2 USB

The conga-TR4 offers signals for eight USB 2.0 ports. The signals for USB 2.0 ports 0-4 are routed from the SoC. The signals for USB 2.0 ports 5-7 are routed from a USB hub on the module.

The USB 2.0 signals can be combined with USB SuperSpeed signals to create up to two USB 3.1 Gen 2 ports and two USB 3.1 Gen 1 ports (1x in R-Series). For more information, see section 7.4 "USB Host Controller".

5.1.3 High Definition Audio (HDA)

The conga-TR4 offers signals for HDA and supports up to three external codecs. This interface supports multiple codec configurations on a single board as long as all codecs operate on the same voltage.

Note

COM Express modules only support up to three data inputs (HDA_SDIN[0:2]) as described in COM Express Specification 3.0. AC'97 audio codecs are not supported.

5.1.4 Ethernet

The conga-TR4 offers signals for one Gigabit Ethernet (GbE) port via GbE PHY or the integrated Intel® i210 controller (i211 available as assembly option). The ethernet interface consists of four pairs of low voltage differential pair signals designated from GBE0_MDI0± to GBE0_MDI3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

Note

The GBE0_LINK# output is only active during a 100Mbit or 1Gbit connection. It is not active during a 10Mbit connection. This is a limitation of Ethernet controller since it only has 3 LED outputs - ACT#, LINK100# and LINK1000#.

The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TR4.

Network Booting (PXE) is not possible with D-Link Switch Model No. DGS-1008D.

5.1.5 LPC Bus

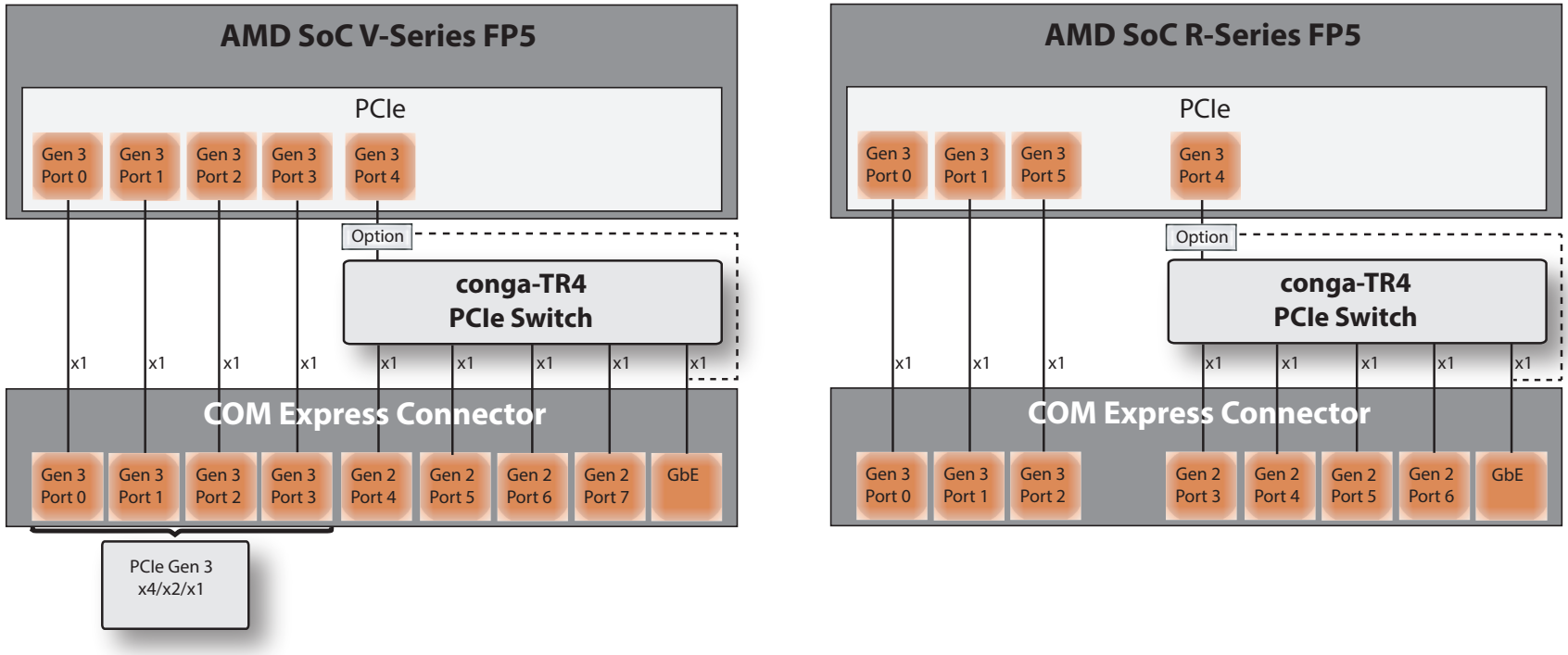
conga-TR4 offers the Low Pin Count (LPC) bus via the integrated controller hub. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific baseboard using this bus. Many devices are available for this cost-efficient, low-speed interface designed to support low bandwidth and legacy devices. The LPC host bus controller supports one master DMA devices. See section 9 "System Resources" for more information about the LPC Bus.

5.1.6 I²C Bus

The I²C bus is implemented through the congatec board controller and is accessed through the congatec CGOS driver and API. The controller provides a fast mode multi-master I²C bus that has maximum I²C bandwidth.

5.1.7 PCI Express™ (PCIe)

The conga-TR4 offers up to four PCIe Gen 3 ports (three in R-Series) and four PCIe Gen 2 ports as shown in the routing diagrams below:



5.1.8 LVDS

The conga-TR4 offers signals for LVDS by default. Optionally, the conga-TR4 can offer signals for eDP instead. The eDP to LVDS bridge (NXP PTN3460) on the module processes the incoming DisplayPort (DP) stream, converts the DP protocol to LVDS protocol and transmits the processed stream in LVDS format.

The LVDS interface supports:

- Single or dual channel LVDS (color depths of 18 bpp or 24 bpp)
- VESA and JEIDA color mappings
- Resolution up to 1920x1200 @60 Hz in in dual LVDS bus mode (color depth 24 bpp)

5.1.9 Optional eDP

The conga-TR4 offers signals for LVDS by default. Optionally, the conga-TR4 can offer signals for eDP instead.

The eDP interface supports:

- VESA eDP Standard version 1.4
- Resolution up to 3840x2160 @60 Hz

5.1.10 GPIO

The conga-TR4 offers general purpose inputs and outputs for custom system designs and can be controlled by the congatec Board Controller (cBC).

5.1.11 UART

The conga-TR4 offers signals for two UART interfaces routed from the SoC by default. Optionally, the signals can be routed from the congatec Board Controller (cBC) instead.

Two TTL compatible two wire ports are available on Type 6 COM Express modules. These pins are designated SER0_TX, SER0_RX, SER1_TX and SER1_RX. Data out of the module is on the _TX pins. Hardware handshaking and hardware flow control are not supported. The module asynchronous serial ports are intended for general purpose use and for use with debugging software that makes use of the "console redirect" features available in many operating systems.

The UART controllers integrated in the cBC support up to 1MBit/s and can operate in low-speed, full-speed and high-speed modes. The UART interfaces are routed to the AB connector and require the congatec driver to function.

Note

The UART interfaces currently do not support legacy COM port emulation.

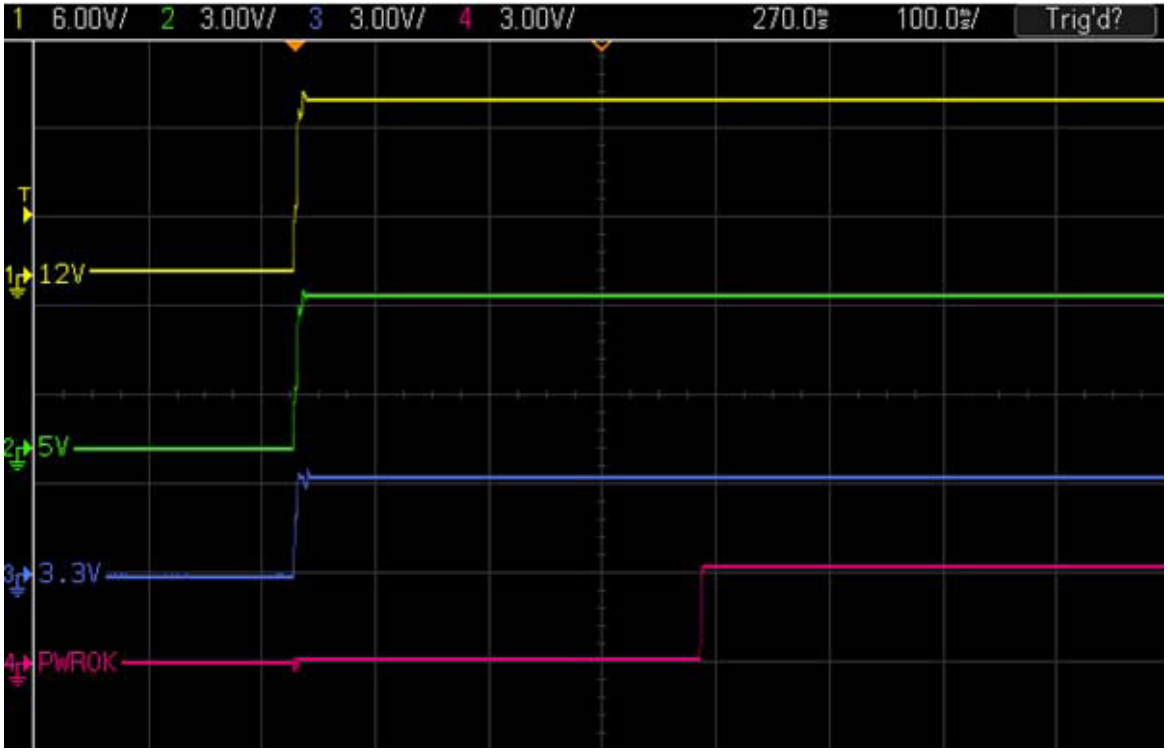
5.1.12 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. The PWR_OK is a 3.3V signal according to the COM Express Specification. The use of this input is optional.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system. Although the PWR_OK input is not mandatory for the onboard power-up sequencing, it is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

A sample screenshot is shown below:



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the "power good" signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, it must be ensured that by the time the 3.3V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-TR4 module is capable of generating it's own power good through the use of an internal monitor on the +12V ± 5% input voltage and/or the internal power supplies. The conga-TR4 also provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-TR4's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

12 volt input power is the sole operational power source for the conga-TR4. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-TR4 application:

- It has also been noticed that on some occasions, problems occur when using a 12V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

5.1.13 Power Management

ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).

5.2 Secondary Connector Rows C and D

The following subsystems can be found on the secondary connector rows C and D.

5.2.1 PCI Express™ Graphics (PEG)

The conga-TR4 offers signals for a PEG x8 interface (x4 in R-Series). The default configuration of the PEG interface is one x8 link. The interface can be configured as a two x4 link in the BIOS setup menu.

5.2.2 Digital Display Interface (DDI)

The conga-TR4 offers signals for up to three DDI (two in R-Series):

- DDI1 is a native port
- DDI2 is multiplexed with a USB 3.1 Gen 2 port. See section section 7.4 "USB Host Controller" for more information.
- DDI3 (N/A in R-Series) is multiplexed with a USB 3.1 Gen 2 port. See section section 7.4 "USB Host Controller" for more information.

Each interface can be configured as DP++, HDMI or DVI. Any display combination is supported.

DP supports:

- VESA DisplayPort Standard version 1.4
- Resolution up to 3840x2160 @ 120 Hz (HBR3, 8.1 GT/s; requires re-timer)

HDMI/DVI supports:

- HDMI Standard version 2.0b
- Resolution up to 4096x2160 @ 60 Hz (6 Gb/s; requires re-timer)
- Single-link DVI with resolution up to 1920x1200 @ 60 Hz

Note

To support HDMI/DVI, an external level shifter (e.g PTN3360D) should be implemented on the user's carrier board.

6 Additional Features

6.1 congatec Board Controller (cBC)

The conga-TR4 is equipped with a Texas Instruments Tiva™ TM4E1231H6ZRB microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features, such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

6.1.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.1.2 Fan Control

The conga-TR4 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

A four wire fan must be used to generate the correct speed readout.

The congatec COM Express Type 6 and Type 10 modules use a Push-Pull output for the fan_pwm signal instead of the open drain output specified in the COM Express specification. Although this does not comply with the COM Express specification 2.0, the benefits are obvious. The Push-Pull output optimizes the power consumed by the fan_pwm signal without functional change.

6.1.3 Power Loss Control

The cBC has full control of the power-up of the module and can be used to specify the behavior of the system after an AC power loss condition. Supported modes are "Always On", "Remain Off" and "Last State".

6.1.4 Watchdog

The conga-TR4 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-TR4 does not support external hardware triggering. For more information about the Watchdog feature, see the BIOS setup description in section 10 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

Note

The conga-TR4 module does not support the watchdog NMI mode.

6.2 OEM BIOS Customization

The conga-TR4 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described in the following sections.

6.2.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.2.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.2.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.2.4 OEM BIOS Code/Data

With the congatec embedded BIOS it is possible for system designers to add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table (OA2.0), Windows 8 OEM activation (OA3.0), verb tables for HDA codecs, PCI/PCIe opROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

6.2.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.3 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-TR4 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about this subject, visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

6.4 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website.

6.5 Security Features

The conga-TR4 offers a discrete TPM 2.0 (Infineon SLB9665). This TPM includes coprocessors to calculate efficient hash and RSA algorithms with key lengths up to 2048 bits as well as a real random number generator. Security sensitive applications like gaming and e-commerce will benefit also with improved authentication, integrity and confidence levels. The conga-TR4 also offers AMD Secure Processor™.

6.6 Suspend to Ram

The Suspend to RAM feature is available on the conga-TR4.

7 conga Tech Notes

The conga-TR4 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

7.1 AMD Processor Features

Zen microarchitecture:

- Fetch Four x86 instructions
- TLBs (Translation Lookaside Buffers) in Branch Prediction pipe
- Micro-op Cache 2K instructions
- 4 Integer Execution units
- 2 Floating Point units x 128 Fmacs
- 2 Load/Store units
- 64K, 4-way L1 Instruction cache
- 32K, 8-way L1 Data cache
- 512K L2 cache

For more information about AMD Technology, visit http://www.amd.com.

7.2 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-TR4 ACPI thermal solution offers three different cooling policies:

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the "active cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points. If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.3 ACPI Suspend Modes and Resume Events

conga-TR4 supports S3 (STR= Suspend to RAM).

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by most operating systems (S4_OS= Hibernate).

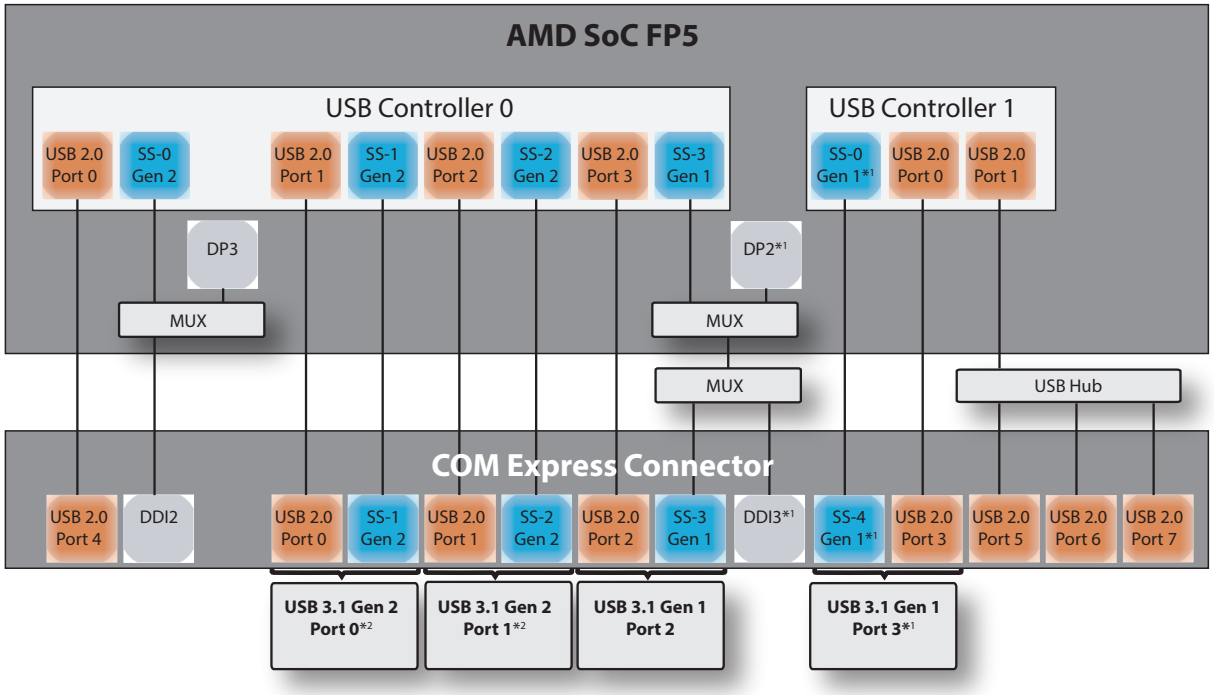
This table lists the "Wake Events" that resume the system from S3 unless otherwise stated in the "Conditions/Remarks" column:

Table 10 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
SMBALERT#	Wakes unconditionally from S3-S5.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
WAKE#	Wakes uncondionally from S3.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

7.4 USB Host Controller

The conga-TR4 offers signals for eight USB 2.0 ports. The signals for USB 2.0 ports 0-4 are routed from the SoC. The signals for USB 2.0 ports 5-7 are routed from a USB hub on the module. The USB 2.0 signals can be combined with USB SuperSpeed signals to create up to two USB 3.1 Gen 2 ports and two USB 3.1 Gen 1 ports (Only one Gen 1 port in R-Series). One USB port is shared with the DDI3 port (N/A in R-Series).



Note

*1 *Not available in the R-Series.*

*2 *The USB ports are configured in the BIOS setup menu to operate in Gen 1 mode. Before changing the setting to Gen 2, ensure the carrier board is designed for Gen 2 operation. For USB 3.1 Gen 2 design considerations, contact congatec technical support.*

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type 6 connectors used for congatec AG modules. The pinout of the modules complies with COM Express Type 6 Rev. 2.1.

Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Table 11 Signal Tables Terminology Descriptions

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PU	Implemented pull-up resistor
PD	Implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O 3.3VSB	Bi-directional signal 3.3V tolerant active in standby state
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
P	Power Input
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification
PEG	PCI Express Graphics
SATA	In compliance with Serial ATA specification, Revision 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

8.1 A-B Connector Signal Descriptions

Table 12 Connector A-B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1 (*)	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	eDP_TX2+ / LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	eDP_TX2- / LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#	A73	eDP_TX1+ / LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	eDP_TX1- / LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	eDP_TX0+ / LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	eDP_TX0- / LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+	B22	SATA3_TX+	A77	eDP / LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX-	B23	SATA3_TX-	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	eDP / LVDS_BKLT_EN
A25	SATA2_RX+	B25	SATA3_RX+	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX-	B26	SATA3_RX-	A81	eDP_TX3+ / LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	eDP_TX3- / LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	HDA_SDIN2	A83	eDP_ AUX+ / LVDS_I2C_CK	B83	eDP / LVDS_BKLT_CTRL
A29	HDA_SYNC	B29	HDA_SDIN1	A84	eDP_AUX- / LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	HDA_RST#	B30	HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	HDA_BITCLK	B32	SPKR	A87	eDP_HPD	B87	VCC_5V_SBY
A33	HDA_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED (*)
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN (*)

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU (*)
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC (*)
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC (*)
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK (*)
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT (*)
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	RSVD
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	RSVD
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	ESPI EN#(*)	A102	SER1_RX	B102	FAN_TACHIN
A48	RSVD	B48	USB0_HOST_PRSNT(*)	A103	LID#	B103	SLEEP#
A49	GBE0_SDP	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-TR4.

Table 13 High Definition Audio Link Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST#	A30	Reset output to CODEC, active low.	O 3.3VSB		AC'97 codecs are not supported.
HDA_SYNC	A29	Sample-synchronization signal to the CODEC(s).	O 3.3VSB		AC'97 codecs are not supported.
HDA_BITCLK	A32	Serial data clock generated by the external CODEC(s).	O 3.3VSB		AC'97 codecs are not supported.
HDA_SDOUT	A33	Serial TDM data output to the CODEC.	O 3.3VSB		AC'97 codecs are not supported.
HDA_SDIN[2:0]	B28-B30	Serial TDM data inputs from up to 3 CODECs.	I 3.3VSB	PD 47k	AC'97 codecs are not supported.

Table 14 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC Mode: LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC Mode: LPC Frame indicates the start of a LPC cycle.	O 3.3V		
LPC_CLK	B10	LPC Mode: LPC clock output, 33MHz	O 3.3V		
LPC_DRQ0#	B8	LPC Mode: LPC serial DMA request	I 3.3V	PU 10K 3.3V	
LPC_DRQ1#	B8	LPC Mode: LPC serial DMA request	I 3.3V		Not supported
LPC_SERIRQ	A50	LPC Mode: LPC serial interrupt	I/O OD 3.3V	PU 10K 3.3V	
SUS_STAT#	B18	LPC Mode: SUS_STAT# indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon. LPC devices may need to preserve memory or isolate outputs during the low power state.	O 3.3V		
ESPI_EN#	B47	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on the module through a resistor. The Carrier should only float this line or pull it low.	I 3.3V		
BIOS_DIS0	A34	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low. Refer to table 4.13 of the COM Express Module Base Specification for strapping options of BIOS disable signals.	I		
BIOS_DIS1	B88		I		

Table 15 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0. Only two SATA ports can be set to active via BIOS setup.
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0. Only two SATA ports can be set to active via BIOS setup.
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0. Only two SATA ports can be set to active via BIOS setup.
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0. Only two SATA ports can be set to active via BIOS setup.
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0. Only two SATA ports can be set to active via BIOS setup.
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0. Only two SATA ports can be set to active via BIOS setup.
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0. Only two SATA ports can be set to active via BIOS setup.
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0. Only two SATA ports can be set to active via BIOS setup.
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V		

Table 16 USB 2.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1. Routed from a USB hub on the module.
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1. Routed from a USB hub on the module.
USB6+	A37	USB Port 6, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1. Routed from a USB hub on the module.
USB6-	A36	USB Port 6, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1. Routed from a USB hub on the module.
USB7+	B37	USB Port 7, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1. Routed from a USB hub on the module.
USB7-	B36	USB Port 7, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1. Routed from a USB hub on the module.
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

Table 17 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 18 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:				I/O Analog		Twisted pair signals for external transformer.
			1000	100	10			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.				O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.				O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.				O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.				O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.						Not connected

Note

The GBE0_LINK# output is only active during a 100Mbit or 1Gbit connection. It is not active during a 10Mbit connection. This is a limitation of Ethernet controller since it only has 3 LED outputs, ACT#, LINK100# and LINK1000#. The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TR4 module.

Table 19 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10K	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10K	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	OD 3.3V	PU 2.2K 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/OD 3.3V	PU 2.2K 3.3V	

Table 20 UART Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O 3.3V		Signal is driven to logic 1 only. External PD is required.
SER1_TX	A101	General purpose serial port transmitter	O 3.3V		Signal is driven to logic 1 only. External PD is required.
SER0_RX	A99	General purpose serial port receiver	I 3.3V	PU 47K 3.3V	
SER1_RX	A102	General purpose serial port receiver	I 3.3V	PU 47K 3.3V	

Table 21 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB		
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or left as no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or left as no-connect

Table 22 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins.	O 3.3V		
GPO1	B54	General purpose output pins.	O 3.3V		
GPO2	B57	General purpose output pins.	O 3.3V		
GPO3	B63	General purpose output pins.	O 3.3V		
GPI0	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI1	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI2	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI3	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	

Table 23 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/OD 3.3V	PU 2.2K 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/OD 3.3V	PU 2.2K 3.3VSB	
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V		
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM.	O OD 3.3V	PU 47K 3.3V	Signal is driven to logic 1 only. External PD is required.
FAN_TACHIN	B102	Fan tachometer input.	I OD	PU 47K 3.3V	Requires a fan with two-pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 10K	A TPM 2.0 chip is assembled on the module by default.

Note

The congatec COM Express Type 6 and Type 10 modules use a Push-Pull output for the fan_pwm signal instead of the open drain output specified in the COM Express specification. Although this does not comply with the COM Express specification 3.0, the benefits are obvious. The Push-Pull output optimizes the power consumed by the fan_pwm signal without functional change.

Table 24 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on rising edge. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V	PU 10K 3.3V	
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		Not supported
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10K 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10K 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10K 3.3VSB	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 10k 3.3V	
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 10k 3.3V	
SMB_CK	B13	System Management Bus bidirectional clock line.	I/O 3.3VSB	PU 2.2K 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line.	I/O OD 3.3VSB	PU 2.2K 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3VSB	PU 10K 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3V	PU 47K 3.3VSB	
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3V	PU 47K 3.3VSB	

Table 25 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

8.2 C-D Connector Signal Descriptions

Table 26 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1-	D56	PEG_TX1-
C2	GND	D2	GND	C57	TYPE1#	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PEG_RX2+	D58	PEG_TX2+
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PEG_RX2-	D59	PEG_TX2-
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PEG_RX3+	D61	PEG_TX3+
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PEG_RX3-	D62	PEG_TX3-
C8	GND	D8	GND	C63	RSVD	D63	DDPC_CTRLCLK (*)
C9	USB_SSRX2-	D9	USB_SSTX2-	C64	RSVD	D64	DDPC_CTRLDATA (*)
C10	USB_SSRX2+	D10	USB_SSTX2+	C65	PEG_RX4+	D65	PEG_TX4+
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4-	D66	PEG_TX4-
C12	USB_SSRX3-	D12	USB_SSTX3-	C67	RAPID SHUTDOWN(*)	D67	GND
C13	USB_SSRX3+	D13	USB_SSTX3+	C68	PEG_RX5+	D68	PEG_TX5+
C14	GND	D14	GND	C69	PEG_RX5-	D69	PEG_TX5-
C15	DDI1_PAIR6+(*)	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	DDI1_PAIR6- (*)	D16	DDI1_CTRLDATA_AUX-	C71	PEG_RX6+	D71	PEG_TX6+
C17	RSVD	D17	RSVD	C72	PEG_RX6-	D72	PEG_TX6-
C18	RSVD	D18	RSVD	C73	GND	D73	GND
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	PEG_RX7+	D74	PEG_TX7+
C20	PCIE_RX6-	D20	PCIE_TX6-	C75	PEG_RX7-	D75	PEG_TX7-
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+	D22	PCIE_TX7+	C77	RSVD	D77	RSVD
C23	PCIE_RX7-	D23	PCIE_TX7-	C78	PEG_RX8+ (*)	D78	PEG_TX8+ (*)
C24	DDI1_HPD	D24	RSVD	C79	PEG_RX8- (*)	D79	PEG_TX8- (*)
C25	DDI1_PAIR4+ (*)	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)
C26	DDI1_PAIR4- (*)	D26	DDI1_PAIR0+	C81	PEG_RX9+ (*)	D81	PEG_TX9+ (*)
C27	RSVD	D27	DDI1_PAIR0-	C82	PEG_RX9- (*)	D82	PEG_TX9- (*)
C28	RSVD	D28	RSVD	C83	RSVD	D83	RSVD
C29	DDI1_PAIR5+ (*)	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	DDI1_PAIR5- (*)	D30	DDI1_PAIR1-	C85	PEG_RX10+ (*)	D85	PEG_TX10+ (*)
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- (*)	D86	PEG_TX10- (*)
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+	C87	GND	D87	GND
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-	C88	PEG_RX11+ (*)	D88	PEG_TX11+ (*)
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11- (*)	D89	PEG_TX11- (*)
C35	RSVD	D35	RSVD	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+	C91	PEG_RX12+ (*)	D91	PEG_TX12+ (*)

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-	C92	PEG_RX12- (*)	D92	PEG_TX12- (*)
C38	DDI3_DDC_AUX_SEL	D38	RSVD	C93	GND	D93	GND
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+	C94	PEG_RX13+ (*)	D94	PEG_TX13+ (*)
C40	DDI3_PAIR0-	D40	DDI2_PAIR0-	C95	PEG_RX13- (*)	D95	PEG_TX13- (*)
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+	C97	RVSD	D97	RSVD
C43	DDI3_PAIR1-	D43	DDI2_PAIR1-	C98	PEG_RX14+ (*)	D98	PEG_TX14+ (*)
C44	DDI3_HPD	D44	DDI2_HPD	C99	PEG_RX14- (*)	D99	PEG_TX14- (*)
C45	RSVD	D45	RSVD	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+	C101	PEG_RX15+ (*)	D101	PEG_TX15+ (*)
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-	C102	PEG_RX15- (*)	D102	PEG_TX15- (*)
C48	RSVD	D48	RSVD	C103	GND	D103	GND
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3-	D50	DDI2_PAIR3-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+	D52	PEG_TX0+	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0-	D53	PEG_TX0-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV# (*)	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+	D55	PEG_TX1+	C110	GND (FIXED)	D110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-TR4.

Table 27 SuperSpeed USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX0-	C3		I		
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX0-	D3		O		
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX1-	C6		I		
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX1-	D6		O		
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX2-	C9		I		
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX2-	D9		O		
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX3-	C12		I		
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX3-	D12		O		

Table 28 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		Not supported in R-Series. Supports PCI Express Base Specification, Revision 3.0
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		Not supported in R-Series. Supports PCI Express Base Specification, Revision 3.0

Table 29 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs.	I PCIE		PEG_RX[8:15]± lanes are not supported.
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_TX0+	D52	PCI Express Graphics Transmit Output differential pairs.	O PCIE		PEG_TX[8:15]± lanes are not supported.
PEG_TX0-	D53				
PEG_TX1+	D55				
PEG_TX1-	D56				
PEG_TX2+	D58				
PEG_TX2-	D59				
PEG_TX3+	D61				
PEG_TX3-	D62				
PEG_TX4+	D65				
PEG_TX4-	D66				
PEG_TX5+	D68				
PEG_TX5-	D69				
PEG_TX6+	D71				
PEG_TX6-	D72				
PEG_TX7+	D74				
PEG_TX7-	D75				
PEG_TX8+	D78				
PEG_TX8-	D79				
PEG_TX9+	D81				
PEG_TX9-	D82				
PEG_TX10+	D85				
PEG_TX10-	D86				
PEG_TX11+	D88				
PEG_TX11-	D89				
PEG_TX12+	D91				
PEG_TX12-	D92				
PEG_TX13+	D94				
PEG_TX13-	D95				
PEG_TX14+	D98				
PEG_TX14-	D99				
PEG_TX15+	D101				
PEG_TX15-	D102				
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I		Not supported.

Note

The conga-TR4 supports PEG only up to x8 (x4 in R-Series).

Table 30 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with DP1_LANE0+ and TMDS1_DATA2+. Multiplexed with DP1_LANE0- and TMDS1_DATA2-.	O PCIE		
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with DP1_LANE1+ and TMDS1_DATA1+. Multiplexed with DP1_LANE1- and TMDS1_DATA1-.	O PCIE		
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with DP1_LANE2+ and TMDS1_DATA0+. Multiplexed with DP1_LANE2- and TMDS1_DATA0-.	O PCIE		
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with DP1_LANE3+ and TMDS1_CLK+. Multiplexed with DP1_LANE3- and TMDS1_CLK-.	O PCIE		
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD.	I 3.3V	PD 100K	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with DP1_AUX+ and HMDI1_CTRLCLK. DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high.	I/O PCIE OD 3.3V	PD 100K	
DDI1_CTRLDATA_AUX-	D16	Multiplexed with DP1_AUX- and HDMI1_CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high.	I/O PCIE I/OD 3.3V	PU 100K 3.3V	
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1M	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+ and TMDS2_DATA2+. Multiplexed with DP2_LANE0- and TMDS2_DATA2-.	O PCIE		
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+ and TMDS2_DATA1+. Multiplexed with DP2_LANE1- and TMDS2_DATA1-.	O PCIE		
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+ and TMDS2_DATA0+. Multiplexed with DP2_LANE2- and TMDS2_DATA0-.	O PCIE		
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+ and TMDS2_CLK+. Multiplexed with DP2_LANE3- and TMDS2_CLK-.	O PCIE		
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD.	I 3.3V	PD 100K	
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+ and HDMI2_CTRLCLK. DP AUX+ function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	I/O PCIE OD 3.3V	PD 100K	
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA. DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE I/OD 3.3V	PU 100K 3.3V	
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V	PD 1M	
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+. Multiplexed with DP3_LANE0- and TMDS3_DATA2-.	O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+. Multiplexed with DP3_LANE1- and TMDS3_DATA1-.	O PCIE		
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+. Multiplexed with DP3_LANE2- and TMDS3_DATA0-.	O PCIE		
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+. Multiplexed with DP3_LANE3- and TMDS3_CLK-.	O PCIE		
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3_HPD.	I 3.3V	PD 100K	
DDI3_CTRLCLK_AUX+	C36	Multiplexed with DP3_AUX+ and HDMI3_CTRLCLK. DP AUX+ function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high	I/O PCIE OD 3.3V	PD 100k	
DDI3_CTRLDATA_AUX-	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA. DP AUX- function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high.	I/O PCIE I/OD 3.3V	PU 100k	
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V	PD 1M	

Note

The DDI interfaces support dual-mode DisplayPort. To support HDMI/DVI, an external level shifter (PTN3360D) should be implemented on the user's carrier board.

Table 31 HDMI/DVI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS1_CLK + TMDS1_CLK -	D36 D37	HDMI/DVI TMDS Clock output differential pair. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
TMDS1_DATA0+ TMDS1_DATA0-	D32 D33	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
TMDS1_DATA1+ TMDS1_DATA1-	D29 D30	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-.	O PCIE		
TMDS1_DATA2+ TMDS1_DATA2-	D26 D27	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
HDMI1_HPD	C24	HDMI/DVI Hot-plug detect. Multiplexed with DDI1_HPD.	I PCIE	PD 100K	
HDMI1_CTRLCLK	D15	HDMI/DVI I^2C Control Clock. Multiplexed with DDI1_CTRLCLK_AUX+	OD 3.3V	PD 100K	2.2k to 3.3V Pull-up must be implemented on the carrier board.
HDMI1_CTRLDATA	D16	HDMI/DVI I^2C Control Data Multiplexed with DDI1_CTRLDATA_AUX-	I/OD 3.3V	PU 100K 3.3V	2.2k to 3.3V Pull-up must be implemented on the carrier board.

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS2_CLK + TMDS2_CLK -	D49 D50	HDMI/DVI TMDS Clock output differential pair.. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-.	O PCIE		
TMDS2_DATA0+ TMDS2_DATA0-	D46 D47	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-.	O PCIE		
TMDS2_DATA1+ TMDS2_DATA1-	D42 D43	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-.	O PCIE		
TMDS2_DATA2+ TMDS2_DATA2-	D39 D40	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-..	O PCIE		
HDMI2_HPD	D44	HDMI/DVI Hot-plug detect. Multiplexed with DDI2_HPD	I PCIE	PD 100K	
HDMI2_CTRLCLK	C32	HDMI/DVI I²C Control Clock Multiplexed with DDI2_CTRLCLK_AUX+	OD 3.3V	PD 100K	2.2k to 3.3V Pull-up must be implemented on the carrier board.
HDM12_CTRLDATA	C33	HDMI/DVI I²C Control Data Multiplexed with DDI2_CTRLDATA_AUX-	I/OD 3.3V	PU 100K 3.3V	2.2k to 3.3V Pull-up must be implemented on the carrier board.
TMDS3_CLK + TMDS3_CLK -	C49 C50	HDMI/DVI TMDS Clock output differential pair.. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		
TMDS3_DATA0+ TMDS3_DATA0-	C46 C47	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		
TMDS3_DATA1+ TMDS3_DATA1-	C42 C43	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-..	O PCIE		
TMDS3_DATA2+ TMDS3_DATA2-	C39 C40	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		
HDMI3_HPD	C44	HDMI/DVI Hot-plug detect. Multiplexed with DDI3_HPD.	I PCIE	PD 100K	
HDMI3_CTRLCLK	C36	HDMI/DVI I²C Control Clock. Multiplexed with DDI3_CTRLCLK_AUX+	OD 3.3V	PD 100K	2.2k to 3.3V Pull-up should be implemented on the carrier board.
HDMI3_CTRLDATA	C37	HDMI/DVI I²C Control Data. Multiplexed with DDI3_CTRLDATA_AUX-	I/OD 3.3V	PU 100K 3.3V	2.2k to 3.3V Pull-up should be implemented on the carrier board.

Note

To support the HDMI interface, an external level translator/shifter (e.g. PTN3360D) should be implemented on the user's baseboard.

Table 32 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP1_LANE3+ DP1_LANE3-	D36 D37	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
DP1_LANE2+ DP1_LANE2-	D32 D33	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
DP1_LANE1+ DP1_LANE1-	D29 D30	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-.	O PCIE		
DP1_LANE0+ DP1_LANE0-	D26 D27	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
DP1_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI1_HPD.	I 3.3V	PD 100K	
DP1_AUX+	D15	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100K	
DP1_AUX-	D16	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100K 3.3V	
DP2_LANE3+ DP2_LANE3-	D49 D50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O PCIE		
DP2_LANE2+ DP2_LANE2-	D46 D47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O PCIE		
DP2_LANE1+ DP2_LANE1-	D42 D43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O PCIE		
DP2_LANE0+ DP2_LANE0-	D39 D40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR0+ and DDI1_PAIR0-	O PCIE		
DP2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI2_HPD.	I 3.3V	PD 100K	
DP2_AUX+	C32	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100K	
DP2_AUX-	C33	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100K 3.3V	
DP3_LANE3+ DP3_LANE3-	C49 C50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		
DP3_LANE2+ DP3_LANE2-	C46 C47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		
DP3_LANE1+ DP3_LANE1-	C42 C43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-.	O PCIE		
DP3_LANE0+ DP3_LANE0-	C39 C40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		
DP3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI3_HPD.	I 3.3V	PD 100K	
DP3_AUX+	C36	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP3_AUX-	C37	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	

Table 33 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins do not matter (X). TYPE2# / TYPE1# / TYPE0# / X / X / X / Pinout Type 1 (deprecated) NC / NC / NC / Pinout Type 2 (deprecated) NC / NC / GND / Pinout Type 3 (deprecated) NC / GND / NC / Pinout Type 4 (deprecated) NC / GND / GND / Pinout Type 5 (deprecated) GND / NC / NC / Pinout Type 6 GND / NC / GND / Pinout Type 7 X / X / X / Pinout Type 10 The carrier board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The carrier board logic may also implement a fault indicator such as an LED.	PDS	TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard. The conga-TR4 is based on the COM Express Type 6 pinout therefore the pins 0 and 1 are not connected and pin 2 is connected to GND.
TYPE10#	A97	Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed. TYPE10# NC – Pinout R2.0 PD – Pinout Type 10 pull down to ground with 4.7k resistor 12V – Pinout R1.0 This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. R3.0 module types 6 and 7 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7K resistor.resistor.	PDS	Not connected to indicate "Pinout R2.0".

Table 34 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-TR4 module is functionally identical with a standard PC/AT.

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.1.1 LPC Bus

On the conga-TR4, the PCIExpress Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCIExpress Bus—not the LPC Bus. Only specified I/O ranges are forwarded to the LPC Bus.

On the conga-TR4, the following I/O address ranges are sent to the LPC Bus:

SupperIO Index	2Eh-2Fh
SerialPort0	3F8h-3FFh
SerialPort1	2F8h-2FFh
SerialPort2	3F0h-3F7h
SerialPort3	3E0h-3E7h
SerialPort4	2F0h-2F7h
SerialPort5	2E0h-2E7h
SerialPort6	3E8h-3EFh
SerialPort7	2E8h-2EFh
KbcPort	60h, 64h
BoardController	E00h-FFFh

Some of these ranges are not available if a Super I/O is used on the carrier board or if they are occupied by the COMExpress on-module UARTs (they can be enabled in BIOS setup). The I/O range E38h-EBFh is always used by on-module LPC devices. Otherwise, the ranges listed above are available for customer use.

If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 35 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Device ID	Description and Device ID
00h	00h	00h	0x15D0	Root Complex
00h	00h	02h	0x15D1	IOMMU
00h	01h	00h	0x1452	PCIe Dummy Host Bridge
00h (see Note 2)	01h	01h	0x15D3	PCIe PEG Bridge 0
00h (see Note 4)	01h	02h	0x15D3	PCIe PEG Bridge 1
00h (see Note 1)	01h	03h	0x15D3	PCIe GPP Bridge 0
00h (see Note 1)	01h	04h	0x15D3	PCIe GPP Bridge 1
00h (see Note 1)	01h	05h	0x15D3	PCIe GPP Bridge 2
00h (see Note 1)	01h	06h	0x15D3	PCIe GPP Bridge 3
00h (see Note 1)	01h	07h	0x15D3	PCIe GPP Bridge 4
00h	08h	00h	0x1452	PCIe Dummy Host Bridge
00h	08h	01h	0x15DB	Internal PCIe GPP Bridge 0 to Bus A
00h	08h	02h	0x15DC	Internal PCIe GPP Bridge 0 to Bus B
00h	14h	00h	0x790B	SMBus Controller
00h	14h	03h	0x790E	LPC Bridge
00h	18h	00h	0x15E8	Data Fabric
00h	18h	01h	0x15E9	Data Fabric
00h	18h	02h	0x15EA	Data Fabric
00h	18h	03h	0x15EB	Data Fabric
00h	18h	04h	0x15EC	Data Fabric
00h	18h	05h	0x15ED	Data Fabric
00h	18h	06h	0x15EE	Data Fabric
00h	18h	07h	0x15EF	Data Fabric
01h (see Note 3)	00h	00h		PCI Express Port 0
02h (see Note 3)	00h	00h		PCI Express Port 1
03h (see Note 3)	00h	00h		PCI Express Port 2
04h (see Note 3)	00h	00h		PCI Express Port 3
05h	00h	00h	0x2608	PCI Express Switch
06h	01h	00h	0x2608	PCI Express Switch port 0
06h	02h	00h	0x2608	PCI Express Switch port 1
06h	03h	00h	0x2608	PCI Express Switch port 2
06h	04h	00h	0x2608	PCI Express Switch port 3
06h	05h	00h	0x2608	PCI Express Switch port 4
07h (see Note 3)	00h	00h		PCI Express Port 4
08h (see Note 3)	00h	00h		PCI Express Port 5
09h (see Note 3)	00h	00h		PCI Express Port 6

0Ah	00h	00h		Intel PCIe Ethernet Network on Module
0Bh (see Note 3)	00h	00h		PCI Express Port 7
Bus A	00h	00h	Internal	Internal GPU
Bus A	00h	01h	Internal	Display HD Audio Controller
Bus A	00h	02h	Internal	Cryptographic Coprocessor
Bus A	00h	03h	Internal	USB 3.1
Bus A	00h	04h	Internal	USB 3.1
Bus A	00h	05h	Internal	Audio Processor
Bus A	00h	06h	Internal	Audio Processor – HD Audio Controller
Bus A	00h	07h	Internal	SCSI PCIe
Bus B	00h	00h	Internal	SATA AHCI Mode

Note

1. *The PCI Express Ports may only be visible if the PCI Express Port is set to "Enabled" in BIOS setup and a device is attached to the corresponding PCI Express port on the carrier board.*

2. *The PCI Express Graphics Ports may only be visible if the PCI Express Graphics Port is set to "Enabled" in BIOS setup and a device is attached to the corresponding PCI Express port on the carrier board.*

3. *The above table represents a case when a single function PCI Express device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*

4. *The PCI Express Port may only be visible if PEG port is set to 2 x4 and a device is attached to the corresponding PCI Express port on the carrier board.*

9.3 I²C Bus

There are no on-board resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.4 SM Bus

System Management (SM) bus signals are connected to the AMD Chipset and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject please contact congatec technical support.

10 BIOS Setup Description

The BIOS setup description of the conga-TR4 can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-TR4 is identified as TR44R1xx, where:

- R is the identifier for a BIOS ROM file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The conga-TR4 binary size is 8 MB.

10.3 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-TR4 features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

10.4 Supported Flash Devices

The conga-TR4 supports the following flash devices:

- Winbond W25Q64JVSSIQ (8MB)

The flash device listed above can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.

11 Industry Specifications

Table 36 References

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	www.intel.com
Universal Serial Bus (USB) Specification, Revision 2.0	www.usb.org
PCI Specification, Revision 2.3	www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0	www.serialata.org
PICMG® COM Express Module™ Base Specification	www.picmg.org
PCI Express Base Specification, Revision 2.0	www.pcisig.com/specifications