



**MODEL:  
HPCIE-Q170**

**Half-Size PICMG 1.3 CPU Card Supports 6th/7th Generation LGA1151 Intel® Core™ i7/i5/i3, Pentium® or Celeron® CPU, Intel® Q170 Chipset, DDR4 SO-DIMM, Dual Intel® PCIe GbE, VGA, iDP, USB 3.0, SATA 6Gb/s, mSATA, Intel® AMT and RoHS**

## **User Manual**

# Revision

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Date	Version	Changes
November 13, 2017	1.03	Updated supported CPUs
September 5, 2017	1.02	Modified <b>J_FLASH1</b> jumper location
February 8, 2017	1.01	Updated 2.4 Optional Items
October 24, 2016	1.00	Initial release

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# Manual Conventions

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**WARNING**

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.

**CAUTION**

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.

**NOTE**

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

**HOT SURFACE**

This symbol indicates a hot surface that should not be touched without taking care.

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Chapter

1

# Introduction

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## 1.1 Introduction



**Figure 1-1: HPCIE-Q170**

The HPCIE-Q170 is a half-size PICMG 1.3 CPU card. It accepts a Socket LGA1151 6th/7th generation Intel® Core™ i7/i5/i3, Pentium® or Celeron® processor and supports two 260-pin 2133/1867 MHz dual-channel DDR4 SO-DIMM modules up to 32 GB.

The HPCIE-Q170 provides two GbE interfaces through the Intel® I219LM (with Intel® AMT 11.0 support) and the Intel® I211 PCIe controllers. The integrated Intel® Q170 chipset supports two SATA 6Gb/s drives with RAID 0/1 function. In addition, the HPCIE-Q170 includes VGA and iDP interfaces for dual independent display.

Two USB 3.0 on the rear panel, four USB 2.0 by pin headers, two RS-232/422/485 and one PCIe Mini interface (supports mSATA and USB 2.0) provide flexible expansion options. High Definition Audio (HDA) support ensures HDA devices can be easily implemented on the HPCIE-Q170.

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 1.2 Features

Some of the HPCIE-Q170 motherboard features are listed below:

- Half-size PICMG 1.3 CPU card
- 6th/7th generation LGA1151 Intel® Core™ i7/i5/i3, Pentium® or Celeron® processor supported
- Intel® Q170 chipset
- Two 260-pin 2133/1867 MHz dual-channel non-ECC unbuffered DDR4 SO-DIMMs support (system max. 32 GB)
- Two Intel® PCIe GbE connectors (LAN1 with Intel® AMT 11.0 support)
- Dual independent display by VGA and iDP interfaces
- One full-size/half-size PCIe Mini slot supports mSATA and USB 2.0
- Two SATA 6Gb/s connectors support RAID 0/1 function
- Two USB 3.0 ports on the rear I/O
- Four USB 2.0 ports via internal pin headers
- Two RS-232/422/485 serial ports
- High Definition Audio
- RoHS compliant

### 1.3 Connectors

The connectors on the HPCIIE-Q170 are shown in the figure below.

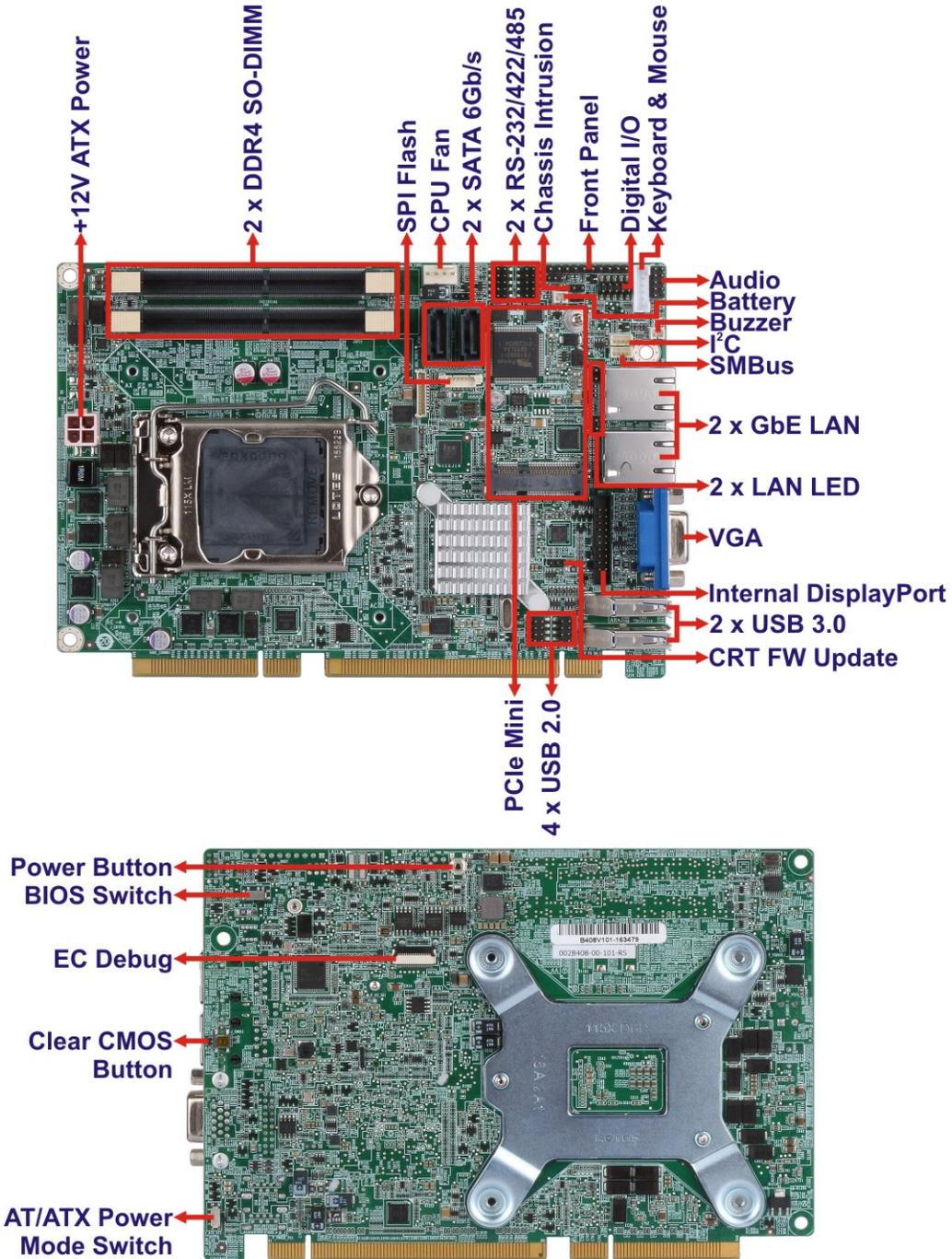
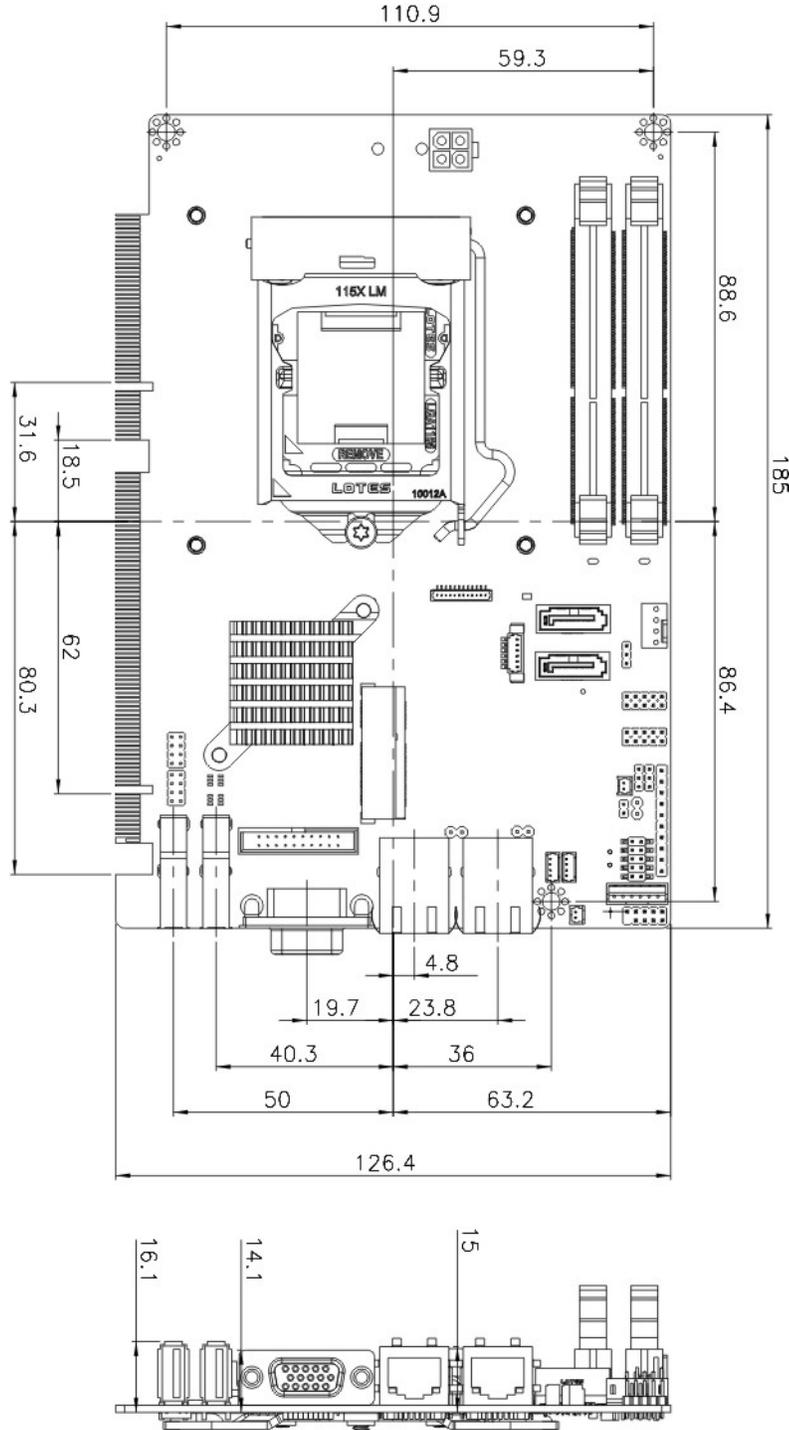


Figure 1-2: Connectors

**HPCIE-Q170 Half-size PICMG 1.3 CPU Card**

**1.4 Dimensions**

The main dimensions of the HPCIE-Q170 are shown in the diagram below.



**Figure 1-3: HPCIE-Q170 Dimensions (mm)**

### 1.5 Data Flow

Figure 1-4 shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

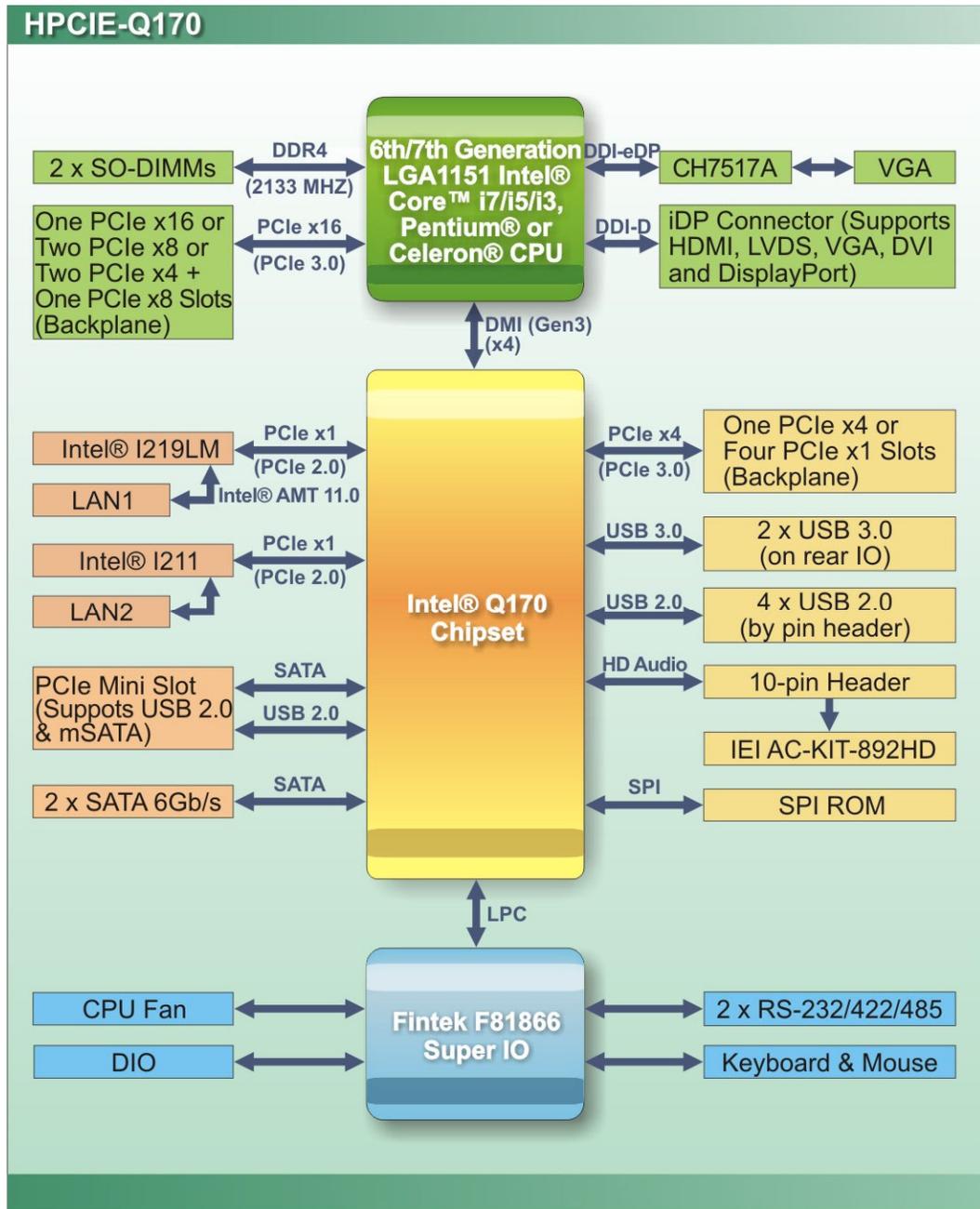


Figure 1-4: Data Flow Diagram

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 1.6 Technical Specifications

The HPCIE-Q170 technical specifications are listed below.

Specification/Model	HPCIE-Q170
<b>Form Factor</b>	Half-size PICMG 1.3 CPU card
<b>CPU Supported</b>	6th/7th generation LGA1151 Intel® Core™ i7/i5/i3, Pentium® or Celeron® CPU
<b>PCH</b>	Intel® Q170
<b>Memory</b>	Two 260-pin 2133/1867 MHz dual-channel non-ECC unbuffered DDR4 SO-DIMMs support (system max. 32 GB)
<b>Graphics Engine</b>	Intel® HD Graphics Gen9 engine supports DirectX 11/12, OpenCL 2.x and OpenGL 4.3/4.4 Decode/encode for HEVC, VP8, VP9, VDENC
<b>Display Output</b>	Supports dual independent display One VGA (via Chrontel CH7517A, up to 1920x1200@60 Hz) One iDP interface for HDMI, LVDS, VGA, DVI and DisplayPort (up to 3840x2160@60 Hz)
<b>Ethernet Controllers</b>	<b>LAN1:</b> Intel® I219LM PCIe GbE controller with Intel® AMT 11.0 support <b>LAN2:</b> Intel® I211 PCIe GbE controller
<b>Audio</b>	Supports 7.1-channel HD audio by IEI AC-KIT-892HD kit
<b>Expansion</b>	One PCIe Mini slot supports mSATA and USB 2.0 <b>16-lane PCIe link from CPU via golden finger:</b> Supports one PCIe x16, or two PCIe x8, or two PCIe x4 + one PCIe x8 slots on the backplane (configured via BIOS) <b>4-lane PCIe link from PCH via golden finger:</b> Supports four PCIe x1 slots or one PCIe x4 slot on the backplane (configured via BIOS switch)
<b>Super I/O Controller</b>	Fintek F81866
<b>Watchdog Timer</b>	Software programmable supports 1~255 sec. system reset
<b>BIOS</b>	UEFI BIOS

External I/O Interface Connectors	
<b>Display Output</b>	One VGA connector
<b>Ethernet</b>	Two RJ-45 ports
<b>USB 3.0</b>	Two USB 3.0 ports * The Windows® 7 installation media does not include native driver support for USB 3.0. In order to use the USB keyboard or mouse connected to a USB 3.0 port during OS installation, the user has to update the Windows® 7 installation image so that it contains USB 3.0 drivers. Please refer to Section 4.10 for detailed installation procedures.
Internal I/O Interface Connectors	
<b>Audio Connector</b>	One audio connector (10-pin header)
<b>Chassis Intrusion</b>	One 2-pin header
<b>Digital I/O</b>	8-bit digital I/O
<b>Fan</b>	One 4-pin CPU smart fan connector
<b>Front Panel</b>	One 10-pin header (power LED, HDD LED, power button, reset button)
<b>I<sup>2</sup>C</b>	One 4-pin wafer connector
<b>Internal DisplayPort</b>	One 20-pin box header
<b>Keyboard and Mouse</b>	One internal keyboard and mouse connector (6-pin wafer)
<b>LAN LED</b>	Two 2-pin headers for LAN1 LED and LAN2 LED
<b>Serial ATA</b>	Two SATA 6Gb/s connectors (support RAID 0, 1)
<b>Serial Ports</b>	Two RS-232/422/485 via internal 10-pin headers
<b>SMBus</b>	One 4-pin wafer connector
<b>USB 2.0</b>	Four USB 2.0 ports by two internal pin headers
Environmental and Power Specifications	
<b>Power Supply</b>	5V/12V, AT/ATX power support
<b>Power Consumption</b>	5V@0.15A, 12V@8.39A, 3.3V@0.11A, 5VSB@0.21A (4.0 GHz Intel® Core™ i7-6700K CPU with two 16 GB 2133 MHz DDR4 memory)

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

<b>Operating Temperature</b>	-20°C ~ 60°C
<b>Storage Temperature</b>	-30°C ~ 70°C
<b>Operating Humidity</b>	5% ~ 95% (non-condensing)
<b>Physical Specifications</b>	
<b>Dimensions</b>	185 mm x 126 mm
<b>Weight (GW/NW)</b>	1000 g/420 g

Table 1-1: HPCIE-Q170 Specifications

Chapter

**2**

# Packing List

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## 2.1 Anti-static Precautions

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### WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

---

Make sure to adhere to the following guidelines:

- **Wear an anti-static wristband:** Wearing an anti-static wristband can prevent electrostatic discharge.
- **Self-grounding:** Touch a grounded conductor every few minutes to discharge any excess static buildup.
- **Use an anti-static pad:** When configuring any circuit board, place it on an anti-static mat.
- **Only handle the edges of the PCB:** Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

## 2.2 Unpacking Precautions

When the HPCIE-Q170 is unpacked, please do the following:

- Follow the anti-static guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

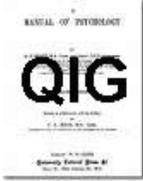
## 2.3 Packing List



**NOTE:**

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the HPCIE-Q170 was purchased from or contact an IEI sales representative directly by sending an email to [sales@ieiworld.com](mailto:sales@ieiworld.com).

The HPCIE-Q170 is shipped with the following components:

Quantity	Item and Part Number	Image
1	HPCIE-Q170 CPU card	
1	SATA cable	
1	Utility CD	
1	Quick installation guide	

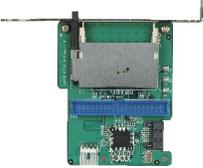
**Table 2-1: Packing List**

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 2.4 Optional Items

The following are optional components which may be separately purchased:

Item and Part Number	Image
RS-232 cable with bracket (P/N: 19800-000300-100-RS)	
PS/2 KB/MS Y-cable with bracket (P/N: 19800-000075-RS)	
SATA power cable (P/N: 32102-000100-200-RS)	
7.1-channel HD audio kit with Realtek ALC892 audio codec supporting dual audio stream (P/N: AC-KIT-892HD-R10)	
High-performance LGA1155/LGA1156 cooler kit (1U chassis compatible, 73W) (P/N: CF-1156A-RS-R11)	
LGA1155/LGA1156 cooler kit (1U chassis compatible, 45W) (P/N: CF-1156C-RS)	
LGA1155/LGA1156 cooler kit (1U chassis compatible, 65W) (P/N: CF-1156D-RS)	
DisplayPort to HDMI converter board (for IEI iDP connector) (P/N: DP-HDMI-R10)	

Item and Part Number	Image
DisplayPort to LVDS converter board (for IEI iDP connector) (P/N: DP-LVDS-R10)	
DisplayPort to VGA converter board (for IEI iDP connector) (P/N: DP-VGA-R10)	
DisplayPort to DVI-D converter board (for IEI iDP connector) (P/N: DP-DVI-R10)	
DisplayPort to DisplayPort converter board (for IEI iDP connector) (P/N: DP-DP-R10)	
SATA to IDE/CompactFlash® converter board (P/N: SAIDE-KIT01-R10)	

**Table 2-2: Optional Items**

Chapter

**3**

# Connectors

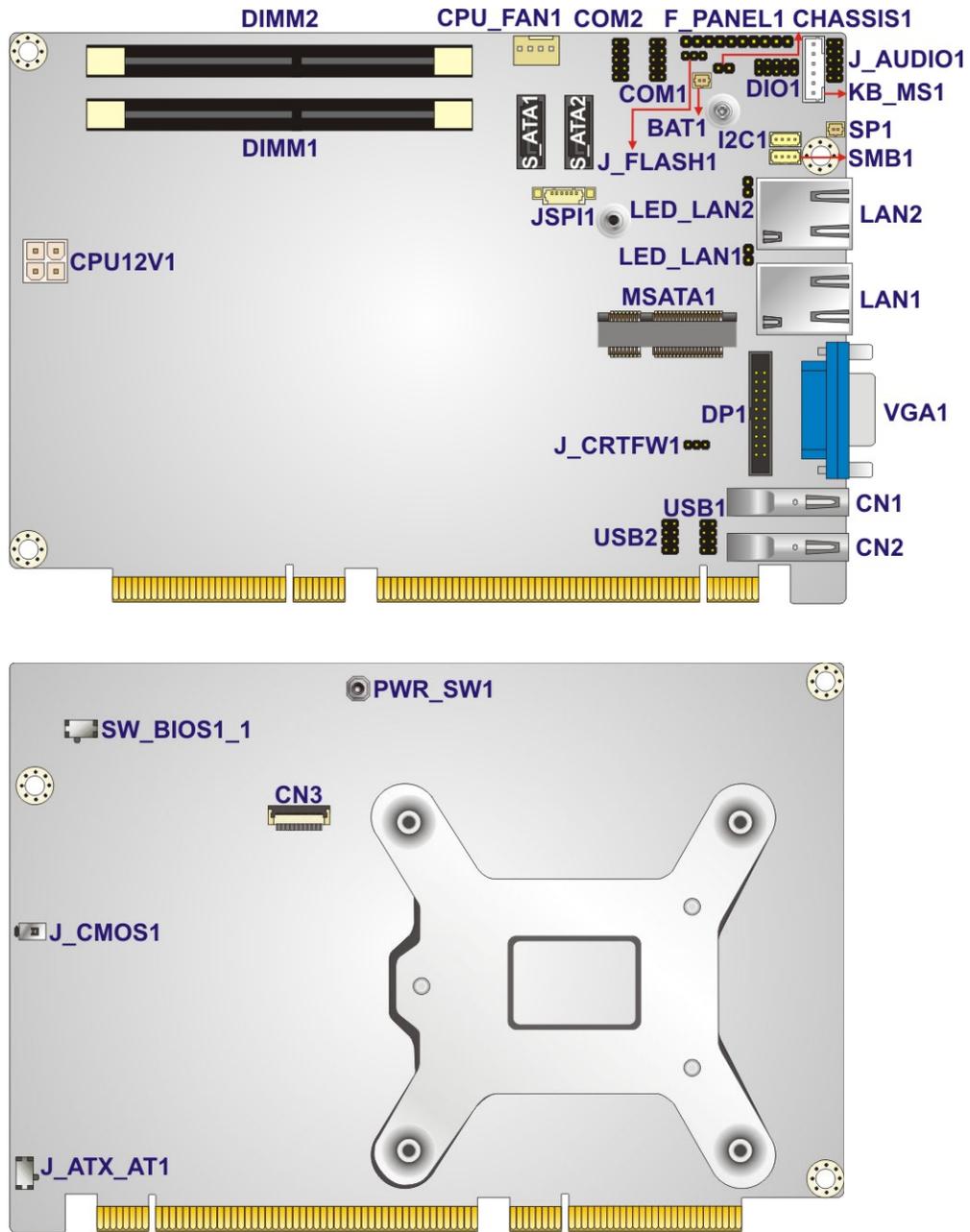
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### 3.1 Peripheral Interface Connectors

This chapter details all the peripheral interface connectors.

#### 3.1.1 HPCIE-Q170 Layout

The figure below shows all the peripheral interface connectors.



**Figure 3-1: Peripheral Interface Connectors**

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
+12V ATX power supply connector	4-pin Molex power connector	CPU12V1
Audio kit connector	10-pin header	J_AUDIO1
Battery connector	2-pin wafer	BAT1
Buzzer connector	2-pin wafer	SP1
Chassis intrusion connector	2-pin header	CHASSIS1
CRT FW update	3-pin header	J_CRTFW1
DDR4 SO-DIMM slots	260-pin DDR4 SO-DIMM slot	DIMM1, DIMM2
Digital I/O connector	10-pin header	DIO1
EC debug connector	20-pin wafer	CN3
Fan connector (CPU)	4-pin wafer	CPU_FAN1
Front panel connector	10-pin header	F_PANEL1
I <sup>2</sup> C connector	4-pin wafer	I2C1
Internal DisplayPort connector	20-pin box header	DP1
Keyboard and mouse connector	6-pin wafer	KB_MS1
LAN LED connectors	2-pin header	LED_LAN1, LED_LAN2
PCIe Mini slot	PCIe Mini slot	MSATA1
Power button	Push button	PWR_SW1
RS-232/422/485 serial ports	10-pin header	COM1, COM2
SATA 6Gb/s drive connector	7-pin SATA connector	S_ATA1, S_ATA2
SMBus connector	4-pin wafer	SMB1
SPI flash connector	6-pin wafer	JSPI1
USB 2.0 connectors	8-pin header	USB1, USB2

**Table 3-1: Peripheral Interface Connectors**

### 3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
Ethernet ports	RJ-45	LAN1, LAN2
USB 3.0 ports	USB 3.0	CN1, CN2
VGA connector	15-pin female	VGA1

**Table 3-2: External Peripheral Connectors**

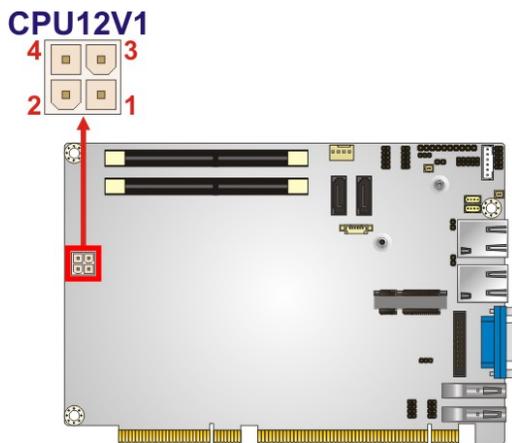
## 3.2 Internal Peripheral Connectors

The section describes all of the connectors on the HPCIE-Q170.

### 3.2.1 +12V ATX Power Connector

- CN Label:** CPU12V1
- CN Type:** 4-pin Molex power connector, p=4.2 mm
- CN Location:** See **Figure 3-2**
- CN Pinouts:** See **Table 3-3**

This connector provides power to the CPU.



**Figure 3-2: +12V ATX Power Connector Pinout Location**

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

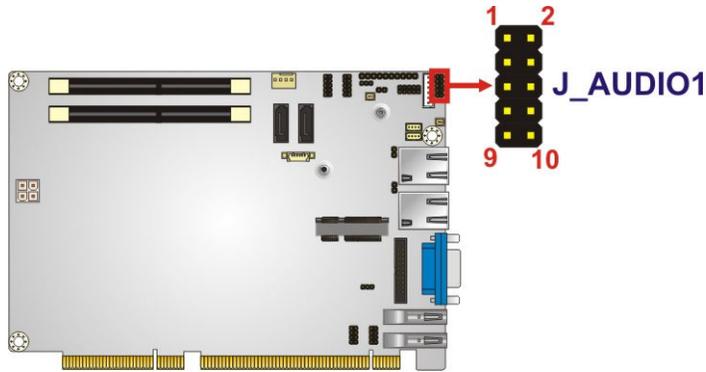
Pin	Description	Pin	Description
1	GND	2	GND
3	+12V	4	+12V

**Table 3-3: +12V ATX Power Connector Pinouts**

### 3.2.2 Audio Kit Connector

- CN Label:** J\_AUDIO1
- CN Type:** 10-pin header, p=2.00 mm
- CN Location:** See Figure 3-3
- CN Pinouts:** See Table 3-4

This connector allows connection to an external audio kit.



**Figure 3-3: Audio Connector Location**

Pin	Description	Pin	Description
1	HDA_SYNC	2	HDA_BIT_CLK
3	HDA_SDOUT	4	HDA_SPKR
5	HDA_SDIN	6	HDA_RST#
7	HDA_VCC	8	HDA_GND
9	HDA_+12V	10	HDA_GND

**Table 3-4: Audio Connector Pinouts**

### 3.2.3 Battery Connector



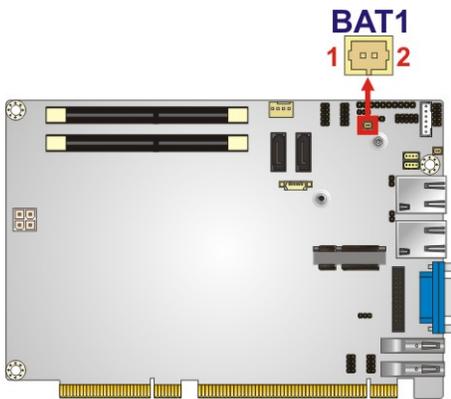
**CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- CN Label:**            **BAT1**
- CN Type:**            2-pin wafer, p=1.25 mm
- CN Location:**      See **Figure 3-4**
- CN Pinouts:**        See **Table 3-5**

This is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.



**Figure 3-4: Battery Connector Location**

Pin	Description
1	VBATT
2	GND

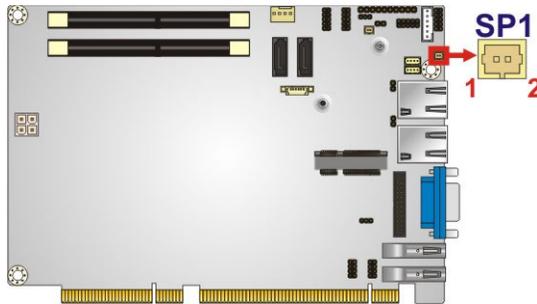
**Table 3-5: Battery Connector Pinouts**

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 3.2.4 Buzzer Connector

- CN Label:** SP1
- CN Type:** 2-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-5**
- CN Pinouts:** See **Table 3-6**

The buzzer connector is connected to the buzzer.



**Figure 3-5: Buzzer Connector Location**

Pin	Description
1	+V5S
2	GND

**Table 3-6: Buzzer Connector Pinouts**

### 3.2.5 Chassis Intrusion Connector

- CN Label:** CHASSIS1
- CN Type:** 2-pin header, p=2.54 mm
- CN Location:** See **Figure 3-6**
- CN Pinouts:** See **Table 3-7**

The chassis intrusion connector is for a chassis intrusion detection sensor or switch that detects if a chassis component is removed or replaced.

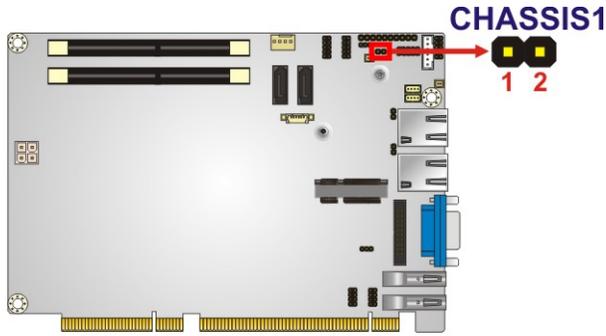


Figure 3-6: Chassis Intrusion Connector Location

Pin	Description
1	+3.3VSB
2	CHASSIS OPEN

Table 3-7: Chassis Intrusion Connector Pinouts

### 3.2.6 CRT FW Update Connector

- CN Label:** J\_CRTFW1
- CN Type:** 3-pin header, p=2.00 mm
- CN Location:** See Figure 3-7
- CN Pinouts:** See Table 3-8

The CRT FW update connector is used to update the CRT firmware.

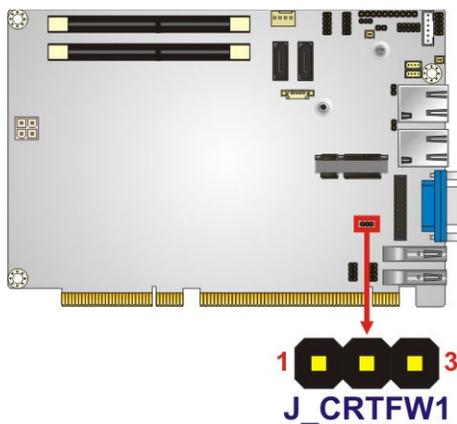


Figure 3-7: CRT FW Update Connector Location

**HPCIE-Q170 Half-size PICMG 1.3 CPU Card**

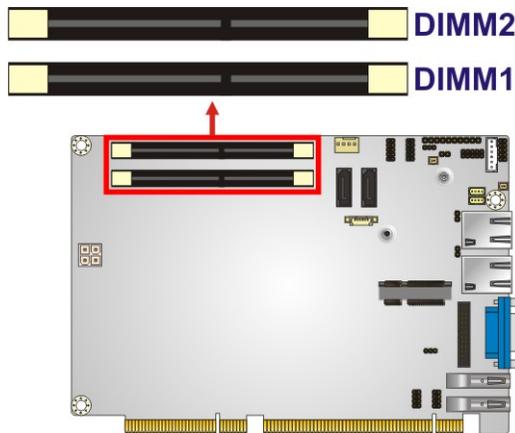
Pin	Description
1	SPC
2	SPD
3	GND

**Table 3-8: CRT FW Update Connector Pinouts**

**3.2.7 DDR4 SO-DIMM Slots**

- CN Label:** DIMM1, DIMM2
- CN Type:** 260-pin DDR4 SO-DIMM slot
- CN Location:** See Figure 3-8

The SO-DIMM slots are for installing the DDR4 SO-DIMMs.

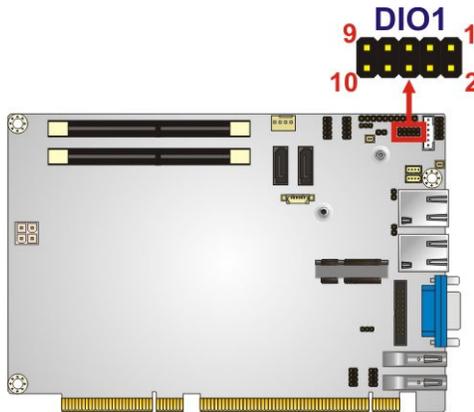


**Figure 3-8: DDR4 SO-DIMM Slot Locations**

### 3.2.8 Digital I/O Connector

- CN Label:** DIO1
- CN Type:** 10-pin header, p=2.00 mm
- CN Location:** See **Figure 3-9**
- CN Pinouts:** See **Table 3-9**

The digital I/O connector provides programmable input and output for external devices.



**Figure 3-9: Digital I/O Connector Location**

Pin	Description	Pin	Description
1	GND	2	VCC
3	Output 3	4	Output 2
5	Output 1	6	Output 0
7	Input 3	8	Input 2
9	Input 1	10	Input 0

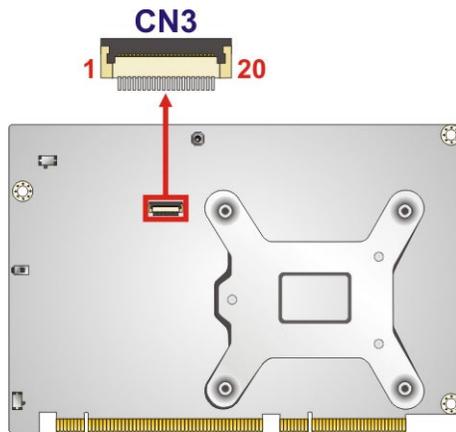
**Table 3-9: Digital I/O Connector Pinouts**

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 3.2.9 EC Debug Connector

- CN Label:** CN1
- CN Type:** 20-pin wafer, p=0.5 mm
- CN Location:** See **Figure 3-10**
- CN Pinouts:** See **Table 3-10**

The EC debug connector is used for EC debug.



**Figure 3-10: EC Debug Connector Location**

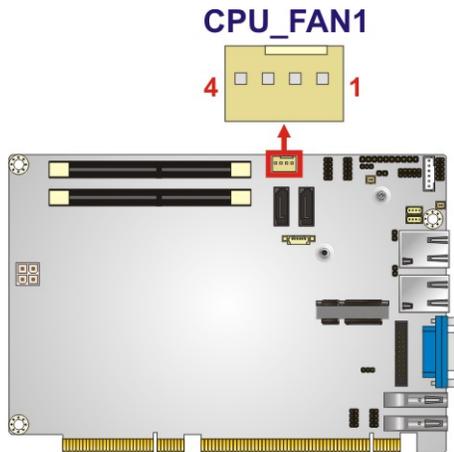
Pin	Description	Pin	Description
1	EC_EPP_STB#	2	EC_EPP_PDO
3	EC_EPP_PD1	4	EC_EPP_PD2
5	EC_EPP_PD3	6	EC_EPP_PD4
7	EC_EPP_PD5	8	EC_EPP_PD6
9	EC_EPP_PD7	10	NC
11	EC_EPP_BUSY	12	EC_EPP_KSI5
13	EC_EPP_KSI4	14	EC_EPP_AFD#
15	NC	16	EC_EPP_INIT#
17	EC_EPP_SLIN#	18	GND
19	GND	20	GND

**Table 3-10: EC Debug Connector Pinouts**

### 3.2.10 Fan Connector (CPU)

- CN Label:** CPU\_FAN1
- CN Type:** 4-pin wafer, p=2.54 mm
- CN Location:** See **Figure 3-11**
- CN Pinouts:** See **Table 3-11**

The fan connector attaches to a CPU cooling fan.



**Figure 3-11: CPU Fan Connector Location**

Pin	Description
1	GND
2	+12V
3	FANIO
4	PWM

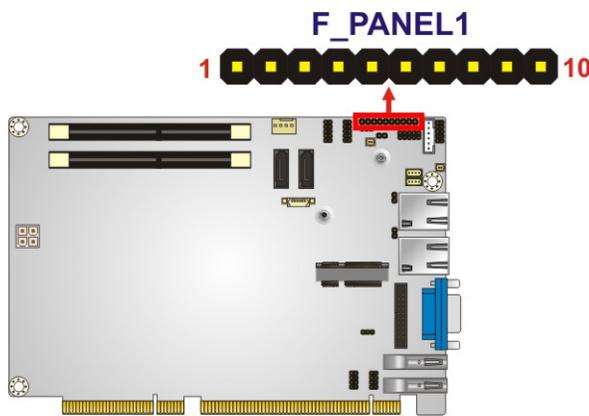
**Table 3-11: CPU Fan Connector Pinouts**

**HPCIE-Q170 Half-size PICMG 1.3 CPU Card**

**3.2.11 Front Panel Connector**

- CN Label:** F\_PANEL1
- CN Type:** 10-pin header, p=2.54 mm
- CN Location:** See **Figure 3-12**
- CN Pinouts:** See **Table 3-12**

The front panel connector connects to the indicator LEDs and buttons on the computer's front panel.



**Figure 3-12: Front Panel Connector Location**

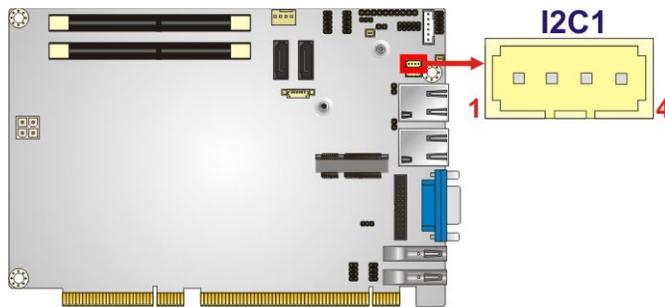
Function	Pin	Description	Function	Pin	Description
Power Button	1	NC	Power LED	6	PWR_LED+
	2	PWRBTN_SW#		7	PWR_LED+
	3	GND		8	GND
HDD LED	4	+V5S	Reset	9	RESET+
	5	HDD_LED-		10	GND

**Table 3-12: Front Panel Connector Pinouts**

### 3.2.12 I<sup>2</sup>C Connector

- CN Label:** I2C1
- CN Type:** 4-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-13**
- CN Pinouts:** See **Table 3-13**

The I<sup>2</sup>C connector is used to connect I<sup>2</sup>C-bus devices to the motherboard.



**Figure 3-13: I<sup>2</sup>C Connector Location**

Pin	Description
1	GND
2	I2C_DAT
3	I2C_CLK
4	+5V

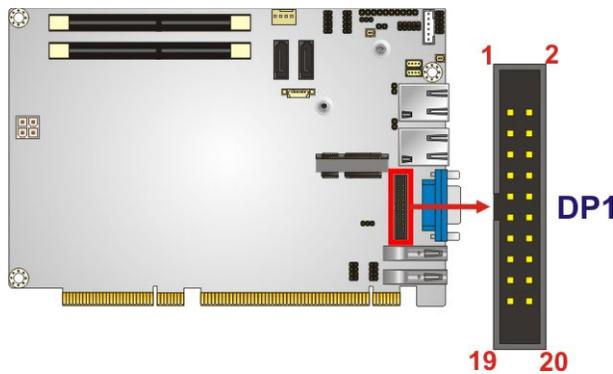
**Table 3-13: I<sup>2</sup>C Connector Pinouts**

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 3.2.13 Internal DisplayPort Connector

- CN Label:** DP1
- CN Type:** 20-pin box header, p=2.00 mm
- CN Location:** See **Figure 3-14**
- CN Pinouts:** See **Table 3-14**

The DisplayPort connector supports HDMI, LVDS, VGA, DVI and DisplayPort graphics interfaces with up to 3840x2160 resolutions.



**Figure 3-14: Internal DisplayPort Connector Location**

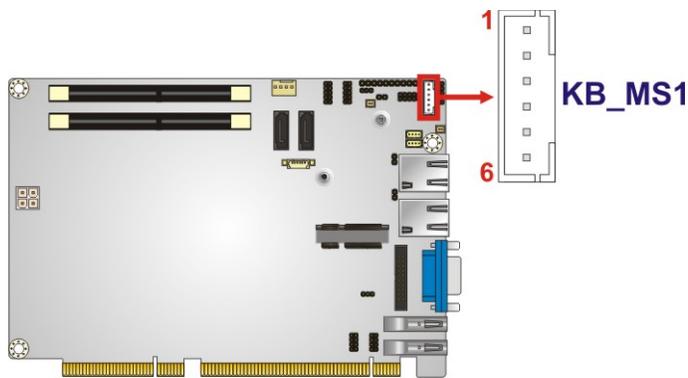
Pin	Description	Pin	Description
1	HPD	11	LANE3N
2	AUXP	12	GND
3	GND	13	GND
4	AUXN	14	LANEOP
5	AUX_CTRL_DET_D	15	LANE1P
6	GND	16	LANEON
7	GND	17	LANE1N
8	LANE2P	18	+3.3V
9	LANE3P	19	+5V
10	LANE2N	20	N/A

**Table 3-14: Internal DisplayPort Connector Pinouts**

**3.2.14 Keyboard and Mouse Connector**

- CN Label:** KB\_MS1
- CN Type:** 6-pin wafer, p=2.00 mm
- CN Location:** See **Figure 3-15**
- CN Pinouts:** See **Table 3-15**

The keyboard and mouse connector connects to a PS/2 Y-cable that can be connected to a PS/2 keyboard and mouse.



**Figure 3-15: Keyboard and Mouse Connector Location**

Pin	Description
1	VCC
2	Mouse Data
3	Mouse Clock
4	Keyboard Data
5	Keyboard Clock
6	GND

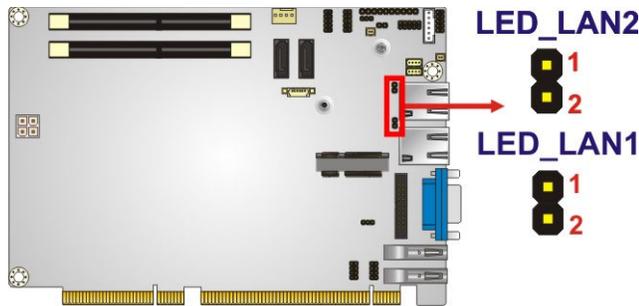
**Table 3-15: Keyboard and Mouse Connector Pinouts**

**HPCIE-Q170 Half-size PICMG 1.3 CPU Card**

**3.2.15 LAN LED Connectors**

- CN Label:** LED\_LAN1, LED\_LAN2
- CN Type:** 2-pin header, p=2.54 mm
- CN Location:** See **Figure 3-16**
- CN Pinouts:** See **Table 3-16** and **Table 3-17**

The LAN LED connectors are used to connect to the LAN LED indicators on the chassis to indicate users the link activities of the two LAN ports.



**Figure 3-16: LAN LED Connector Locations**

Pin	Description
1	+3.3V
2	LAN1_LED_LINK#_ACT

**Table 3-16: LAN1 LED Connector (LED\_LAN1) Pinouts**

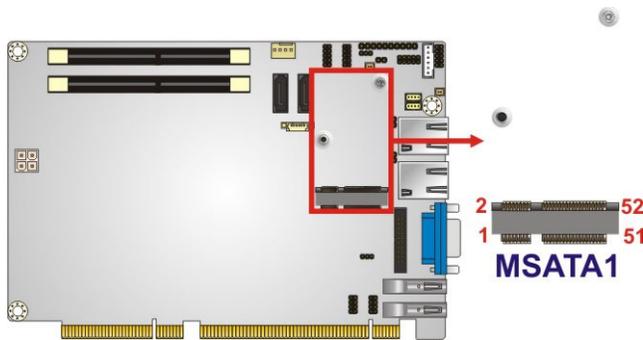
Pin	Description
1	+3.3V
2	LAN2_LED_LINK#_ACT

**Table 3-17: LAN2 LED Connector (LED\_LAN2) Pinouts**

## 3.2.16 PCIe Mini Slot

- CN Label:** MSATA1
- CN Type:** PCIe Mini slot
- CN Location:** See **Figure 3-17**
- CN Pinouts:** See **Table 3-18**

The PCIe Mini slot is for installing a full-size/half-size PCIe Mini expansion card, such as an mSATA SSD or wireless LAN card.



**Figure 3-17: PCIe Mini Slot Location**

Pin	Description	Pin	Description
1	PCIE_WAKE#	2	+3.3V
3	N/C	4	GND
5	N/C	6	1.5V
7	N/C	8	N/C
9	GND	10	N/C
11	MSATA_CLK#	12	N/C
13	MSATA_CLK	14	N/C
15	GND	16	N/C
17	PLTRST_N	18	GND
19	N/C	20	+3.3V
21	GND	22	PLTRST_N
23	SATA_RX+	24	+3.3V
25	SATA_RX-	26	GND
27	GND	28	1.5V

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

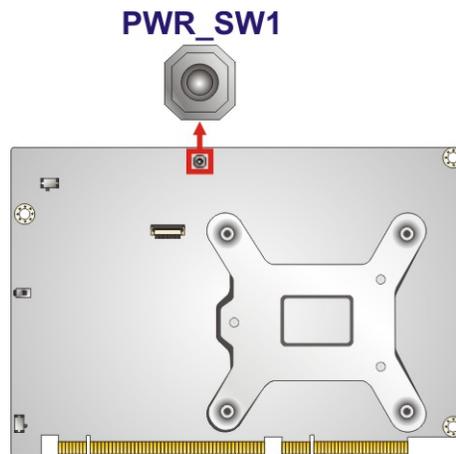
Pin	Description	Pin	Description
29	GND	30	SMB_CLK
31	SATA_TX-	32	SMB_DATA
33	SATA_TX+	34	GND
35	GND	36	USB_DATA-
37	GND	38	USB_DATA+
39	+3.3V	40	GND
41	+3.3V	42	N/C
43	+3.3V	44	N/C
45	CLINK_CLK	46	N/C
47	CLINK_DATA	48	1.5V
49	CLINK_RST#	50	GND
51	MSATA_DET	52	+3.3V

**Table 3-18: PCIe Mini Slot Pinouts**

### 3.2.17 Power Button

- CN Label:** PWR\_SW1
- CN Type:** Push button
- CN Location:** See **Figure 3-18**

The on-board power button controls system power.

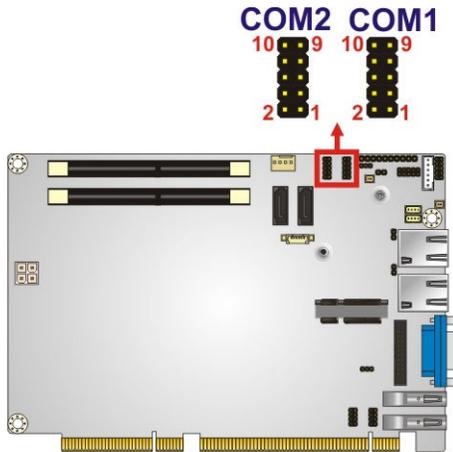


**Figure 3-18: Power Button Location**

**3.2.18 RS-232/422/485 Serial Port Connectors**

- CN Label:** COM1, COM2
- CN Type:** 10-pin header, p=2.00 mm
- CN Location:** See **Figure 3-19**
- CN Pinouts:** See **Table 3-19**

Each of these connectors provides RS-232/422/485 connections.



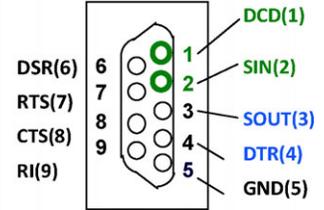
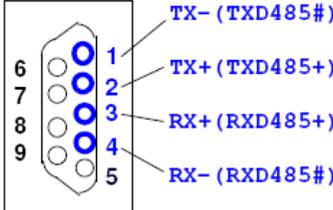
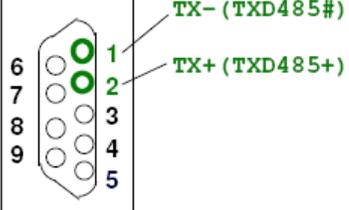
**Figure 3-19: RS-232/422/485 Serial Port Connector Locations**

Pin	Description	Pin	Description
1	DCD	2	DSR
3	SIN	4	RTS
5	SOUT	6	CTS
7	DTR	8	RI
9	GND	10	GND

**Table 3-19: RS-232/422/485 Serial Port Connector Pinouts**

The user may use the RS-232/422/485 cable to connect to a serial device. The pinouts of the DB-9 connector are listed below.

**HPCIE-Q170 Half-size PICMG 1.3 CPU Card**

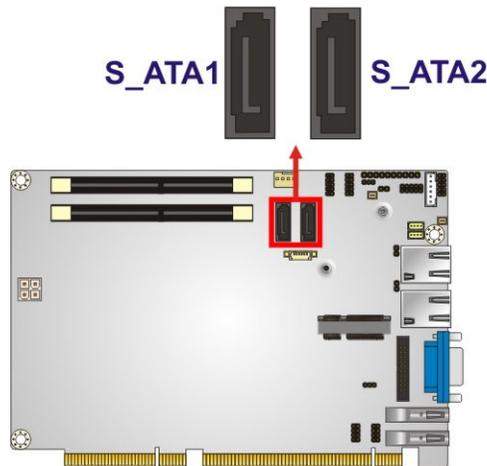
RS-232 Pinouts	RS-422 Pinouts	RS-485 Pinouts
		

**Table 3-20: DB-9 RS-232/422/485 Pinouts**

**3.2.19 SATA 6Gb/s Drive Connector**

- CN Label:** S\_ATA1, S\_ATA2
- CN Type:** 7-pin SATA drive connector
- CN Location:** See **Figure 3-20**
- CN Pinouts:** See **Table 3-21**

The SATA drive connectors can be connected to SATA drives and supports up to 6Gb/s data transfer rate.



**Figure 3-20: SATA 6Gb/s Drive Connector Locations**

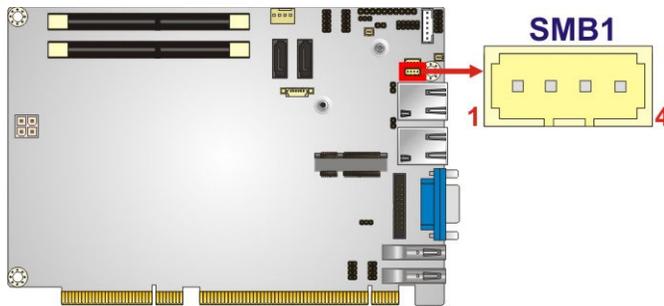
Pin	Description	Pin	Description
1	GND	2	TX+
3	TX-	4	GND
5	RX-	6	RX+
7	GND		

**Table 3-21: SATA 6Gb/s Drive Connector Pinouts**

**3.2.20 SMBus Connector**

- CN Label:** SMB1
- CN Type:** 4-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-21**
- CN Pinouts:** See **Table 3-22**

The SMBus (System Management Bus) connector provides low-speed system management communications.



**Figure 3-21: SMBus Connector Location**

Pin	Description
1	GND
2	SMB_DATA
3	SMB_CLK
4	+5V

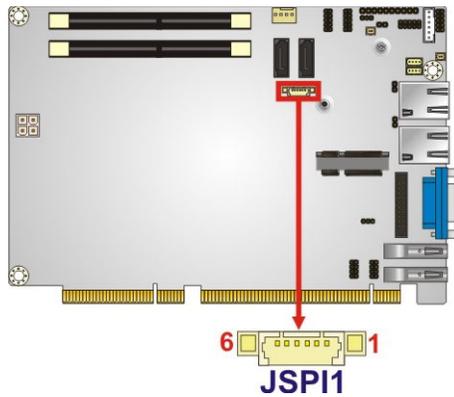
**Table 3-22: SMBus Connector Pinouts**

**HPCIE-Q170 Half-size PICMG 1.3 CPU Card**

**3.2.21 SPI Flash Connector**

- CN Label:** JSPI1
- CN Type:** 6-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-22**
- CN Pinouts:** See **Table 3-23**

The SPI flash connector is used to flash the SPI ROM.



**Figure 3-22: SPI Flash Connector Location**

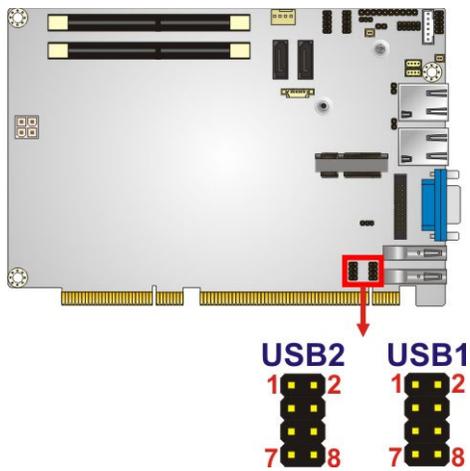
Pin	Description	Pin	Description
1	+V3.3M_SPI_CON	2	SPI_CS
3	SPI_SO_SW	4	SPI_CLK_SW
5	SPI_SI_SW	6	GND

**Table 3-23: SPI Flash Connector Pinouts**

**3.2.22 USB 2.0 Connectors**

- CN Label:** USB1, USB2
- CN Type:** 8-pin header, p=2.00 mm
- CN Location:** See **Figure 3-23**
- CN Pinouts:** See **Table 3-24**

The USB 2.0 connectors connect to USB 2.0 devices. Each pin header provides two USB 2.0 ports.



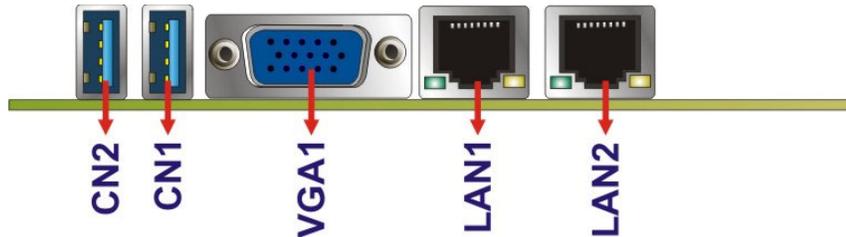
**Figure 3-23: USB 2.0 Connector Locations**

Pin	Description	Pin	Description
1	VCC	2	GND
3	USB_DATA-	4	USB_DATA+
5	USB_DATA+	6	USB_DATA-
7	GND	8	VCC

**Table 3-24: USB 2.0 Connector Pinouts**

### 3.3 External Peripheral Interface Connector Panel

The figure below shows the external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:



**Figure 3-24: External Peripheral Interface Connector**

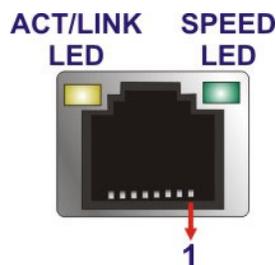
#### 3.3.1 Ethernet Connectors

- CN Label:** LAN1, LAN2
- CN Type:** RJ-45
- CN Location:** See **Figure 3-24**
- CN Pinouts:** See **Table 3-25**

Each LAN connector connects to a local network

Pin	Description	Pin	Description
1	LAN_MDI0P	5	LAN_MDI2P
2	LAN_MDI0N	6	LAN_MDI2N
3	LAN_MDI1P	7	LAN_MDI3P
4	LAN_MDI1N	8	LAN_MDI3N

**Table 3-25: LAN Pinouts**



**Figure 3-25: Ethernet Connector**

### 3.3.2 USB 3.0 Connectors

- CN Label:** CN1, CN2
- CN Type:** USB 3.0
- CN Location:** See **Figure 3-24**
- CN Pinouts:** See **Table 3-26**

There is one external USB 3.0 connector on the HPCIE-Q170.

Pin	Description	Pin	Description
1	VBUS	2	D-
3	D+	4	GND
5	STDA_SSRX_N	6	STDA_SSRX_P
7	GND_DRAIN	8	STDA_SSTX_N
9	STDA_SSTX_P		

**Table 3-26: USB 3.0 Port Pinouts**

### 3.3.3 VGA Connector

- CN Label:** VGA1
- CN Type:** 15-pin VGA
- CN Location:** See **Figure 3-24**
- CN Pinouts:** See **Table 3-27**

The 15-pin VGA connector connects to a monitor that accepts a standard VGA input.



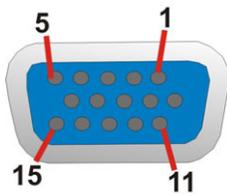
**NOTE:**

The user has to connect the VGA connector to the monitor before system booting as the VGA output function is supported via the eDP to VGA converter.

**HPCIE-Q170 Half-size PICMG 1.3 CPU Card**

Pin	Description	Pin	Description
1	RED	2	GREEN
3	BLUE	4	NC
5	GND	6	HOT PLUG DETECT
7	GND	8	GND
9	VCC	10	GND
11	NC	12	DCCDA
13	HSYNC	14	VSYNC
15	DDCCLK		

**Table 3-27: VGA Connector Pinouts**



**Figure 3-26: VGA Connector**

Chapter

4

# Installation

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## 4.1 Anti-static Precautions

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### WARNING:

Failure to take ESD precautions during the installation of the HPCIE-Q170 may result in permanent damage to the HPCIE-Q170 and severe injury to the user.

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Electrostatic discharge (ESD) can cause serious damage to electronic components, including the HPCIE-Q170. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the HPCIE-Q170 or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- **Wear an anti-static wristband:** - Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- **Self-grounding:** - Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- **Use an anti-static pad:** When configuring the HPCIE-Q170, place it on an anti-static pad. This reduces the possibility of ESD damaging the HPCIE-Q170.
- **Only handle the edges of the PCB:-:** When handling the PCB, hold the PCB by the edges.

## 4.2 Installation Considerations

---



### NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

---

**WARNING:**

The installation instructions described in this manual should be carefully followed in order to prevent damage to the components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  - The user manual provides a complete description of the HPCIE-Q170 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the HPCIE-Q170 on an anti-static pad:
  - When installing or configuring the motherboard, place it on an anti-static pad. This helps to prevent potential ESD damage.
- Turn all power to the HPCIE-Q170 off:
  - When working with the HPCIE-Q170, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the HPCIE-Q170, **DO NOT**:

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

### 4.3 Socket LGA1151 CPU Installation

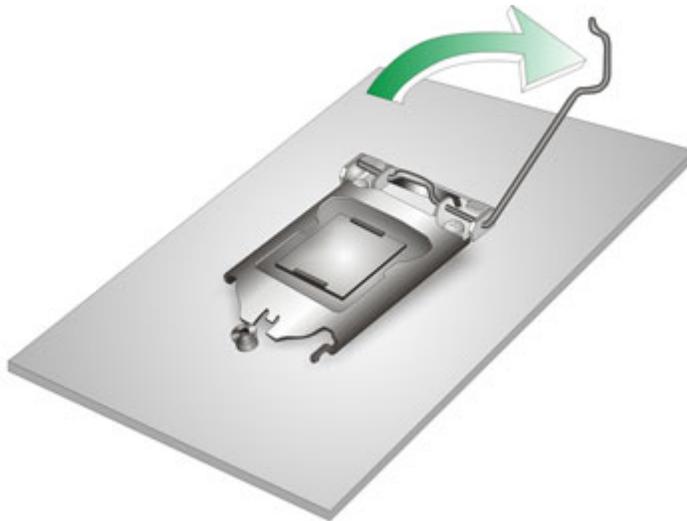
**WARNING:**

CPUs are expensive and sensitive components. When installing the CPU please be careful not to damage it in anyway. Make sure the CPU is installed properly and ensure the correct cooling kit is properly installed.

DO NOT touch the pins at the bottom of the CPU. When handling the CPU, only hold it on the sides.

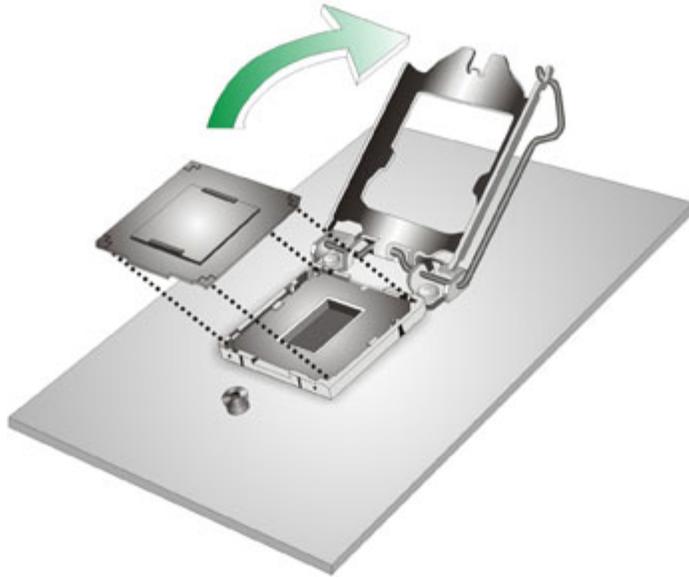
To install the CPU, follow the steps below.

**Step 1:** **Disengage the load lever** by pressing the lever down and slightly outward to clear the retention tab. Fully open the lever. See **Figure 4-1**.



**Figure 4-1: Disengage the CPU Socket Load Lever**

**Step 2:** **Open the socket and remove the protective cover.** The black protective cover can be removed by pulling up on the tab labeled "Remove". See **Figure 4-2**.



**Figure 4-2: Remove Protective Cover**

- Step 3: Inspect the CPU socket.** Make sure there are no bent pins and make sure the socket contacts are free of foreign material. If any debris is found, remove it with compressed air.
- Step 4: Orientate the CPU properly.** The contact array should be facing the CPU socket.



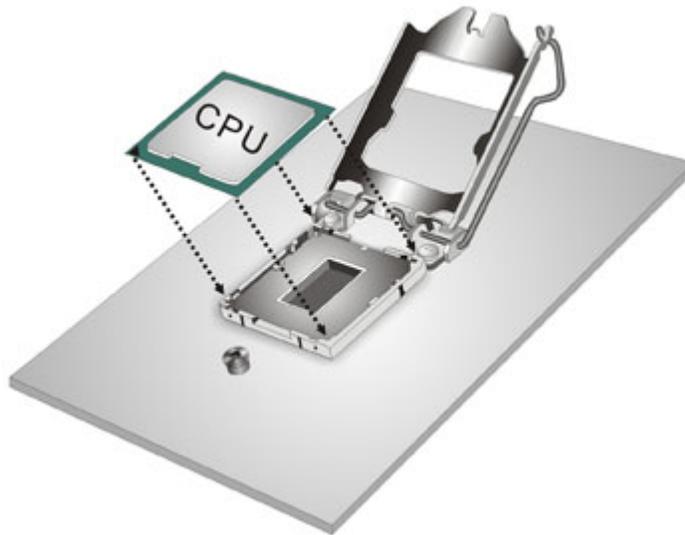
**WARNING:**

DO NOT touch the pins at the bottom of the CPU. When handling the CPU, only hold it on the sides.

- 
- Step 5: Correctly position the CPU.** Match the Pin 1 mark with the cut edge on the CPU socket.
- Step 6: Align the CPU pins.** Locate pin 1 and the two orientation notches on the CPU. Carefully match the two orientation notches on the CPU with the socket alignment keys.

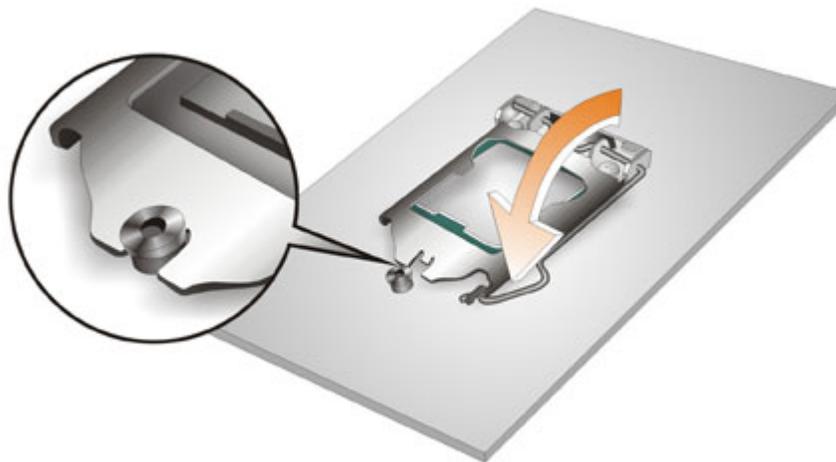
## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

**Step 7: Insert the CPU.** Gently insert the CPU into the socket. If the CPU pins are properly aligned, the CPU should slide into the CPU socket smoothly. See **Figure 4-3**.



**Figure 4-3: Insert the Socket LGA1151 CPU**

**Step 8: Close the CPU socket.** Close the load plate and pull the load lever back a little to have the load plate be able to secure to the knob. Engage the load lever by pushing it back to its original position (**Figure 4-4**). There will be some resistance, but will not require extreme pressure.



**Figure 4-4: Close the Socket LGA1151**

**Step 9:** Connect the 12 V power to the board. Connect the 12 V power from the power supply to the board.

## 4.4 Socket LGA1151 Cooling Kit Installation

---



### **WARNING:**

**DO NOT** attempt to install a push-pin cooling fan.

The pre-installed support bracket prevents the board from bending and is **ONLY** compatible with captive screw type cooling fans.

---

The cooling kit can be bought from IEI. The cooling kit has a heat sink and fan.

---



### **WARNING:**

Do not wipe off (accidentally or otherwise) the pre-sprayed layer of thermal paste on the bottom of the heat sink. The thermal paste between the CPU and the heat sink is important for optimum heat dissipation.

---

To install the cooling kit, follow the instructions below.

**Step 1:** A cooling kit bracket is pre-installed on the rear of the motherboard. See **Figure 4-5**.

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

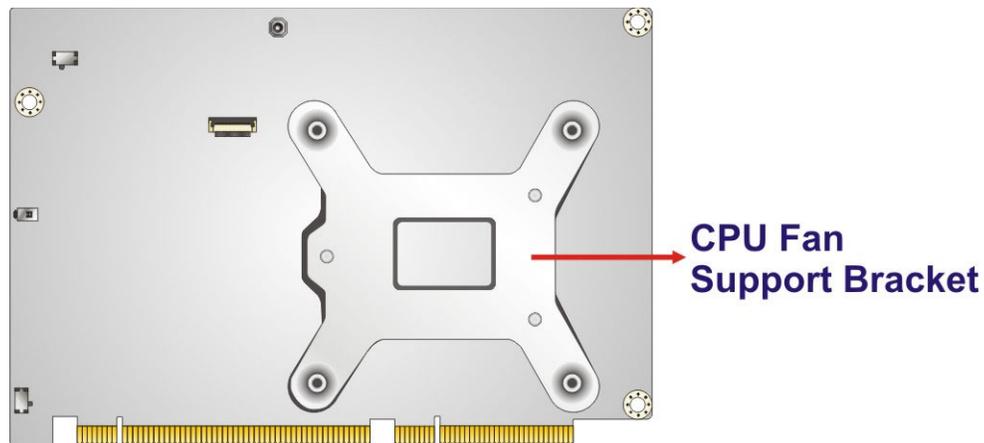
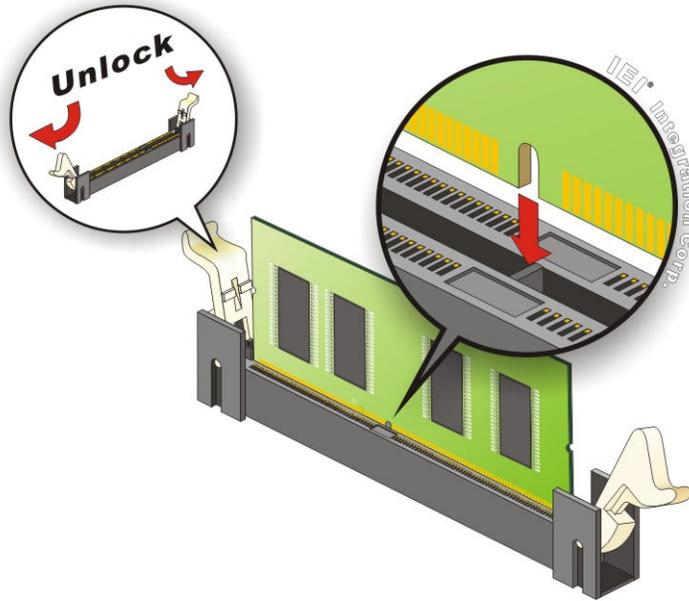


Figure 4-5: Cooling Kit Support Bracket

- Step 2:** Place the cooling kit onto the socket LGA1151 CPU. Make sure the CPU cable can be properly routed when the cooling kit is installed.
- Step 3:** Mount the cooling kit. Gently place the cooling kit on top of the CPU. Make sure the four threaded screws on the corners of the cooling kit properly pass through the holes of the cooling kit bracket.
- Step 4:** Tighten the screws. Use a screwdriver to tighten the four screws. In a diagonal pattern, tighten each screw a few turns then move to the next one, until they are all secured. Do not overtighten the screws.
- Step 5:** Connect the fan cable. Connect the cooling kit fan cable to the CPU fan connector on the HPCIE-Q170. Carefully route the cable and avoid heat generating chips and fan blades.

## 4.5 SO-DIMM Installation

To install a SO-DIMM, please follow the steps below and refer to **Figure 4-6**.



**Figure 4-6: SO-DIMM Installation**

- Step 1:** **Open the SO-DIMM socket handles.** Open the two handles outwards as far as they can. See **Figure 4-6**.
- Step 2:** **Align the SO-DIMM with the socket.** Align the SO-DIMM so the notch on the memory lines up with the notch on the memory socket. See **Figure 4-6**.
- Step 3:** **Insert the SO-DIMM.** Once aligned, press down until the SO-DIMM is properly seated. Clip the two handles into place. See **Figure 4-6**.
- Step 4:** To remove a SO-DIMM, push both handles outward. The memory module is ejected by a mechanism in the socket.

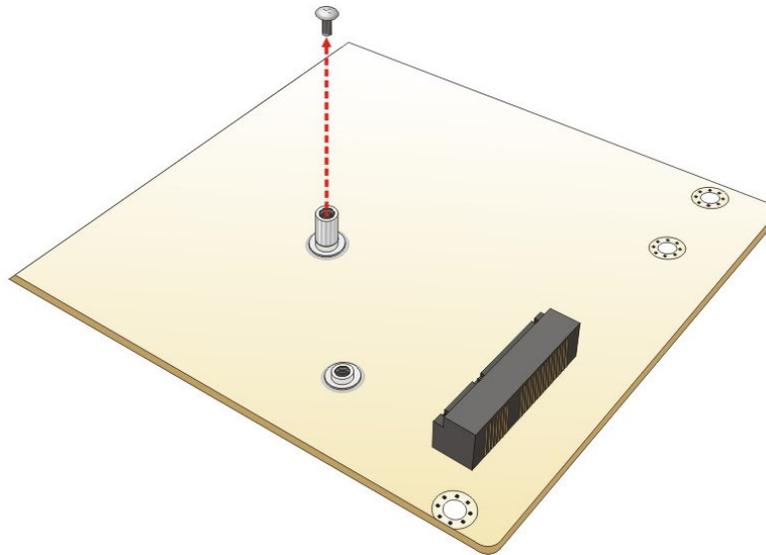
## 4.6 Full-size PCIe Mini Card Installation

The PCIe Mini card slot allows installation of either a full-size or half-size PCIe Mini card. To install a full-size PCIe Mini card, please follow the steps below.

- Step 1:** **Locate the PCIe Mini card slot.** See **Chapter 3**.

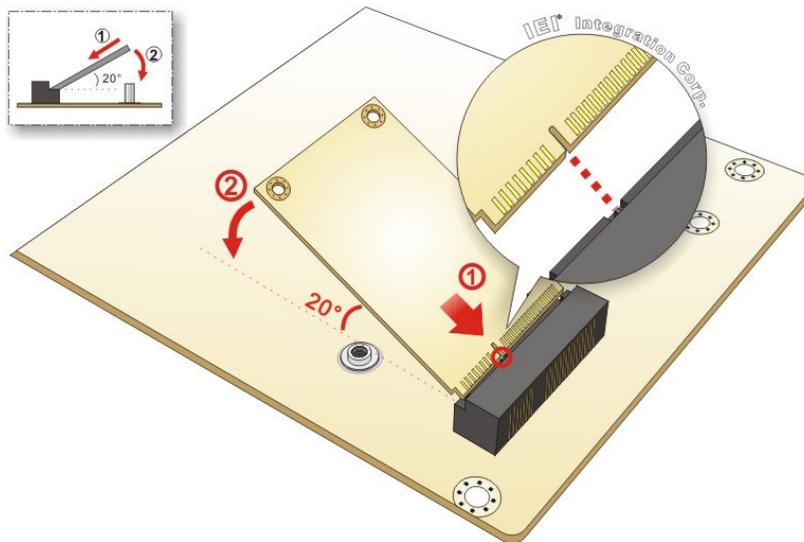
**HPCIE-Q170 Half-size PICMG 1.3 CPU Card**

**Step 2:** Remove the retention screw. Remove the retention screw as shown in Figure 4-7.



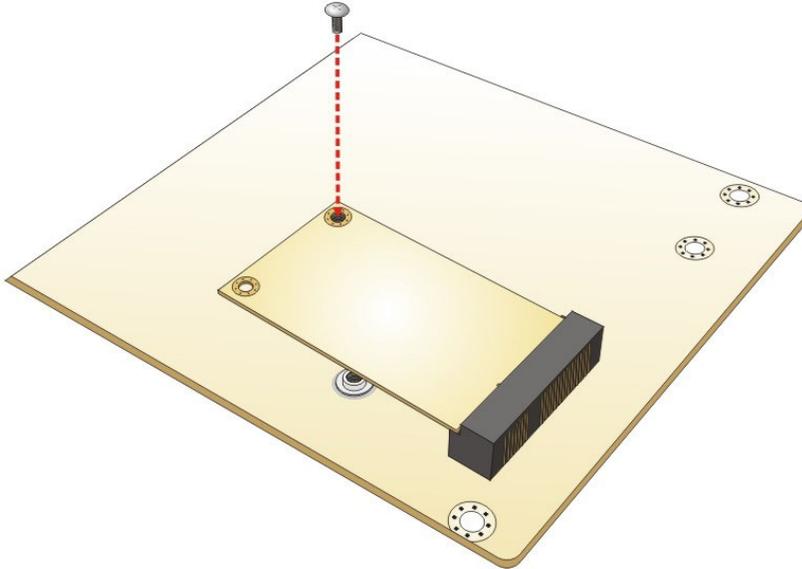
**Figure 4-7: Removing the Retention Screw**

**Step 3:** Insert into the socket at an angle. Line up the notch on the card with the notch on the slot. Slide the PCIe Mini card into the socket at an angle of about 20° (Figure 4-8).



**Figure 4-8: Inserting the Full-size PCIe Mini Card into the Slot at an Angle**

**Step 4:** **Secure the full-size PCIe Mini card.** Secure the full-size PCIe Mini card with the retention screw previously removed (**Figure 4-9**).



**Figure 4-9: Securing the Full-size PCIe Mini Card**

## 4.7 Half-size PCIe Mini Card Installation

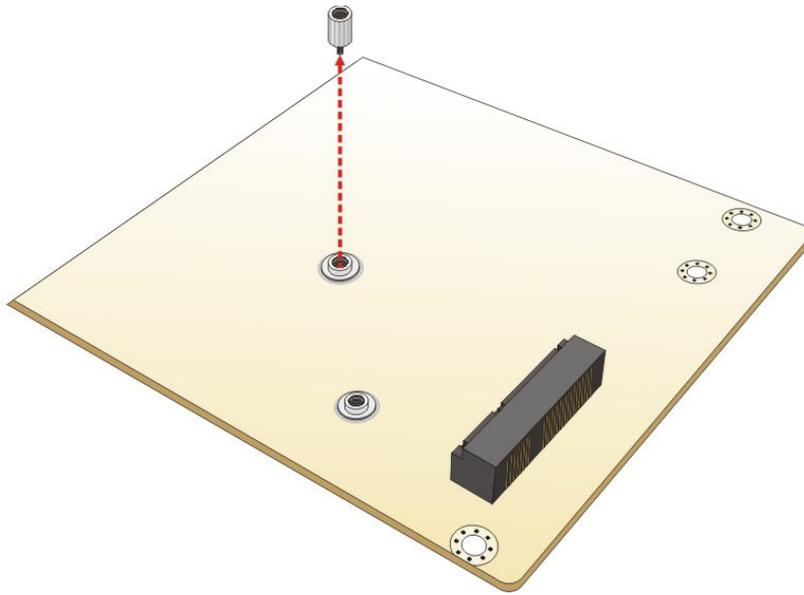
The PCIe Mini card slot allows installation of either a full-size or half-size PCIe Mini card. To install a half-size PCIe Mini card, please follow the steps below.

**Step 1:** **Locate the PCIe Mini card slot.** See **Chapter 3**.

**Step 2:** **Remove the retention screw.** Remove the retention screw as shown in **Figure 4-7**.

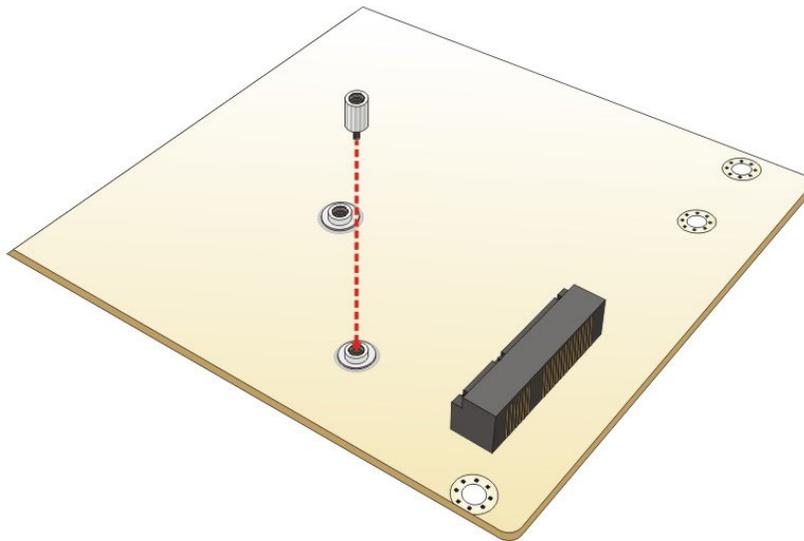
**Step 3:** **Remove the standoff.** Unscrew and remove the standoff secured on the motherboard as shown in **Figure 4-10**.

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card



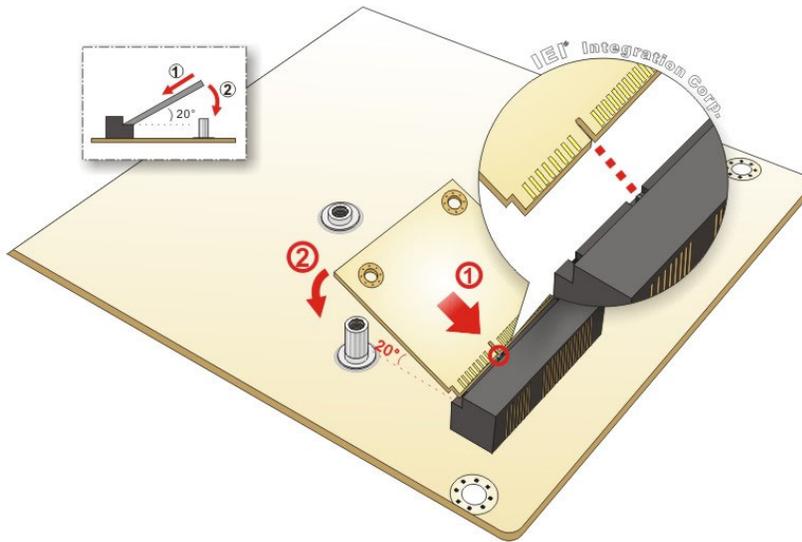
**Figure 4-10: Removing the Standoff**

**Step 4:** Install the standoff to the screw hole for the half-size PCIe Mini card. Install the previously removed standoff to the screw hole for the half-size PCIe Mini card (**Figure 4-11**).



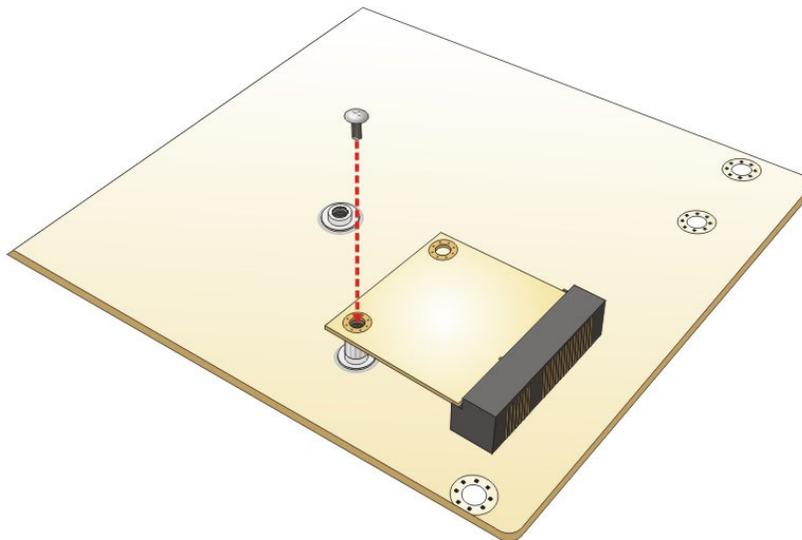
**Figure 4-11: Installing the Standoff**

**Step 5:** Insert into the socket at an angle. Line up the notch on the card with the notch on the slot. Slide the PCIe Mini card into the slot at an angle of about 20° (Figure 4-12).



**Figure 4-12: Inserting the Half-size PCIe Mini Card into the Slot at an Angle**

**Step 6:** Secure the half-size PCIe Mini card. Secure the half-size PCIe Mini card with the retention screw previously removed (Figure 4-13).



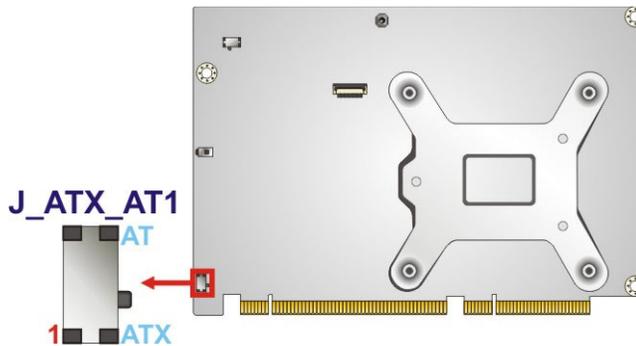
**Figure 4-13: Securing the Half-size PCIe Mini Card**

## 4.8 System Configuration

The system configuration should be performed before installation.

### 4.8.1 AT/ATX Power Mode Setting

The AT and ATX power mode selection is made through the AT/ATX power mode switch which is shown in **Figure 4-14**.



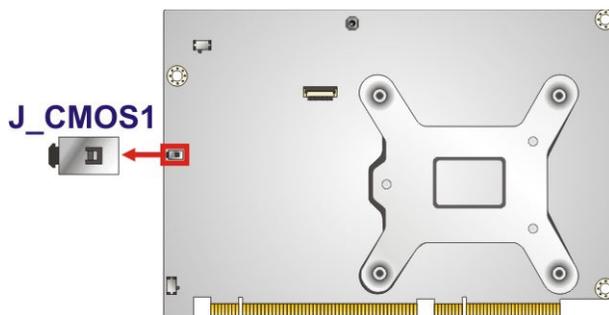
**Figure 4-14: AT/ATX Power Mode Switch Location**

Setting	Description
1-2 (down)	ATX power mode (default)
2-3 (up)	AT power mode

**Table 4-1: AT/ATX Power Mode Switch Settings**

### 4.8.2 Clear CMOS Button

To reset the BIOS, remove the on-board battery and press the clear CMOS button for three seconds or more. The clear CMOS button location is shown in **Figure 4-15**.



**Figure 4-15: Clear CMOS Button Location**

### 4.8.3 PCIe x4 Channel Mode Setup

The user can select to use either one PCIe x4 slot or four PCIe x1 slots on the backplane via the BIOS switch. Refer to below table for the BIOS switch settings.

Setting	Description
1-2 (BIOS1)	Sets the PCIe x4 link width as four PCIe x1 slots (default)
2-3 (BIOS2)	Sets the PCIe x4 link width as one PCIe x4 slot

**Table 4-2: BIOS Switch Settings**

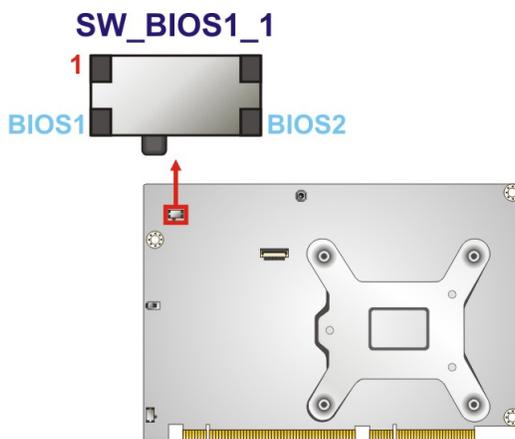
To switch BIOS1 to BIOS2 or BIOS2 to BIOS1 successfully, please follow the steps below.

- Step 1:** Unplug the system power cord.
- Step 2:** Switch BIOS1 to BIOS2 or BIOS2 to BIOS1 by moving the BIOS switch to BIOS1 or BIOS2 position as shown in **Figure 4-16**.
- Step 3:** Remove the on-board battery, and then reinstall it.
- Step 4:** Clear CMOS by pressing the clear CMOS button for three seconds or more.
- Step 5:** Perform the system booting.



**NOTE:**

The user can check which BIOS is being used from the **BIOS Number** item in the **Main BIOS menu (BIOS Menu 1)**.



**Figure 4-16: BIOS Switch Location**

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 4.8.4 PCIe x16 Channel Mode Setup

The HPCIE-Q170 supports one PCIe x16 interface on the backplane. The PCIe x16 channel mode setup is made through the BIOS menu in “Chipset → System Agent (SA) Configuration → PEG Port Configuration”. Use the **PEG Link Width Configuration** BIOS option to configure the PCIe x16 channel mode.

Options	Description
1x16	Sets the PCIe x16 link width as one PCIe x16 slot (default)
2x8	Sets the PCIe x16 link width as two PCIe x8 slots
1x8, 2x4	Sets the PCIe x16 link width as one PCIe x8 and two PCIe x4

**Table 4-3: PCIe x16 Channel Mode Setup**

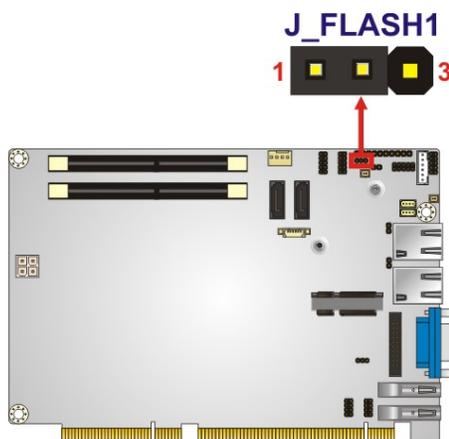
Please refer to **Section 5.4.1.2** for detailed information.

### 4.8.5 Flash Descriptor Security Override Jumper

The flash descriptor security override jumper (J\_FLASH1) allows to enable or disable the ME firmware update. Refer to **Table 4-4** and **Figure 4-17** for the jumper location and settings.

Setting	Description
Short 1-2	Disabled (default)
Short 2-3	Enabled

**Table 4-4: Flash Descriptor Security Override Jumper Settings**



**Figure 4-17: Flash Descriptor Security Override Jumper Location**

To update the ME firmware, please follow the steps below.

- Step 1:** Before turning on the system power, short pin 2-3 of the flash descriptor security override jumper.
- Step 2:** Update the BIOS and ME firmware, and then turn off the system power.
- Step 3:** Remove the metal clip on the flash descriptor security override jumper or return to its default setting (short pin 1-2).
- Step 4:** Restart the system. The system will reboot 2 ~ 3 times to complete the ME firmware update.

### 4.8.6 USB Power Selection

The USB power selection is made through the BIOS menu in “Chipset → PCH-IO Configuration”. Use the **USB Power SW1** and the **USB Power SW2** BIOS options to configure the correspondent USB ports (see **Table 4-5**) and refer to **Table 4-6** to select the USB power source.

BIOS Options	Configured USB Ports
USB Power SW1	CN1 (external USB 3.0 port) CN2 (external USB 3.0 port)
USB Power SW2	USB1 (internal USB 2.0 ports) USB2 (internal USB 2.0 ports)

**Table 4-5: BIOS Options and Configured USB Ports**

Options	Description
+5V DUAL	+5V dual (default)
+5V	+5V

**Table 4-6: USB Power Source Setup**

Please refer to **Section 5.4.2** for BIOS setup.

## 4.9 Internal Peripheral Device Connections

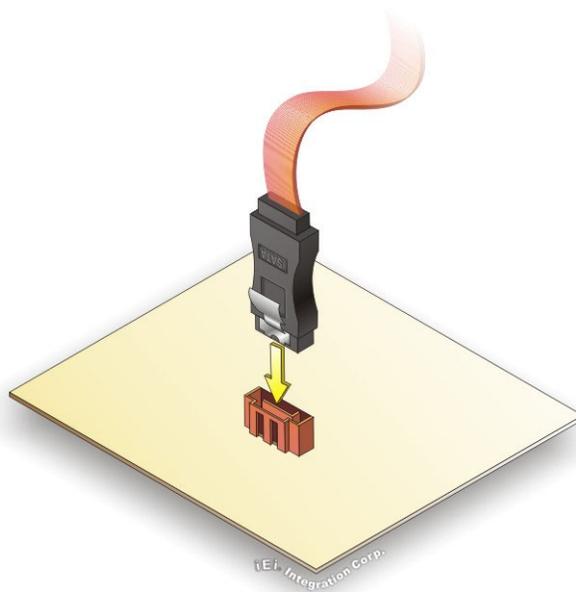
This section outlines the installation of peripheral devices to the onboard connectors.

### 4.9.1 SATA Drive Connection

The HPCIE-Q170 is shipped with two SATA drive cables. To connect the SATA drives to the connectors, please follow the steps below.

**Step 1: Locate the connectors.** The locations of the SATA drive connectors are shown in **Chapter 3**.

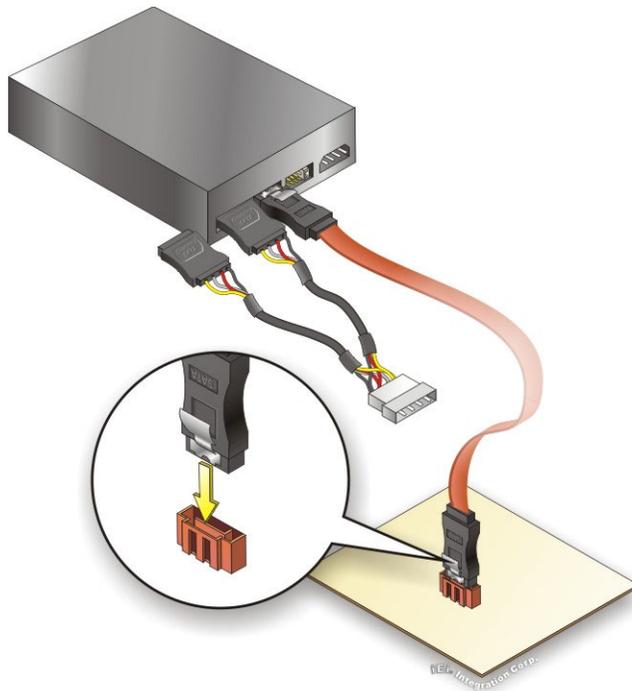
**Step 2: Insert the cable connector.** Insert the cable connector into the on-board SATA drive connector until it clips into place. See **Figure 4-18**.



**Figure 4-18: SATA Drive Cable Connection**

**Step 3: Connect the cable to the SATA disk.** Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 4-19**.

**Step 4: Connect the SATA power cable.** Connect the SATA power connector to the back of the SATA drive. See **Figure 4-19**.



**Figure 4-19: SATA Power Drive Connection**

The SATA power cable can be bought from IEI. See Optional Items in Section 2.4.

#### 4.10 Adding USB 3.0 Drivers to a Windows 7 Installation Image

The Windows 7 installation media does not include native driver support for USB 3.0. In order to use the USB keyboard or mouse connected to a USB 3.0 port during OS installation, the user has to update the Windows 7 installation image so that it contains USB 3.0 drivers. Please follow the instructions below to complete the task.

**Step 1:** Prepare a USB flash drive installer.

On a working computer, use your Windows 7 DVD or ISO image to create a bootable USB flash drive.

**Step 2:** Download the Windows 7 USB 3.0 Creator Utility from:

<https://downloadcenter.intel.com/download/25476/Windows-7-USB-3-0-Creator-Utility>.

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**Step 3:** Extract the downloaded file to a temporary folder on a computer where the user has logged in as the administrator.

**NOTE:**

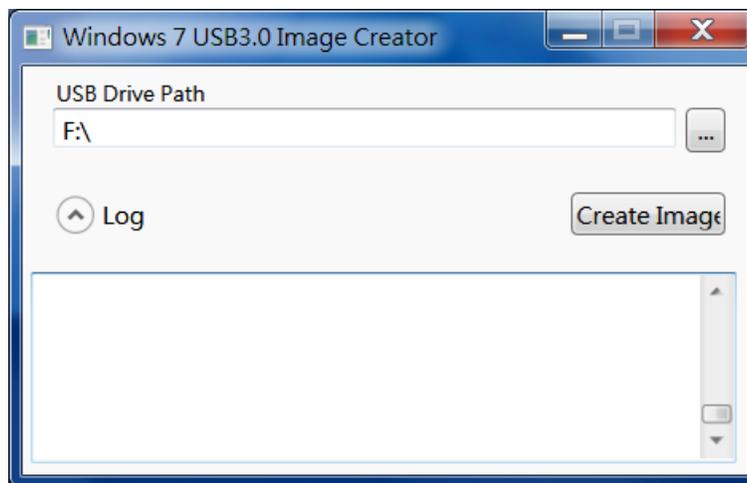
The OS version of the computer can be Windows 7, Windows 8.1 or Windows 10.

---

**Step 4:** Connect the USB drive containing the Windows 7 installation image to the computer.

**Step 5:** Right click on **Installer\_Creator.exe** from the extracted files and select **Run as administrator**.

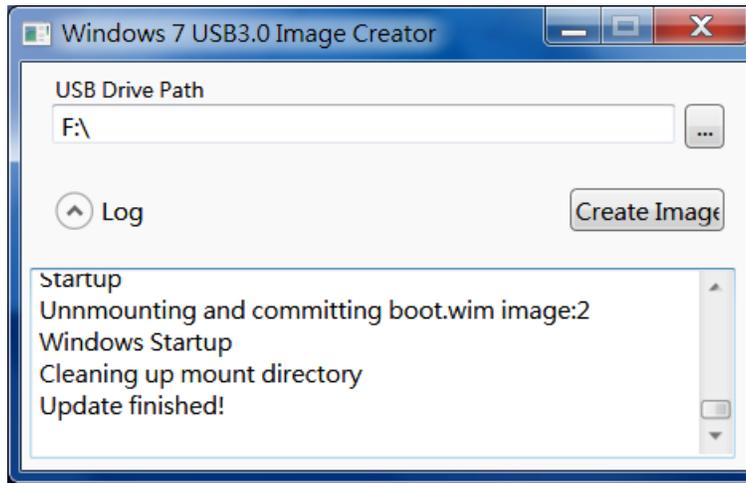
**Step 6:** The Windows 7 USB 3.0 Creator Utility screen appears (**Figure 4-20**). Click  to browse to the root of the USB drive containing the Windows 7 image.



**Figure 4-20: Windows 7 USB 3.0 Creator Utility**

**Step 7:** Click **Create Image** to start the update process.

**Step 8:** Wait for the process to finish. It may take up to 15 minutes.



**Figure 4-21: Update Process is Complete**

**Step 9:** Now the user can proceed with the Windows 7 installation using the updated installer.

## 4.11 Intel® AMT Setup Procedure

The HPCIE-Q170 is featured with the Intel® Active Management Technology (AMT). To enable the Intel® AMT function, follow the steps below.

- Step 1:** Make sure at least one of the memory sockets is installed with a DDR4 SO-DIMM.
- Step 2:** Connect an Ethernet cable to the RJ-45 connector labeled **LAN1**.
- Step 3:** The AMI BIOS options regarding the Intel® ME or Intel® AMT must be enabled,
- Step 4:** Properly install the Intel® Management Engine Components drivers from the iAMT Driver & Utility directory in the driver CD.
- Step 5:** Configure the Intel® Management Engine BIOS extension (MEBx). To get into the Intel® MEBx settings, press <Ctrl+P> after a single beep during boot-up process. Enter the Intel® current ME password as it requires (the Intel® default password is **admin**).

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

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### NOTE:

To change the password, enter a new password following the strong password rule (containing at least one upper case letter, one lower case letter, one digit and one special character, and be at least eight characters).

---

Chapter

**5**

**BIOS**

---

## 5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.



### NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

### 5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. Press the **DEL** or **F2** key as soon as the system is turned on or
2. Press the **DEL** or **F2** key when the “**Press DEL or F2 to enter SETUP**” message appears on the screen.

If the message disappears before the **DEL** or **F2** key is pressed, restart the computer and try again.

### 5.1.2 Using Setup

Use the arrow keys to highlight items, press **ENTER** to select, use the PageUp and PageDown keys to change entries, press **F1** for help and press **ESC** to quit. Navigation keys are shown in the following table.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes
-	Decrease the numeric value or make changes
Page Up	Move to the previous page
Page Dn	Move to the next page

Key	Function
Esc	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2	Load previous values
F3	Load optimized defaults
F4	Save changes and Exit BIOS

**Table 5-1: BIOS Navigation Keys**

### 5.1.3 Getting Help

When **F1** is pressed, a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window, press **Esc**.

### 5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the clear CMOS button described in **Chapter 4**.

### 5.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Security – Sets User and Supervisor Passwords.
- Boot – Changes the system boot configuration.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

## 5.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered.

The **Main** menu gives an overview of the basic system information.

## HPCI-E-Q170 Half-size PICMG 1.3 CPU Card

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.

Main    Advanced    Chipset    Security    Boot    Save & Exit

BIOS Information		Set the Date. Use Tab to switch between Date elements.
BIOS Vendor	American Megatrends	
Core Version	5.11	
Compliance	UEFI 2.4; PI 1.3	
Project Version	B375AR10.ROM	
Build Date and Time	05/03/2016 16:20:22	
BIOS Number	BIOS No.1	
iWDD Vendor	iEi	
iWDD Version	B375ET05.bin	
IPMI Module	N/A	
Processor Information		
Name	SkyLake DT	
Brand String	Intel(R) Core(TM) i5-6500 CPU @ 3.20GHz	----- →←: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Frequency	3200 MHz	
Processor ID	506E3	
Stepping	R0/S0/N0	
Number of Processors	4Core(s) / 4Thread(s)	
Microcode Revision	7C	
GT Info	GT2	
Memory RC Version	1.8.0.1	
Total Memory	4096 MB	
Memory Frequency	2133 MHz	
PCH Information		
Name	SKL PCH-H	
PCH SKU	PCH-H Desktop Q170 SKU	
Stepping	31/D1	
LAN PHY Revision	B2	
ME FW Version	11.0.0.1205	
ME Firmware SKU	Corporate SKU	
SPI Clock Frequency		
DOFR Support	Unsupported	
Read Status Clock Frequency	17 MHz	
Write Status Clock Frequency	48 MHz	
Fast Read Status Clock Frequency	48 MHz	
Access Level	Administrator	
System Date	[Thu 05/19/2016]	
System Time	[15:10:27]	

Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.

BIOS Menu 1: Main

The **Main** menu has two user configurable fields:

→ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

→ **System Time [xx:xx:xx]**

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

### 5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 2**) to configure the CPU and peripheral devices through the following sub-menus:



#### WARNING!

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
Main  Advanced  Chipset  Security  Boot  Save & Exit
-----
> ACPI Settings
> AMT Configuration
> Super IO Configuration
> iWDD H/M Monitor
> RTC Wake Settings
> Serial Port Console Redirection
> CPU Configuration
> SATA Configuration
> NVMe Configuration
> USB Configuration
> iEi Feature

Configure Active Management Technology Parameters
-----
→←: Select Screen
↑ ↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

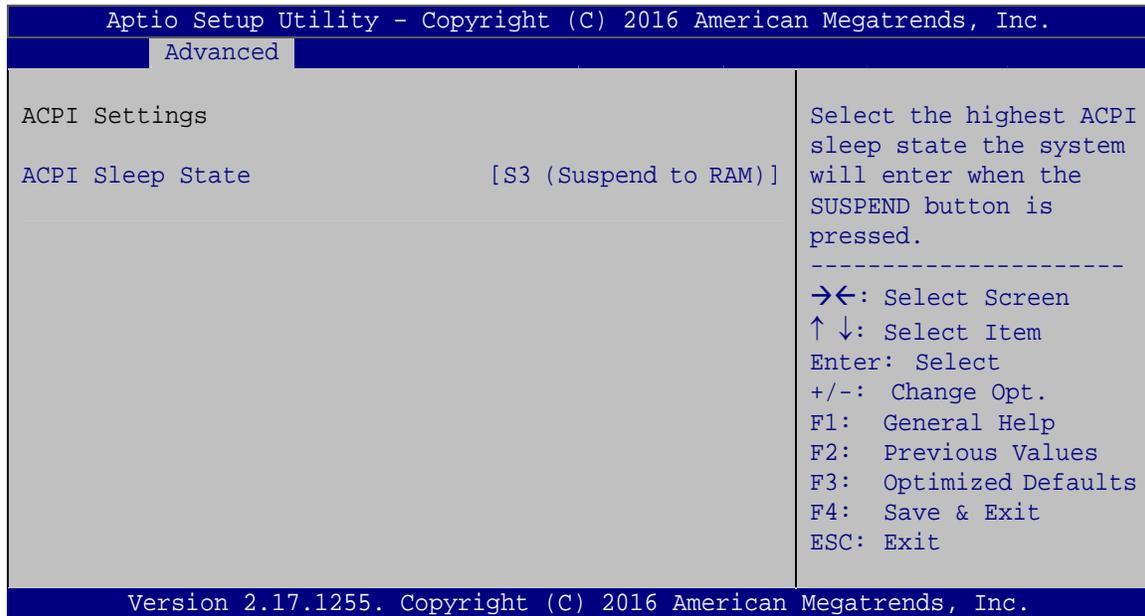
Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
    
```

**BIOS Menu 2: Advanced**

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 5.3.1 ACPI Settings

The **ACPI Settings** menu (**BIOS Menu 3**) configures the Advanced Configuration and Power Interface (ACPI) options.



#### BIOS Menu 3: ACPI Configuration

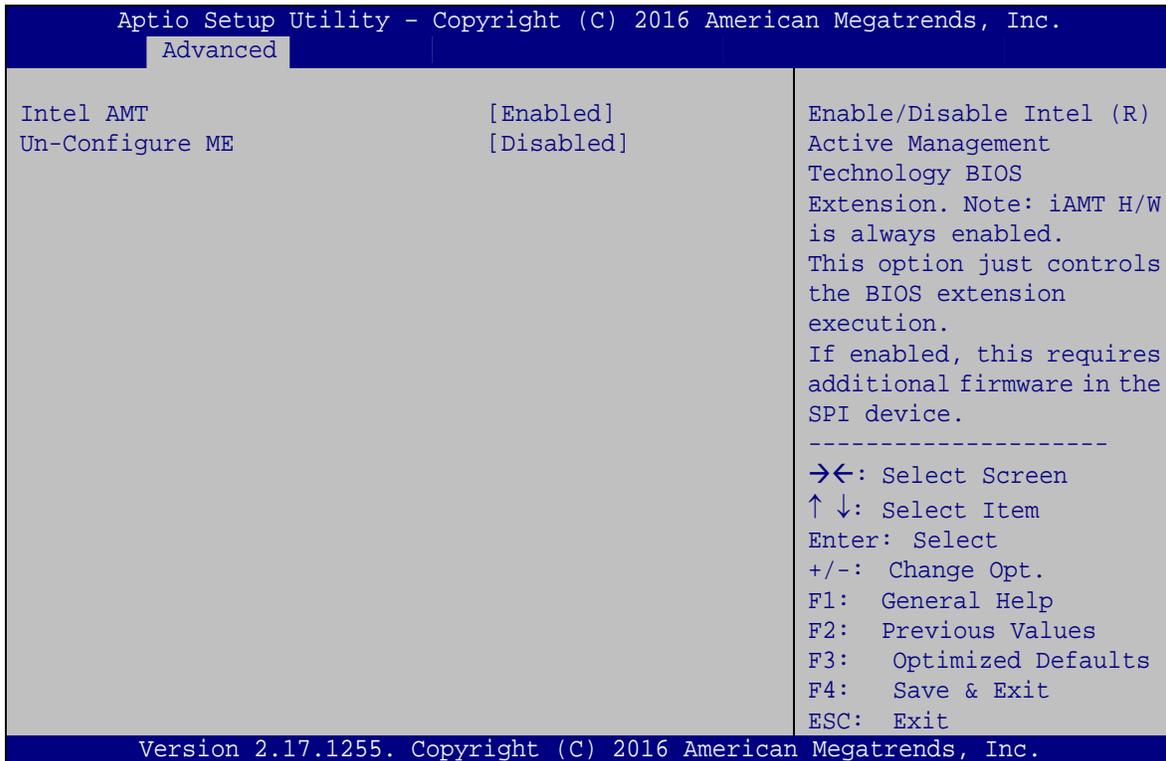
##### → ACPI Sleep State [S3 (Suspend to RAM)]

Use the **ACPI Sleep State** option to specify the sleep state the system enters when it is not being used.

- **S3 (Suspend to RAM)**      **DEFAULT**      The caches are flushed and the CPU is powered off. Power to the RAM is maintained. The computer returns slower to a working state, but more power is saved.

### 5.3.2 AMT Configuration

The **AMT Configuration** menu (**BIOS Menu 4**) allows the Intel® AMT options to be configured.



#### BIOS Menu 4: AMT Configuration

##### → Intel AMT [Enabled]

Use **Intel AMT** option to enable or disable the Intel® AMT function.

- **Disabled** Intel® AMT is disabled
- **Enabled** **DEFAULT** Intel® AMT is enabled

##### → Un-Configure ME [Disabled]

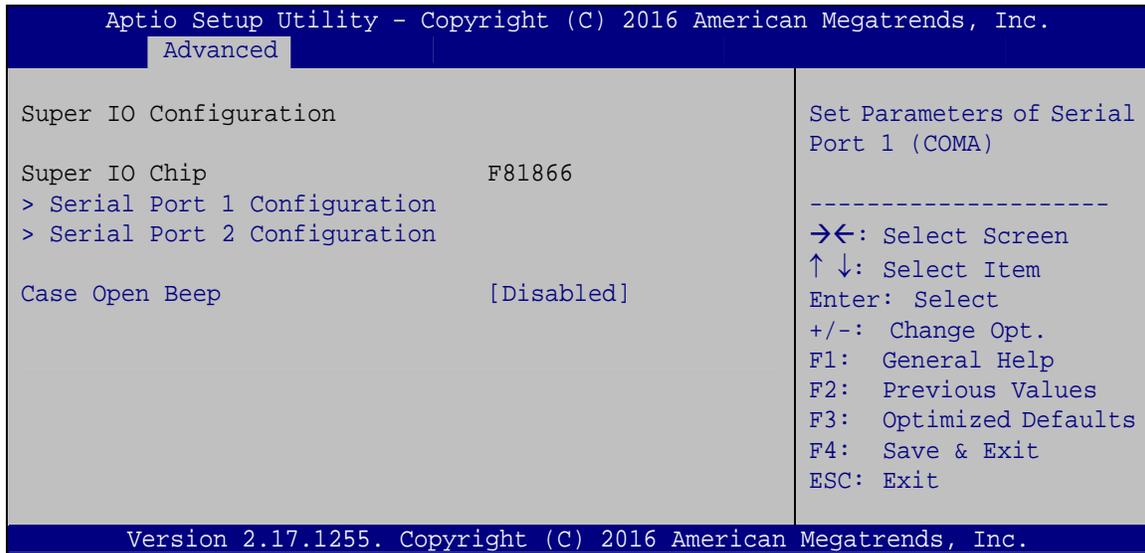
Use the **Un-Configure ME** option to perform ME unconfigure without password operation.

- **Disabled** **DEFAULT** Not perform ME unconfigure
- **Enabled** To perform ME unconfigure

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 5.3.3 Super IO Configuration

Use the **Super IO Configuration** menu (**BIOS Menu 5**) to set or change the configurations for the serial ports and parallel port.



#### BIOS Menu 5: Super IO Configuration

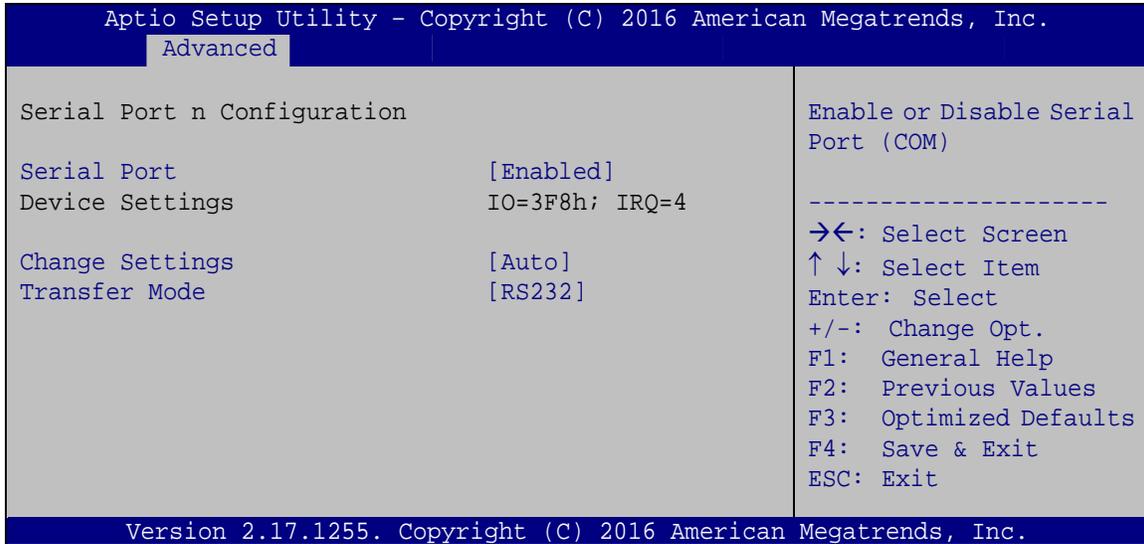
##### → Case Open Beep [Disabled]

Use the **Case Open Beep** option to enable or disable the case open beep function.

- **Disabled**      **DEFAULT**      Disable the case open beep function
- **Enabled**                      Enable the case open beep function

### 5.3.3.1 Serial Port n Configuration

Use the **Serial Port n Configuration** menu (**BIOS Menu 6**) to configure the serial port n.



#### BIOS Menu 6: Serial Port n Configuration Menu

#### 5.3.3.1.1 Serial Port 1 Configuration

##### → Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

- **Disabled**                      Disable the serial port
- **Enabled**            **DEFAULT**      Enable the serial port

##### → Change Settings [Auto]

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

- **Auto**            **DEFAULT**      The serial port IO port address and interrupt address are automatically detected.
- **IO=3F8h;**  
**IRQ=4**                      Serial Port I/O port address is 3F8h and the interrupt address is IRQ4

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

- ➔ **IO=3F8h;**  
**IRQ=3, 4, 11**      Serial Port I/O port address is 3F8h and the interrupt address is IRQ3, 4, 11
- ➔ **IO=2F8h;**  
**IRQ=3, 4, 11**      Serial Port I/O port address is 2F8h and the interrupt address is IRQ3, 4, 11
- ➔ **IO=3E8h;**  
**IRQ=3, 4, 11**      Serial Port I/O port address is 3E8h and the interrupt address is IRQ3, 4, 11
- ➔ **IO=2E8h;**  
**IRQ=3, 4, 11**      Serial Port I/O port address is 2E8h and the interrupt address is IRQ3, 4, 11
- ➔ **IO=2D0h;**  
**IRQ=3, 4, 11**      Serial Port I/O port address is 2D0h and the interrupt address is IRQ3, 4, 11
- ➔ **IO=2E0h;**  
**IRQ=3, 4, 11**      Serial Port I/O port address is 2E0h and the interrupt address is IRQ3, 4, 11

### ➔ **Transfer Mode [RS232]**

The serial port allows setting the data transfer mode to RS-232, RS-422 or RS-485.

### 5.3.3.1.2 Serial Port 2 Configuration

#### ➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled**      Disable the serial port
- ➔ **Enabled**      **DEFAULT**      Enable the serial port

#### ➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

- ➔ **Auto**      **DEFAULT**      The serial port IO port address and interrupt address are automatically detected.

- **IO=2F8h;**  
**IRQ=3**                      Serial Port I/O port address is 2F8h and the interrupt address is IRQ3
- **IO=3F8h;**  
**IRQ=3, 4, 11**              Serial Port I/O port address is 3F8h and the interrupt address is IRQ3, 4, 11
- **IO=2F8h;**  
**IRQ=3, 4, 11**              Serial Port I/O port address is 2F8h and the interrupt address is IRQ3, 4, 11
- **IO=3E8h;**  
**IRQ=3, 4, 11**              Serial Port I/O port address is 3E8h and the interrupt address is IRQ3, 4, 11
- **IO=2E8h;**  
**IRQ=3, 4, 11**              Serial Port I/O port address is 2E8h and the interrupt address is IRQ3, 4, 11
- **IO=2D0h;**  
**IRQ=3, 4, 11**              Serial Port I/O port address is 2D0h and the interrupt address is IRQ3, 4, 11
- **IO=2E0h;**  
**IRQ=3, 4, 11**              Serial Port I/O port address is 2E0h and the interrupt address is IRQ3, 4, 11

→ **Transfer Mode [RS232]**

The serial port allows setting the data transfer mode to RS-232, RS-422 or RS-485.

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 5.3.4 iWDD H/W Monitor

The **iWDD H/W Monitor** menu (**BIOS Menu 7**) contains the fan configuration submenu, and displays operating temperature, fan speeds and system voltages.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
-----
Advanced
-----
PC Health Status
CPU temperature           : +55°C
SYS temperature          : +41°C

CPU_FAN1 Speed           : 1212 RPM

CPU_CORE                  : +1.114 V
+5V                       : +5.005 V
+12V                      : +11.645 V
DDR                        : +1.196 V
+5VSB                     : +4.961 V
+3.3V                     : +3.296 V
+3.3VSB                   : +3.311 V

> Smart Fan Mode Configuration

Smart Fan Mode Select

-----
-><: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
  
```

#### BIOS Menu 7: iWDD H/W Monitor

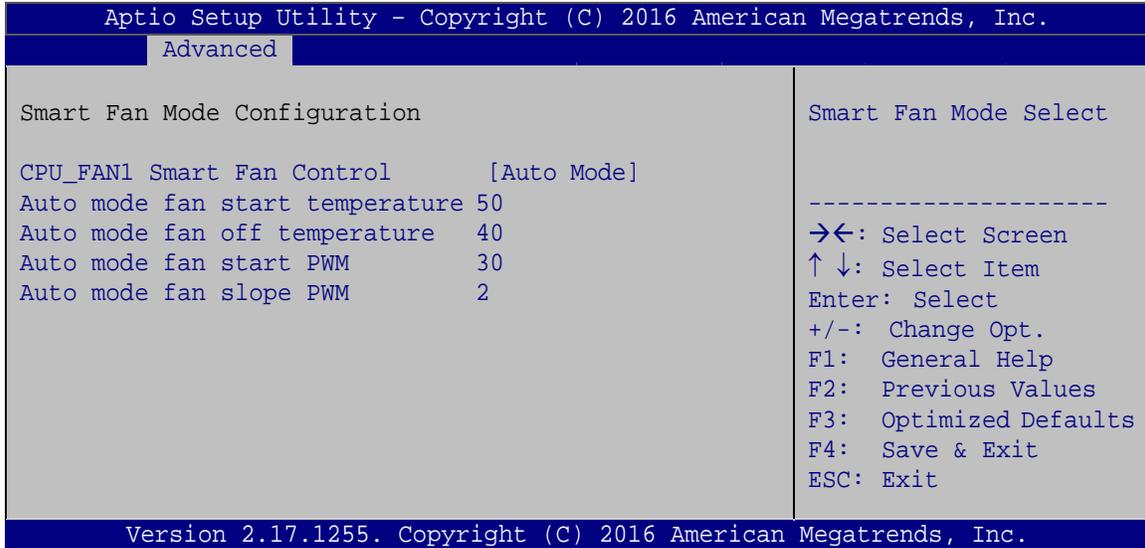
##### → PC Health Status

The following system parameters and values are shown. The system parameters that are monitored are:

- System Temperatures:
  - CPU Temperature
  - System Temperature
- Fan Speed:
  - CPU Fan Speed
- Voltages:
  - CPU\_CORE
  - +5V
  - +12V
  - DDR
  - +5VSB
  - +3.3V
  - +3.3VSB

### 5.3.4.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 8**) to configure fan speed settings.



#### BIOS Menu 8: Smart Fan Mode Configuration

##### → CPU\_FAN1 Smart Fan Control [Auto Mode]

Use the **CPU\_FAN1 Smart Fan Control** option to configure the CPU fan.

- **Auto Mode**      **DEFAULT**      The fan adjusts its speed using Auto Mode settings.
- **Manual Mode**                      The fan spins at the speed set in Manual Mode settings.

##### → Auto mode fan start/off temperature

Use the + or – key to change the **Auto mode fan start/off temperature** value. Enter a decimal number between 1 and 100.

##### → Auto mode fan start PWM

Use the + or – key to change the **Auto mode fan start PWM** value. Enter a decimal number between 1 and 100.

##### → Auto mode fan slope PWM

Use the + or – key to change the **Auto mode fan slope PWM** value. Enter a decimal number between 1 and 8.

### 5.3.5 RTC Wake Settings

The **RTC Wake Settings** menu (**BIOS Menu 9**) enables the system to wake at the specified time.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
-----
Advanced
-----
Wake system with Fixed Time      [Disabled]
                                  Enable or disable System
                                  wake on alarm event. When
                                  enabled, System will
                                  wake on the
                                  date::hr::min::sec
                                  specified
                                  -----
                                  →←: Select Screen
                                  ↑↓: Select Item
                                  Enter: Select
                                  +/-: Change Opt.
                                  F1:  General Help
                                  F2:  Previous Values
                                  F3:  Optimized Defaults
                                  F4:  Save & Exit
                                  ESC: Exit
-----
Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
    
```

#### BIOS Menu 9: RTC Wake Settings

##### → Wake system with Fixed Time [Disabled]

Use the **Wake system with Fixed Time** option to enable or disable the system wake on alarm event.

- **Disabled**      **DEFAULT**      The real time clock (RTC) cannot generate a wake event.
- **Enabled**      If selected, the **Wake up every day** option appears allowing you to enable to disable the system to wake every day at the specified time. Besides, the following options appear with values that can be selected:

Wake up date

Wake up hour

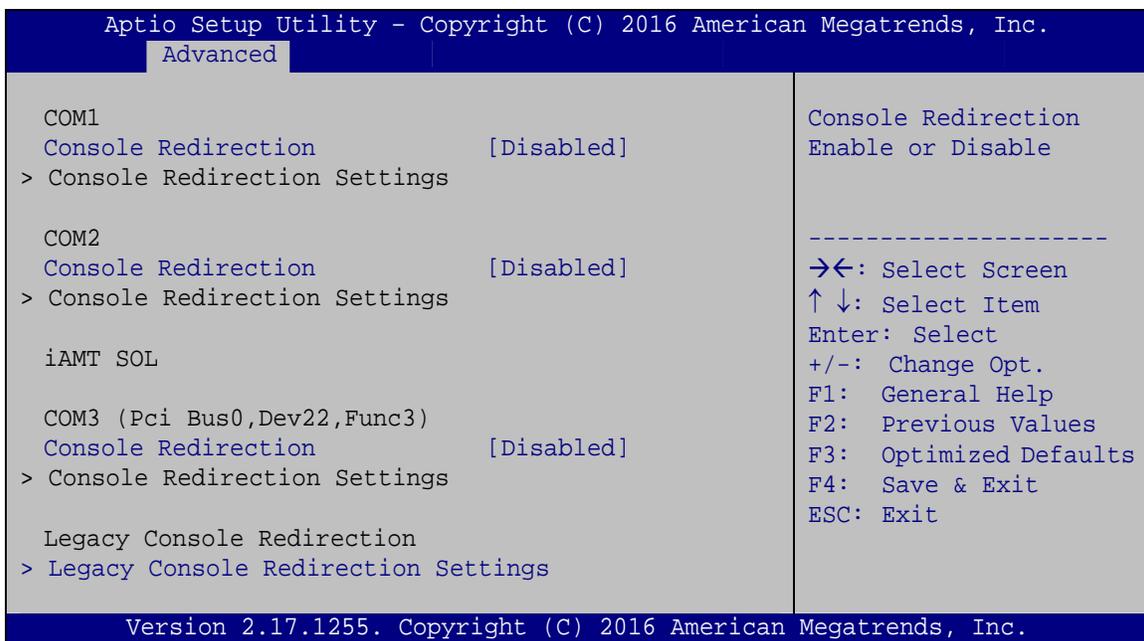
Wake up minute

Wake up second

After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

### 5.3.6 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 10**) allows the console redirection options to be configured. Console redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



#### BIOS Menu 10: Serial Port Console Redirection

##### → Console Redirection [Disabled]

Use **Console Redirection** option to enable or disable the console redirection function.

- **Disabled**    **DEFAULT**    Disabled the console redirection function
- **Enabled**                    Enabled the console redirection function

The following options are available in the **Console Redirection Settings** submenu when the **Console Redirection** option is enabled.

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### → Terminal Type [ANSI]

Use the **Terminal Type** option to specify the remote terminal type.

- **VT100**                                      The target terminal type is VT100
- **VT100+**                                    The target terminal type is VT100+
- **VT-UTF8**                                   The target terminal type is VT-UTF8
- **ANSI**                      **DEFAULT**      The target terminal type is ANSI

### → Bits per second [115200]

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match the other side. Long or noisy lines may require lower speeds.

- **9600**                                        Sets the serial port transmission speed at 9600.
- **19200**                                      Sets the serial port transmission speed at 19200.
- **57600**                                      Sets the serial port transmission speed at 57600.
- **115200**                      **DEFAULT**      Sets the serial port transmission speed at 115200.

### → Data Bits [8]

Use the **Data Bits** option to specify the number of data bits.

- **7**    Sets the data bits at 7.
- **8**    **DEFAULT**      Sets the data bits at 8.

### → Parity [None]

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

- **None**                      **DEFAULT**      No parity bit is sent with the data bits.
- **Even**                                        The parity bit is 0 if the number of ones in the data bits is even.

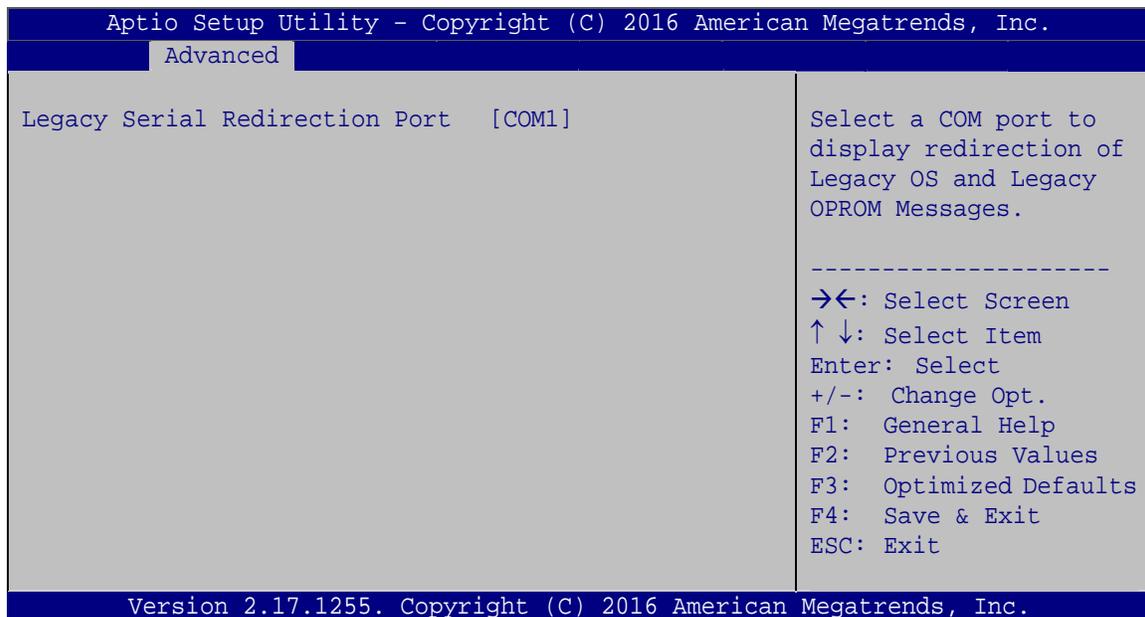
- **Odd**                      The parity bit is 0 if the number of ones in the data bits is odd.
- **Mark**                     The parity bit is always 1. This option does not provide error detection.
- **Space**                    The parity bit is always 0. This option does not provide error detection.

### → **Stop Bits [1]**

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

- **1**                      **DEFAULT**              Sets the number of stop bits at 1.
- **2**                      Sets the number of stop bits at 2.

### 5.3.6.1 Legacy Console Redirection Settings



**BIOS Menu 11: Legacy Console Redirection Settings**

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### → Legacy Serial Redirection Port [COM1]

Use the **Legacy Serial Redirection Port** option to select a COM port to display redirection of legacy OS and legacy OPRM messages. Configuration options are listed below.

- COM1 **Default**
- COM2
- COM3 (Pci Bus0,Dev22,Func3)

### 5.3.7 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 12**) to view detailed CPU specifications or enable the Intel Virtualization Technology.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
  Advanced
-----
CPU Configuration
Intel(R) Core(TM) i5-6500 CPU @ 3.20GHz
CPU Signature          506E3
Microcode Patch       7C
Max CPU Speed         3200 MHz
Min CPU Speed         800 MHz
CPU Speed             3200 MHz
Processor Cores       4
Hyper Threading Technology Not Supported
Intel VT-x Technology Supported
Intel SMX Technology  Not Supported
64-bit                Supported
EIST Technology       Supported

L1 Data Cache        32 kB x 4
L1 Code Cache        32 kB x 4
L2 Cache             256 kB x 4
L3 Cache             6 MB

Active Processor Cores [All]
Intel Virtualization Technology [Disabled]
Intel(R) SpeedStep(tm) [Enabled]
CPU C states         [Disabled]
Intel TXT(LT) Support [Disabled]

Number of cores to enable
in each processor
package.

-----
-><: Select Screen
↑ ↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

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```

**BIOS Menu 12: CPU Configuration**

→ **Active Processor Cores [All]**

Use the **Active Processor Cores** BIOS option to enable numbers of cores in the processor package.

- **All**            **DEFAULT**    Enable all cores in the processor package.
- **1**                                    Enable one core in the processor package.
- **2**                                    Enable two cores in the processor package.
- **3**                                    Enable three cores in the processor package.

→ **Intel Virtualization Technology [Disabled]**

Use the **Intel Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel® Virtualization technology allows several OSs to run on the same system at the same time.

- **Disabled**                    **DEFAULT**    Disables Intel Virtualization Technology.
- **Enabled**                                    Enables Intel Virtualization Technology.

→ **Intel(R) SpeedStep(tm) [Enabled]**

Use the **Intel(R) SpeedStep(tm)** option to enable or disable the Intel® SpeedStep Technology which allows more than two frequency ranges to be supported.

- **Disabled**                                    Disables Intel® SpeedStep Technology
- **Enabled**                    **DEFAULT**    Enables Intel® SpeedStep Technology

→ **CPU C states [Disabled]**

Use the **CPU C states** option to enable or disable the CPU C states.

- **Disabled**                    **DEFAULT**    Disables the CPU C states.
- **Enabled**                                    Enables the CPU C states.

## HPCI-E-Q170 Half-size PICMG 1.3 CPU Card

### → Intel TXT(LT) Support [Disabled]

Use the **Intel TXT(LT) Support** option to enable or disable the Intel(R) TXT(LT) support.

- **Disabled** Disables Intel® TXT(LT) support
- **Enabled** **DEFAULT** Enables Intel® TXT(LT) support

### 5.3.8 SATA Configuration

Use the **SATA Configuration** menu (**BIOS Menu 13**) to change and/or set the configuration of the SATA devices installed in the system.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
  Advanced
-----
SATA Controller(s)      [Enabled]      Enable or disable SATA
SATA Mode Selection    [AHCI]        Device.
-----
mSATA                  Empty
  Hot Plug             [Disabled]
SATA1                  Empty
  Hot Plug             [Disabled]
SATA2                  Empty
  Hot Plug             [Disabled]
-----
-><: Select Screen
↑ ↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
-----
Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
  
```

#### BIOS Menu 13: SATA Configuration

### → SATA Controller(s) [Enabled]

Use the **SATA Controller(s)** option to configure the SATA controller(s).

- **Enabled** **DEFAULT** Enables the on-board SATA controller(s).
- **Disabled** Disables the on-board SATA controller(s).

### → SATA Mode Selection [AHCI]

Use the **SATA Mode Selection** option to determine how the SATA devices operate.

- **AHCI** **DEFAULT** Configures SATA devices as AHCI device.
- **RAID** Configures SATA devices as RAID device.

### → Hot Plug [Disabled]

Use the **Hot Plug** option to designate the correspondent SATA port as hot-pluggable.

- **Disabled**      **DEFAULT**      Disables the hot-pluggable function of the SATA port.
- **Enabled**                      Designates the SATA port as hot-pluggable.

### 5.3.9 NVMe Configuration

Use the **NVMe Configuration (BIOS Menu 14)** menu to display the NVMe controller and device information.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
-----
Advanced
-----
NVMe controller and Drive information
No NVMe Device Found

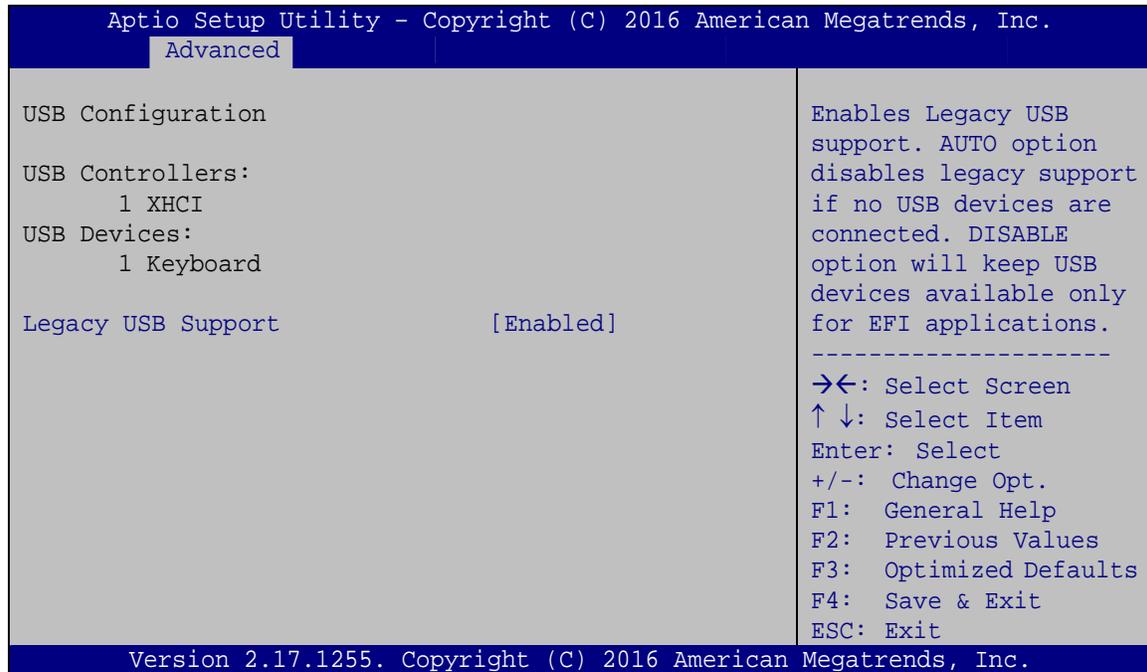
-----
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
-----
Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
    
```

**BIOS Menu 14: NVMe Configuration**

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 5.3.10 USB Configuration

Use the **USB Configuration** menu (**BIOS Menu 15**) to read USB configuration information and configure the USB settings.



#### BIOS Menu 15: USB Configuration

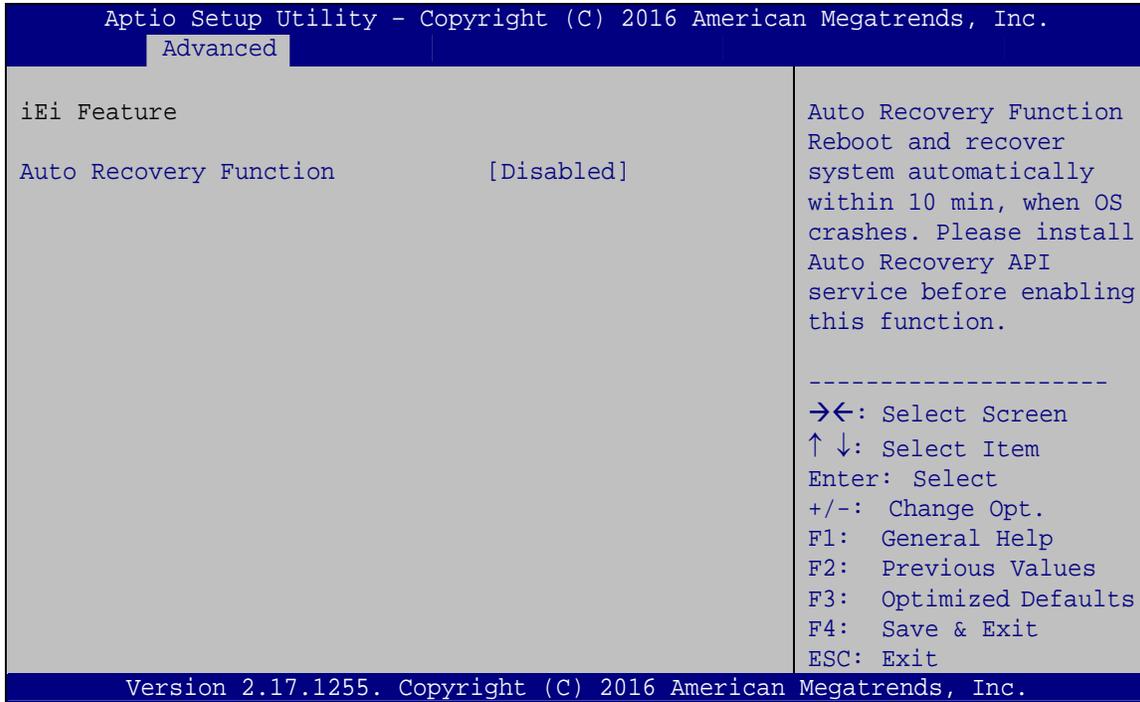
##### → Legacy USB Support [Enabled]

Use the **Legacy USB Support** BIOS option to enable USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.

- **Enabled**      **DEFAULT**      Legacy USB support enabled
- **Disabled**                      Legacy USB support disabled
- **Auto**                              Legacy USB support disabled if no USB devices are connected

### 5.3.11 iEi Feature

Use the **iEi Feature** menu (**BIOS Menu 16**) to configure One Key Recovery function.



#### BIOS Menu 16: iEi Feature

##### → Auto Recovery Function [Disabled]

Use the **Auto Recovery Function** BIOS option to enable or disable the auto recovery function of the IEI One Key Recovery.

- **Disabled**      **DEFAULT**      Auto recovery function disabled
- **Enabled**      Auto recovery function enabled

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 17**) to access the PCH IO and System Agent (SA) configuration menus.



#### **WARNING!**

Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.

```

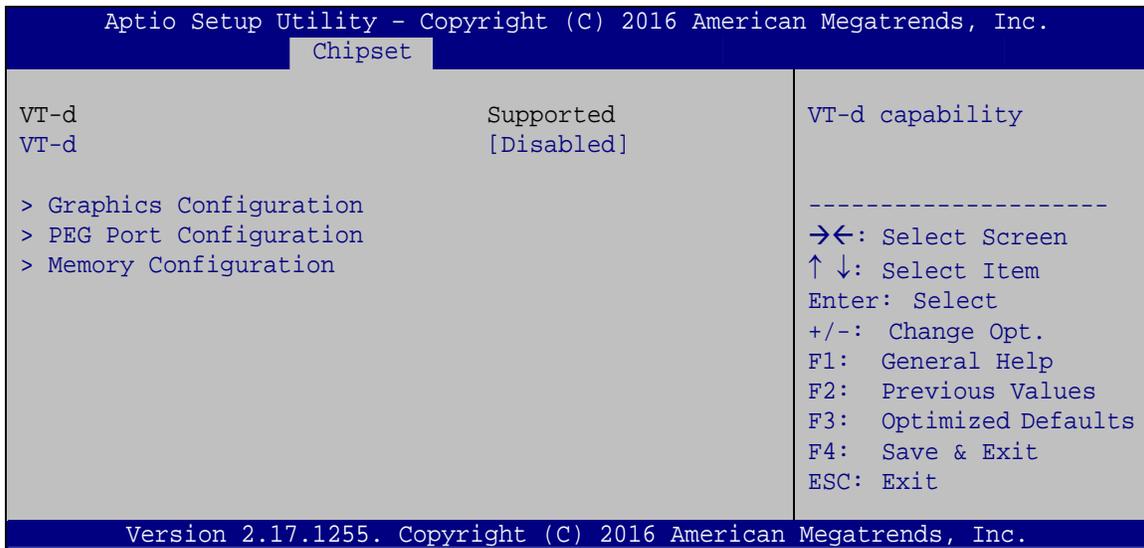
Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
Main   Advanced  Chipset  Security  Boot   Save & Exit
-----
> System Agent (SA) Configuration      System Agent (SA)
> PCH-IO Configuration                 Parameters
-----
-><: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
    
```

**BIOS Menu 17: Chipset**

### 5.4.1 System Agent (SA) Configuration

Use the **System Agent (SA) Configuration** menu (**BIOS Menu 18**) to configure the System Agent (SA) parameters.



#### BIOS Menu 18: System Agent (SA) Configuration

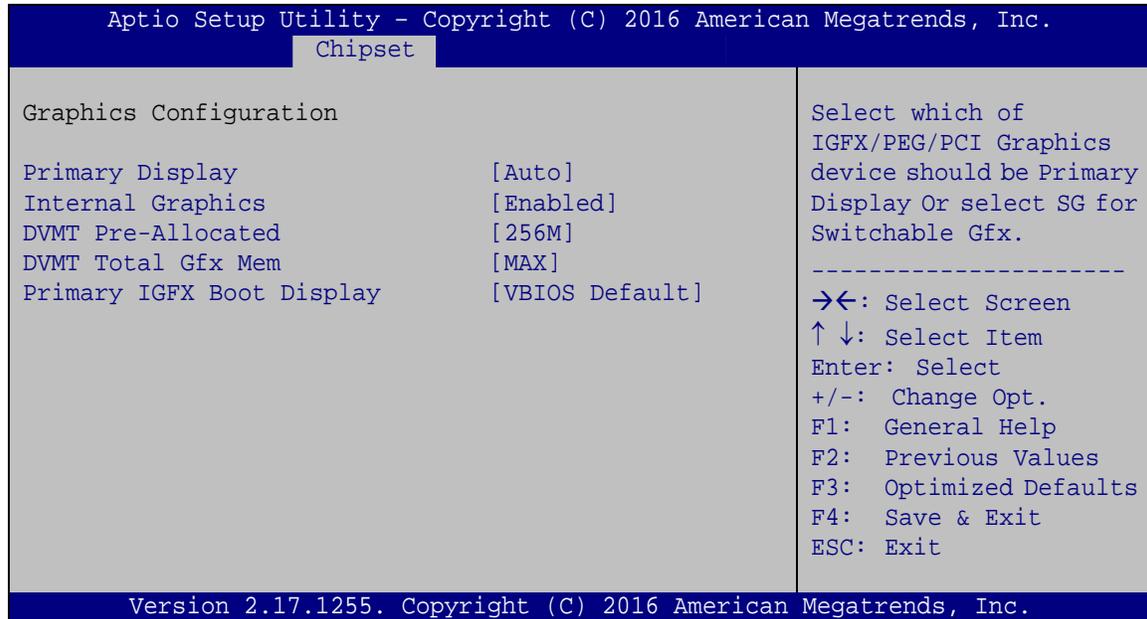
##### → VT-d [Disabled]

Use the **VT-d** option to enable or disable VT-d capability.

- **Disabled**                      **DEFAULT**      Disables VT-d capability.
- **Enabled**    Enables VT-d capability.

### 5.4.1.1 Graphics Configuration

Use the **Graphics Configuration (BIOS Menu 19)** menu to configure the video device connected to the system.



#### BIOS Menu 19: Graphics Configuration

##### → Primary Display [Auto]

Use the **Primary Display** option to select the primary graphics controller the system uses.

The following options are available:

- Auto **Default**
- IGFX
- PEG
- PCIE

##### → Internal Graphics [Enabled]

Use the **Internal Graphics** option to keep IGFX enabled basing on the setup options. The following options are available:

- Auto
- Disabled
- Enabled **Default**

**→ DVMT Pre-Allocated [256M]**

Use the **DVMT Pre-Allocated** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

- 32M
- 64M
- 128M
- 256M                   **Default**
- 512M

**→ DVMT Total Gfx Mem [MAX]**

Use the **DVMT Total Gfx Mem** option to select DVMT5.0 total graphic memory size used by the internal graphic device. The following options are available:

- 128M
- 256M
- MAX                   **Default**

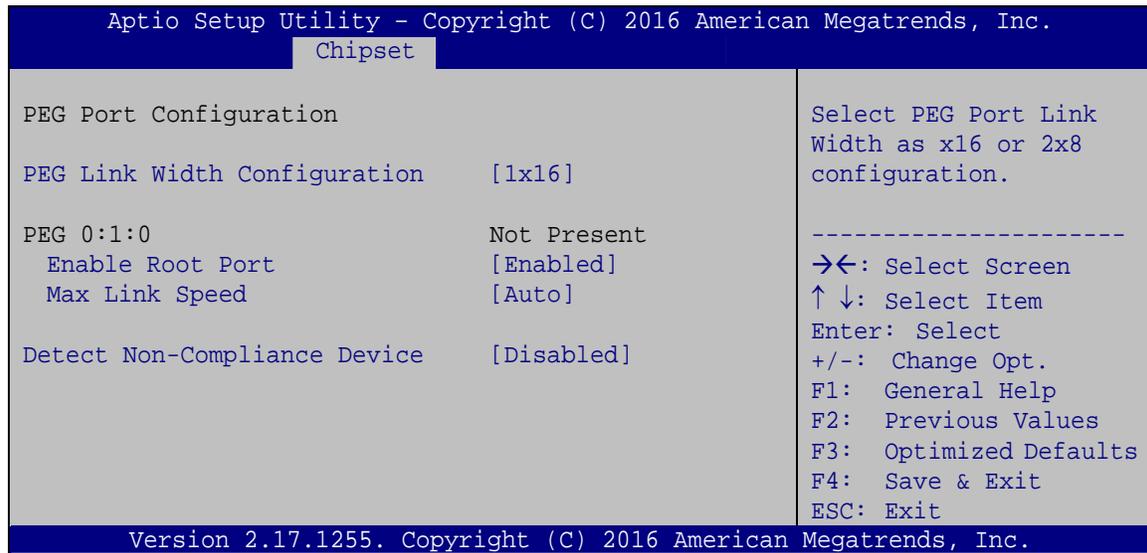
**→ Primary IGFX Boot Display [VBIOS Default]**

Use the **Primary IGFX Boot Display** option to select the display device used by the system when it boots. Configuration options are listed below.

- VBIOS Default       **Default**
- CRT
- IDP

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 5.4.1.2 PEG Port Configuration



#### BIOS Menu 20: PEG Port Configuration

##### → PEG Link Width Configuration [1x16]

Use the **PEG Link Width Configuration** option to configure the PCIe x16 channel mode on the backplane.

- **1x16**                      **DEFAULT**      Sets the PCIe x16 link width as one PCIe x16 slot
- **2x8**                                      Sets the PCIe x16 link width as two PCIe x8 slots
- **1x8, 2x4**                              Sets the PCIe x16 link width as one PCIe x8 and two PCIe x4 slots

##### → Enable Root Port [Enabled]

Use the **Enable Root Port** option to enable or disable the PCI Express (PEG) controller.

- **Disabled**                              Disables the PCI Express (PEG) controller.
- **Enabled**                              **DEFAULT**      Enables the PCI Express (PEG) controller.

### → Max Link Speed [Auto]

Use the **Max Link Speed** option to select the maximum link speed of the PCI Express slot. The following options are available:

- Auto                      **Default**
- Gen1
- Gen2
- Gen3

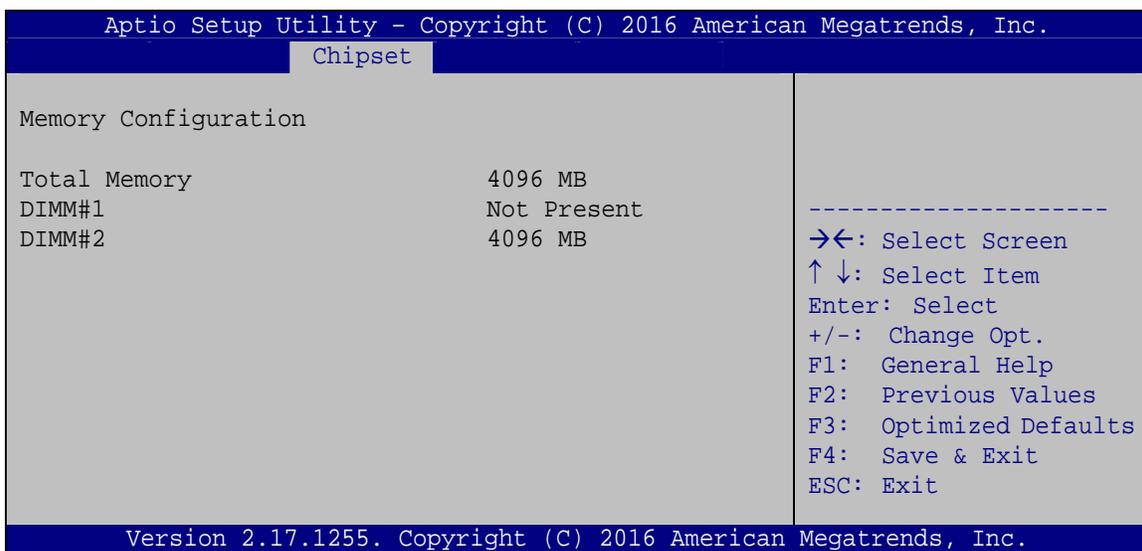
### → Detect Non-Compliance Device [Disabled]

Use the **Detect Non-Compliance Device** option to enable or disable detecting if a non-compliance PCI Express device is connected to the PCI Express slot.

- **Disabled**                      **DEFAULT**      Disables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.
- **Enabled**                              Enables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.

### 5.4.1.3 Memory Configuration

Use the **Memory Configuration** submenu (**BIOS Menu 21**) to view memory information.

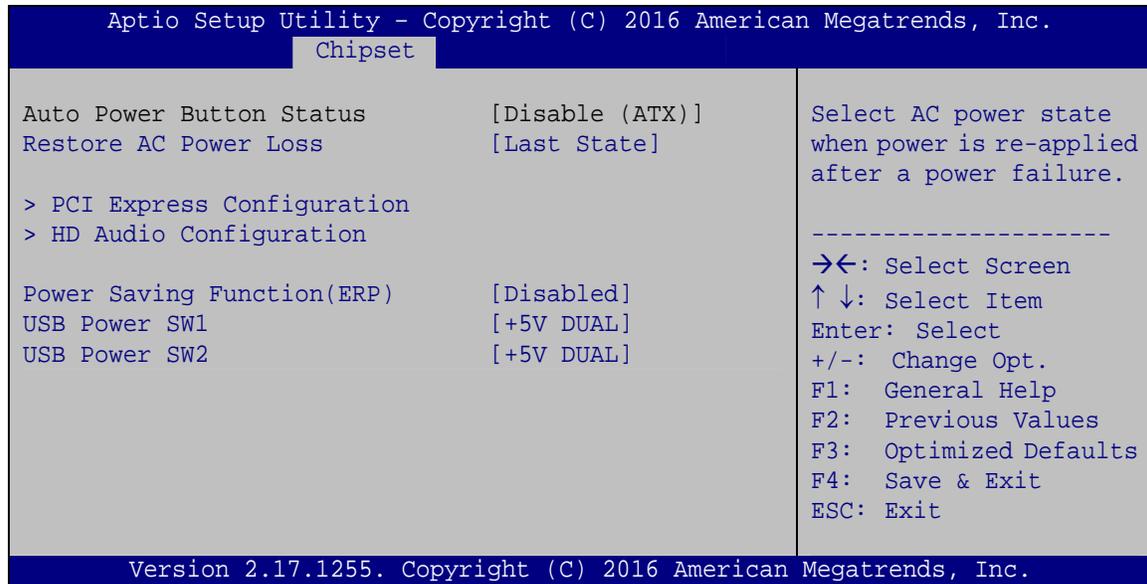


**BIOS Menu 21: Memory Configuration**

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 5.4.2 PCH-IO Configuration

Use the **PCH-IO Configuration** menu (**BIOS Menu 22**) to configure the PCH parameters.



#### BIOS Menu 22: PCH-IO Configuration

##### → Restore AC Power Loss [Last State]

Use the **Restore AC Power Loss** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system.

- **Power Off**                      The system remains turned off
- **Power On**                        The system turns on
- **Last State    DEFAULT**        The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

##### → Power Saving Function(ERP) [Disabled]

Use the **Power Saving Function(ERP)** BIOS option to enable or disable the power saving function.

- **Disabled    DEFAULT**        Power saving function is disabled.
- **Enabled**                        Power saving function is enabled. It will reduce power consumption when the system is off.

### → USB Power SW1 [+5V DUAL]

Use the **USB Power SW1** BIOS option to configure the USB power source for the corresponding USB connectors (**Table 5-2**).

- **+5V** Sets the USB power source to +5V
- **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual

### → USB Power SW2 [+5V DUAL]

Use the **USB Power SW2** BIOS option to configure the USB power source for the corresponding USB connectors (**Table 5-2**).

- **+5V** Sets the USB power source to +5V
- **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual

BIOS Options	Configured USB Ports
USB Power SW1	CN1 (external USB 3.0 port) CN2 (external USB 3.0 port)
USB Power SW2	USB1 (internal USB 2.0 ports) USB2 (internal USB 2.0 ports)

**Table 5-2: BIOS Options and Configured USB Ports**

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### 5.4.2.1 PCI Express Configuration

The PCI Express port number in the **PCI Express Configuration** menu varies by BIOS (BIOS1 or BIOS2). For detailed information, please refer to **Section 4.8.3**.

#### For BIOS1:

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
  Chipset
-----
PCI Express Configuration
(BIOS No.1)

> PCI Express Port 1
> PCI Express Port 2
> PCI Express Port 3
> PCI Express Port 4

PCI Express Port 1
Settings.

-----
-><: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
  
```

**BIOS Menu 23: PCI Express Configuration (For BIOS1)**

#### For BIOS2:

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
  Chipset
-----
PCI Express Configuration
(BIOS No.2)

> PCI Express Port 1

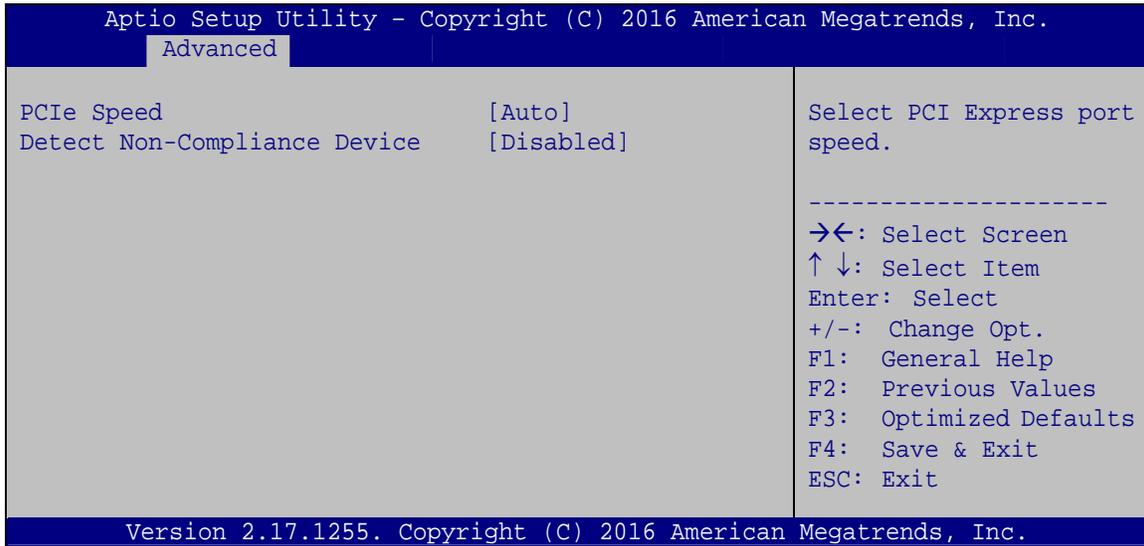
PCI Express Port 1
Settings.

-----
-><: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
  
```

**BIOS Menu 24: PCI Express Configuration (For BIOS2)**

### 5.4.2.1.1 PCI Express Port 1/2/3/4



#### BIOS Menu 25: PCI Express Port 1/2/3/4

##### → PCIe Speed [Auto]

Use this option to select the support type of the PCI Express slots. The following options are available:

- Auto                      **Default**
- Gen1
- Gen2
- Gen3

##### → Detect Non-Compliance Device [Disabled]

Use the **Detect Non-Compliance Device** option to enable or disable detecting if a non-compliance PCI Express device is connected to the PCI Express slot.

- **Disabled**                      **DEFAULT**      Disables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.
- **Enabled**                              Enables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.

### 5.4.2.2 HD Audio Configuration

Use the **HD Audio Configuration** menu (**BIOS Menu 26**) to configure the PCH Azalia settings.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
Chipset
HD Audio Configuration
HD Audio [Auto]
Control Detection of the
HD-Audio device.
Disable = HDA will be
unconditionally
disabled
Enabled = HDA will be
unconditionally enabled
Auto = HDA will be
enabled if present,
disabled otherwise.
-----
-><: Select Screen
↑ ↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.

```

#### BIOS Menu 26: HD Audio Configuration

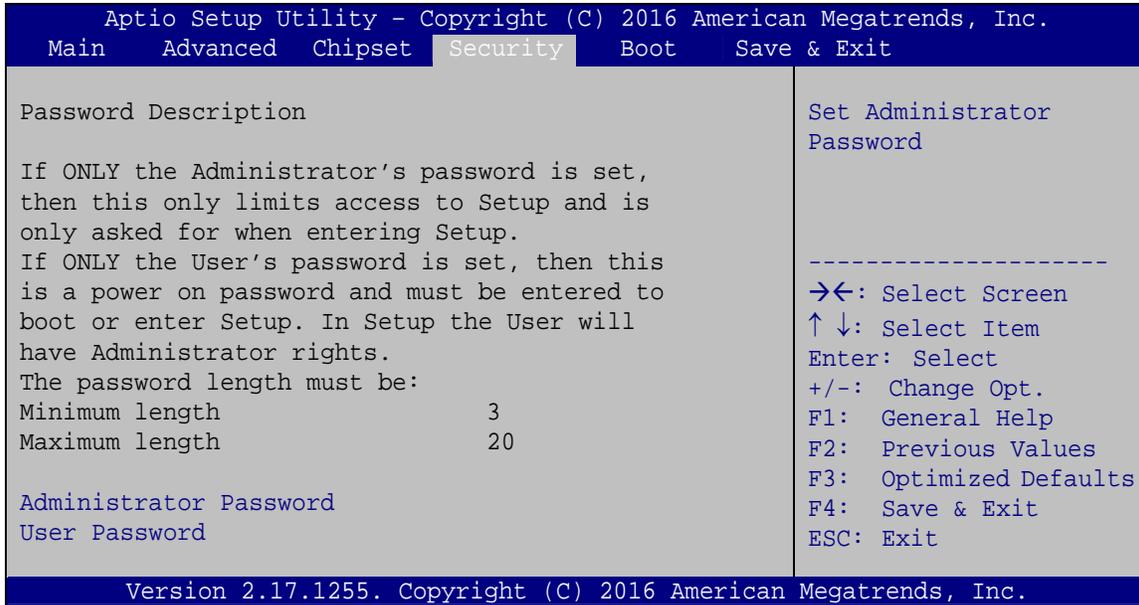
##### → HD Audio [Auto]

Use the **HD Audio** option to enable or disable the High Definition Audio controller.

- **Disabled**                      The onboard High Definition Audio controller is disabled.
- **Enabled**                        The onboard High Definition Audio controller is enabled.
- **Auto**                      **DEFAULT**      The onboard High Definition Audio controller automatically detected and enabled

## 5.5 Security

Use the **Security** menu (**BIOS Menu 27**) to set system and user passwords.



### BIOS Menu 27: Security

#### → Administrator Password

Use the **Administrator Password** to set or change a administrator password.

#### → User Password

Use the **User Password** to set or change a user password.

### 5.6 Boot

Use the **Boot** menu (**BIOS Menu 28**) to configure system boot options.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
Main   Advanced  Chipset  Security  Boot   Save & Exit
-----
Boot Configuration
Bootup NumLock State      [On]
Quiet Boot                 [Enabled]
Launch PXE OpROM          [Disabled]
Option ROM Messages       [Force BIOS]
UEFI Boot                 [Disabled]

Boot Option Priorities

-----
Select the keyboard
NumLock state

-----
-><: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.

```

#### BIOS Menu 28: Boot

##### → Bootup NumLock State [On]

Use the **Bootup NumLock State** BIOS option to specify if the number lock setting must be modified during boot up.

- **On**                      **DEFAULT**                      Allows the Number Lock on the keyboard to be enabled automatically when the computer system boots up. This allows the immediate use of the 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard is lit.
- **Off**                                      Does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard lights up when the Number Lock is engaged.

→ **Quiet Boot [Enabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

- **Disabled** Normal POST messages displayed
- **Enabled** **DEFAULT** OEM Logo displayed instead of POST messages

→ **Launch PXE OpROM [Disabled]**

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

- **Disabled** **DEFAULT** Ignore all PXE Option ROMs
- **Enabled** Load PXE Option ROMs.

→ **Option ROM Messages [Force BIOS]**

Use the **Option ROM Messages** option to set the Option ROM display mode.

- **Force BIOS** **DEFAULT** Sets display mode to force BIOS.
- **Keep Current** Sets display mode to current.

→ **UEFI Boot [Disabled]**

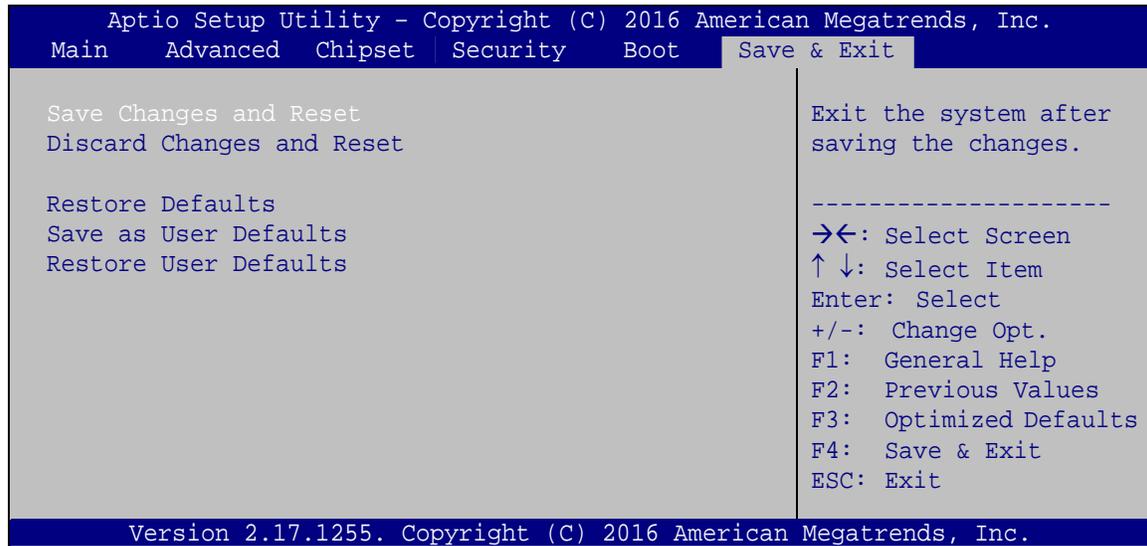
Use the **UEFI Boot** option to enable or disable to boot from the UEFI devices.

- **Enabled** Boot from UEFI devices is enabled.
- **Disabled** **DEFAULT** Boot from UEFI devices is disabled.

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

## 5.7 Save &amp; Exit

Use the **Safe & Exit** menu (**BIOS Menu 29**) to load default BIOS values, optimal failsafe values and to save configuration changes.

**BIOS Menu 29: Save & Exit**→ **Save Changes and Reset**

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and reset the system.

→ **Discard Changes and Reset**

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

→ **Restore Defaults**

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

→ **Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

→ **Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Chapter

**6**

# Software Drivers

---

## 6.1 Available Software Drivers

---

**NOTE:**

The content of the CD may vary throughout the life cycle of the product and is subject to change without prior notice. Visit the IEI website or contact technical support for the latest updates.

---

The following drivers can be installed on the system:

- Chipset
- VGA
- LAN
- Audio
- ME (Intel® AMT)
- USB 3.0 (Windows 7 OS only)
- Kernel-Mode Driver Framework (Windows 7 OS only)
- Intel® Serial IO (Windows 8.1/10 64-bit OS only)

## 6.2 Software Installation

All the drivers for the HPCIE-Q170 are on the CD that came with the system. To install the drivers, please follow the steps below.

**Step 1:** Insert the CD into a CD drive connected to the system.

**NOTE:**

If the installation program doesn't start automatically:  
Click "Start->My Computer->CD Drive->autorun.exe"

---

**Step 2:** The driver main menu appears. Click HPCIE-Q170.

**Step 3:** A new screen with a list of available drivers appears (**Figure 6-1**).



**Figure 6-1: Available Drivers**

**Step 4:** Install all of the necessary drivers in this menu.

Appendix

**A**

# Regulatory Compliance

---

**DECLARATION OF CONFORMITY**

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

**FCC WARNING**

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

**B**

# Product Disposal

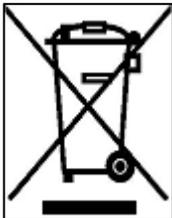
---

**CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- Outside the European Union – If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union – The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.



EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

# BIOS Options

---

Below is a list of BIOS configuration options in the BIOS chapter.

<b>System Date [xx/xx/xx]</b> .....	<b>68</b>
<b>System Time [xx:xx:xx]</b> .....	<b>68</b>
<b>ACPI Sleep State [S3 (Suspend to RAM)]</b> .....	<b>69</b>
<b>Intel AMT [Enabled]</b> .....	<b>70</b>
<b>Un-Configure ME [Disabled]</b> .....	<b>70</b>
<b>Case Open Beep [Disabled]</b> .....	<b>71</b>
<b>Serial Port [Enabled]</b> .....	<b>72</b>
<b>Change Settings [Auto]</b> .....	<b>72</b>
<b>Transfer Mode [RS232]</b> .....	<b>73</b>
<b>Serial Port [Enabled]</b> .....	<b>73</b>
<b>Change Settings [Auto]</b> .....	<b>73</b>
<b>Transfer Mode [RS232]</b> .....	<b>74</b>
<b>PC Health Status</b> .....	<b>75</b>
<b>CPU_FAN1 Smart Fan Control [Auto Mode]</b> .....	<b>76</b>
<b>Auto mode fan start/off temperature</b> .....	<b>76</b>
<b>Auto mode fan start PWM</b> .....	<b>76</b>
<b>Auto mode fan slope PWM</b> .....	<b>76</b>
<b>Wake system with Fixed Time [Disabled]</b> .....	<b>77</b>
<b>Console Redirection [Disabled]</b> .....	<b>78</b>
<b>Terminal Type [ANSI]</b> .....	<b>79</b>
<b>Bits per second [115200]</b> .....	<b>79</b>
<b>Data Bits [8]</b> .....	<b>79</b>
<b>Parity [None]</b> .....	<b>79</b>
<b>Stop Bits [1]</b> .....	<b>80</b>
<b>Legacy Serial Redirection Port [COM1]</b> .....	<b>81</b>
<b>Active Processor Cores [All]</b> .....	<b>82</b>
<b>Intel Virtualization Technology [Disabled]</b> .....	<b>82</b>
<b>Intel(R) SpeedStep(tm) [Enabled]</b> .....	<b>82</b>
<b>CPU C states [Disabled]</b> .....	<b>82</b>
<b>Intel TXT(LT) Support [Disabled]</b> .....	<b>83</b>
<b>SATA Controller(s) [Enabled]</b> .....	<b>83</b>
<b>SATA Mode Selection [AHCI]</b> .....	<b>83</b>
<b>Hot Plug [Disabled]</b> .....	<b>84</b>

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Legacy USB Support [Enabled].....	85
Auto Recovery Function [Disabled].....	86
VT-d [Disabled].....	88
Primary Display [Auto] .....	89
Internal Graphics [Enabled].....	89
DVMT Pre-Allocated [256M] .....	90
DVMT Total Gfx Mem [MAX].....	90
Primary IGFX Boot Display [VBIOS Default] .....	90
PEG Link Width Configuration [1x16].....	91
Enable Root Port [Enabled] .....	91
Max Link Speed [Auto] .....	92
Detect Non-Compliance Device [Disabled] .....	92
Restore AC Power Loss [Last State] .....	93
Power Saving Function(ERP) [Disabled].....	93
USB Power SW1 [+5V DUAL].....	94
USB Power SW2 [+5V DUAL].....	94
PCIe Speed [Auto].....	96
Detect Non-Compliance Device [Disabled] .....	96
HD Audio [Auto].....	97
Administrator Password .....	98
User Password .....	98
Bootup NumLock State [On].....	99
Quiet Boot [Enabled] .....	100
Launch PXE OpROM [Disabled].....	100
Option ROM Messages [Force BIOS].....	100
UEFI Boot [Disabled] .....	100
Save Changes and Reset .....	101
Discard Changes and Reset .....	101
Restore Defaults .....	101
Save as User Defaults .....	101
Restore User Defaults .....	101

Appendix

**D**

# Terminology

---

## HPCI-E-Q170 Half-size PICMG 1.3 CPU Card

<b>AC '97</b>	Audio Codec 97 (AC'97) refers to a codec standard developed by Intel® in 1997.
<b>ACPI</b>	Advanced Configuration and Power Interface (ACPI) is an OS-directed configuration, power management, and thermal management interface.
<b>AHCI</b>	Advanced Host Controller Interface (AHCI) is a SATA Host controller register-level interface.
<b>ATA</b>	The Advanced Technology Attachment (ATA) interface connects storage devices including hard disks and CD-ROM drives to a computer.
<b>ARMD</b>	An ATAPI Removable Media Device (ARMD) is any ATAPI device that supports removable media, besides CD and DVD drives.
<b>ASKIR</b>	Amplitude Shift Keyed Infrared (ASKIR) is a form of modulation that represents a digital signal by varying the amplitude (“volume”) of the signal. A low amplitude signal represents a binary 0, while a high amplitude signal represents a binary 1.
<b>BIOS</b>	The Basic Input/Output System (BIOS) is firmware that is first run when the computer is turned on and can be configured by the end user
<b>CODEC</b>	The Compressor-Decompressor (CODEC) encodes and decodes digital audio data on the system.
<b>CMOS</b>	Complimentary metal-oxide-conductor is an integrated circuit used in chips like static RAM and microprocessors.
<b>COM</b>	COM refers to serial ports. Serial ports offer serial communication to expansion devices. The serial port on a personal computer is usually a male DB-9 connector.
<b>DAC</b>	The Digital-to-Analog Converter (DAC) converts digital signals to analog signals.
<b>DDR</b>	Double Data Rate refers to a data bus transferring data on both the rising and falling edges of the clock signal.
<b>DMA</b>	Direct Memory Access (DMA) enables some peripheral devices to bypass the system processor and communicate directly with the system memory.

<b>DIMM</b>	Dual Inline Memory Modules are a type of RAM that offer a 64-bit data bus and have separate electrical contacts on each side of the module.
<b>DIO</b>	The digital inputs and digital outputs are general control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.
<b>EHCI</b>	The Enhanced Host Controller Interface (EHCI) specification is a register-level interface description for USB 2.0 Host Controllers.
<b>EIDE</b>	Enhanced IDE (EIDE) is a newer IDE interface standard that has data transfer rates between 4.0 MBps and 16.6 MBps.
<b>EIST</b>	Enhanced Intel® SpeedStep Technology (EIST) allows users to modify the power consumption levels and processor performance through application software. The application software changes the bus-to-core frequency ratio and the processor core voltage.
<b>FSB</b>	The Front Side Bus (FSB) is the bi-directional communication channel between the processor and the Northbridge chipset.
<b>GbE</b>	Gigabit Ethernet (GbE) is an Ethernet version that transfers data at 1.0 Gbps and complies with the IEEE 802.3-2005 standard.
<b>GPIO</b>	General purpose input
<b>HDD</b>	Hard disk drive (HDD) is a type of magnetic, non-volatile computer storage device that stores digitally encoded data.
<b>ICH</b>	The Input/Output Control Hub (ICH) is an Intel® Southbridge chipset.
<b>IrDA</b>	Infrared Data Association (IrDA) specify infrared data transmission protocols used to enable electronic devices to wirelessly communicate with each other.
<b>L1 Cache</b>	The Level 1 Cache (L1 Cache) is a small memory cache built into the system processor.
<b>L2 Cache</b>	The Level 2 Cache (L2 Cache) is an external processor memory cache.
<b>LCD</b>	Liquid crystal display (LCD) is a flat, low-power display device that consists of two polarizing plates with a liquid crystal panel in between.

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

<b>LVDS</b>	Low-voltage differential signaling (LVDS) is a dual-wire, high-speed differential electrical signaling system commonly used to connect LCD displays to a computer.
<b>POST</b>	The Power-on Self Test (POST) is the pre-boot actions the system performs when the system is turned-on.
<b>RAM</b>	Random Access Memory (RAM) is volatile memory that loses data when power is lost. RAM has very fast data transfer rates compared to other storage like hard drives.
<b>SATA</b>	Serial ATA (SATA) is a serial communications bus designed for data transfers between storage devices and the computer chipsets. The SATA bus has transfer speeds up to 1.5 Gbps and the SATA II bus has data transfer speeds of up to 3.0 Gbps.
<b>S.M.A.R.T</b>	Self Monitoring Analysis and Reporting Technology (S.M.A.R.T) refers to automatic status checking technology implemented on hard disk drives.
<b>UART</b>	Universal Asynchronous Receiver-transmitter (UART) is responsible for asynchronous communications on the system and manages the system's serial communication (COM) ports.
<b>UHCI</b>	The Universal Host Controller Interface (UHCI) specification is a register-level interface description for USB 1.1 Host Controllers.
<b>USB</b>	The Universal Serial Bus (USB) is an external bus standard for interfacing devices. USB 1.1 supports 12Mbps data transfer rates and USB 2.0 supports 480Mbps data transfer rates.
<b>VGA</b>	The Video Graphics Array (VGA) is a graphics display system developed by IBM.

Appendix

**E**

# Digital I/O Interface

---

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

### E.1 Introduction

The DIO connector on the HPCIE-Q170 is interfaced to GPIO ports on the Super I/O chipset. The digital inputs and digital outputs are generally control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.



#### NOTE:

For further information, please refer to the datasheet for the Super I/O chipset.

---

The BIOS interrupt call **INT 15H** controls the digital I/O.

#### INT 15H:

<b>AH – 6FH</b>	
<u>Sub-function:</u>	
<b>AL – 8</b>	: Set the digital port as INPUT
<b>AL</b>	: Digital I/O input value

### E.2 Assembly Language Sample 1

```
MOV     AX, 6F08H      ;setting the digital port as input
INT     15H           ;
```

AL low byte = value

AH – 6FH
<u>Sub-function:</u>
AL – 9 : Set the digital port as OUTPUT
BL : Digital I/O input value

### E.3 Assembly Language Sample 2

```
MOV     AX, 6F09H      ;setting the digital port as output
MOV     BL, 09H        ;digital value is 09H
INT     15H           ;
```

Digital Output is 1001b

Appendix

**F**

# Watchdog Timer

---



**NOTE:**

The following discussion applies to DOS environment. Contact IEI support or visit the IEI website for specific drivers for other operating systems.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMIs or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

<b>AH – 6FH Sub-function:</b>	
AL – 2:	Sets the Watchdog Timer’s period.
BL:	Time-out value (Its unit-second is dependent on the item “Watchdog Timer unit select” in CMOS setup).

**Table F-1: AH-6FH Sub-function**

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.



**NOTE:**

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

**EXAMPLE PROGRAM:**

**; INITIAL TIMER PERIOD COUNTER**

;

**W\_LOOP:**

;

```

MOV      AX, 6F02H      ;setting the time-out value
MOV      BL, 30         ;time-out value is 48 seconds
INT      15H

```

;

**; ADD THE APPLICATION PROGRAM HERE**

;

```

CMP      EXIT_AP, 1     ;is the application over?
JNE      W_LOOP        ;No, restart the application

MOV      AX, 6F02H     ;disable Watchdog Timer
MOV      BL, 0         ;
INT      15H

```

;

**; EXIT ;**

Appendix

**G**

# Hazardous Materials Disclosure

---

## HPCIE-Q170 Half-size PICMG 1.3 CPU Card

The details provided in this appendix are to ensure that the product is compliant with the Peoples Republic of China (China) RoHS standards. The table below acknowledges the presences of small quantities of certain materials in the product, and is applicable to China RoHS only.

A label will be placed on each product to indicate the estimated “Environmentally Friendly Use Period” (EFUP). This is an estimate of the number of years that these substances would “not leak out or undergo abrupt change.” This product may contain replaceable sub-assemblies/components which have a shorter EFUP such as batteries and lamps. These components will be separately marked.

Please refer to the table on the next page.

Part Name	Toxic or Hazardous Substances and Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
Housing	O	O	O	O	O	O
Display	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O
Battery	O	O	O	O	O	O

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in SJ/T11363-2006 (now replaced by GB/T 26572-2011).

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in SJ/T11363-2006 (now replaced by GB/T 26572-2011).

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有“环境友好使用期限”的标签，此期限是估算这些物质“不会有泄漏或突变”的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯 醚 (PBDE)
壳体	○	○	○	○	○	○
显示	○	○	○	○	○	○
印刷电路板	○	○	○	○	○	○
金属螺帽	○	○	○	○	○	○
电缆组装	○	○	○	○	○	○
风扇组装	○	○	○	○	○	○
电力供应组装	○	○	○	○	○	○
电池	○	○	○	○	○	○

○: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T 11363-2006 (现由 GB/T 26572-2011 取代) 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 (现由 GB/T 26572-2011 取代) 标准规定的限量要求。