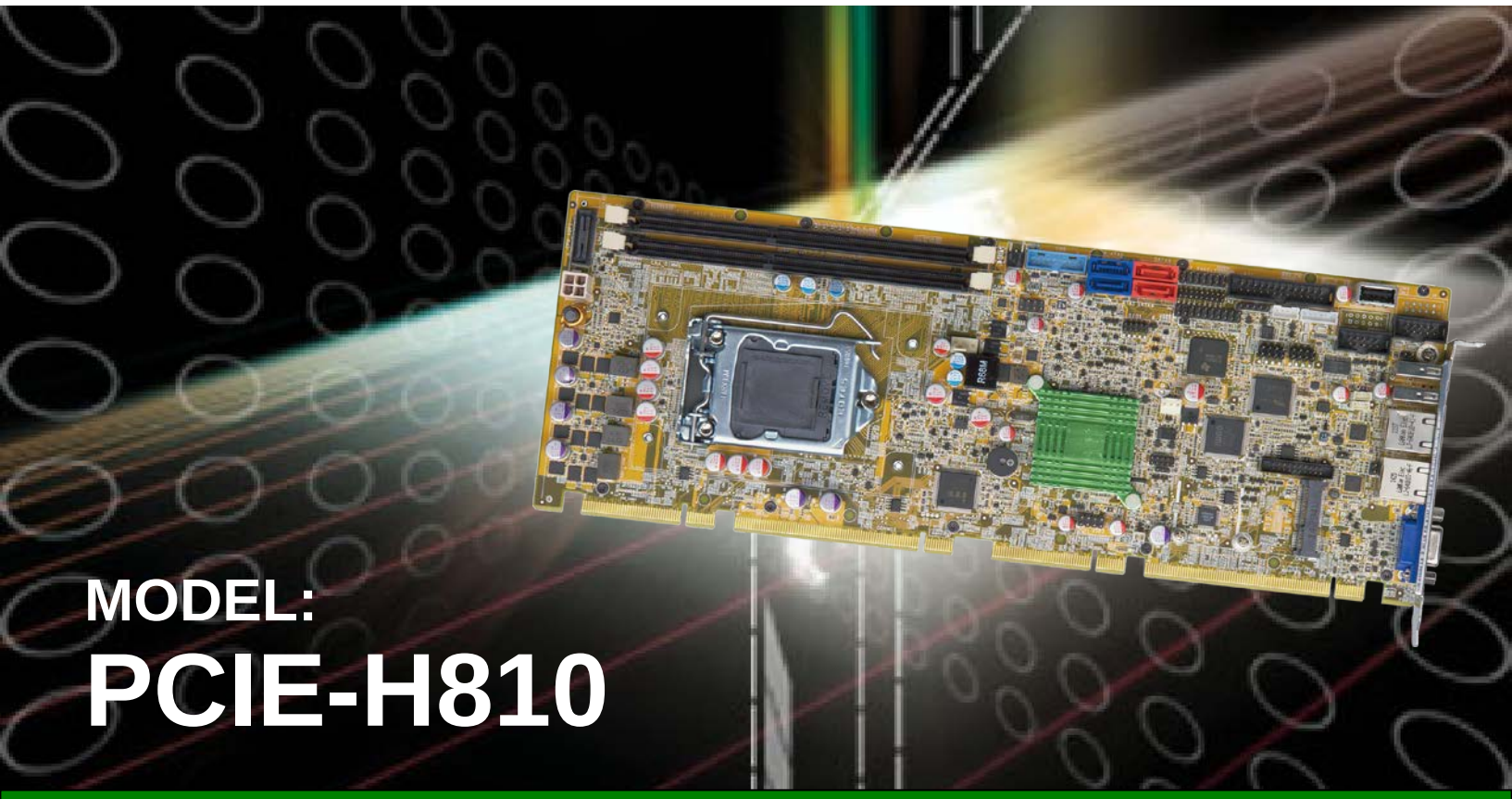
IEI Integration Corp.



MODEL:

PCIE-H810

Full-Size PICMG 1.3 CPU Card Supports 4th Generation LGA1150 Intel® Core™ i7/i5/i3, Pentium® or Celeron® CPU, Intel® H81 Chipset, DDR3, VGA, iDP, Dual PCIe GbE, SATA 6Gb/s, mSATA, RS-232, HD Audio and RoHS

User Manual

Rev. 1.02 – February 14, 2019

RoHS Lead Free

Revision

Date	Version	Changes
February 14, 2019	1.02	Modified Figure 3-27: USB 2.0 Connector Pinout Locations
December 18, 2015	1.01	Updated Section 1.6: Technical Specifications Modified Table 3-14: Internal DisplayPort Connector Pinouts
March 2, 2015	1.00	Initial release

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Manual Conventions

WARNING

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.

CAUTION

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.

NOTE

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

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Chapter

1

Introduction

1.1 Introduction

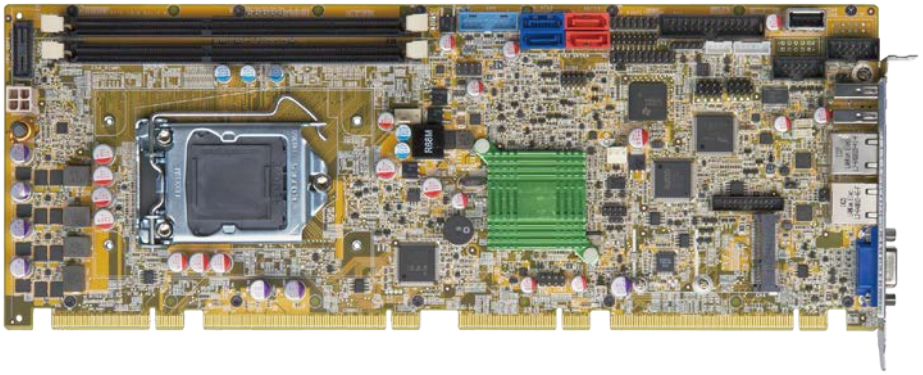


Figure 1-1: PCIE-H810

The PCIE-H810 PICMG 1.3 CPU card is a Socket LGA1150 Intel® Core™ i7/i5/i3, Pentium® or Celeron® processor platform that supports two 240-pin 1600/1333 MHz dual-channel DDR3/DDR3L DIMMs up to 16 GB.

The PCIE-H810 supports two GbE interfaces through the Realtek RTL8111E PCIe Ethernet controllers. The integrated Intel® H81 chipset supports two SATA 6Gb/s and two SATA 3Gb/s drives. In addition, the PCIE-H810 includes VGA and iDP interfaces for dual independent display.

Two USB 3.1 Gen 1 by pin header, two USB 2.0 on the rear panel, four USB 2.0 by pin header, one USB 2.0 by internal Type A connector, four USB 2.0 by backplane pin header (via golden fingers), two RS-232 and one PCIe Mini interface with mSATA support provide flexible expansion options. High Definition Audio (HDA) support ensures HDA devices can be easily implemented on the PCIE-H810.

1.2 Features

Some of the PCIE-H810 motherboard features are listed below:

- PICMG 1.3 full-size solution
- 4th generation LGA1150 Intel® Core™ i7/i5/i3, Pentium® or Celeron® processor supported
- Intel® H81 PCH

- Two 240-pin 1600/1333 MHz dual-channel DDR3/DDR3L DIMMs support up to 16 GB
- Dual independent display by VGA and iDP interfaces
- Two Realtek PCIe Gigabit Ethernet connectors
- One PCIe Mini slot with mSATA support
- Stiffener bars prevent the PCB bending and damage of components on the solder side
- TPM V1.2 hardware security function supported by the TPM module
- High Definition Audio
- RoHS compliant

1.3 Connectors

The connectors on the PCIE-H810 are shown in the figure below.

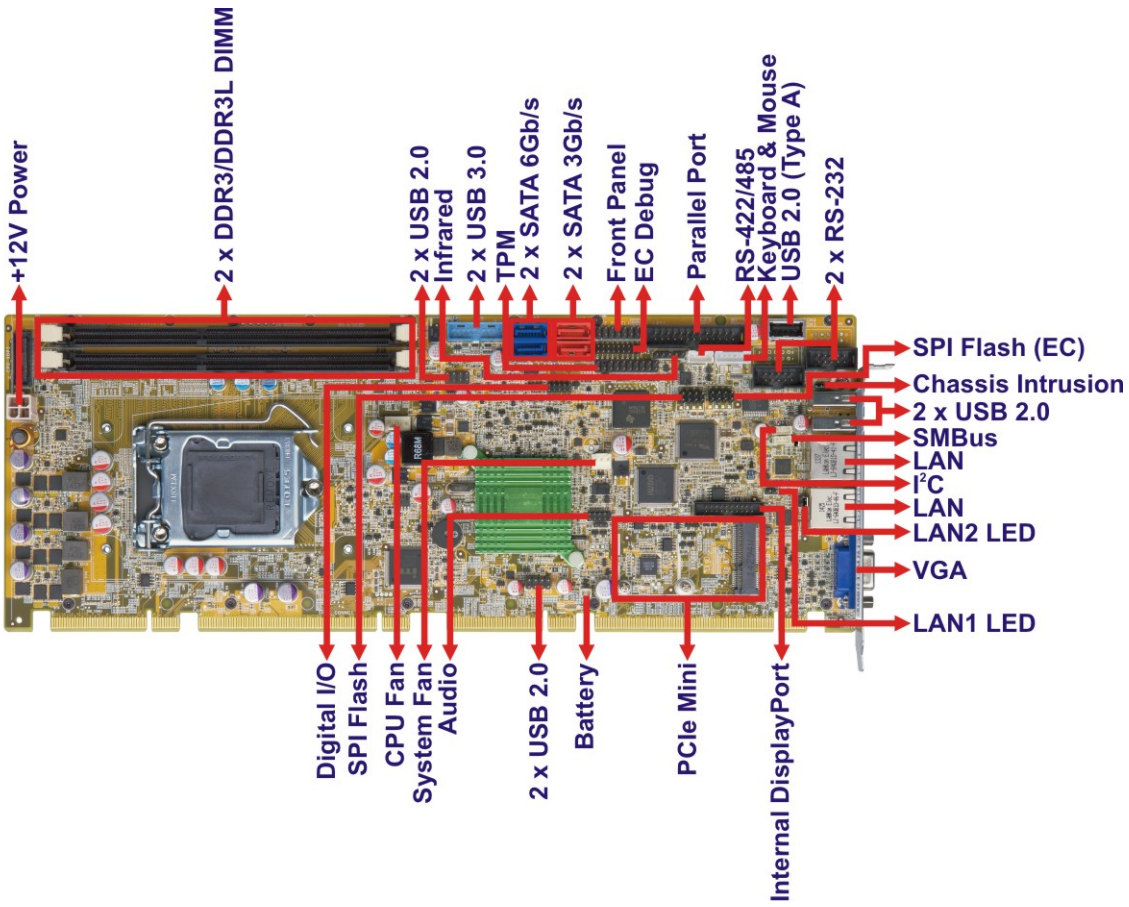


Figure 1-2: Connectors

1.4 Dimensions

The main dimensions of the PCIE-H810 are shown in the diagram below.

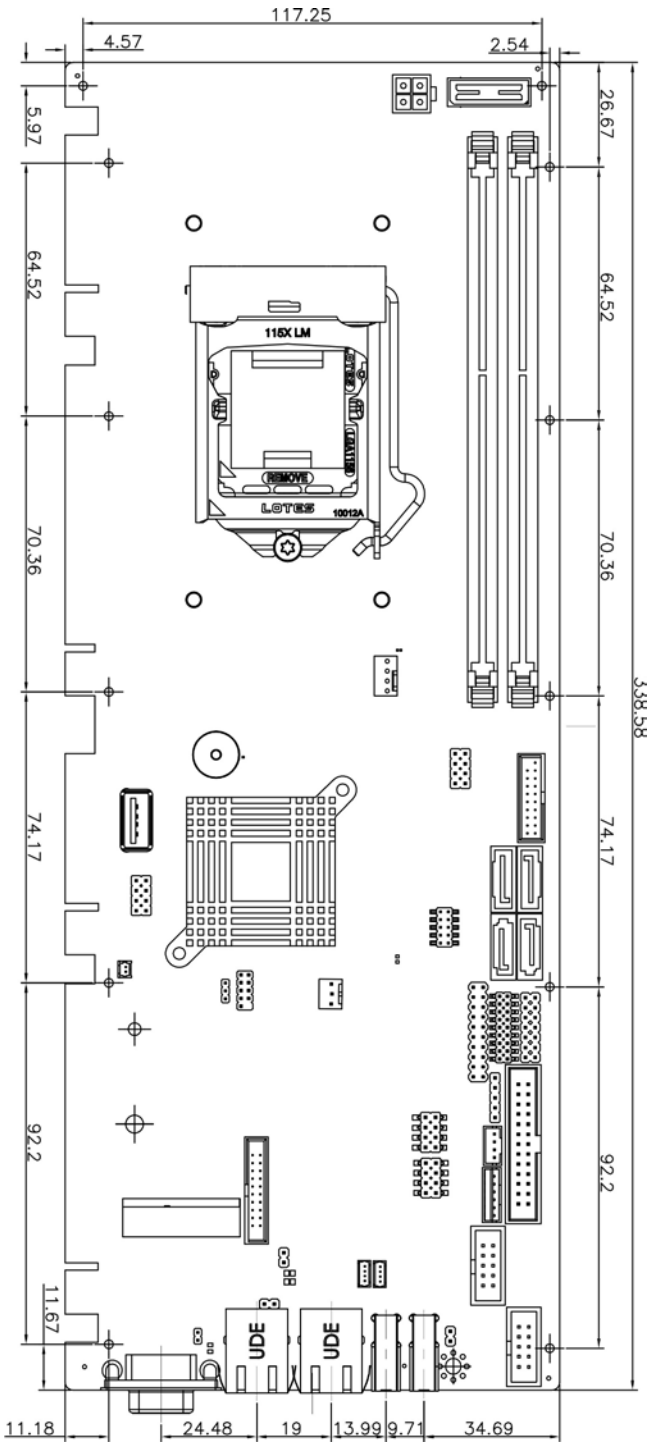


Figure 1-3: PCIE-H810 Dimensions (mm)

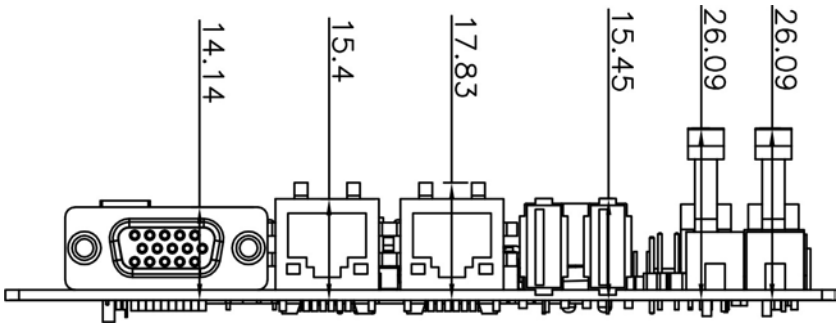


Figure 1-4: External Interface Panel Dimensions (mm)

1.5 Data Flow

Figure 1-5 shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

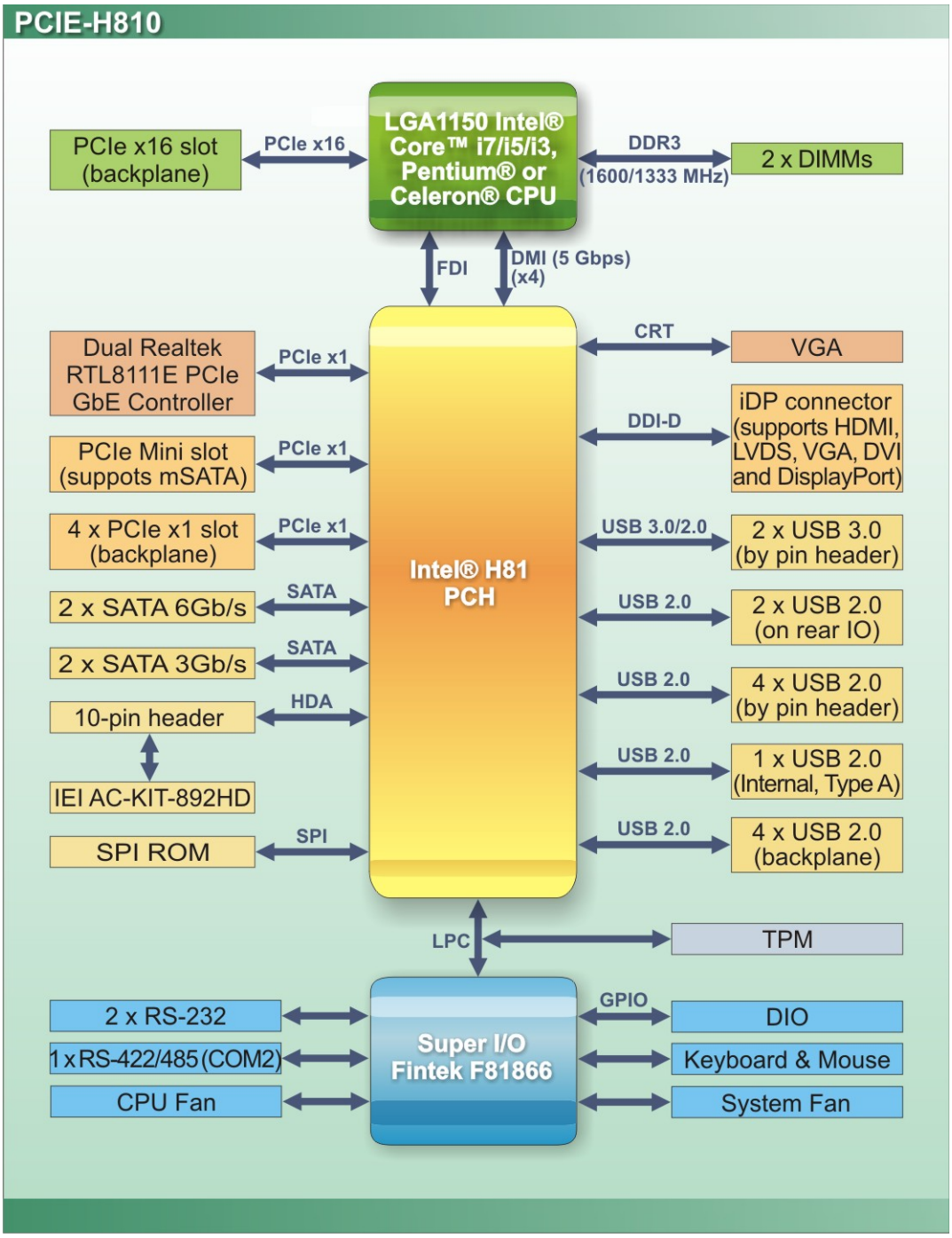


Figure 1-5: Data Flow Diagram

1.6 Technical Specifications

The PCIE-H810 technical specifications are listed below.

Specification/Model	PCIE-H810
Form Factor	PICMG 1.3
CPU Supported	4th generation LGA1150 Intel® Core™ i7/i5/i3, Pentium® or Celeron® CPU
PCH	Intel® H81
Memory	Two 240-pin 1600/1333 MHz dual-channel unbuffered DDR3/DDR3L SDRAM DIMMs support up to 16 GB
Graphics Engine	Intel® HD Graphics Gen 7.5 supports DirectX 11.1, OpenCL 1.2, OpenGL 3.2, Full MPEG2, VC1, AVC Decode
Display Output	Dual independent display One VGA (up to 1920x1200@60 Hz) One iDP interface for HDMI, LVDS, VGA, DVI and DisplayPort (up to 3840x2160@60 Hz)
Ethernet Controllers	Dual Realtek RTL8111E PCIe GbE controller
Audio	Supports 7.1 channel HD Audio by IEI AC-KIT-892HD kit
BIOS	UEFI BIOS B321APxx supports four PCIe x1 slots (default) B321ARxx supports one PCIe x4 slot
Super I/O Controller	Fintek F81866
Watchdog Timer	Software programmable supports 1~255 sec. system reset

Expansions	One PCIe Mini slot (PCIe Mini and mSATA co-lay) PCI signal by ITE IT8892 (PCIe to PCI bridge) 4 x PCI link via golden finger **16-lane PCIe link from CPU via golden finger:** Support one PCIe x16 slot on the backplane **4-lane PCIe link from PCH via golden finger:** Support either one PCIe x4 slot or four PCIe x1 slots on the backplane For installing the PCIe x4 device on the backplane, the user must update BIOS to the version which supports one PCIe x4 slot
I/O Interface Connectors	
Audio Connector	One internal audio connector (10-pin header)
Chassis Intrusion	One 2-pin header
Digital I/O	8-bit digital I/O
Ethernet	Two RJ-45 GbE ports
Fan	One 4-pin smart fan connector (CPU fan) One 3-pin smart fan connector (system fan)
Front Panel	One 14-pin header (power LED, HDD LED, speaker, power button, reset button)
I^2C	One 4-pin wafer connector
Infrared	One via 5-pin header
Keyboard and Mouse	One 6-pin wafer connector
LAN LEDs	Two 2-pin headers
Parallel Port	One parallel port via internal 26-pin box header
Serial ATA	Two SATA 6Gb/s connectors (support AHCI, no RAID) Two SATA 3Gb/s connectors (support AHCI, no RAID)
Serial Ports	Two RS-232 via internal box headers One RS-422/485 via internal 4-pin wafer connector
SMBus	One 4-pin wafer connector

TPM	One via 20-pin header
USB Ports	Two USB 3.1 Gen 1 (5 Gb/s) ports by pin header Two USB 2.0 ports on rear IO Four USB 2.0 ports by two pin headers One USB 2.0 port by internal Type A connector Four USB 2.0 ports (signal to backplane)
Environmental and Power Specifications	
Power Supply	5V/12V, AT/ATX power supported
Power Consumption	5V@3.41A , 12V@0.35A, Vcore_12V@7.52A, 3.3V@1.41A, 5VSB@0.12A (3.9 GHz Intel® Core™ i7-4770K CPU with two 4 GB 1333 MHz DDR3 memory)
Operating Temperature	-20ºC ~ 60ºC
Storage Temperature	-30ºC ~ 70ºC
Humidity	5% ~ 95% (non-condensing)
Physical Specifications	
Dimensions	338 mm x 126 mm
Weight (GW/NW)	1000 g/260 g

Table 1-1: PCIE-H810 Specifications

Chapter

2

Packing List

2.1 Anti-static Precautions

WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- ***Wear an anti-static wristband***: Wearing an anti-static wristband can prevent electrostatic discharge.
- ***Self-grounding***: Touch a grounded conductor every few minutes to discharge any excess static buildup.
- ***Use an anti-static pad***: When configuring any circuit board, place it on an anti-static mat.
- ***Only handle the edges of the PCB***: Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

2.2 Unpacking Precautions

When the PCIE-H810 is unpacked, please do the following:

- Follow the anti-static guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

2.3 Packing List

NOTE:

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the PCIE-H810 was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

The PCIE-H810 is shipped with the following components:

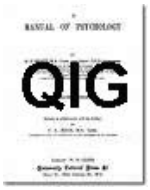
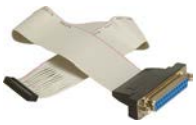
Quantity	Item and Part Number	Image
1	PCIE-H810 CPU card	
2	SATA cable	
1	Quick Installation Guide	

Table 2-1: Packing List

2.4 Optional Items

The following are optional components which may be separately purchased:

Item and Part Number	Image
Dual RS-232 cable, 230 mm, P=2.54 (**P/N**: 32205-000702-100-RS)	

Item and Part Number	Image
RS-422/485 cable, 200 mm, P=2.0 (**P/N**: 32205-003800-300-RS)	
Dual-port USB 3.1 Gen 1 cable with bracket (**P/N**: 19800-010500-200-RS)	
Dual-port USB 2.0 cable with bracket, 300 mm, P=2.54 (**P/N**: 19800-003100-300-RS)	
KB/MS cable with bracket, 220 mm, P=2.0 (**P/N**: 19800-000075-RS)	
SATA power cable (**P/N**: 32102-000100-200-RS)	
LPT flat cable, 240 mm, P=2.54 (**P/N**: 19800-000049-RS)	
LGA1150 cooler kit ,high-performance compatible, 65W (**P/N**: CF-1150SB-R11)	
LGA1150 cooler kit, 1U chassis compatible, 65W (**P/N**: CF-1150SC-R20)	
LGA1150 cooler kit, high-performance compatible, 95W (**P/N**: CF-1150SE-R10)	

Item and Part Number	Image
LGA1150 cooler kit, high-performance compatible, 54W (**P/N**: CF-1150SF-R10)	
DisplayPort to HDMI converter board (for IEI iDP connector) (**P/N**: DP-HDMI-R10)	
DisplayPort to LVDS converter board (for IEI iDP connector) (**P/N**: DP-LVDS-R10)	
DisplayPort to VGA converter board (for IEI iDP connector) (**P/N**: DP-VGA-R10)	
DisplayPort to DVI-D converter board (for IEI iDP connector) (**P/N**: DP-DVI-R10)	
DisplayPort to DisplayPort converter board (for IEI iDP connector) (**P/N**: DP-DP-R10)	
7.1-channel HD audio kit with Realtek ALC892 audio codec supporting dual audio stream (**P/N**: AC-KIT-892HD-R10)	
20-pin Infineon TPM module, software management tool, firmware v3.17 (**P/N**: TPM-IN01-R20)	

Table 2-2: Optional Items

Chapter

3

Connectors

3.1 Peripheral Interface Connectors

This chapter details all the jumpers and connectors.

3.1.1 PCIE-H810 Layout

The figures below show all the connectors and jumpers.

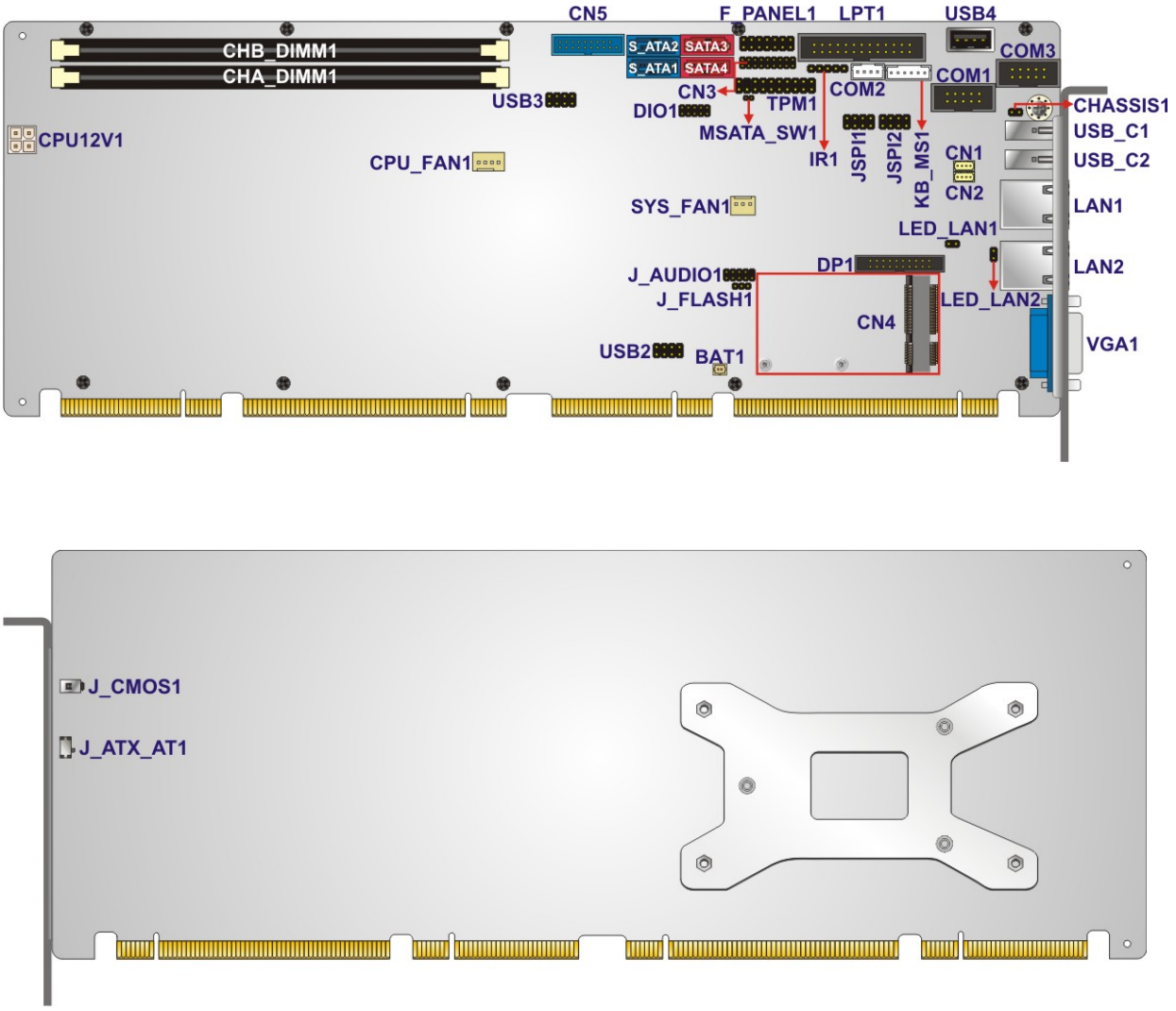


Figure 3-1: Connectors and Jumpers

3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
+12V power connector	4-pin Molex power connector	CPU12V1
Audio kit connector	10-pin header	J_AUDIO1
Battery connector	2-pin wafer	BAT1
Chassis intrusion connector	2-pin header	CHASSIS1
DDR3 DIMM sockets	240-pin socket	CHA_DIMM1 CHB_DIMM1
Digital I/O connector	10-pin header	DIO1
EC debug connector	18-pin header	CN3
Fan connector (CPU)	4-pin wafer	CPU_FAN1
Fan connector (system)	3-pin wafer	SYS_FAN1
Front panel connector	14-pin header	F_PANEL1
I^2C connector	4-pin wafer	CN1
Infrared connector	5-pin header	IR1
Internal DisplayPort connector	19-pin box header	DP1
Keyboard and mouse connector	6-pin wafer	KB_MS1
LAN LED connectors	2-pin header	LED_LAN1, LED_LAN2
Parallel port connector	26-pin box header	LPT1
PCIe Mini slot	PCIe Mini	CN4
SATA 3Gb/s drive connectors	7-pin SATA connector	SATA3, SATA4
SATA 6Gb/s drive connectors	7-pin SATA connector	S_ATA1, S_ATA2,
Serial port, RS-232	10-pin box header	COM1, COM3
Serial port, RS-422/485	4-pin wafer	COM2

Connector	Type	Label
SMBus connector	4-pin wafer	CN2
SPI flash connector	8-pin header	JSPI1
SPI flash connector (EC)	8-pin header	JSPI2
TPM connector	20-pin header	TPM1
USB 2.0 connector (Type A)	Type A	USB4
USB 2.0 connectors	8-pin header	USB2, USB3
USB 3.1 Gen 1 connector	19-pin box header	CN5

Table 3-1: Peripheral Interface Connectors

3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
Ethernet connector	RJ-45	LAN1
Ethernet connector	RJ-45	LAN2
USB 2.0 ports	USB 2.0	USB_C1, USB_C2
VGA connector	15-pin female	VGA1

Table 3-2: Rear Panel Connectors

3.2 Internal Peripheral Connectors

The section describes all of the connectors on the PCIE-H810.

3.2.1 +12V Power Connector

CN Label: **CPU12V1**

CN Type: 4-pin Molex power connector, p=4.2 mm

CN Location: See **Figure 3-2**

CN Pinouts: See **Table 3-3**

This connector provides power to the CPU.

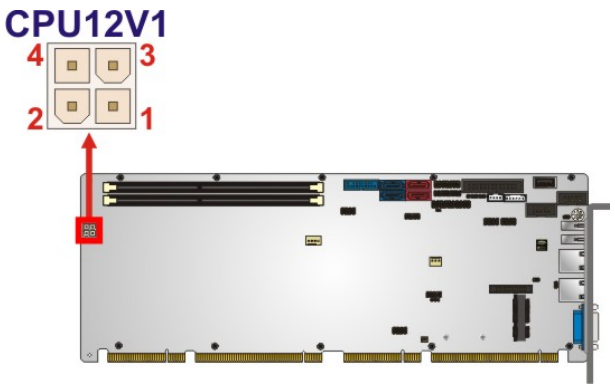


Figure 3-2: +12V Power Connector Pinout Location

Pin	Description	Pin	Description
1	GND	2	GND
3	+12V	4	+12V

Table 3-3: +12V Power Connector Pinouts

3.2.2 Audio Kit Connector

CN Label: **J_AUDIO1**

CN Type: 10-pin header, p=2 mm

CN Location: See **Figure 3-3**

CN Pinouts: See **Table 3-4**

This connector connects to an external audio kit.

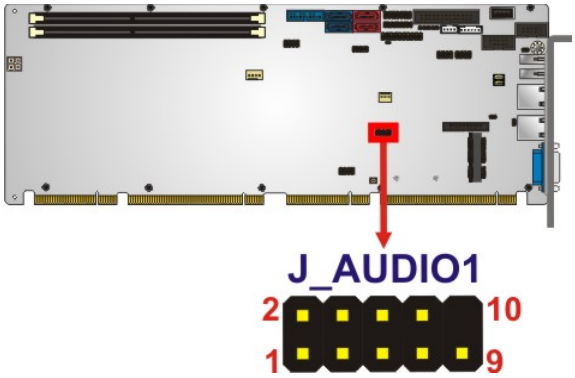


Figure 3-3: Audio Kit Connector Location

Pin	Description	Pin	Description
1	HDA_SYNC	2	HDA_BIT_CLK
3	HDA_SDOUT	4	HDA_SPKR
5	HDA_SDIN	6	HDA_RST#
7	HDA_VCC	8	HDA_GND
9	HDA_+12V	10	HDA_GND

Table 3-4: Audio Kit Connector Pinouts

3.2.3 Battery Connector

CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

CN Label:	**BAT1**
CN Type:	2-pin wafer, p=1.25 mm
CN Location:	See **Figure 3-4**
CN Pinouts:	See **Table 3-5**

This is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.

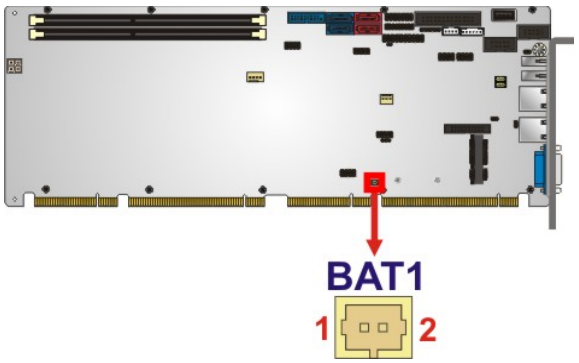


Figure 3-4: Battery Connector Location

Pin	Description
1	Battery+
2	GND

Table 3-5: Battery Connector Pinouts

3.2.4 Chassis Intrusion Connector

CN Label: **CHASSIS1**

CN Type: 2-pin header, p=2.54 mm

CN Location: See **Figure 3-5**

CN Pinouts: See **Table 3-6**

The chassis intrusion connector is for a chassis intrusion detection sensor or switch that detects if a chassis component is removed or replaced.

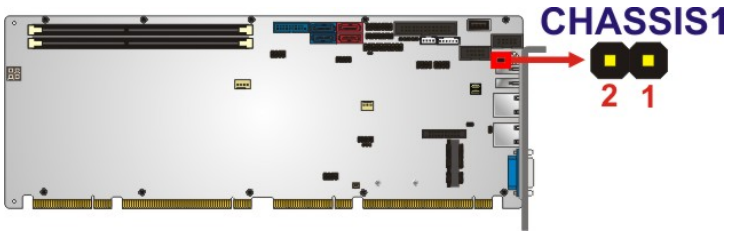


Figure 3-5: Chassis Intrusion Connector Location

Pin	Description
1	+3.3VSB
2	CHASSIS OPEN

Table 3-6: Chassis Intrusion Connector Pinouts

3.2.5 DDR3 DIMM Slots

CN Label: **CHA_DIMM1, CHB_DIMM1**

CN Type: DDR3 DIMM slot

CN Location: See **Figure 3-6**

The DIMM slots are for DDR3/DDR3L DIMM memory modules.

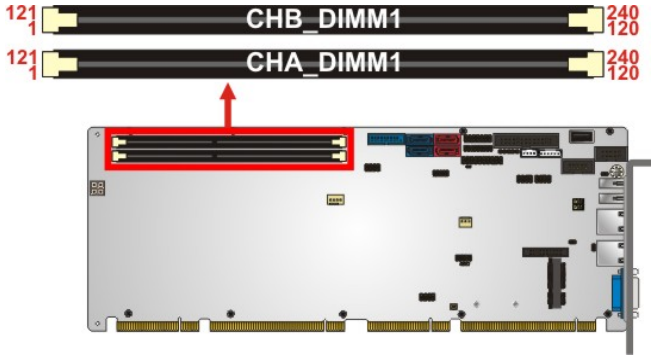


Figure 3-6: DDR3 DIMM Slot Locations

3.2.6 Digital I/O Connector

CN Label: **DIO1**

CN Type: 10-pin header, p=2 mm

CN Location: See **Figure 3-7**

CN Pinouts: See **Table 3-7**

The digital I/O connector provides programmable input and output for external devices.

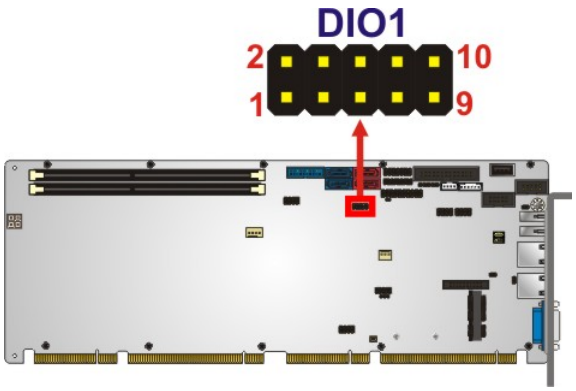


Figure 3-7: Digital I/O Connector Location

Pin	Description	Pin	Description
1	GND	2	VCC
3	Output 3	4	Output 2
5	Output 1	6	Output 0
7	Input 3	8	Input 2
9	Input 1	10	Input 0

Table 3-7: Digital I/O Connector Pinouts

3.2.7 EC Debug Connector

CN Label: **CN3**

CN Type: 18-pin header, p=2 mm

CN Location: See **Figure 3-8**

CN Pinouts: See **Table 3-8**

The EC debug connector is used for EC debug.

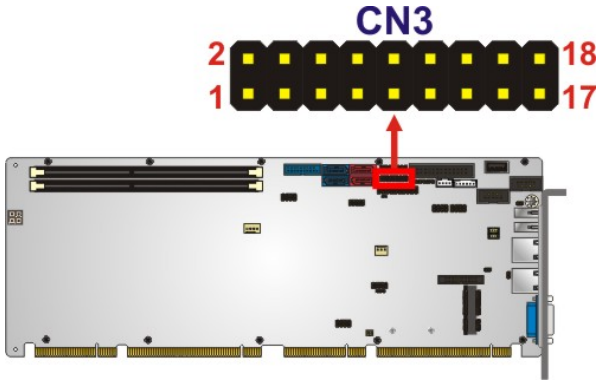


Figure 3-8: EC Debug Connector Location

Pin	Description	Pin	Description
1	EC_EPP_STB#	2	EC_EPP_AFD#
3	EC_EPP_PD0	4	NC
5	EC_EPP_PD1	6	EC_EPP_INIT#
7	EC_EPP_PD2	8	EC_EPP_SLIN#
9	EC_EPP_PD3	10	GND
11	EC_EPP_PD4	12	NC
13	EC_EPP_PD5	14	EC_EPP_BUSY
15	EC_EPP_PD6	16	EC_EPP_KSI5
17	EC_EPP_PD7	18	EC_EPP_KSI4

Table 3-8: EC Debug Connector Pinouts

3.2.8 Fan Connector (CPU)

CN Label: **CPU_FAN1**

CN Type: 4-pin wafer, p=2.54 mm

CN Location: See **Figure 3-9**

CN Pinouts: See **Table 3-9**

The fan connector attaches to a CPU cooling fan.

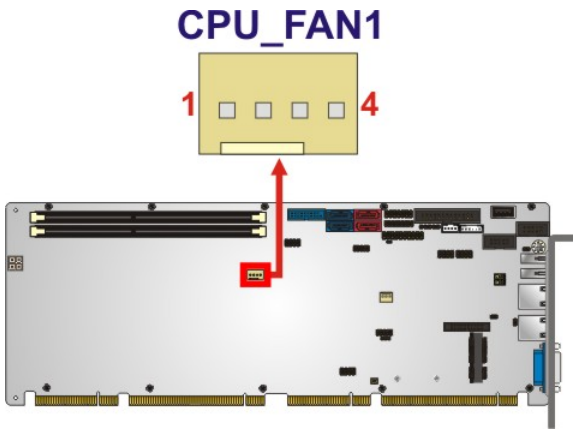


Figure 3-9: CPU Fan Connector Location

Pin	Description
1	GND
2	+12 V
3	FANIO
4	PWM

Table 3-9: CPU Fan Connector Pinouts

3.2.9 Fan Connector (System)

CN Label: **SYS_FAN1**

CN Type: 3-pin wafer, p=2.54 mm

CN Location: See **Figure 3-10**

CN Pinouts: See **Table 3-10**

The fan connector attaches to a system cooling fan.

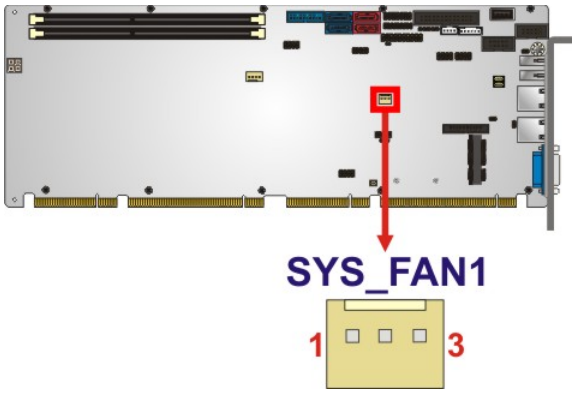


Figure 3-10: System Fan Connector Location

Pin	Description
1	FANIO
2	+12 V (PWM)
3	GND

Table 3-10: System Fan Connector Pinouts

3.2.10 Front Panel Connector

CN Label: **F_PANEL1**

CN Type: 14-pin header, p=2.54 mm

CN Location: See **Figure 3-11**

CN Pinouts: See **Table 3-11**

The front panel connector connects to the indicator LEDs and buttons on the computer's front panel.

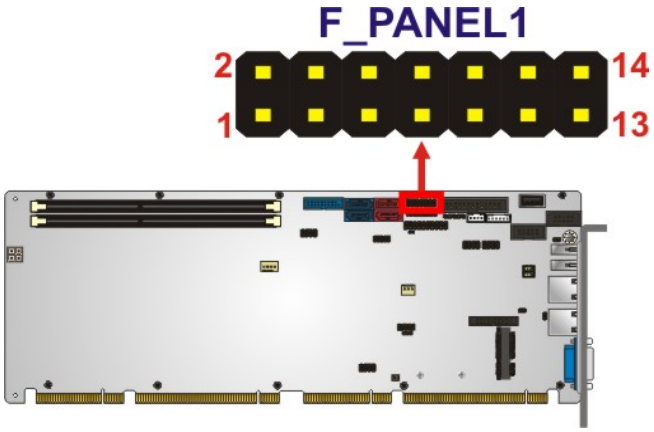


Figure 3-11: Front Panel Connector Location

Function	Pin	Description	Function	Pin	Description
Power LED	1	+5V	Speaker	2	BEEP_PWR
	3	N/C		4	N/C
	5	GND		6	N/C
Power Button	7	PWRBTN_SW#		8	PC_BEEP
	9	GND	Reset	10	N/C
HDD LED	11	+5V		12	EXTRST-
	13	SATA_LED#		14	GND

Table 3-11: Front Panel Connector Pinouts

3.2.11 I²C Connector

CN Label: **CN1**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-12**

CN Pinouts: See **Table 3-12**

The I²C connector is for system debug.

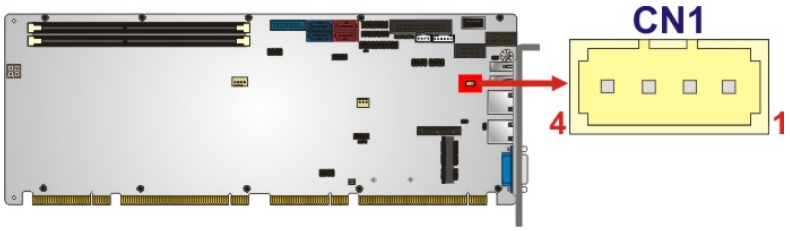


Figure 3-12: I²C Connector Location

Pin	Description
1	GND
2	I2C_DAT
3	I2C_CLK
4	+5V

Table 3-12: I2C Connector Pinouts

3.2.12 Infrared Connector

CN Label: **IR1**

CN Type: 5-pin header, p=2.54 mm

CN Location: See **Figure 3-13**

CN Pinouts: See **Table 3-13**

The infrared connector attaches to an infrared receiver for use with remote controls.

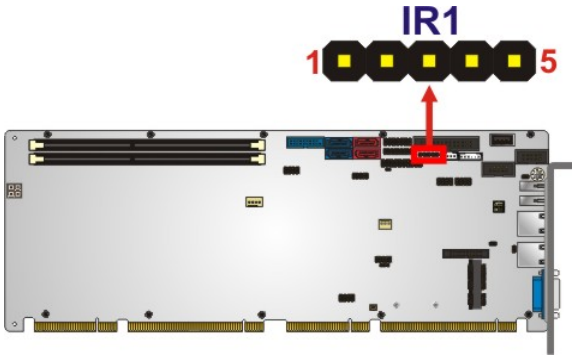


Figure 3-13: Infrared Connector Location

Pin	Description
1	+V5S
2	NC
3	IR-RX
4	GND
5	IR-TX

Table 3-13: Infrared Connector Pinouts

3.2.13 Internal DisplayPort Connector

CN Label: **DP1**

CN Type: 19-pin box header, p=2 mm

CN Location: See **Figure 3-14**

CN Pinouts: See **Table 3-14**

The DisplayPort connector supports HDMI, LVDS, VGA, DVI and DisplayPort graphics interfaces with up to 3840x2160 resolutions.

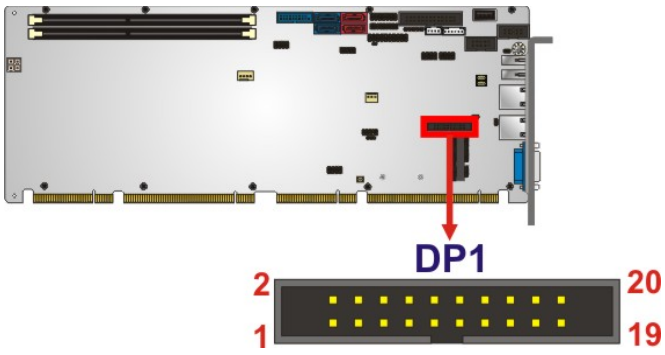


Figure 3-14: Internal DisplayPort Connector Location

Pin	Description	Pin	Description
1	HPD	11	LANE3N
2	AUXP	12	GND
3	GND	13	GND
4	AUXN	14	LANE0P
5	AUX_CTRL_DET_D	15	LANE1P
6	GND	16	LANE0N
7	GND	17	LANE1N
8	LANE2P	18	+3.3V
9	LANE3P	19	+5V
10	LANE2N	20	N/A

Table 3-14: Internal DisplayPort Connector Pinouts

3.2.14 Keyboard and Mouse Connector

CN Label: **KB_MS1**

CN Type: 6-pin wafer, p=2 mm

CN Location: See **Figure 3-15**

CN Pinouts: See **Table 3-15**

The keyboard/mouse connector connects to a PS/2 Y-cable that can be connected to a PS/2 keyboard and mouse.

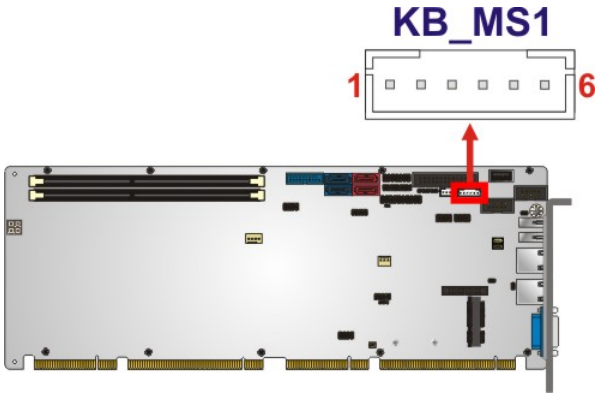


Figure 3-15: Keyboard and Mouse Connector Location

Pin	Description
1	+5 VCC
2	Mouse Data
3	Mouse Clock
4	Keyboard Data
5	Keyboard Clock
6	GROUND

Table 3-15: Keyboard and Mouse Connector Pinouts

3.2.15 LAN LED Connectors

CN Label: **LED_LAN1, LED_LAN2**

CN Type: 2-pin header, p=2.54 mm

CN Location: See **Figure 3-16**

CN Pinouts: See **Table 3-16** and **Table 3-17**

The LAN LED connectors are used to connect to the LAN LED indicators on the chassis to indicate users the link activities of the two LAN ports.

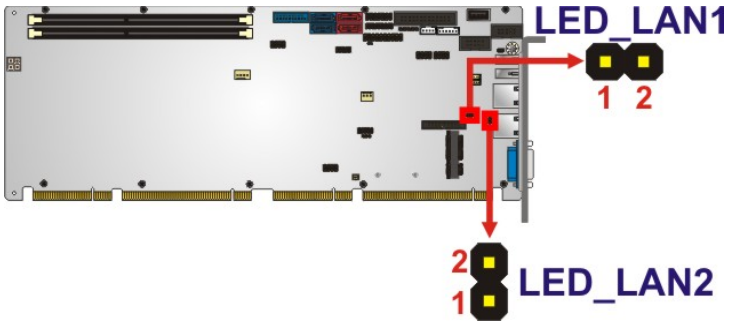


Figure 3-16: LAN LED Connector Locations

Pin	Description
1	+3.3V
2	LAN1_LED_LINK#_ACT

Table 3-16: LAN1 LED Connector (LED_LAN1) Pinouts

Pin	Description
1	+3.3V
2	LAN2_LED_LINK#_ACT

Table 3-17: LAN2 LED Connector (LED_LAN2) Pinouts

3.2.16 Parallel Port Connector

CN Label: **LPT1**

CN Type: 26-pin box header, p=2.54 mm

CN Location: See **Figure 3-17**

CN Pinouts: See **Table 3-18**

The parallel port connector connects to a parallel port connector interface or some other parallel port device such as a printer.

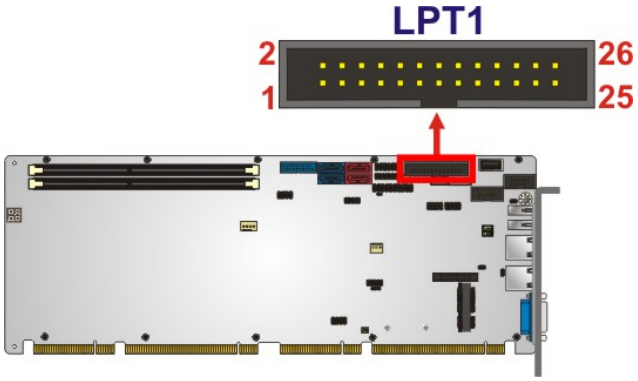


Figure 3-17: Parallel Port Connector Location

Pin	Description	Pin	Description
1	STB	2	AFD
3	PPD0	4	ERROR
5	PPD1	6	INIT
7	PPD2	8	SLIN
9	PPD3	10	GND
11	PPD4	12	GND
13	PPD5	14	GND
15	PPD6	16	GND
17	PPD7	18	GND
19	ACK	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT		

Table 3-18: Parallel Port Connector Pinouts

3.2.17 PCIe Mini Slot

CN Label: **CN4**

CN Type: PCIe Mini slot

CN Location: See **Figure 3-18**

CN Pinouts: See **Table 3-19**

The PCIe Mini slot is for installing a full-size or half-size PCIe Mini expansion card.

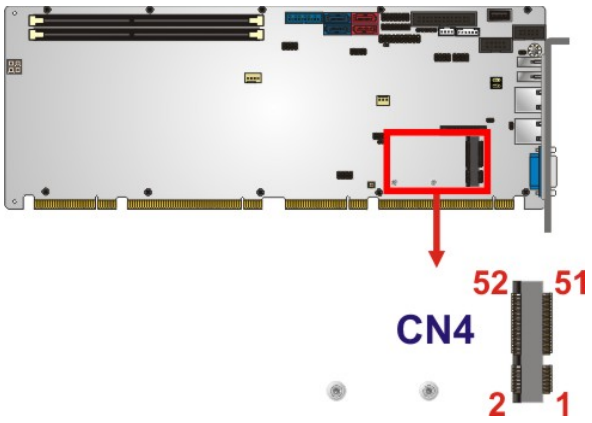


Figure 3-18: PCIe Mini Slot Location

Pin	Description	Pin	Description
1	PCIE_WAKE#	2	+3.3V
3	N/C	4	GND
5	N/C	6	1.5V
7	N/C	8	N/C
9	GND	10	N/C
11	MSATA_CLK#	12	N/C
13	MSATA _CLK	14	N/C
15	GND	16	N/C
17	PLTRST_N	18	GND
19	N/C	20	+3.3V
21	GND	22	PLTRST_N
23	SATA_RX+	24	+3.3V
25	SATA_RX-	26	GND

Pin	Description	Pin	Description
27	GND	28	1.5V
29	GND	30	SMB_CLK
31	SATA_TX-	32	SMB_DATA
33	SATA_TX+	34	GND
35	GND	36	USB_DATA-
37	GND	38	USB_DATA+
39	+3.3V	40	GND
41	+3.3V	42	N/C
43	+3.3V	44	N/C
45	CLINK_CLK	46	N/C
47	CLINK_DATA	48	1.5V
49	CLINK_RST#	50	GND
51	MSATA_DET	52	+3.3V

Table 3-19: PCIe Mini Slot Pinouts

3.2.18 SATA 3Gb/s Drive Connectors

CN Label: **SATA3, SATA4**

CN Type: 7-pin SATA drive connector

CN Location: See **Figure 3-19**

CN Pinouts: See **Table 3-20**

The SATA drive connectors can be connected to SATA drives and support up to 3Gb/s data transfer rate.

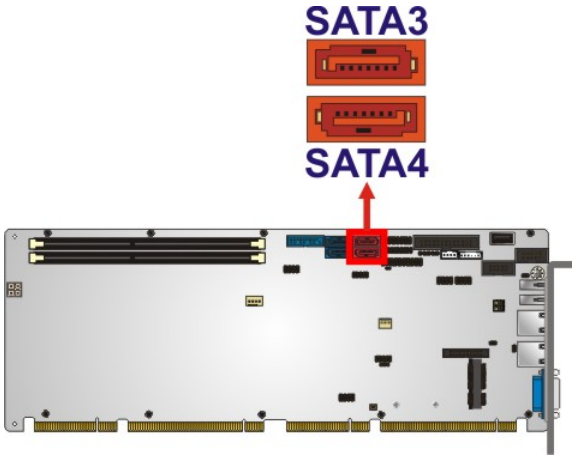


Figure 3-19: SATA 3Gb/s Drive Connector Location

Pin	Description	Pin	Description
1	GND	2	TX+
3	TX-	4	GND
5	RX-	6	RX+
7	GND		

Table 3-20: SATA 3Gb/s Drive Connector Pinouts

3.2.19 SATA 6Gb/s Drive Connectors

CN Label: **S_ATA1, S_ATA2**

CN Type: 7-pin SATA drive connector

CN Location: See **Figure 3-20**

CN Pinouts: See **Table 3-21**

The SATA drive connectors can be connected to SATA drives and support up to 6Gb/s data transfer rate.

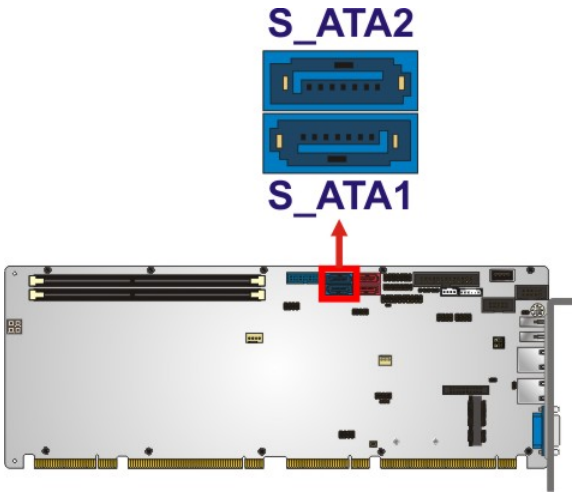


Figure 3-20: SATA 6Gb/s Drive Connector Location

Pin	Description	Pin	Description
1	GND	2	TX+
3	TX-	4	GND
5	RX-	6	RX+
7	GND		

Table 3-21: SATA 6Gb/s Drive Connector Pinouts

3.2.20 Serial Port Connectors, RS-232

CN Label: **COM1, COM3**

CN Type: 10-pin box header, p=2.54 mm

CN Location: See **Figure 3-21**

CN Pinouts: See **Table 3-22**

Each of these connectors provides RS-232 connections.

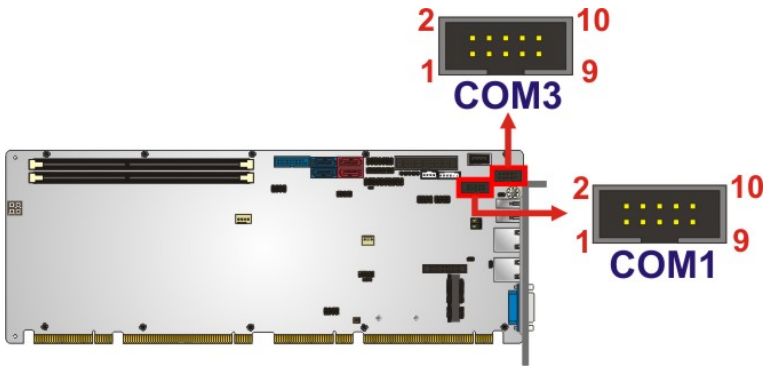


Figure 3-21: Serial Port Connector Location

Pin	Description	Pin	Description
1	DCD	2	DSR
3	RXD	4	RTS
5	TXD	6	CTS
7	DTR	8	RI
9	GND	10	N/C

Table 3-22: Serial Port Connector Pinouts

3.2.21 Serial Port Connector, RS-422/485

CN Label: **COM2**

CN Type: 4-pin wafer, p=2 mm

CN Location: See **Figure 3-22**

CN Pinouts: See **Table 3-23**

This connector provides RS-422 or RS-485 communications.

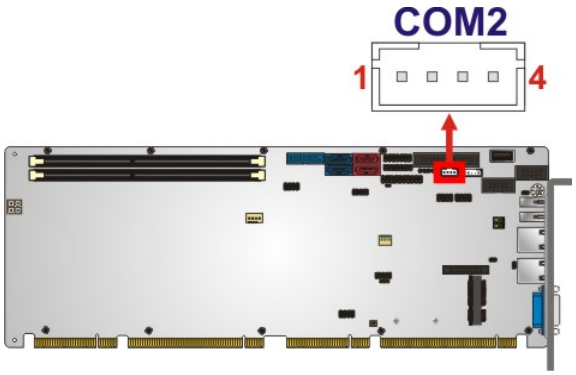


Figure 3-22: RS-422/485 Connector Location

Pin	Description
1	RXD422-
2	RXD422+
3	TXD422+/TXD485+
4	TXD422-/TXD485-

Table 3-23: RS-422/485 Connector Pinouts

Use the optional RS-422/485 cable to connect to a serial device. The pinouts of the DB-9 connector are listed below.

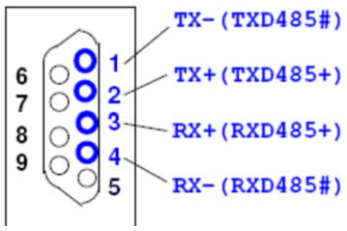
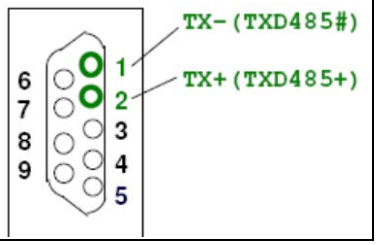
RS-422 Pinouts	RS-485 Pinouts
	

Table 3-24: DB-9 RS-422/485 Pinouts

3.2.22 SMBus Connector

CN Label: **CN2**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-23**

CN Pinouts: See **Table 3-25**

The SMBus (System Management Bus) connector provides low-speed system management communications.

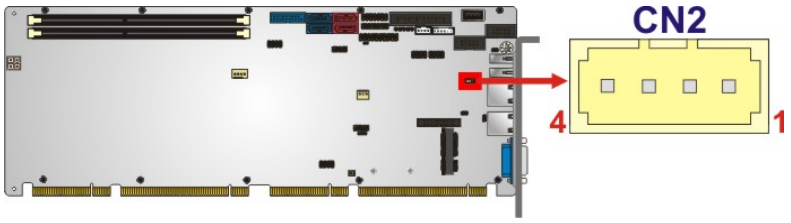


Figure 3-23: SMBus Connector Location

Pin	Description
1	GND
2	SMB_DATA
3	SMB_CLK
4	+5V

Table 3-25: SMBus Connector Pinouts

3.2.23 SPI Flash Connector

CN Label: **JSPI1**

CN Type: 8-pin header, p=2.54 mm

CN Location: See **Figure 3-24**

CN Pinouts: See **Table 3-26**

The SPI flash connector is used to flash the BIOS.

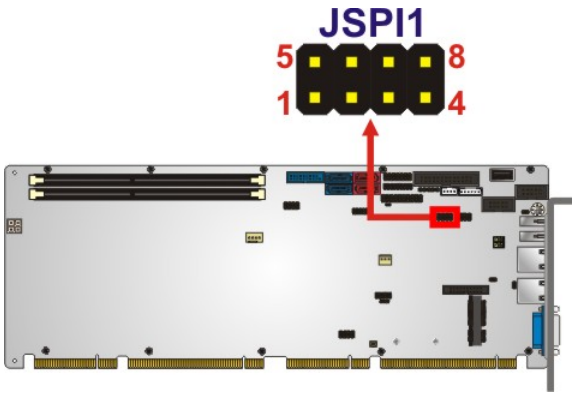


Figure 3-24: SPI Flash Connector Location

Pin	Description	Pin	Description
1	+3.3V	2	SPI_CS#
3	SPI_SO	4	NC
5	GND	6	SPI_CLK
7	SPI_SI	8	NC

Table 3-26: SPI Flash Connector Pinouts

3.2.24 SPI Flash Connector (EC)

CN Label: **JSPI2**

CN Type: 8-pin header, p=2.54 mm

CN Location: See **Figure 3-25**

CN Pinouts: See **Table 3-27**

The SPI flash connector is used to flash the EC ROM.

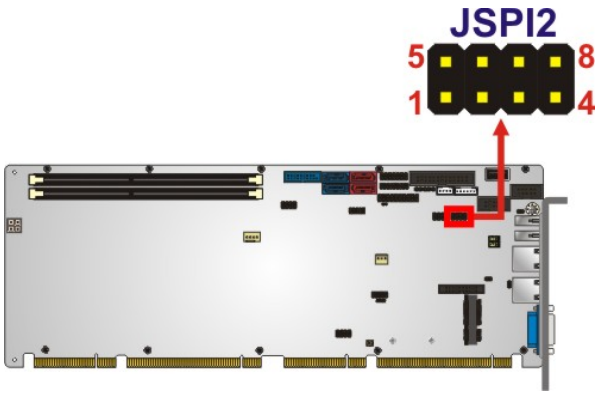


Figure 3-25: SPI EC Flash Connector Location

Pin	Description	Pin	Description
1	+3.3V	2	SPI_CS#
3	SPI_SO	4	NC
5	GND	6	SPI_CLK
7	SPI_SI	8	NC

Table 3-27: SPI EC Flash Connector Pinouts

3.2.25 TPM Connector

CN Label: **TPM1**

CN Type: 20-pin header, p=2.54 mm

CN Location: See **Figure 3-26**

CN Pinouts: See **Table 3-28**

The TPM connector connects to a TPM module.

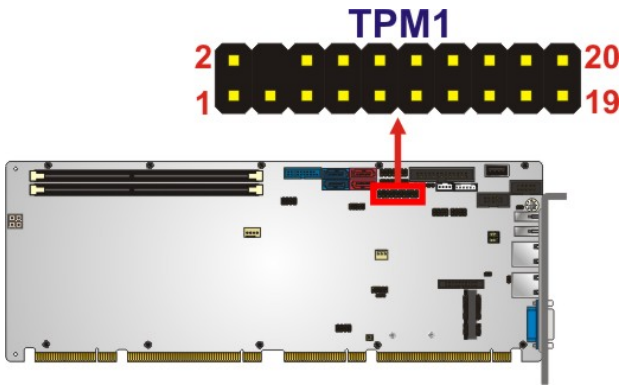


Figure 3-26: TPM Connector Location

Pin	Description	Pin	Description
1	LCLK	2	GND
3	LFRAME#	4	KEY
5	LRERST#	6	+5V
7	LAD3	8	LAD2
9	+3.3V	10	LAD1
11	LAD0	12	GND
13	SCL	14	SDA
15	SB3V	16	SERIRQ
17	GND	18	GLKRUN#
19	LPCPD#	20	LDRQ#

Table 3-28: TPM Connector Pinouts

3.2.26 USB 2.0 Connectors

CN Label:	**USB2, USB3**
CN Type:	8-pin header, p=2.54 mm
CN Location:	See **Figure 3-27**
CN Pinouts:	See **Table 3-29**

The USB 2.0 connectors connect to USB 2.0/1.1 devices. Each pin header provides two USB 2.0 ports.

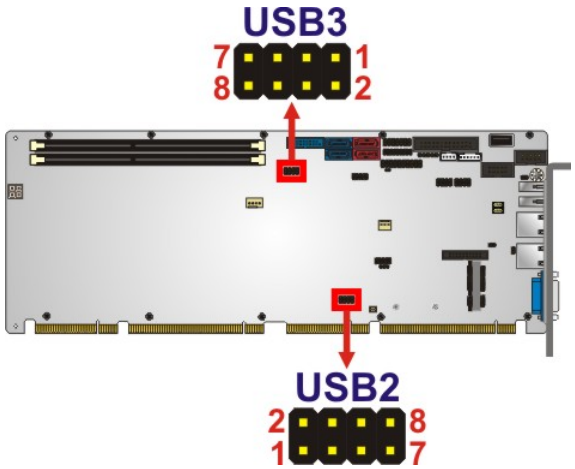


Figure 3-27: USB 2.0 Connector Pinout Locations

Pin	Description	Pin	Description
1	VCC	2	GND
3	DATA-	4	DATA+
5	DATA+	6	DATA-
7	GND	8	VCC

Table 3-29: USB 2.0 Connector Pinouts

3.2.27 USB 2.0 Connector (Type A)

CN Label: **USB4**

CN Type: USB Type A

CN Location: See **Figure 3-28**

CN Pinouts: See **Table 3-30**

The USB Type A connector connects to a USB 2.0/1.1 device.

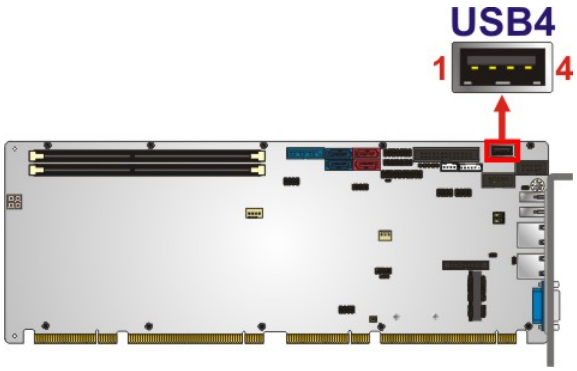


Figure 3-28: USB 2.0 Connector (Type A) Pinout Location

Pin	Description
1	VCC
2	DATA-
3	DATA+
4	GROUND

Table 3-30: USB 2.0 Connector (Type A) Pinouts

3.2.28 USB 3.1 Gen 1 Connector

CN Label: **CN5**

CN Type: 19-pin box header, p=2 mm

CN Location: See **Figure 3-29**

CN Pinouts: See **Table 3-31**

The USB 3.1 Gen 1 (5 Gb/s) connector connects to USB 3.1 Gen 1 devices. This connector provides two USB 3.1 Gen 1 ports.

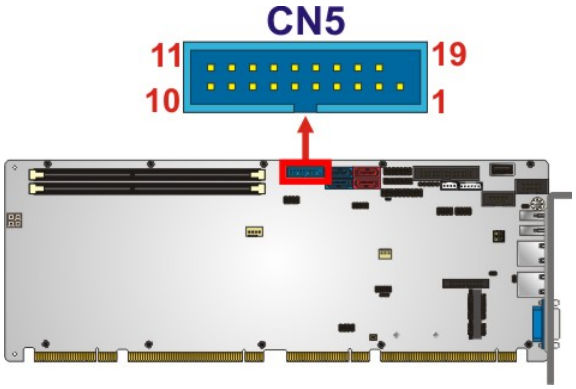


Figure 3-29: USB 3.1 Gen 1 Connector Location

Pin	Description	Pin	Description
1	VCC	11	USB_DATA+
2	USB3_RX-	12	USB_DATA-
3	USB3_RX+	13	GND
4	GND	14	USB3_TX+
5	USB3_TX-	15	USB3_TX-
6	USB3_TX+	16	GND
7	GND	17	USB3_RX+
8	USB_DATA-	18	USB3_RX-
9	USB_DATA+	19	VCC
10	NC		

Table 3-31: USB 3.1 Gen 1 Connector Pinouts

3.3 External Peripheral Interface Connector Panel

The figure below shows the external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

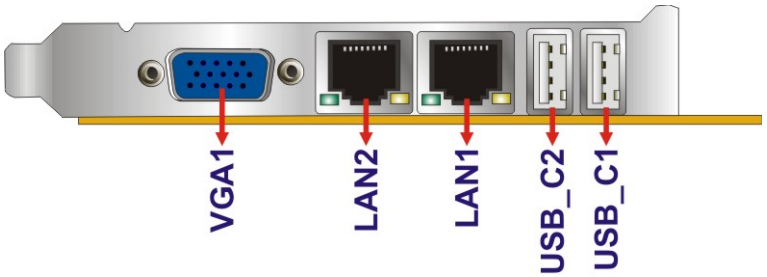


Figure 3-30: External Peripheral Interface Connector

3.3.1 Ethernet Connectors

CN Label: **LAN1** and **LAN2**

CN Type: RJ-45

CN Location: See **Figure 3-30**

CN Pinouts: See **Figure 3-31** and **Table 3-32**

The PCIE-H810 is equipped with two built-in RJ-45 Ethernet controllers. Each controller can connect to the LAN through one RJ-45 LAN connector.

Pin	Description	Pin	Description
1	MDIA3-	5	MDIA2+
2	MDIA3+	6	MDIA1+
3	MDIA1-	7	MDIA0-
4	MDIA2-	8	MDIA0+

Table 3-32: LAN Pinouts

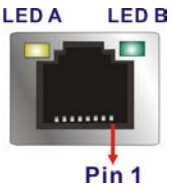


Figure 3-31: Ethernet Connector

LED	Description	LED	Description
A	on: linked blinking: data is being sent/received	B	off: 10 Mb/s green: 100 Mb/s orange: 1000 Mb/s

Table 3-33: Connector LEDs

3.3.2 USB 2.0 Connectors

CN Label: **USB_C1** and **USB_C2**

CN Type: USB port

CN Location: See **Figure 3-30**

CN Pinouts: See **Table 3-34**

The PCIE-H810 has two external USB 2.0 ports. The ports connect to both USB 2.0 and USB 1.1 devices.

Pin	Description
1	VCC
2	DATA-
3	DATA+
4	GROUND

Table 3-34: USB 2.0 Port Pinouts

3.3.3 VGA Connector

CN Label: **VGA1**

CN Type: 15-pin female

CN Location: See **Figure 3-30**

CN Pinouts: See **Figure 3-32** and **Table 3-35**

The VGA connector connects to a monitor that accepts a standard VGA input.

Pin	Description	Pin	Description
1	RED	2	GREEN
3	BLUE	4	NC
5	GND	6	GND
7	GND	8	GND
9	VCC	10	GND
11	NC	12	DDCDA
13	HSYNC	14	VSYNC
15	DDCCLK		

Table 3-35: VGA Connector Pinouts

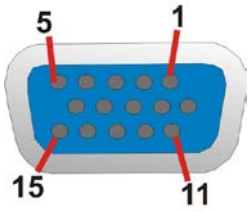


Figure 3-32: VGA Connector

Chapter

4

Installation

4.1 Anti-static Precautions

WARNING:

Failure to take ESD precautions during the installation of the PCIE-H810 may result in permanent damage to the PCIE-H810 and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the PCIE-H810. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the PCIE-H810 or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband***: - Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding***:- Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad***: When configuring the PCIE-H810, place it on an anti-static pad. This reduces the possibility of ESD damaging the PCIE-H810.
- ***Only handle the edges of the PCB***:-: When handling the PCB, hold the PCB by the edges.

4.2 Installation Considerations

NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

WARNING:

The installation instructions described in this manual should be carefully followed in order to prevent damage to the components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  - The user manual provides a complete description of the PCIE-H810 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the PCIE-H810 on an anti-static pad:
  - When installing or configuring the motherboard, place it on an anti-static pad. This helps to prevent potential ESD damage.
- Turn all power to the PCIE-H810 off:
  - When working with the PCIE-H810, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the PCIE-H810 **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

4.3 Socket LGA1150 CPU Installation

WARNING:

CPUs are expensive and sensitive components. When installing the CPU please be careful not to damage it in anyway. Make sure the CPU is installed properly and ensure the correct cooling kit is properly installed.

DO NOT touch the pins at the bottom of the CPU. When handling the CPU, only hold it on the sides.

To install the CPU, follow the steps below.

Step 1: **Disengage the load lever** by pressing the lever down and slightly outward to clear the retention tab. Fully open the lever. See **Figure 4-1**.

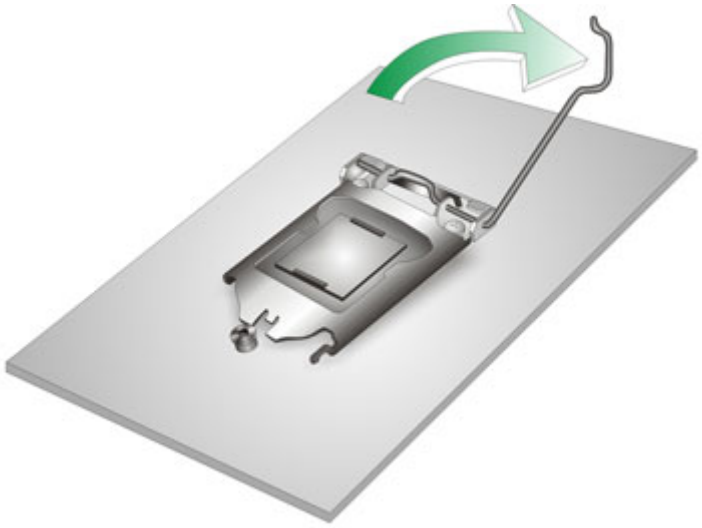


Figure 4-1: Disengage the CPU Socket Load Lever

Step 2: **Open the socket and remove the protective cover.** The black protective cover can be removed by pulling up on the tab labeled "Remove". See **Figure 4-2**.

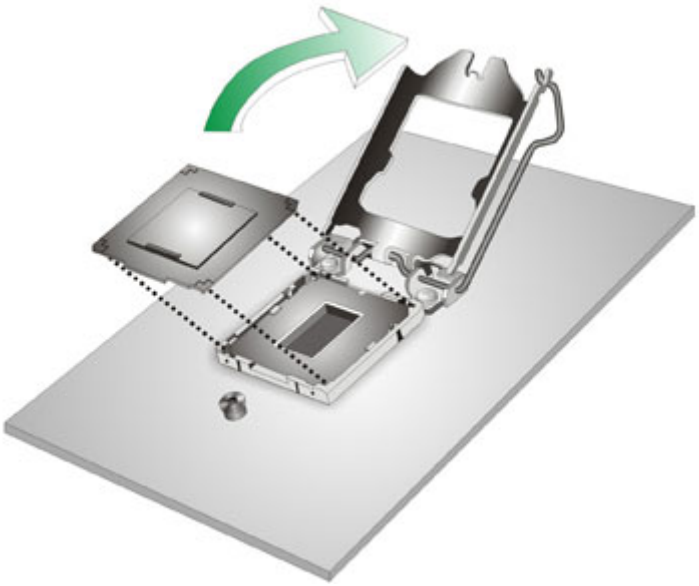


Figure 4-2: Remove Protective Cover

Step 3: **Inspect the CPU socket.** Make sure there are no bent pins and make sure the socket contacts are free of foreign material. If any debris is found, remove it with compressed air.

Step 4: **Orientate the CPU properly.** The contact array should be facing the CPU socket.

Step 5: **Correctly position the CPU.** Match the Pin 1 mark with the cut edge on the CPU socket.

Step 6: **Align the CPU pins.** Locate pin 1 and the two orientation notches on the CPU. Carefully match the two orientation notches on the CPU with the socket alignment keys.

Step 7: **Insert the CPU.** Gently insert the CPU into the socket. If the CPU pins are properly aligned, the CPU should slide into the CPU socket smoothly. See **Figure 4-3**.

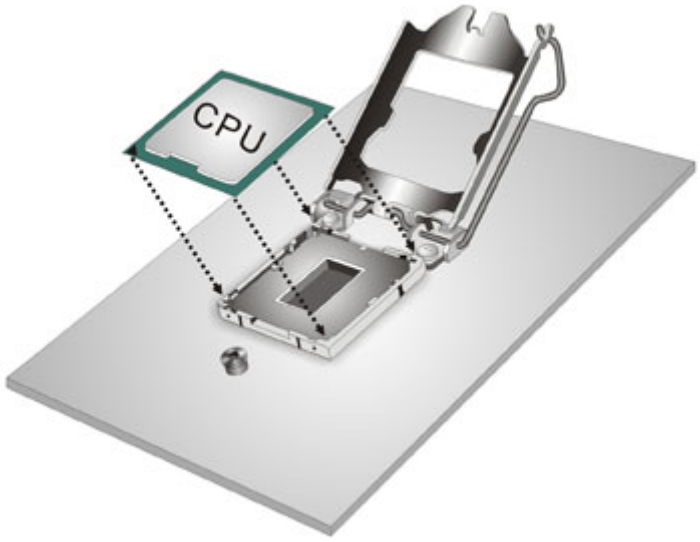


Figure 4-3: Insert the Socket LGA1150 CPU

Step 8: **Close the CPU socket.** Close the load plate and pull the load lever back a little to have the load plate be able to secure to the knob. Engage the load lever by pushing it back to its original position (**Figure 4-4**). There will be some resistance, but will not require extreme pressure.

Figure 4-4: Close the Socket LGA1150

Step 9: **Connect the 12 V power to the board.** Connect the 12 V power from the power supply to the board.

4.4 Socket LGA1150 Cooling Kit Installation

The cooling kit can be bought from IEI. The cooling kit has a heatsink and fan.

WARNING:

Do not wipe off (accidentally or otherwise) the pre-sprayed layer of thermal paste on the bottom of the heat sink. The thermal paste between the CPU and the heat sink is important for optimum heat dissipation.

To install the cooling kit, follow the instructions below.

Step 1: A cooling kit bracket is pre-installed on the rear of the motherboard. See **Figure 4-5.**

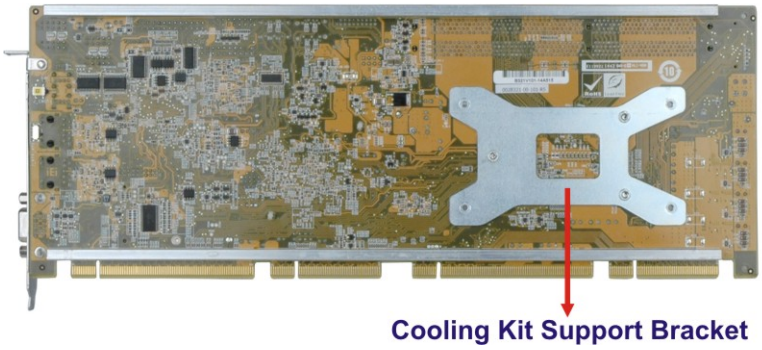


Figure 4-5: Cooling Kit Support Bracket

Step 2: **Place the cooling kit onto the socket LGA1150 CPU**. Make sure the CPU cable can be properly routed when the cooling kit is installed.

Step 3: **Mount the cooling kit**. Gently place the cooling kit on top of the CPU. Make sure the four threaded screws on the corners of the cooling kit properly pass through the holes of the cooling kit bracket.

Step 4: **Secure the cooling kit** by fastening the four retention screws of the cooling kit.

Step 5: **Connect the fan cable**. Connect the cooling kit fan cable to the fan connector on the PCIE-H810. Carefully route the cable and avoid heat generating chips and fan blades.

4.5 DIMM Installation

To install a DIMM, please follow the steps below and refer to **Figure 4-6**.

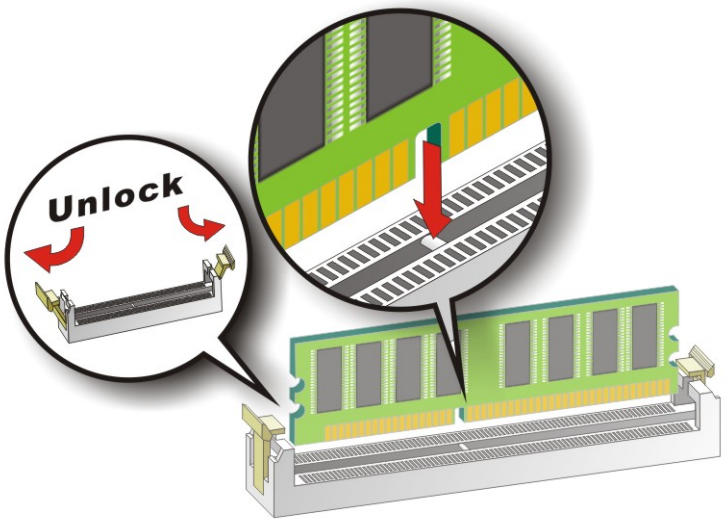


Figure 4-6: DIMM Installation

Step 1: **Open the DIMM socket handles**. Open the two handles outwards as far as they can. See **Figure 4-6**.

Step 2: **Align the DIMM with the socket**. Align the DIMM so the notch on the memory lines up with the notch on the memory socket. See **Figure 4-6**.

Step 3: **Insert the DIMM**. Once aligned, press down until the DIMM is properly seated. Clip the two handles into place. See **Figure 4-6**.

Step 4: **Removing a DIMM**. To remove a DIMM, push both handles outward. The memory module is ejected by a mechanism in the socket.

4.6 Full-size PCIe Mini Card Installation

The PCIe Mini slot allows installation of either a full-size or half-size PCIe Mini card. To install a full-size PCIe Mini card, please follow the steps below.

Step 1: **Locate the PCIe Mini slot**. See **Figure 3-18**.

Step 2: **Remove the retention screw and standoff for a half-size PCIe Mini card**. To avoid interference of the board circuit, remove the retention screw and standoff for a half-size PCIe Mini card as shown in **Figure 4-7**.

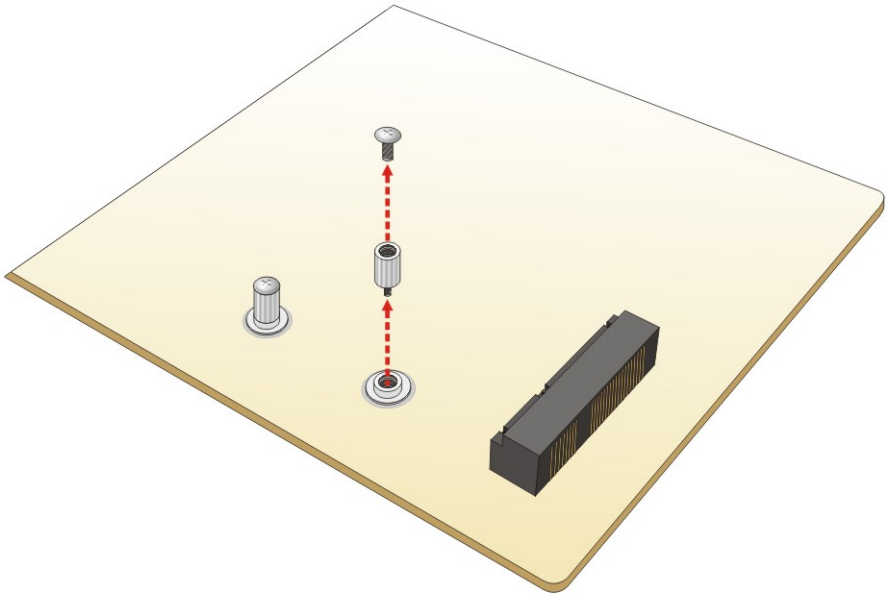


Figure 4-7: Removing the Retention Screw and Standoff for a Half-size PCIe Mini Card

Step 3: **Remove the retention screw**. Remove the retention screw as shown in **Figure 4-8**.

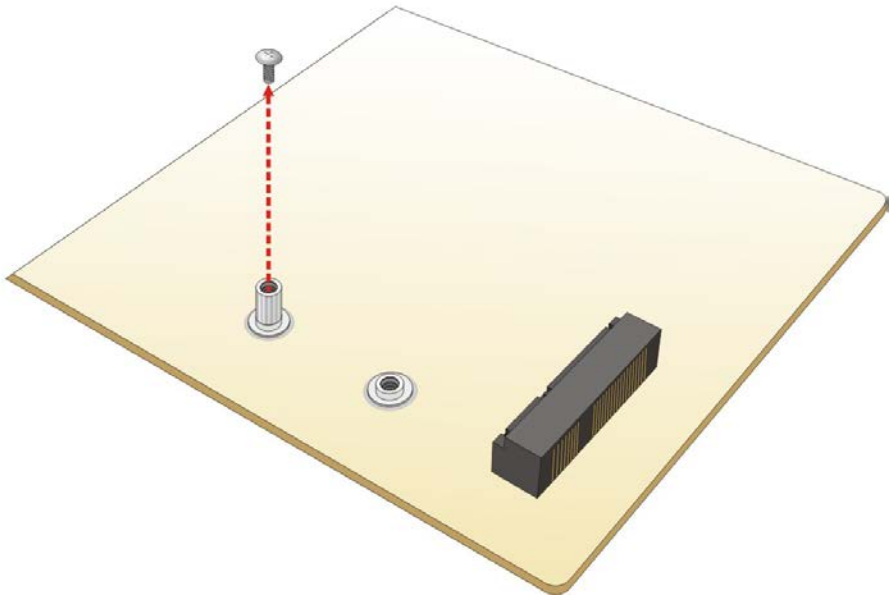


Figure 4-8: Removing the Retention Screw

Step 4: **Insert into the socket at an angle**. Line up the notch on the card with the notch on the slot. Slide the PCIe Mini card into the socket at an angle of about 20º (**Figure 4-9**).

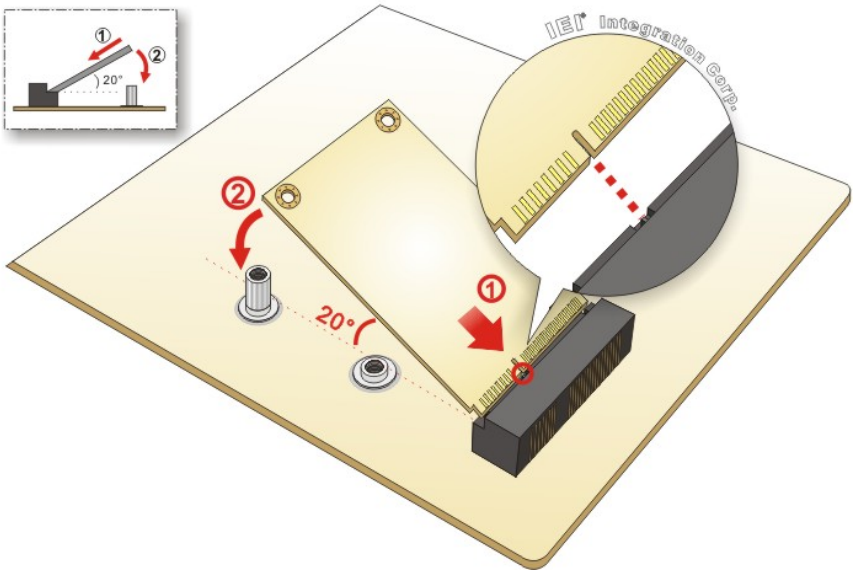


Figure 4-9: Inserting the Full-size PCIe Mini Card into the Slot at an Angle

Step 5: **Secure the full-size PCIe Mini card**. Secure the full-size PCIe Mini card with the retention screw previously removed (**Figure 4-10**).

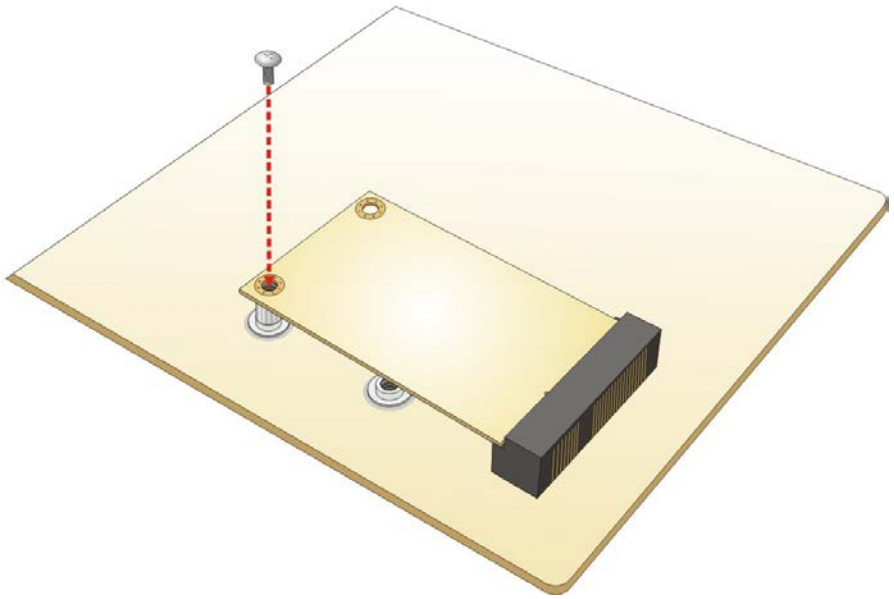


Figure 4-10: Securing the Full-size PCIe Mini Card

4.7 Half-size PCIe Mini Card Installation

The PCIe Mini card slot allows installation of either a full-size or half-size PCIe Mini card. To install a half-size PCIe Mini card, please follow the steps below.

Step 1: **Locate the PCIe Mini card slot**. See **Figure 3-18**.

Step 2: **Remove the retention screw**. Remove the retention screw as shown in **Figure 4-11**.

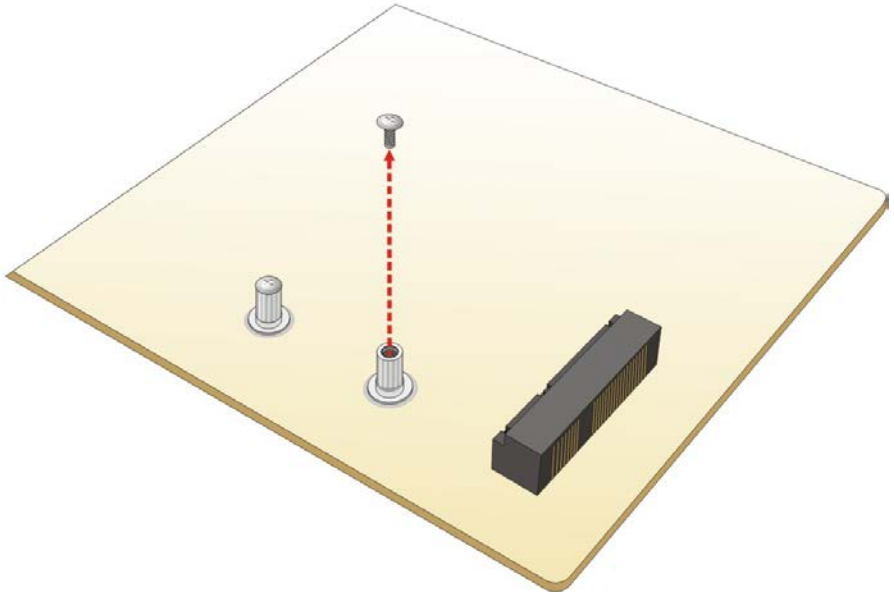


Figure 4-11: Removing the Retention Screw

Step 3: **Insert into the socket at an angle**. Line up the notch on the card with the notch on the slot. Slide the PCIe Mini card into the slot at an angle of about 20º (**Figure 4-12**).

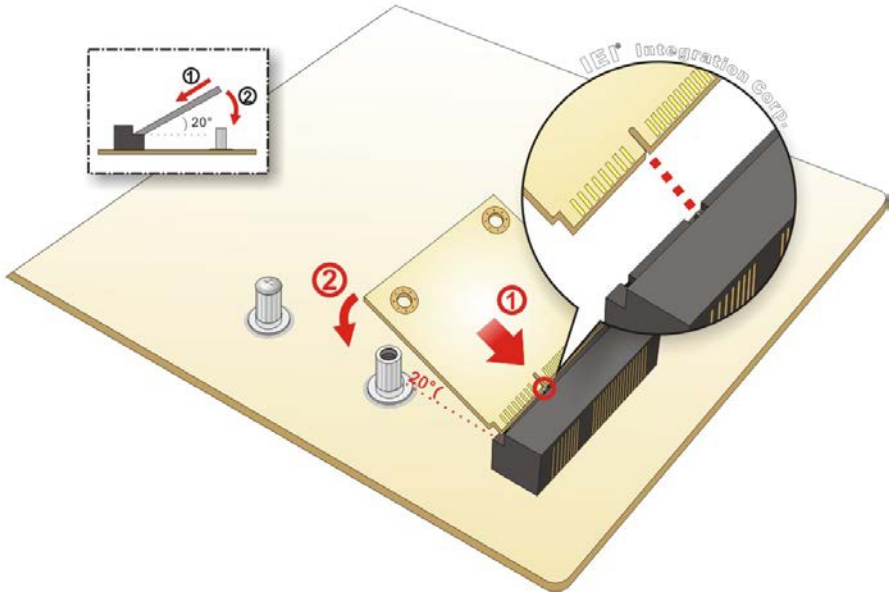


Figure 4-12: Inserting the Half-size PCIe Mini Card into the Slot at an Angle

Step 4: **Secure the half-size PCIe Mini card**. Secure the half-size PCIe Mini card with the retention screw previously removed (**Figure 4-13**).

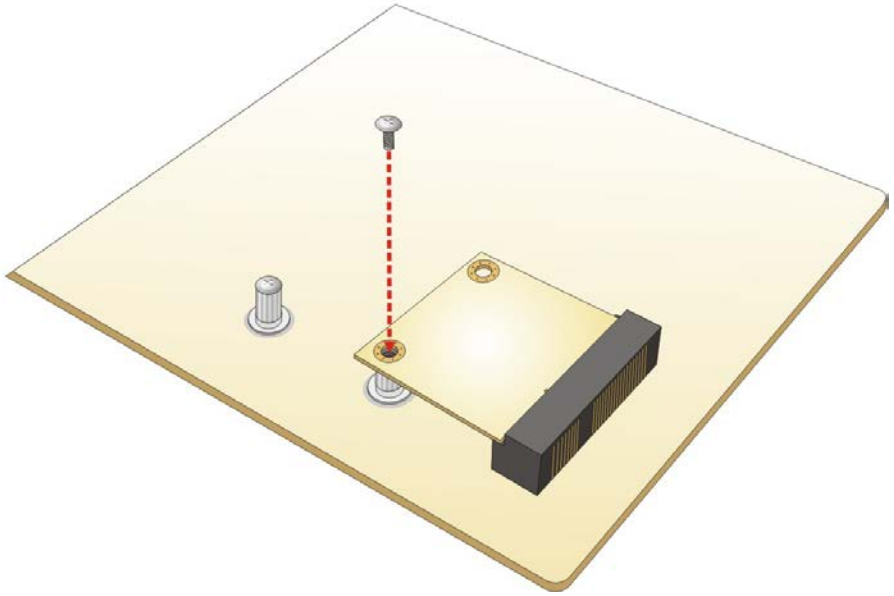


Figure 4-13: Securing the Half-size PCIe Mini Card

4.8 System Configuration

The system configuration should be performed before installation.

4.8.1 AT/ATX Power Mode Setting

The AT and ATX power mode selection is made through the AT/ATX power mode switch which is shown in **Figure 4-14**.

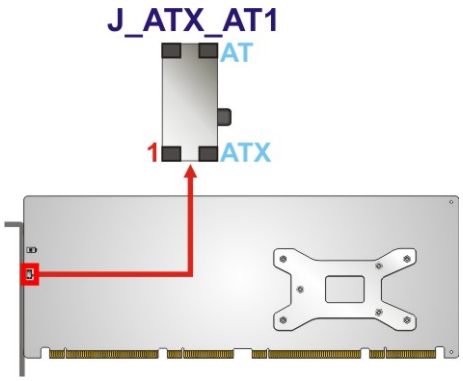


Figure 4-14: AT/ATX Power Mode Switch Location

Setting	Description
1-2 (down)	ATX power mode (default)
2-3 (up)	AT power mode

Table 4-1: AT/ATX Power Mode Switch Settings

4.8.2 Clear CMOS Button

To reset the BIOS, remove the on-board battery and press the clear CMOS button for three seconds or more. The clear CMOS button location is shown in **Figure 4-15**.

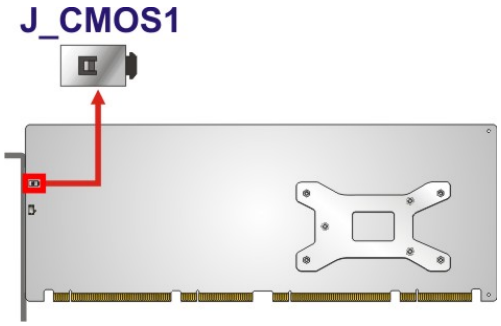


Figure 4-15: Clear CMOS Button Location

4.8.3 Flash Descriptor Security Override

The Flash Descriptor Security Override jumper specifies whether to override the flash descriptor.

Setting	Description
Short 1-2	No override (default)
Short 2-3	Override

Table 4-2: Flash Descriptor Security Override Jumper Settings

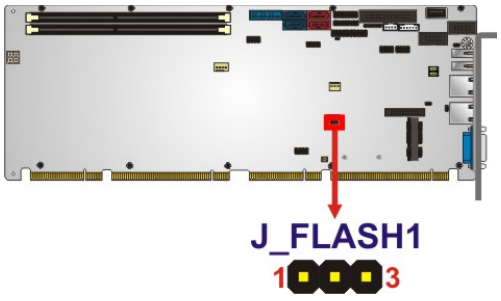


Figure 4-16: Flash Descriptor Security Override Jumper Location

4.8.4 mSATA Mode Selection

The jumper configures the PCIe Mini slot (CN4) to automatically detect mSATA device or to force mSATA to be enabled.

Setting	Description
Open	Auto-detect mSATA device (default)
Short 1-2	Enable mSATA

Table 4-3: mSATA Mode Selection Jumper Settings

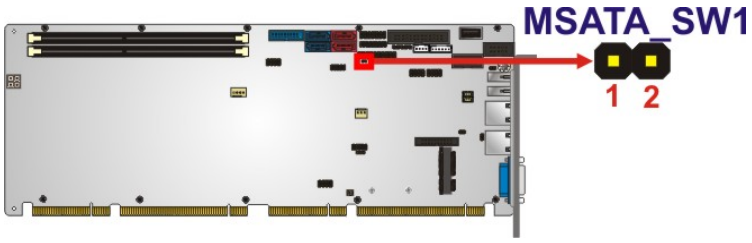


Figure 4-17: mSATA Mode Selection Jumper Location

4.8.5 USB Power Selection

The USB power selection is made through the BIOS menu in "Chipset → PCH-IO Configuration". Use the **USB SW1 Power** and the **USB SW2 Power** BIOS options to configure the correspondent USB ports (see **Table 4-4**) and refer to **Table 4-5** to select the USB power source.

BIOS Options	Configured USB Ports
USB SW1 Power	USB_C1 (external USB 2.0 port) USB_C2 (external USB 2.0 port)
USB SW2 Power	USB2 (internal USB 2.0 ports) USB3 (internal USB 2.0 ports) USB4 (internal USB 2.0 port, Type A) CN5 (internal USB 3.1 Gen 1 ports)

Table 4-4: BIOS Options and Configured USB Ports

Options	Description
+5V DUAL	+5V dual (default)
+5V	+5V

Table 4-5: USB Power Source Setup

Please refer to Section **5.4.1** for detailed information.

4.9 Chassis Installation

4.9.1 Airflow

WARNING:

Airflow is critical to the cooling of the CPU and other onboard components. The chassis in which the PCIE-H810 must have air vents to allow cool air to move into the system and hot air to move out.

The PCIE-H810 must be installed in a chassis with ventilation holes on the sides allowing airflow to travel through the heat sink surface. In a system with an individual power supply unit, the cooling fan of a power supply can also help generate airflow through the board surface.

4.9.2 CPU Card Installation

To install the CPU card onto the backplane, carefully align the CPU card edge connector with the CPU card socket on the backplane. To do this, please refer to the reference material that came with the backplane. Next, secure the CPU card to the chassis. To do this, please refer to the reference material that came with the chassis.

4.10 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the onboard connectors.

4.10.1 SATA Drive Connection

The PCIE-H810 is shipped with four SATA drive cables. To connect the SATA drives to the connectors, please follow the steps below.

Step 1: **Locate the connectors**. The locations of the SATA drive connectors are shown in **Chapter 3**.

Step 2: **Insert the cable connector**. Insert the cable connector into the on-board SATA drive connector until it clips into place. See **Figure 4-18**.

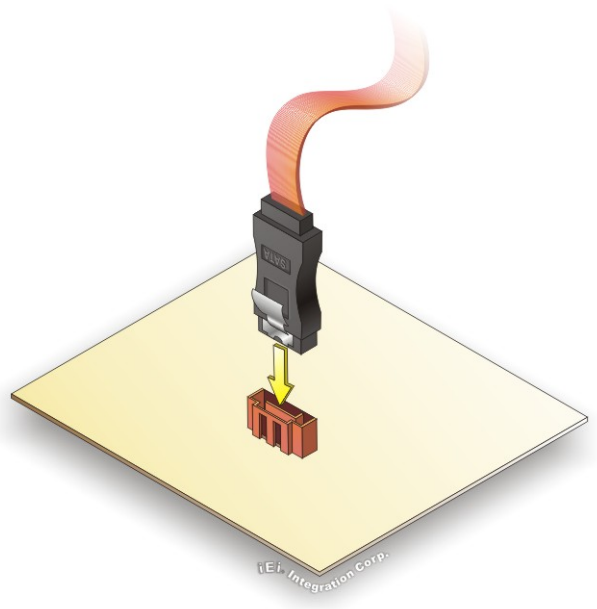


Figure 4-18: SATA Drive Cable Connection

Step 3: **Connect the cable to the SATA disk**. Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 4-19**.

Step 4: **Connect the SATA power cable (optional)**. Connect the SATA power connector to the back of the SATA drive. See **Figure 4-19**.

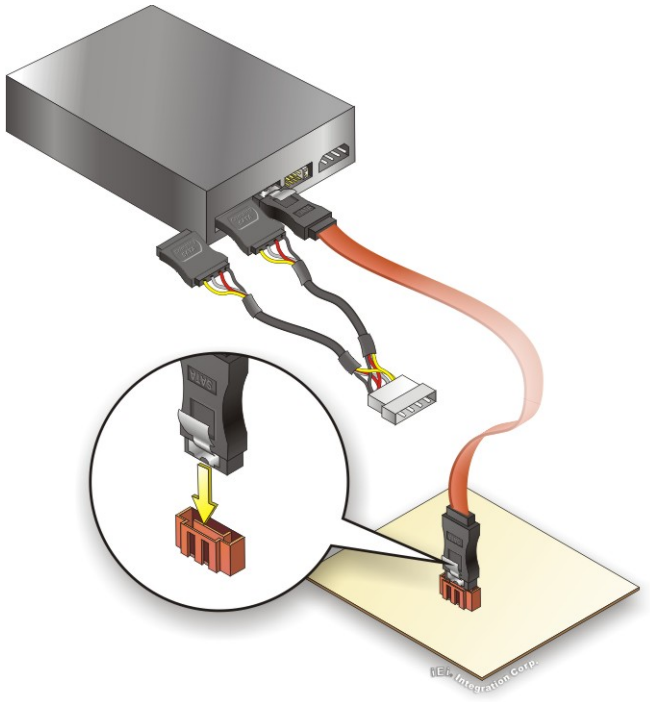


Figure 4-19: SATA Power Drive Connection

Chapter

5

BIOS

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.

NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. Press the **DEL** or **F2** key as soon as the system is turned on or
2. Press the **DEL** or **F2** key when the "**Press DEL or F2 to enter SETUP**" message appears on the screen.

If the message disappears before the **DEL or F2** key is pressed, restart the computer and try again.

5.1.2 Using Setup

Use the arrow keys to highlight items, press **ENTER** to select, use the PageUp and PageDown keys to change entries, press **F1** for help and press **Esc** to quit. Navigation keys are shown in the following table.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes
-	Decrease the numeric value or make changes
Page Up	Move to the previous page

Key	Function
Page Dn	Move to the next page
Esc	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2	Previous values
F3	Load optimized defaults
F4	Save changes and Exit BIOS

Table 5-1: BIOS Navigation Keys

5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window press **Esc** or the **F1** key again.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the jumper described in Chapter **4**.

5.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

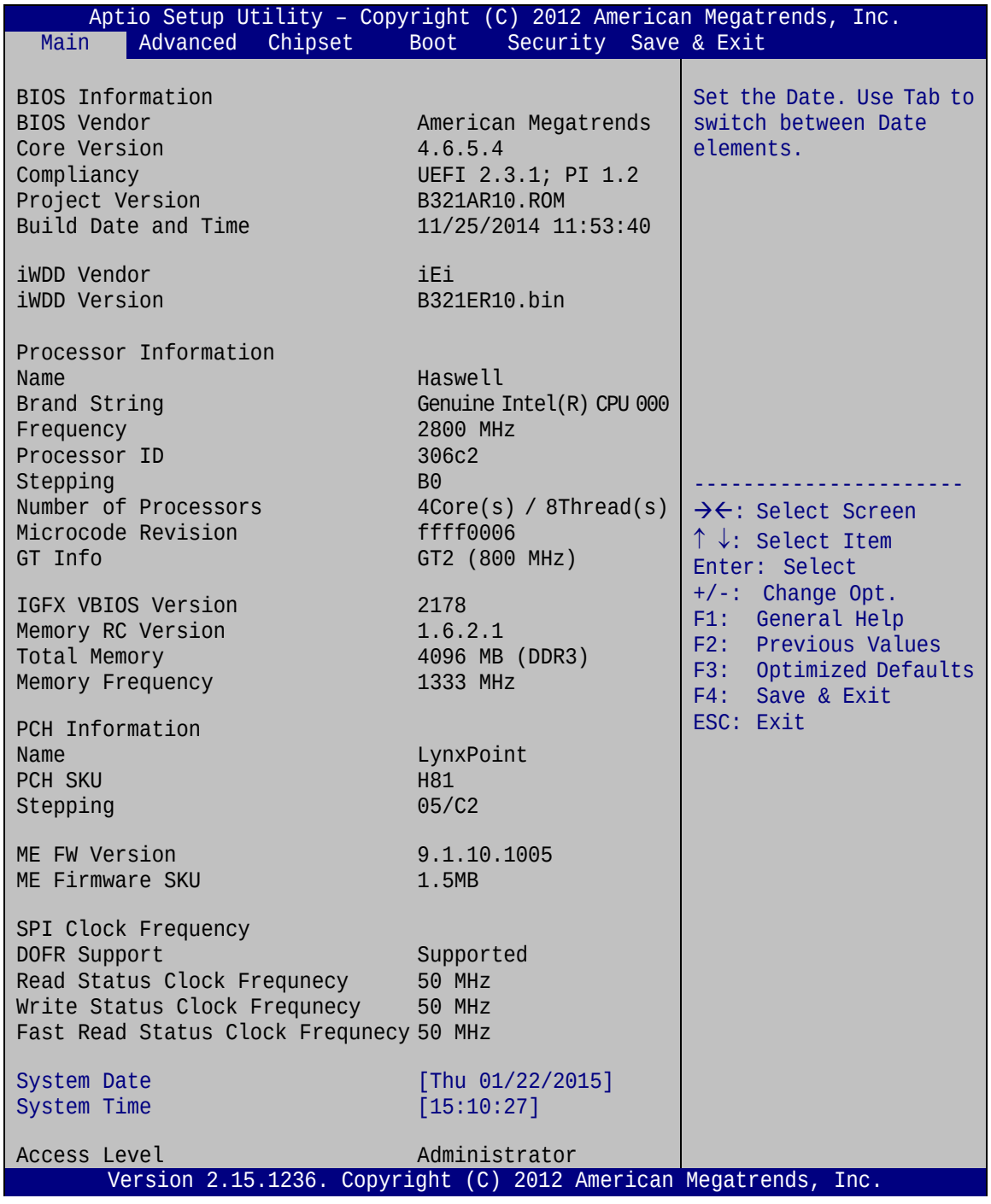
- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Boot – Changes the system boot configuration.
- Security – Sets User and Supervisor Passwords.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

5.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered.

The **Main** menu gives an overview of the basic system information.



BIOS Menu 1: Main

➔ **System Overview**

The system overview lists a brief summary of the BIOS. The fields in system overview cannot be changed. The items shown in the system overview include:

- BIOS Information
- Processor Information
- Memory Information
- PCH Information
- SPI Clock Frequency

The **Main** menu has two user configurable fields:

➔ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

➔ **System Time [xx:xx:xx]**

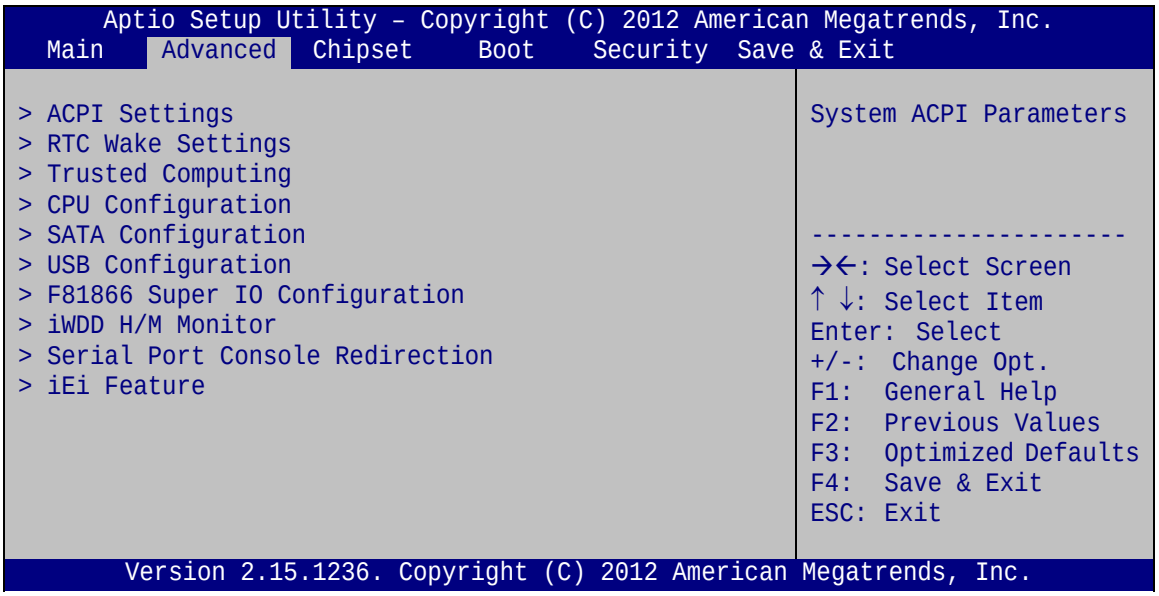
Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 2**) to configure the CPU and peripheral devices through the following sub-menus:

WARNING!

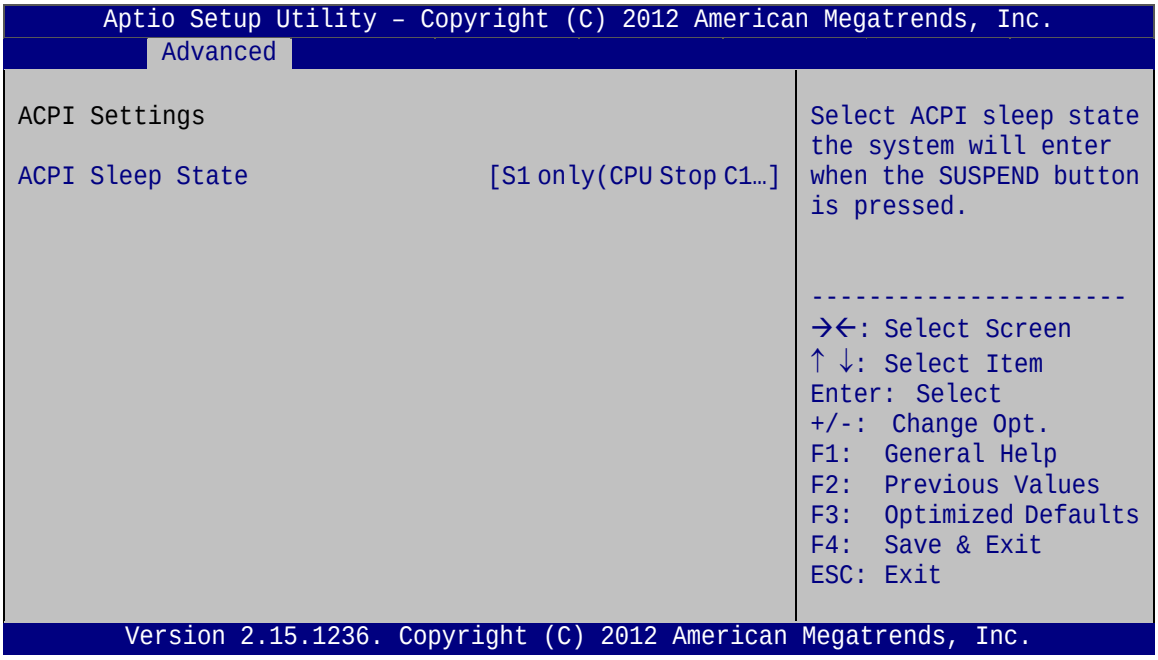
Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.



BIOS Menu 2: Advanced

5.3.1 ACPI Settings

The **ACPI Settings** menu (**BIOS Menu 3**) configures the Advanced Configuration and Power Interface (ACPI) options.



BIOS Menu 3: ACPI Configuration

➔ **ACPI Sleep State [S1 only (CPU Stop Clock)]**

Use the **ACPI Sleep State** option to specify the sleep state the system enters when it is not being used.

➔ **S1 only (CPU Stop Clock)**	**DEFAULT**	The system enters S1 (POS) sleep state. The system appears off. The CPU is stopped; RAM is refreshed; the system is running in a low power mode.
➔ **S3 only (Suspend to RAM)**		The caches are flushed and the CPU is powered off. Power to the RAM is maintained. The computer returns slower to a working state, but more power is saved.

5.3.2 RTC Wake Settings

The **RTC Wake Settings** menu (**BIOS Menu 4**) enables the system to wake at the specified time.

```
Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
        Advanced
Wake system with Fixed Time      [Disabled]

Enable or disable System
wake on alarm event. When
enabled, System will
wake on the
date::hr::min::sec
specified

----------------------
→←: Select Screen
↑ ↓: Select Item
Enter:  Select
+/-:  Change Opt.
F1:   General Help
F2:   Previous Values
F3:   Optimized Defaults
F4:   Save & Exit
ESC:  Exit
Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.
```

BIOS Menu 4: RTC Wake Settings

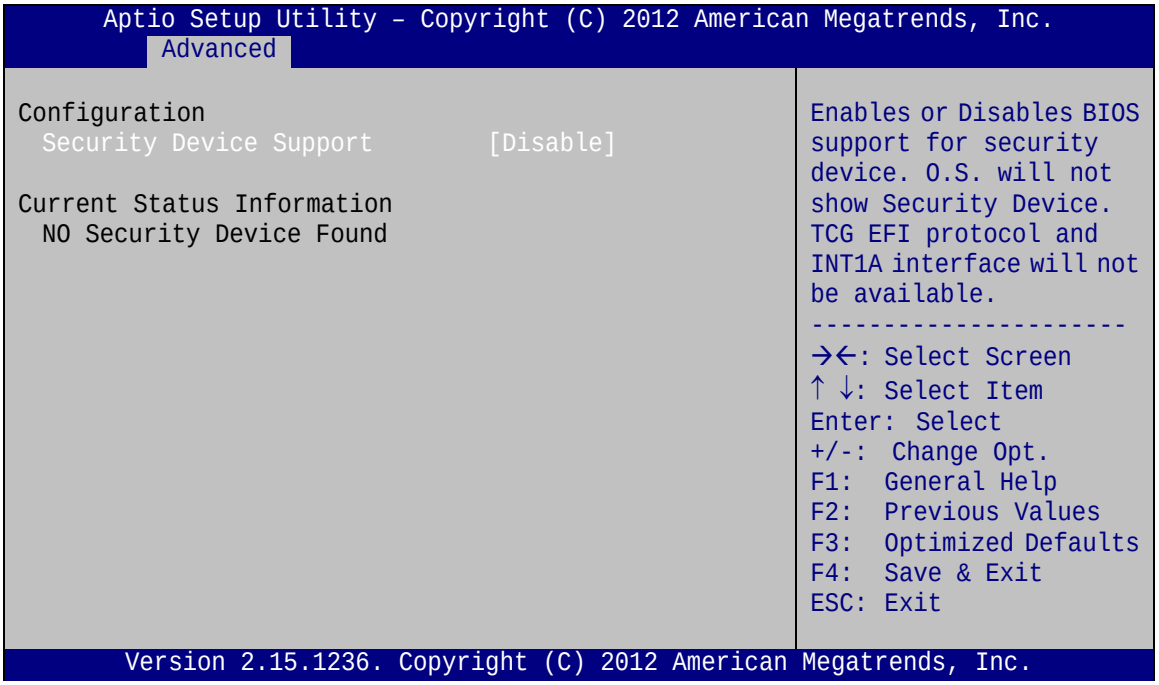
➔ **Wake system with Fixed Time [Disabled]**

Use the **Wake system with Fixed Time** option to enable or disable the system wake on alarm event.

➔ **Disabled**	**DEFAULT**	The real time clock (RTC) cannot generate a wake event
➔ **Enabled**		If selected, the **Wake up every day** option appears allowing you to enable to disable the system to wake every day at the specified time. Besides, the following options appear with values that can be selected: Wake up date Wake up hour Wake up minute Wake up second After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

5.3.3 Trusted Computing

Use the **Trusted Computing** menu (**BIOS Menu 5**) to configure settings related to the Trusted Computing Group (TCG) Trusted Platform Module (TPM).



BIOS Menu 5: TPM Configuration

➔ **Security Device Support [Disable]**

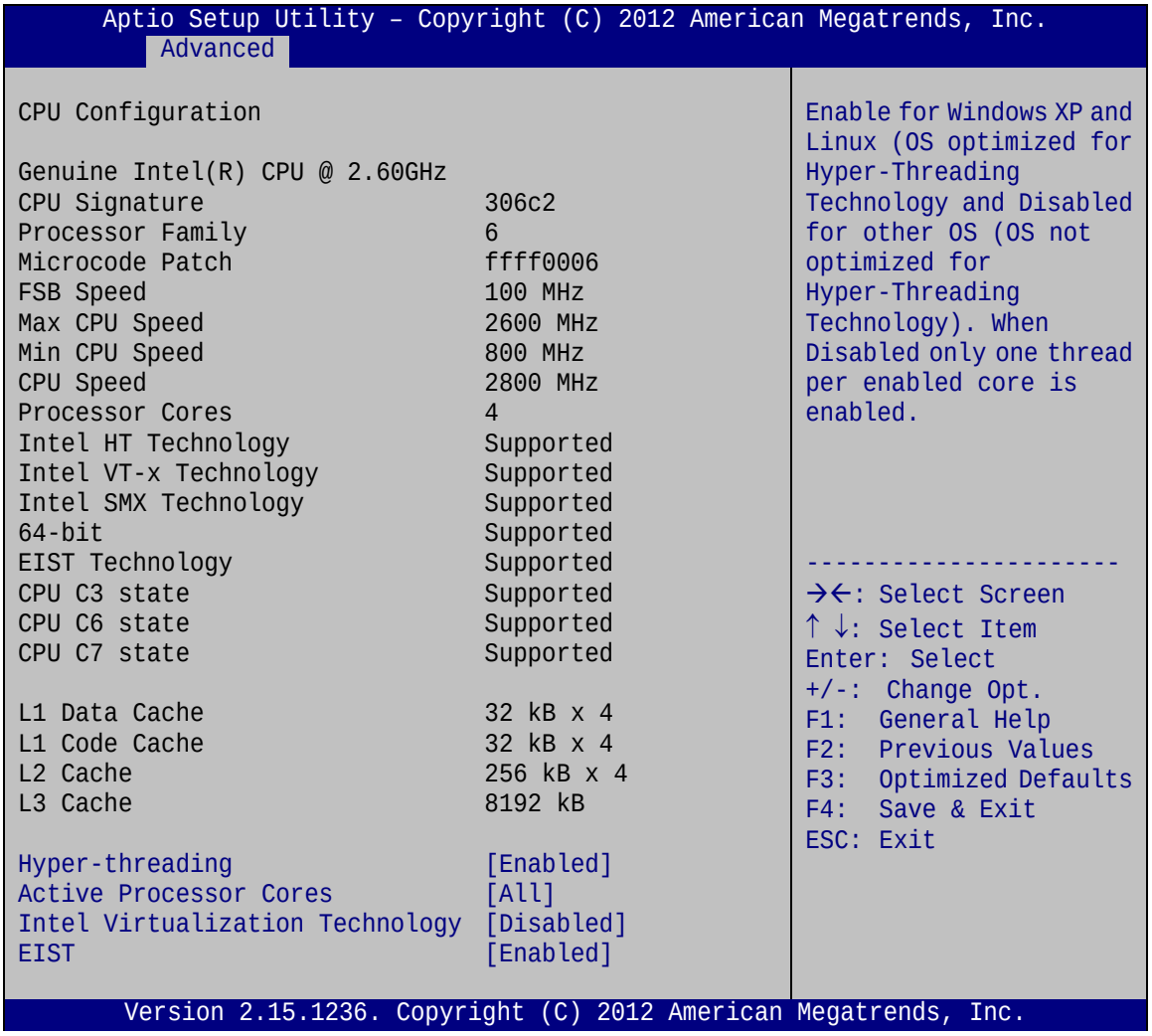
Use the **Security Device Support** option to configure support for the TPM.

➔ **Disable** **DEFAULT** TPM support is disabled.

➔ **Enable** TPM support is enabled.

5.3.4 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 6**) to view detailed CPU specifications or enable the Intel Virtualization Technology.



BIOS Menu 6: CPU Configuration

➔ **Hyper-threading [Enabled]**

Use the **Hyper-threading** BIOS option to enable or disable the Intel Hyper-Threading Technology.

➔ **Disabled** Disables the Intel Hyper-Threading Technology.

➔ **Enabled** **DEFAULT** Enables the Intel Hyper-Threading Technology.

➔ **Active Processor Cores [All]**

Use the **Active Processor Cores** BIOS option to enable numbers of cores in the processor package.

➔	**All**	**DEFAULT**	Enable all cores in the processor package.
➔	**1**		Enable one core in the processor package.
➔	**2**		Enable two cores in the processor package.
➔	**3**		Enable three cores in the processor package.

➔ **Intel Virtualization Technology [Disabled]**

Use the **Intel Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel® Virtualization technology allows several OSs to run on the same system at the same time.

➔	**Disabled**	**DEFAULT**	Disables Intel Virtualization Technology.
➔	**Enabled**		Enables Intel Virtualization Technology.

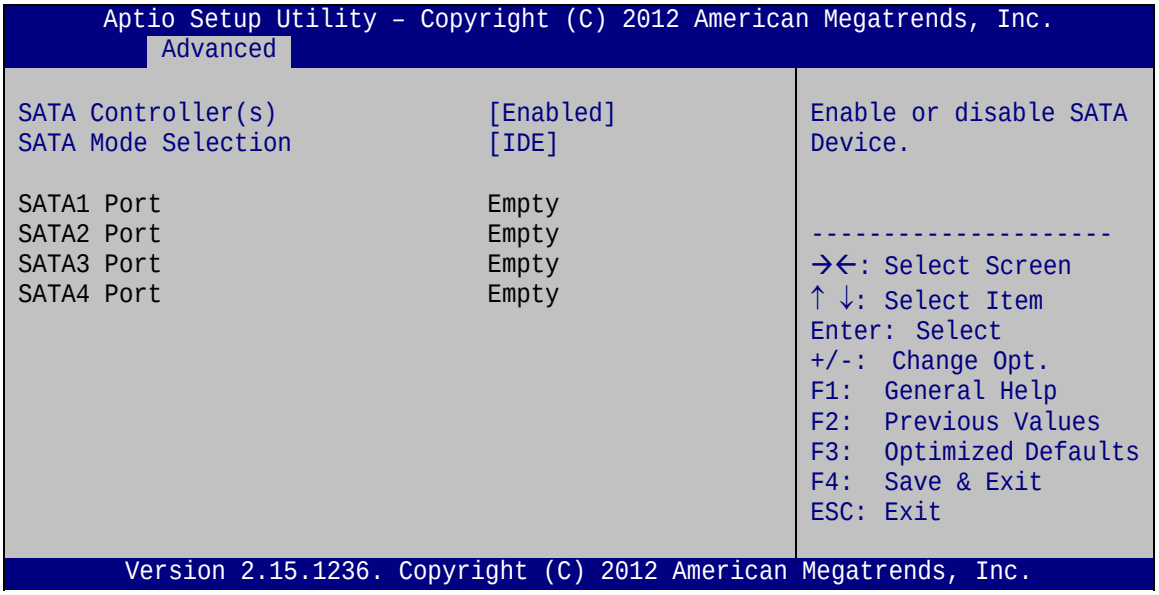
➔ **EIST [Enabled]**

Use the **EIST** option to enable or disable the Enhanced Intel® SpeedStep Technology (EIST).

➔	**Disabled**		Disables Enhanced Intel® SpeedStep Technology
➔	**Enabled**	**DEFAULT**	Enables Enhanced Intel® SpeedStep Technology

5.3.5 SATA Configuration

Use the **SATA Configuration** menu (**BIOS Menu 7**) to change and/or set the configuration of the SATA devices installed in the system.



BIOS Menu 7: SATA Configuration

➔ **SATA Controller(s) [Enabled]**

Use the **SATA Controller(s)** option to configure the SATA controller(s).

- ➔ **Enabled** **DEFAULT** Enables the on-board SATA controller(s).
- ➔ **Disabled** Disables the on-board SATA controller(s).

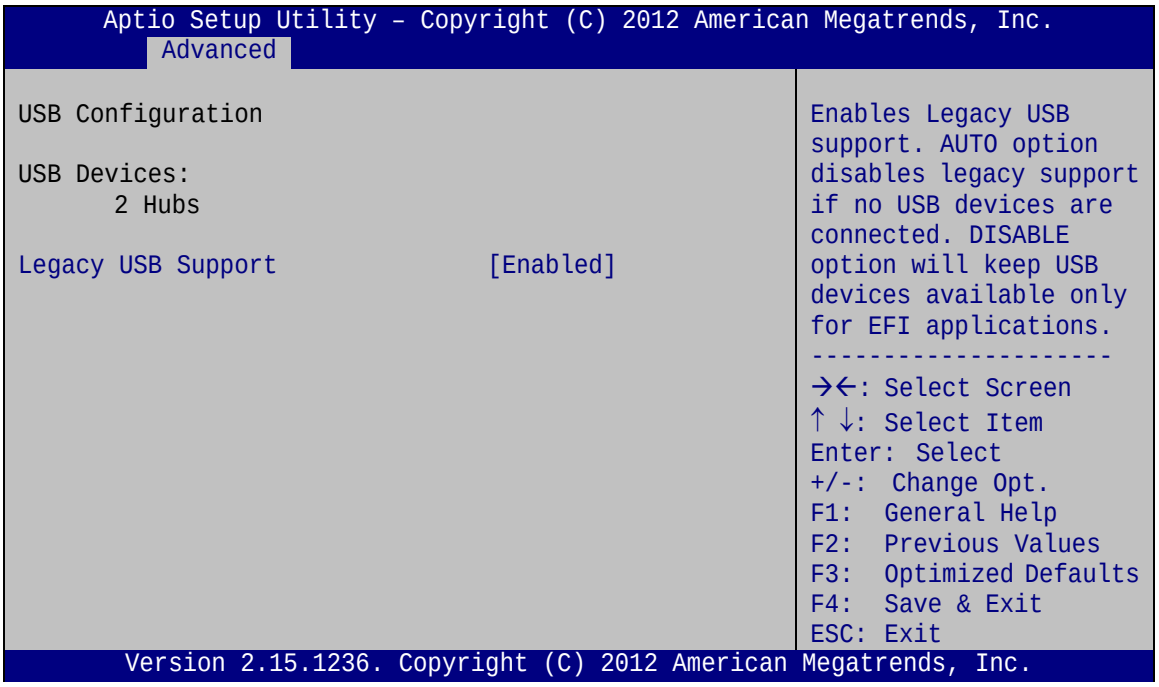
➔ **SATA Mode Selection [IDE]**

Use the **SATA Mode Selection** option to determine how SATA devices operate.

- ➔ **IDE** **DEFAULT** Configures SATA devices as normal IDE device.
- ➔ **AHCI** Configures SATA devices as AHCI device.

5.3.6 USB Configuration

Use the **USB Configuration** menu (**BIOS Menu 8**) to read USB configuration information and configure the USB settings.



BIOS Menu 8: USB Configuration

➔ **USB Devices**

The **USB Devices** field lists the USB devices that are enabled on the system

➔ **Legacy USB Support [Enabled]**

Use the **Legacy USB Support** BIOS option to enable USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.

➔	**Enabled**	**DEFAULT**	Legacy USB support enabled
➔	**Disabled**		Legacy USB support disabled
➔	**Auto**		Legacy USB support disabled if no USB devices are connected

5.3.7 F81866 Super IO Configuration

Use the **F81866 Super IO Configuration** menu (**BIOS Menu 9**) to set or change the configurations for the serial ports and parallel port.

```
      Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
          Advanced
 F81866 Super IO Configuration                  | Set Parameters of Serial
                                                | Port 1 (COMA)
 F81866 Super IO Chip            F81866         |
 > Serial Port 1 Configuration                  |
 > Serial Port 2 Configuration                  | ---------------------
 > Serial Port 3 Configuration                  | →←: Select Screen
 > Serial Port 4 Configuration                  | ↑ ↓: Select Item
 > Serial Port 5 Configuration                  | Enter: Select
 > IrDA Configuration                           | +/-: Change Opt.
 > Parallel Port Configuration                  | F1: General Help
                                                | F2: Previous Values
                                                | F3: Optimized Defaults
                                                | F4: Save & Exit
                                                | ESC: Exit
      Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.
```

BIOS Menu 9: F81866 Super IO Configuration

5.3.7.1 Serial Port n Configuration

Use the **Serial Port n Configuration** menu (**BIOS Menu 10**) to configure the serial port n.

```
      Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
          Advanced
 Serial Port n Configuration                    | Enable or Disable Serial
                                                | Port (COM)
 Serial Port                     [Enabled]      |
 Device Settings                 IO=3F8h; IRQ=4 |
                                                | ---------------------
 Change Settings                 [Auto]         | →←: Select Screen
                                                | ↑ ↓: Select Item
                                                | Enter: Select
                                                | +/-: Change Opt.
                                                | F1: General Help
                                                | F2: Previous Values
                                                | F3: Optimized Defaults
                                                | F4: Save & Exit
                                                | ESC: Exit
      Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.
```

BIOS Menu 10: Serial Port n Configuration Menu

5.3.7.1.1 Serial Port 1 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔ **IO=3F8h; IRQ=4**		Serial Port I/O port address is 3F8h and the interrupt address is IRQ4.
➔ **IO=3F8h; IRQ=3, 4**		Serial Port I/O port address is 3F8h and the interrupt address is IRQ3, 4.
➔ **IO=2C0h; IRQ=3, 4**		Serial Port I/O port address is 2C0h and the interrupt address is IRQ3, 4.
➔ **IO=2C8h; IRQ=3, 4**		Serial Port I/O port address is 2C8h and the interrupt address is IRQ3, 4.

5.3.7.1.2 Serial Port 2 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔ **IO=2F8h; IRQ=3**		Serial Port I/O port address is 2F8h and the interrupt address is IRQ3.
➔ **IO=3F8h; IRQ=3, 4**		Serial Port I/O port address is 3F8h and the interrupt address is IRQ3, 4.
➔ **IO=2F8h; IRQ=3, 4**		Serial Port I/O port address is 2F8h and the interrupt address is IRQ3, 4.
➔ **IO=2C0h; IRQ=3, 4**		Serial Port I/O port address is 2C0h and the interrupt address is IRQ3, 4.
➔ **IO=2C8h; IRQ=3, 4**		Serial Port I/O port address is 2C8h and the interrupt address is IRQ3, 4.

5.3.7.1.3 Serial Port 3 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.

➔ **IO=2D0h; IRQ=11**	Serial Port I/O port address is 2D0h and the interrupt address is IRQ11
➔ **IO=2D0h; IRQ=10, 11**	Serial Port I/O port address is 2D0h and the interrupt address is IRQ10, 11
➔ **IO=2D8h; IRQ=10, 11**	Serial Port I/O port address is 2D8h and the interrupt address is IRQ10, 11
➔ **IO=2C0h; IRQ=10, 11**	Serial Port I/O port address is 2C0h and the interrupt address is IRQ10, 11
➔ **IO=2C8h; IRQ=10, 11**	Serial Port I/O port address is 2C8h and the interrupt address is IRQ10, 11

5.3.7.1.4 Serial Port 4 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔ **IO=2D8h; IRQ=10**		Serial Port I/O port address is 2D8h and the interrupt address is IRQ10
➔ **IO=2D0h; IRQ=10, 11**		Serial Port I/O port address is 2D0h and the interrupt address is IRQ10, 11
➔ **IO=2D8h; IRQ=10, 11**		Serial Port I/O port address is 2D8h and the interrupt address is IRQ10, 11

➔	**IO=2C0h; IRQ=10, 11**	Serial Port I/O port address is 2C0h and the interrupt address is IRQ10, 11
➔	**IO=2C8h; IRQ=10, 11**	Serial Port I/O port address is 2C8h and the interrupt address is IRQ10, 11

5.3.7.1.5 Serial Port 5 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔	**Disabled**		Disable the serial port
➔	**Enabled**	**DEFAULT**	Enable the serial port

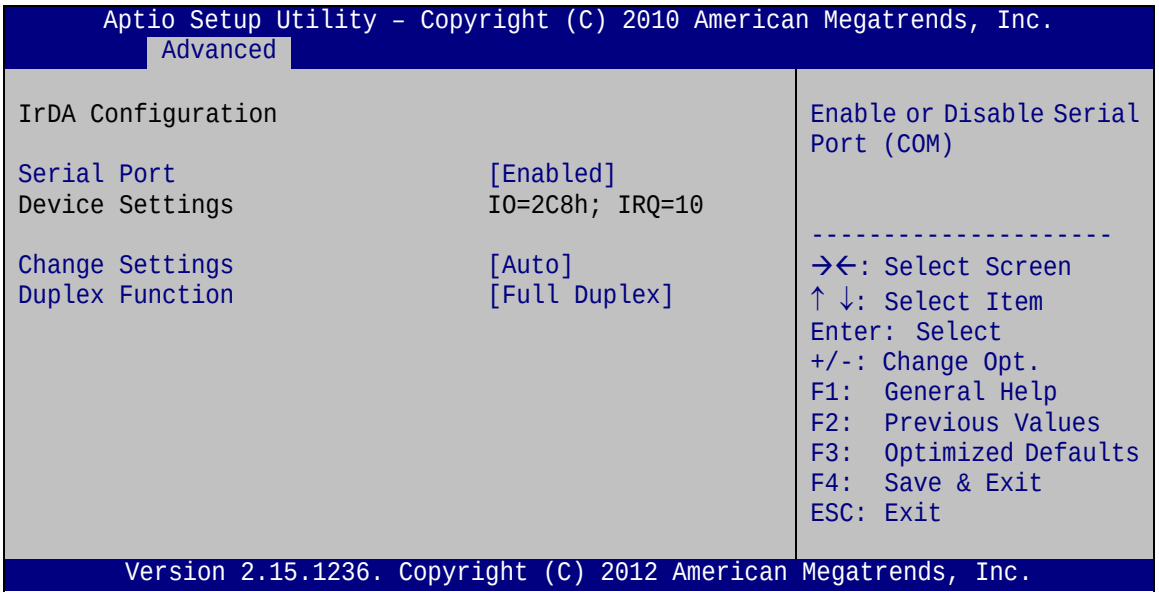
➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔	**Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔	**IO=2C0h; IRQ=11**		Serial Port I/O port address is 2C0h and the interrupt address is IRQ11
➔	**IO=2D0h; IRQ=10, 11**		Serial Port I/O port address is 2D0h and the interrupt address is IRQ10, 11
➔	**IO=2D8h; IRQ=10, 11**		Serial Port I/O port address is 2D8h and the interrupt address is IRQ10, 11
➔	**IO=2C0h; IRQ=10, 11**		Serial Port I/O port address is 2C0h and the interrupt address is IRQ10, 11
➔	**IO=2C8h; IRQ=10, 11**		Serial Port I/O port address is 2C8h and the interrupt address is IRQ10, 11

5.3.7.2 IrDA Configuration

Use the **IrDA Configuration** menu (**BIOS Menu 11**) to configure the infrared port.



BIOS Menu 11: IrDA Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the infrared port.

➔ **Disabled**		Disable the infrared port
➔ **Enabled**	**DEFAULT**	Enable the infrared port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the infrared port IO port address and interrupt address.

➔ **Auto**	**DEFAULT**	The infrared port IO port address and interrupt address are automatically detected.
➔ **IO=2C8h; IRQ=10**		Infrared port I/O port address is 2C8h and the interrupt address is IRQ10

- **IO=2D0h; IRQ=10, 11** — Infrared port I/O port address is 2D0h and the interrupt address is IRQ10, 11
- **IO=2D8h; IRQ=10, 11** — Infrared port I/O port address is 2D8h and the interrupt address is IRQ10, 11
- **IO=2C0h; IRQ=10, 11** — Infrared port I/O port address is 2C0h and the interrupt address is IRQ10, 11
- **IO=2C8h; IRQ=10, 11** — Infrared port I/O port address is 2C8h and the interrupt address is IRQ10, 11

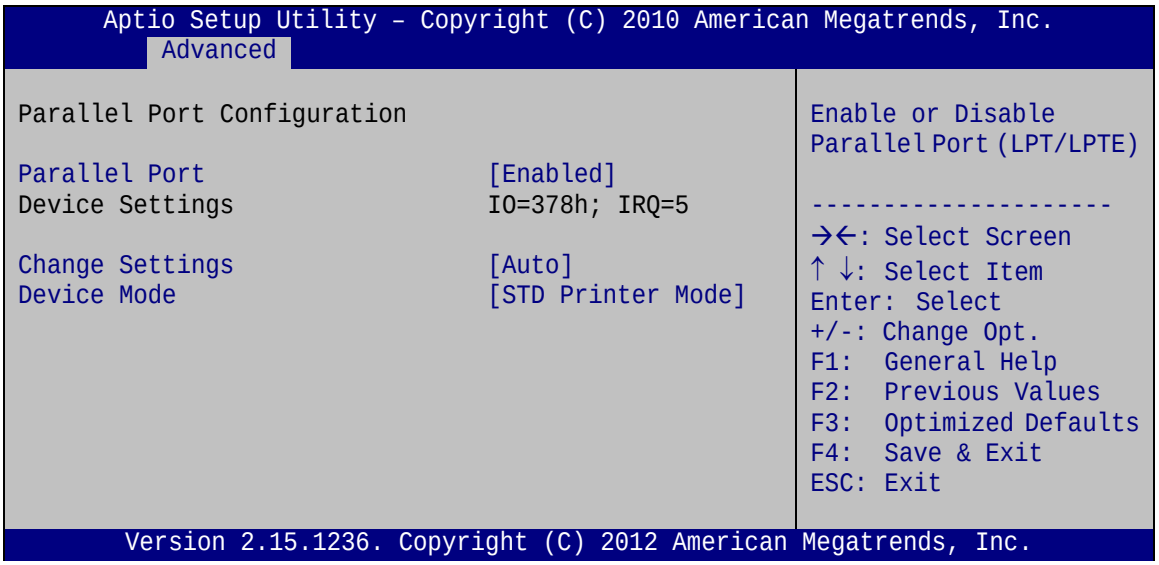
➔ **Duplex Function [Full Duplex]**

Use the **Duplex Function** option to select the IR data transmission mode.

- **Full Duplex** **DEFAULT** — The communication channels is used to send and receive the data in both directions at the same time.
- **Half Duplex** — Transmission signals are sent in both directions but one direction at a time so half duplex lines can alternatively send and receive data.

5.3.7.3 Parallel Port Configuration

Use the **Parallel Port Configuration** menu (**BIOS Menu 12**) to configure the serial port n.



BIOS Menu 12: Parallel Port Configuration Menu

➔ **Parallel Port [Enabled]**

Use the **Parallel Port** option to enable or disable the parallel port.

➔ **Disabled**		Disable the parallel port
➔ **Enabled**	**DEFAULT**	Enable the parallel port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the parallel port IO port address and interrupt address.

➔ **Auto**	**DEFAULT**	The parallel port IO port address and interrupt address are automatically detected.
➔ **IO=378h; IRQ=5**		Parallel Port I/O port address is 378h and the interrupt address is IRQ5
➔ **IO=378h; IRQ=5, 7**		Parallel Port I/O port address is 378h and the interrupt address is IRQ5, 7

➔ **IO=278h; IRQ=5, 7** Parallel Port I/O port address is 278h and the interrupt address is IRQ5, 7

➔ **IO=3BCh; IRQ=5, 7** Parallel Port I/O port address is 3BCh and the interrupt address is IRQ5, 7

➔ **Device Mode [STD Printer Mode]**

Use the **Device Mode** option to select the mode the parallel port operates in. Configuration options are listed below.

- STD Printer Mode **Default**
- SPP Mode
- EPP-1.9 and SPP Mode
- EPP-1.7 and SPP Mode
- ECP Mode
- ECP and EPP 1.9 Mode
- ECP and EPP 1.7 Mode

5.3.8 iWDD H/W Monitor

The **iWDD H/W** Monitor menu (**BIOS Menu 13**) contains the fan configuration submenu and displays operating temperature, fan speeds and system voltages.

```
Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
        Advanced
PC Health Status                                  Smart Fan Mode Select

> Smart Fan Mode Configuration
CPU temperature                 :+44°C
System temperature              :+34°C
CPU_FAN1 Speed                  :1883 RPM
SYS_FAN1 Speed                  :N/A
CPU_CORE                        :+1.780 V
+5V                             :+5.131 V
+12V                            :+11.903 V
DDR                             :+1.513 V
+5VSB                           :+4.991 V
+3.3V                           :+3.296 V
+3.3VSB                         :+3.306 V
                                  ---------------------
                                  →←: Select Screen
                                  ↑ ↓: Select Item
                                  Enter: Select
                                  +/-: Change Opt.
                                  F1: General Help
                                  F2: Previous Values
                                  F3: Optimized Defaults
                                  F4: Save & Exit
                                  ESC: Exit
Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.
```

BIOS Menu 13: iWDD H/W Monitor

➔ **PC Health Status**

The following system parameters and values are shown. The system parameters that are monitored are:

- System Temperatures:
  - CPU Temperature
  - System Temperature
- Fan Speeds:
  - CPU Fan Speed
  - System Fan Speed
- Voltages:
  - CPU_CORE
  - +5V
  - +12V
  - DDR
  - +5VSB
  - +3.3V
  - +3.3VSB

5.3.8.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 14**) to configure fan speed settings.

```
Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
        Advanced

Smart Fan Mode Configuration

CPU_FAN1 Smart Fan Control      [Auto Mode]
Fan start temperature           50
Fan off temperature             40
Fan start PWM                   30
Fan slope PWM                   1
SYS_FAN1 Smart Fan Control      [Auto Mode]
Fan start temperature           50
Fan off temperature             40
Fan start PWM                   30
Fan slope PWM                   1

                                ---------------------
                                →←: Select Screen
                                ↑ ↓: Select Item
                                Enter: Select
                                +/-: Change Opt.
                                F1: General Help
                                F2: Previous Values
                                F3: Optimized Defaults
                                F4: Save & Exit
                                ESC: Exit

Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.
```

BIOS Menu 14: Smart Fan Mode Configuration

➔ **CPU_FAN1 Smart Fan Control/SYS_FAN1 Smart Fan Control [Auto Mode]**

Use the **CPU_FAN1 Smart Fan Control/SYS_FAN1 Smart Fan Control** option to configure the CPU/System Smart Fan.

➔ **Auto Mode**	**DEFAULT**	The fan adjusts its speed using Auto Mode settings.
➔ **Manual Mode**		The fan spins at the speed set in Manual Mode settings.

➔ **Fan start/off temperature**

Use the + or – key to change the **Fan start/off temperature** value. Enter a decimal number between 1 and 100.

➔ **Fan start PWM**

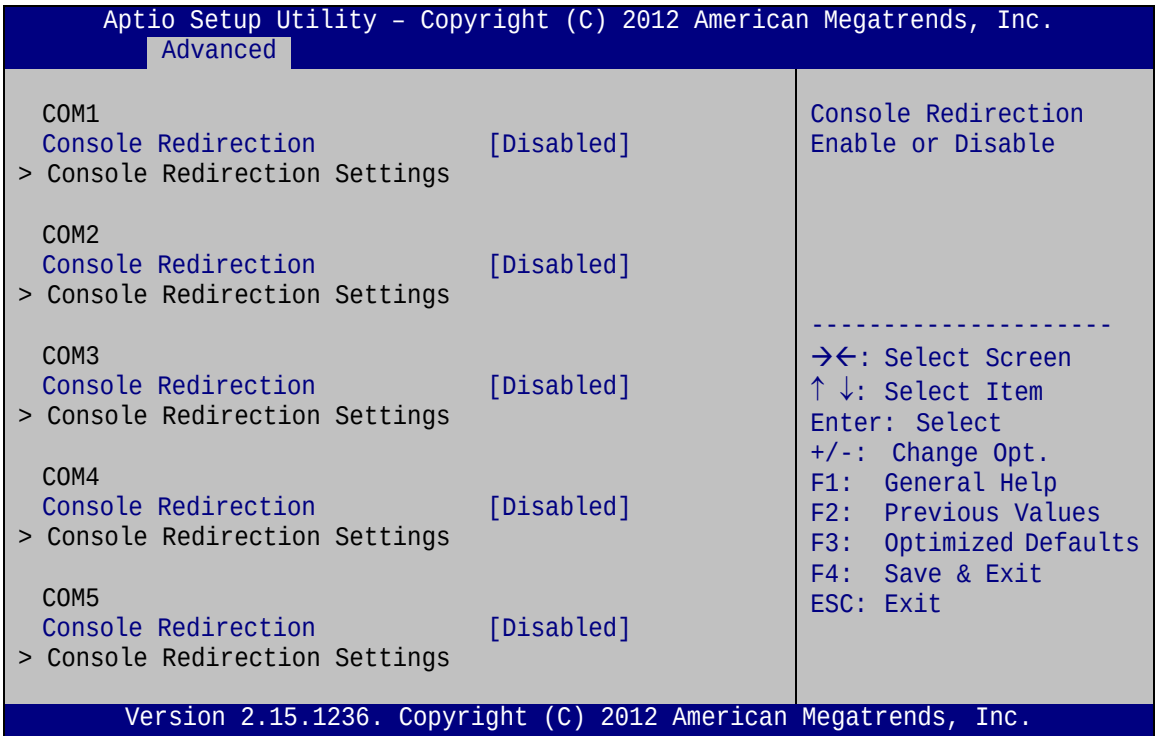
Use the + or – key to change the **Fan start PWM** value. Enter a decimal number between 1 and 100.

➔ **Fan slope PWM**

Use the + or – key to change the **Fan slope PWM** value. Enter a decimal number between 1 and 8.

5.3.9 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 15**) allows the console redirection options to be configured. Console redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



BIOS Menu 15: Serial Port Console Redirection

➔ **Console Redirection [Disabled]**

Use **Console Redirection** option to enable or disable the console redirection function.

➔ **Disabled** **DEFAULT** Disabled the console redirection function

➔ **Enabled** Enabled the console redirection function

➔ **Terminal Type [ANSI]**

Use the **Terminal Type** option to specify the remote terminal type.

➔ **VT100** The target terminal type is VT100

➔ **VT100+** The target terminal type is VT100+

➔ **VT-UTF8** The target terminal type is VT-UTF8

➔ **ANSI** **DEFAULT** The target terminal type is ANSI

➔ **Bits per second [115200]**

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match the other side. Long or noisy lines may require lower speeds.

➔ **9600**		Sets the serial port transmission speed at 9600.
➔ **19200**		Sets the serial port transmission speed at 19200.
➔ **57600**		Sets the serial port transmission speed at 57600.
➔ **115200**	**DEFAULT**	Sets the serial port transmission speed at 115200.

➔ **Data Bits [8]**

Use the **Data Bits** option to specify the number of data bits.

➔ **7**		Sets the data bits at 7.
➔ **8**	**DEFAULT**	Sets the data bits at 8.

➔ **Parity [None]**

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

➔ **None**	**DEFAULT**	No parity bit is sent with the data bits.
➔ **Even**		The parity bit is 0 if the number of ones in the data bits is even.
➔ **Odd**		The parity bit is 0 if the number of ones in the data bits is odd.
➔ **Mark**		The parity bit is always 1. This option does not provide error detection.
➔ **Space**		The parity bit is always 0. This option does not provide error detection.

➔ **Stop Bits [1]**

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

➔ **1**	**DEFAULT**	Sets the number of stop bits at 1.
➔ **2**		Sets the number of stop bits at 2.

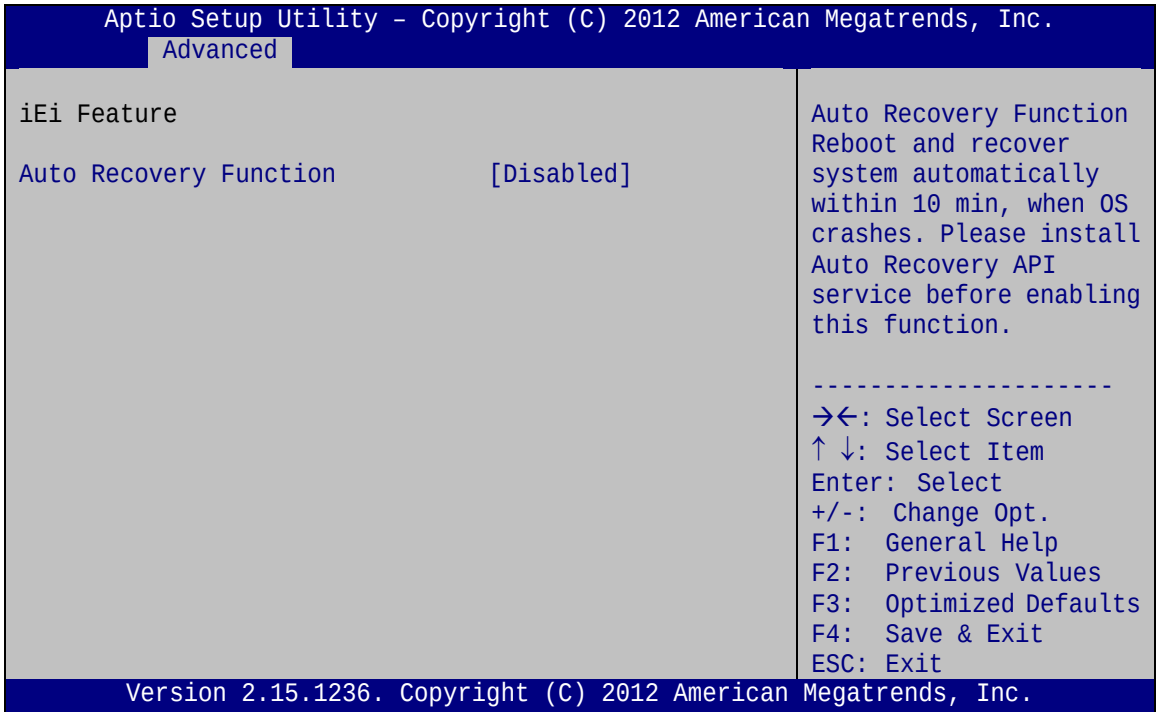
➔ **Flow Control [None]**

Use the **Flow Control** option to report the flow control method for the console redirection application.

➔ **None**	**DEFAULT**	No control flow.
➔ **Hardware RTS/CTS**		Hardware is set as the console redirection.

5.3.10 iEi Feature

Use the **iEi Feature** menu (**BIOS Menu 16**) to configure One Key Recovery function.



BIOS Menu 16: IEI Feature

➔ **Auto Recovery Function [Disabled]**

Use the **Auto Recovery Function** BIOS option to enable or disable the auto recovery function of the IEI One Key Recovery.

➔ **Disabled**	**DEFAULT**	Auto recovery function disabled
➔ **Enabled**		Auto recovery function enabled

5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 17**) to access the PCH IO and System Agent (SA) configuration menus.

WARNING!

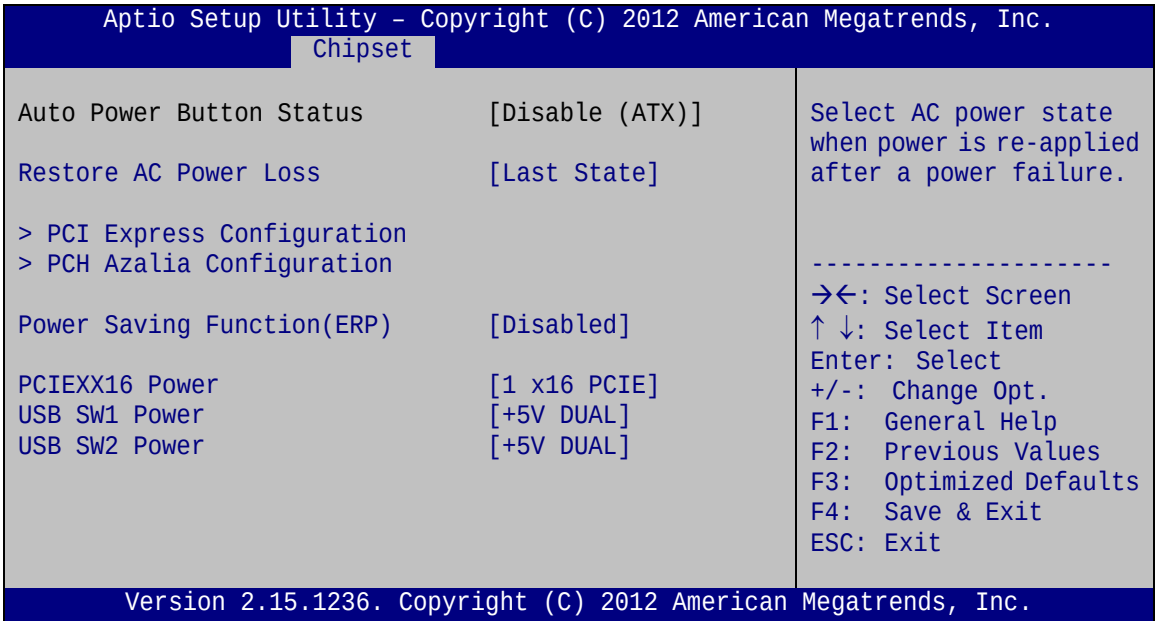
Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.

```
      Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
  Main    Advanced  Chipset    Boot    Security  Save & Exit

> PCH-IO Configuration                    PCH Parameters
> System Agent (SA) Configuration


                                          ---------------------
                                          →←: Select Screen
                                          ↑ ↓: Select Item
                                          Enter:  Select
                                          +/-:  Change Opt.
                                          F1:   General Help
                                          F2:   Previous Values
                                          F3:   Optimized Defaults
                                          F4:   Save & Exit
                                          ESC:  Exit
        Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.
```

BIOS Menu 17: Chipset

5.4.1 PCH-IO Configuration

Use the **PCH-IO Configuration** menu (**BIOS Menu 18**) to configure the PCH parameters.



BIOS Menu 18: PCH-IO Configuration

➔ **Restore AC Power Loss [Last State]**

Use the **Restore AC Power Loss** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system.

- ➔ **Power Off** The system remains turned off
- ➔ **Power On** The system turns on
- ➔ **Last State** **DEFAULT** The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

➔ **Power Saving Function(ERP) [Disabled]**

Use the **Power Saving Function(ERP)** BIOS option to enable or disable the power saving function.

- ➔ **Disabled** **DEFAULT** Power saving function is disabled.
- ➔ **Enabled** Power saving function is enabled. It will reduce power consumption when the system is off.

➔ **PCIEX16 Power [1 x16 PCIE]**

Use the **PCIEX16 Power** BIOS option to configure the PCIe x16 channel mode on the backplane.

➔ **1 x16 PCIE** **DEFAULT** Sets the PCIe x16 slot as one PCIe x16

➔ **USB SW1 Power [+5V DUAL]**

Use the **USB SW1 Power** BIOS option to configure the USB power source for the corresponding USB connectors (**Table 5-2**).

➔ **+5V** Sets the USB power source to +5V

➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual

➔ **USB SW2 Power [+5V DUAL]**

Use the **USB SW2 Power** BIOS option to configure the USB power source for the corresponding USB connectors (**Table 5-2**).

➔ **+5V** Sets the USB power source to +5V

➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual

BIOS Options	Configured USB Ports
USB SW1 Power	USB_C1 (external USB 2.0 port) USB_C2 (external USB 2.0 port)
USB SW2 Power	USB2 (internal USB 2.0 ports) USB3 (internal USB 2.0 ports) USB4 (internal USB 2.0 port, Type A) CN5 (internal USB 3.1 Gen 1 ports)

Table 5-2: BIOS Options and Configured USB Ports

5.4.1.1 PCI Express Configuration

Use the **PCI Express Configuration** menu (**BIOS Menu 19**) to configure the PCI Express slots on the backplane.

```
Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
                    Chipset
PCI Express Configuration                  | PCIEX4_1 Settings.
                                           |
> PCIEX4_1 Slot                            |
                                           | ----------------------
                                           | →←: Select Screen
                                           | ↑ ↓: Select Item
                                           | Enter: Select
                                           | +/-: Change Opt.
                                           | F1: General Help
                                           | F2: Previous Values
                                           | F3: Optimized Defaults
                                           | F4: Save & Exit
                                           | ESC: Exit
        Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.
```

BIOS Menu 19: PCI Express Configuration

5.4.1.1.1 PCIEX4_1 Slot

Use the **PCIEX4_1 Slot** menu (**BIOS Menu 20**) to configure the **PCIEX4_1** slot settings.

```
Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
        Advanced
PCIe Speed                    [Auto]       | Select PCI Express port
Detect Non-Compliance Device  [Disabled]   | speed.
                                           |
                                           | ----------------------
                                           | →←: Select Screen
                                           | ↑ ↓: Select Item
                                           | Enter: Select
                                           | +/-: Change Opt.
                                           | F1: General Help
                                           | F2: Previous Values
                                           | F3: Optimized Defaults
                                           | F4: Save & Exit
                                           | ESC: Exit
        Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.
```

BIOS Menu 20: PCIEX4_1 Slot Configuration Menu

➔ **PCIe Speed [Auto]**

Use this option to select the support type of the PCI Express slot. The following options are available:

- Auto **Default**
- Gen1
- Gen2

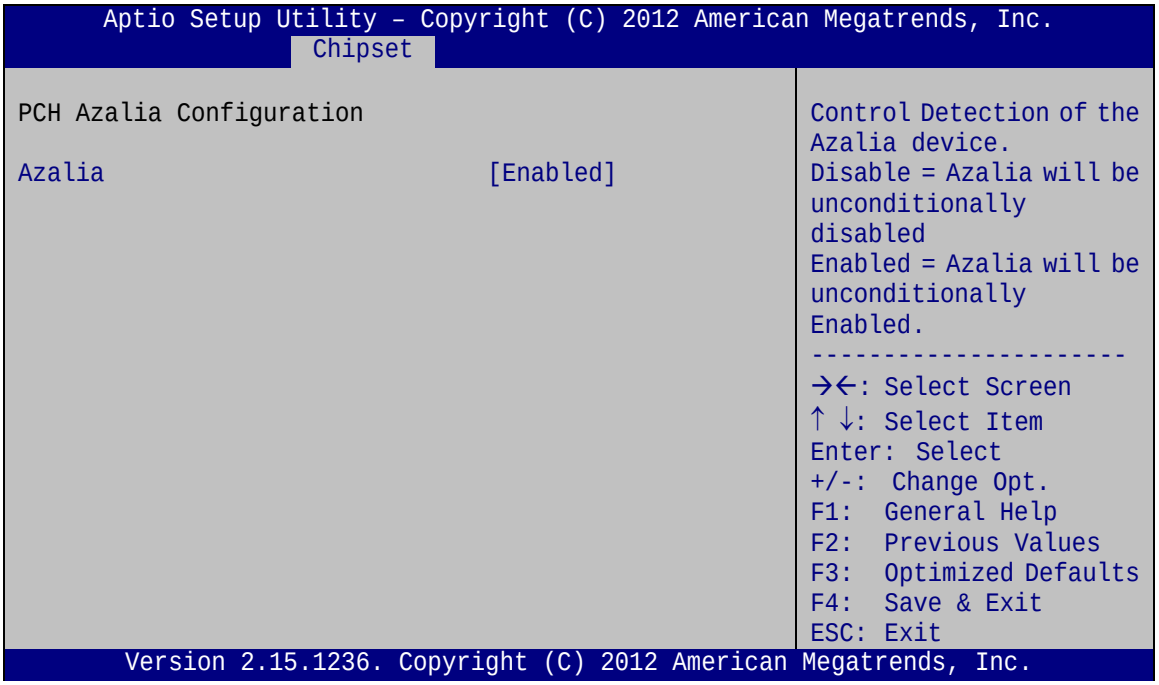
➔ **Detect Non-Compliance Device [Disabled]**

Use the **Detect Non-Compliance Device** option to enable or disable detecting if a non-compliance PCI Express device is connected to the PCI Express slot.

➔ **Disabled**	**DEFAULT**	Disables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.
➔ **Enabled**		Enables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.

5.4.1.2 PCH Azalia Configuration

Use the **PCH Azalia Configuration** menu (**BIOS Menu 21**) to configure the PCH Azalia settings.



BIOS Menu 21: PCH Azalia Configuration

➔ **Azalia [Enabled]**

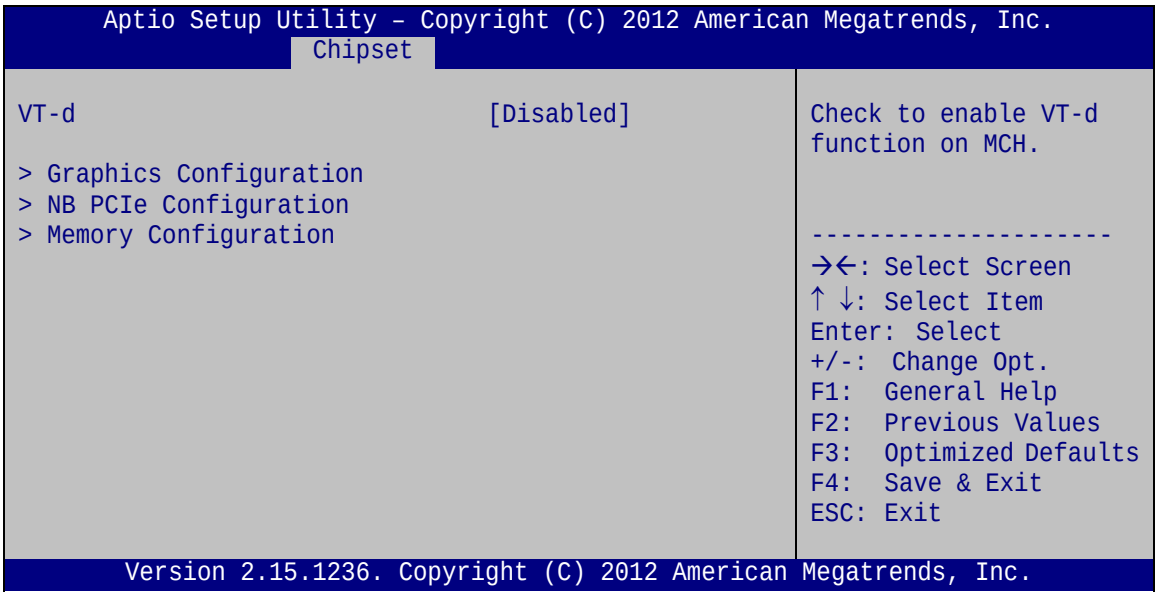
Use the **Azalia** option to enable or disable the High Definition Audio controller.

➔ **Disabled** The onboard High Definition Audio controller is disabled

➔ **Enabled** **DEFAULT** The onboard High Definition Audio controller automatically detected and enabled

5.4.2 System Agent (SA) Configuration

Use the **System Agent (SA) Configuration** menu (**BIOS Menu 22**) to configure the System Agent (SA) parameters.



BIOS Menu 22: System Agent (SA) Configuration

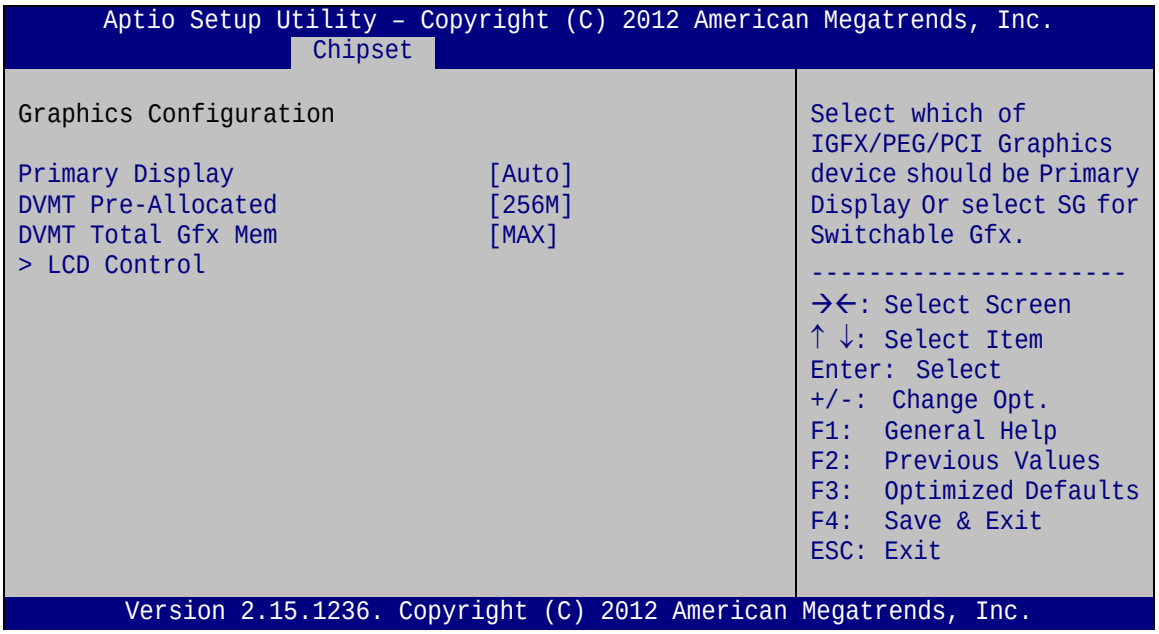
➔ **VT-d [Disabled]**

Use the **VT-d** option to enable or disable VT-d support.

➔	**Disabled**	**DEFAULT**	Disables VT-d support.
➔	**Enabled**		Enables VT-d support.

5.4.2.1 Graphics Configuration

Use the **Graphics Configuration** (**BIOS Menu 23**) menu to configure the video device connected to the system.



BIOS Menu 23: Graphics Configuration

➔ **Primary Display [Auto]**

Use the **Primary Display** option to select the primary graphics controller the system uses. The following options are available:

- Auto **Default**
- IGFX
- PEG
- PCIE/PCI

➔ **DVMT Pre-Allocated [256M]**

Use the **DVMT Pre-Allocated** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

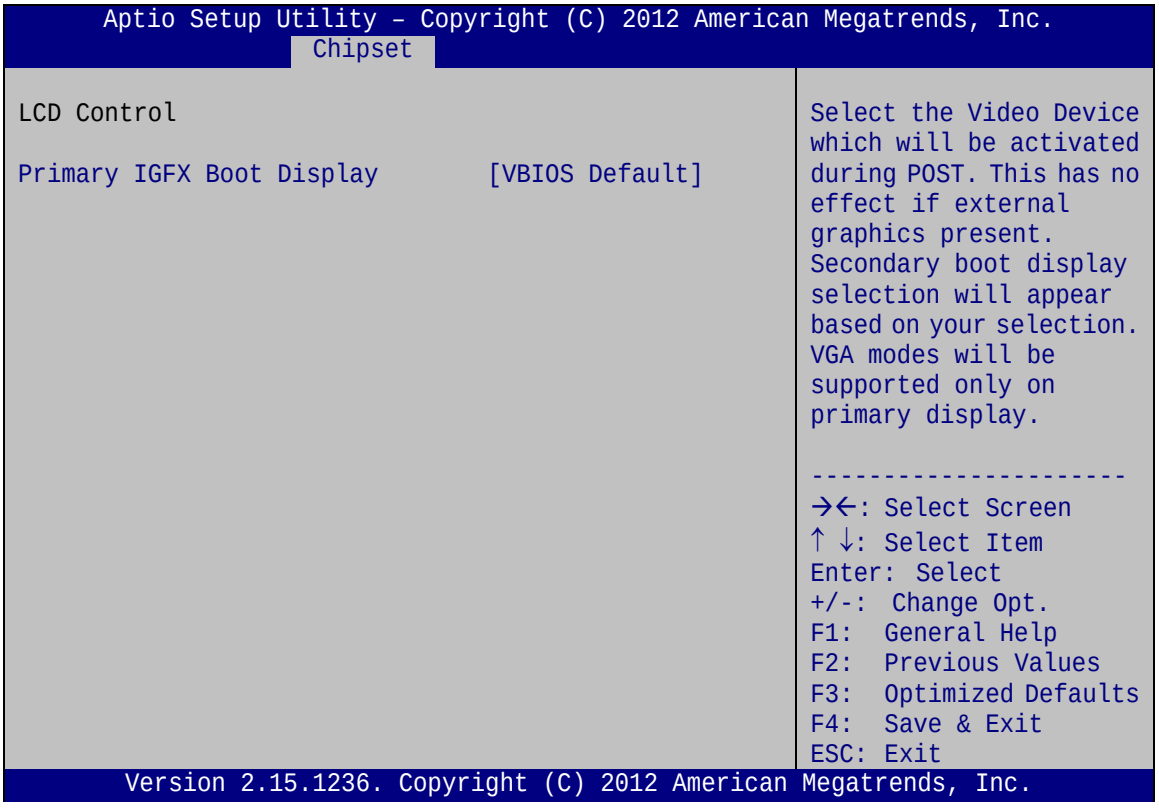
- 32M
- 64M
- 128M
- 256M **Default**
- 512M

➔ **DVMT Total Gfx Mem [MAX]**

Use the **DVMT Total Gfx Mem** option to select DVMT5.0 total graphic memory size used by the internal graphic device. The following options are available:

- 128M
- 256M
- MAX **Default**

5.4.2.1.1 LCD Control



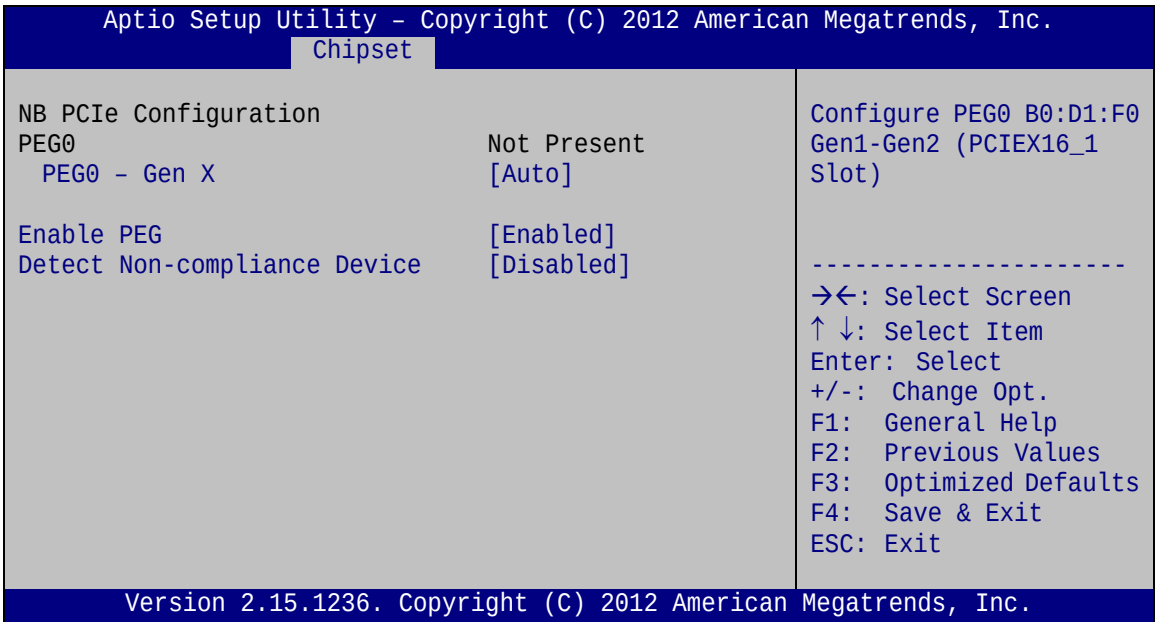
BIOS Menu 24: LCD Control

➔ **Primary IGFX Boot Display [VBIOS Default]**

Use the **Primary IGFX Boot Display** option to select the display device used by the system when it boots. Configuration options are listed below.

- VBIOS Default **DEFAULT**
- CRT
- DP

5.4.2.2 NB PCIe Configuration



BIOS Menu 25: NB PCIe Configuration

➔ **PEG0 – Gen X [Auto]**

Use the **PEG0 – Gen X** option to select the support type of the PCI Express x16 slot. The following options are available:

- Auto **Default**
- Gen1
- Gen2

➔ **Enable PEG [Enabled]**

Use the **Enable PEG** option to enable or disable the PCI Express (PEG) controller.

➔ **Disabled** Disables the PCI Express (PEG) controller.

➔ **Enabled** **DEFAULT** Enables the PCI Express (PEG) controller.

➔ **Auto** The PCI Express (PEG) controller is disabled if no PCI Express devices are connected.

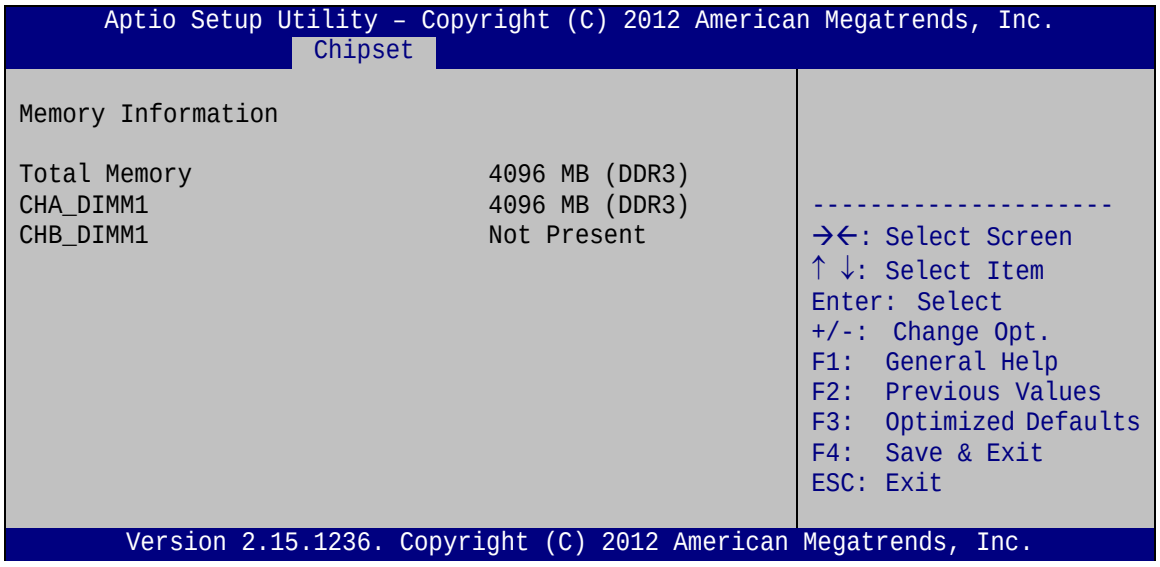
➔ **Detect Non-Compliance Device [Disabled]**

Use the **Detect Non-Compliance Device** option to enable or disable detecting if a non-compliance PCI Express device is connected to the PCI Express port.

➔ **Disabled**	**DEFAULT**	Disables to detect if a non-compliance PCI Express device is connected to the PCI Express port.
➔ **Enabled**		Enables to detect if a non-compliance PCI Express device is connected to the PCI Express port.

5.4.2.3 Memory Configuration

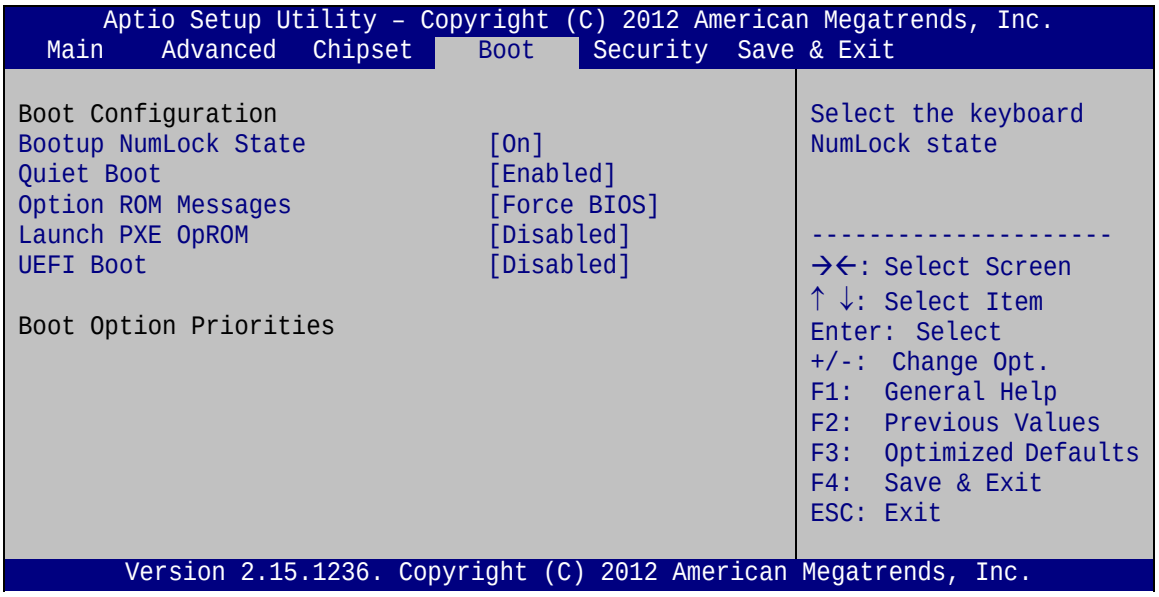
Use the **Memory Configuration** submenu (**BIOS Menu 26**) to view memory information.



BIOS Menu 26: Memory Configuration

5.5 Boot

Use the **Boot** menu (**BIOS Menu 27**) to configure system boot options.



BIOS Menu 27: Boot

➔ **Bootup NumLock State [On]**

Use the **Bootup NumLock State** BIOS option to specify if the number lock setting must be modified during boot up.

➔ **On** **DEFAULT** Allows the Number Lock on the keyboard to be enabled automatically when the computer system boots up. This allows the immediate use of the 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard is lit.

➔ **Off** Does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard lights up when the Number Lock is engaged.

➔ **Quiet Boot [Enabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

➔ **Disabled**		Normal POST messages displayed
➔ **Enabled**	**DEFAULT**	OEM Logo displayed instead of POST messages

➔ **Option ROM Messages [Force BIOS]**

Use the **Option ROM Messages** option to set the Option ROM display mode.

➔ **Force BIOS**	**DEFAULT**	Sets display mode to force BIOS.
➔ **Keep Current**		Sets display mode to current.

➔ **Launch PXE OpROM [Disabled]**

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

➔ **Disabled**	**DEFAULT**	Ignore all PXE Option ROMs
➔ **Enabled**		Load PXE Option ROMs.

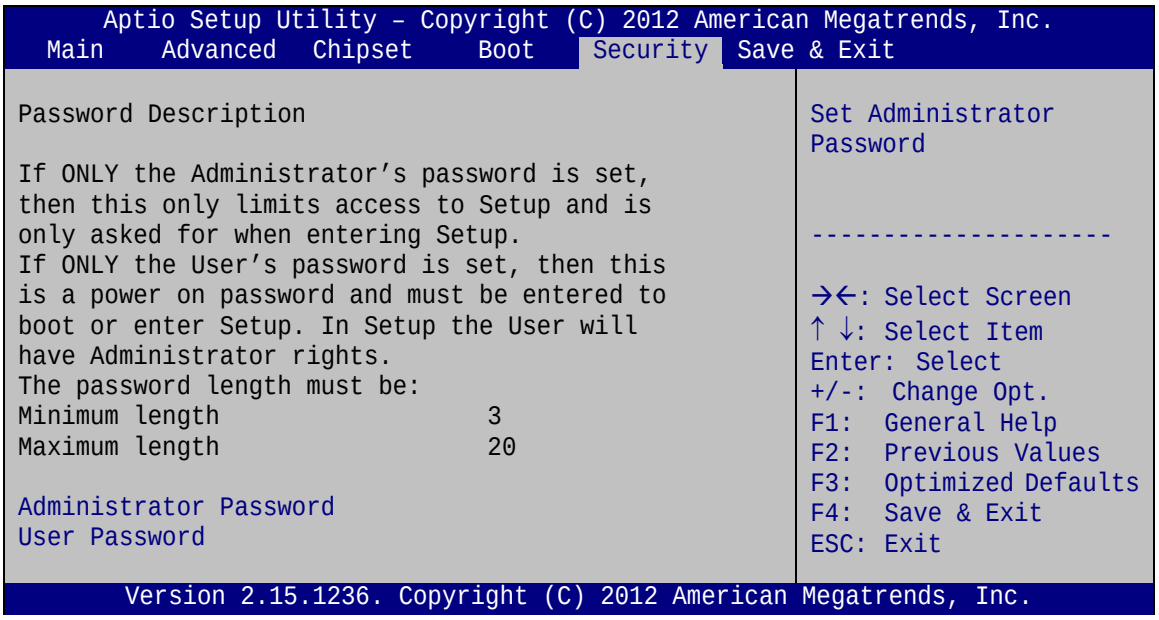
➔ **UEFI Boot [Disabled]**

Use the **UEFI Boot** option to enable or disable to boot from the UEFI devices.

➔ **Enabled**		Boot from UEFI devices is enabled.
➔ **Disabled**	**DEFAULT**	Boot from UEFI devices is disabled.

5.6 Security

Use the **Security** menu (**BIOS Menu 28**) to set system and user passwords.



BIOS Menu 28: Security

➔ **Administrator Password**

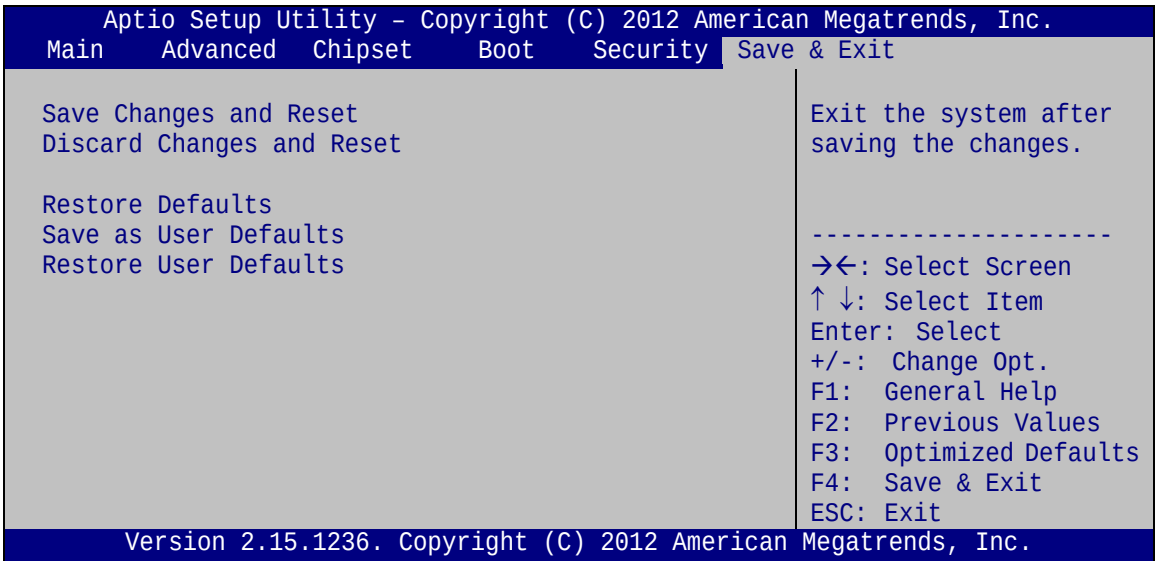
Use the **Administrator Password** to set or change a administrator password.

➔ **User Password**

Use the **User Password** to set or change a user password.

5.7 Save & Exit

Use the **Save & Exit** menu (**BIOS Menu 29**) to load default BIOS values, optimal failsafe values and to save configuration changes.



BIOS Menu 29: Save & Exit

➔ **Save Changes and Reset**

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and reset the system.

➔ **Discard Changes and Reset**

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

➔ **Restore Defaults**

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

➔ **Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

➔ **Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Chapter

6

Software Drivers

6.1 Available Drivers

All the drivers for the PCIE-H810 are available on IEI Resource Download Center (https://download.ieiworld.com). Type PCIE-H810 and press Enter to find all the relevant software, utilities, and documentation.

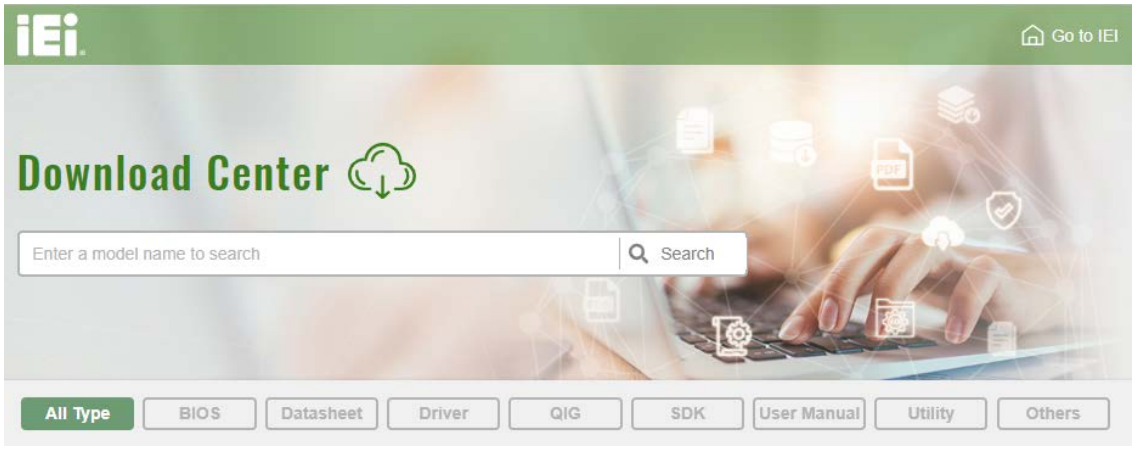
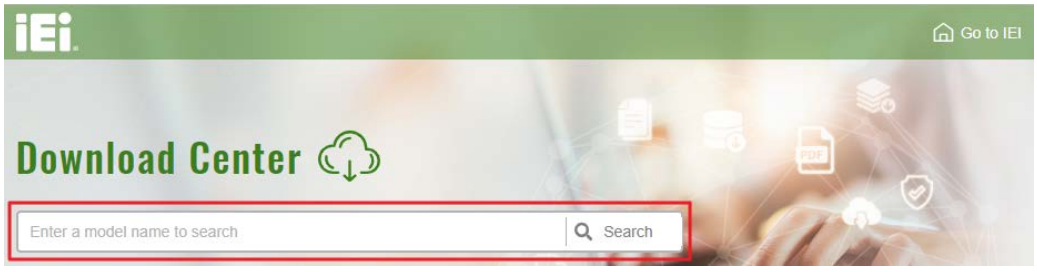


Figure 6-1: IEI Resource Download Center

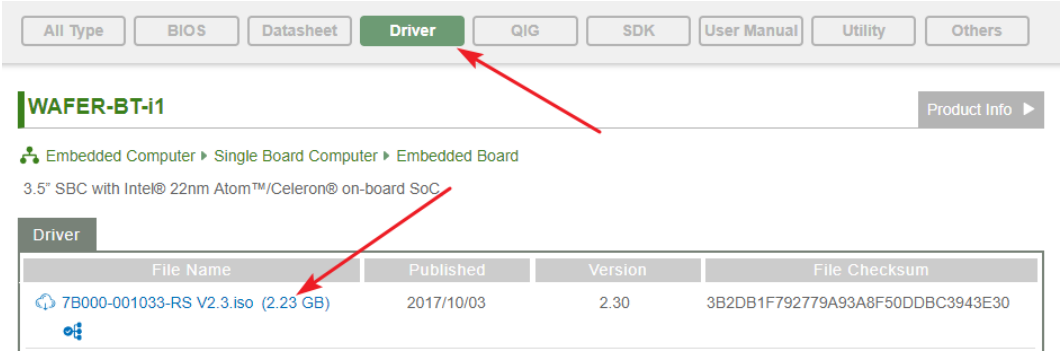
6.2 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

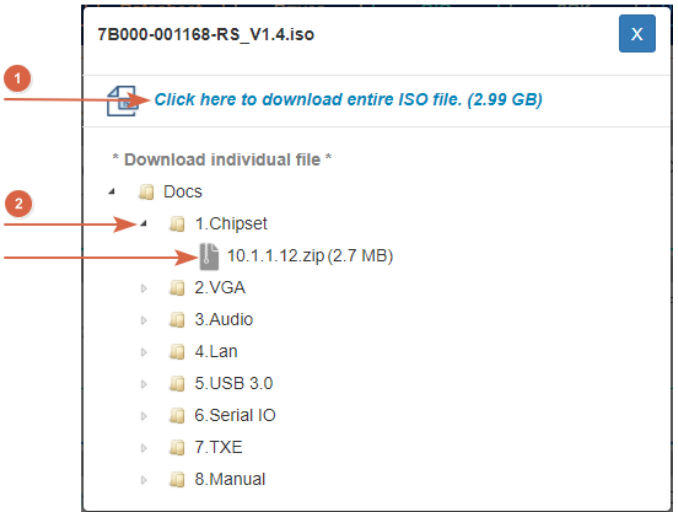
Step 5: Go to https://download.ieiworld.com. Type PCIE-H810 and press Enter.



Step 6: All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.



Step 7: Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (❶), or click the small arrow to find an individual driver and click the file name to download (❷).



NOTE:

To install software from the downloaded ISO image file in Windows 8, 8.1 or 10, double-click the ISO file to mount it as a virtual drive to view its content. On Windows 7 system, an additional tool (such as Virtual CD-ROM Control Panel from Microsoft) is needed to mount the file.

Appendix

A

Regulatory Compliance

DECLARATION OF CONFORMITY

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

BIOS Options

Below is a list of BIOS configuration options in the BIOS chapter.

Appendix

C

Terminology

AC '97	Audio Codec 97 (AC'97) refers to a codec standard developed by Intel® in 1997.
ACPI	Advanced Configuration and Power Interface (ACPI) is an OS-directed configuration, power management, and thermal management interface.
AHCI	Advanced Host Controller Interface (AHCI) is a SATA Host controller register-level interface.
ATA	The Advanced Technology Attachment (ATA) interface connects storage devices including hard disks and CD-ROM drives to a computer.
ARMD	An ATAPI Removable Media Device (ARMD) is any ATAPI device that supports removable media, besides CD and DVD drives.
ASKIR	Amplitude Shift Keyed Infrared (ASKIR) is a form of modulation that represents a digital signal by varying the amplitude ("volume") of the signal. A low amplitude signal represents a binary 0, while a high amplitude signal represents a binary 1.
BIOS	The Basic Input/Output System (BIOS) is firmware that is first run when the computer is turned on and can be configured by the end user
CODEC	The Compressor-Decompressor (CODEC) encodes and decodes digital audio data on the system.
CMOS	Complimentary metal-oxide-conductor is an integrated circuit used in chips like static RAM and microprocessors.
COM	COM refers to serial ports. Serial ports offer serial communication to expansion devices. The serial port on a personal computer is usually a male DB-9 connector.
DAC	The Digital-to-Analog Converter (DAC) converts digital signals to analog signals.
DDR	Double Data Rate refers to a data bus transferring data on both the rising and falling edges of the clock signal.
DMA	Direct Memory Access (DMA) enables some peripheral devices to bypass the system processor and communicate directly with the system memory.

DIMM	Dual Inline Memory Modules are a type of RAM that offer a 64-bit data bus and have separate electrical contacts on each side of the module.
DIO	The digital inputs and digital outputs are general control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.
EHCI	The Enhanced Host Controller Interface (EHCI) specification is a register-level interface description for USB 2.0 Host Controllers.
EIDE	Enhanced IDE (EIDE) is a newer IDE interface standard that has data transfer rates between 4.0 MBps and 16.6 MBps.
EIST	Enhanced Intel® SpeedStep Technology (EIST) allows users to modify the power consumption levels and processor performance through application software. The application software changes the bus-to-core frequency ratio and the processor core voltage.
FSB	The Front Side Bus (FSB) is the bi-directional communication channel between the processor and the Northbridge chipset.
GbE	Gigabit Ethernet (GbE) is an Ethernet version that transfers data at 1.0 Gbps and complies with the IEEE 802.3-2005 standard.
GPIO	General purpose input
HDD	Hard disk drive (HDD) is a type of magnetic, non-volatile computer storage device that stores digitally encoded data.
ICH	The Input/Output Control Hub (ICH) is an Intel® Southbridge chipset.
IrDA	Infrared Data Association (IrDA) specify infrared data transmission protocols used to enable electronic devices to wirelessly communicate with each other.
L1 Cache	The Level 1 Cache (L1 Cache) is a small memory cache built into the system processor.
L2 Cache	The Level 2 Cache (L2 Cache) is an external processor memory cache.
LCD	Liquid crystal display (LCD) is a flat, low-power display device that consists of two polarizing plates with a liquid crystal panel in between.

LVDS	Low-voltage differential signaling (LVDS) is a dual-wire, high-speed differential electrical signaling system commonly used to connect LCD displays to a computer.
POST	The Power-on Self Test (POST) is the pre-boot actions the system performs when the system is turned-on.
RAM	Random Access Memory (RAM) is volatile memory that loses data when power is lost. RAM has very fast data transfer rates compared to other storage like hard drives.
SATA	Serial ATA (SATA) is a serial communications bus designed for data transfers between storage devices and the computer chipsets. The SATA bus has transfer speeds up to 1.5 Gbps and the SATA II bus has data transfer speeds of up to 3.0 Gbps.
S.M.A.R.T	Self Monitoring Analysis and Reporting Technology (S.M.A.R.T) refers to automatic status checking technology implemented on hard disk drives.
UART	Universal Asynchronous Receiver-transmitter (UART) is responsible for asynchronous communications on the system and manages the system's serial communication (COM) ports.
UHCI	The Universal Host Controller Interface (UHCI) specification is a register-level interface description for USB 1.1 Host Controllers.
USB	The Universal Serial Bus (USB) is an external bus standard for interfacing devices. USB 1.1 supports 12Mbps data transfer rates and USB 2.0 supports 480Mbps data transfer rates.
VGA	The Video Graphics Array (VGA) is a graphics display system developed by IBM.

Appendix

D

Digital I/O Interface

The DIO connector on the PCIE-H810 is interfaced to GPIO ports on the Super I/O chipset. The DIO has both 8-bit digital inputs and 8-bit digital outputs. The digital inputs and digital outputs are generally control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.

NOTE:

For further information, please refer to the datasheet for the Super I/O chipset.

The BIOS interrupt call **INT 15H** controls the digital I/O.

INT 15H:

AH – 6FH	
Sub-function:	
AL – 8	:Set the digital port as INPUT
AL	:Digital I/O input value

Assembly Language Sample 1

```
MOV     AX, 6F08H       ;setting the digital port as input
INT     15H             ;
```

AL low byte = value

AH – 6FH	
Sub-function:	
AL – 9	:Set the digital port as OUTPUT
BL	:Digital I/O output value

Assembly Language Sample 2

```
MOV     AX, 6F09H       ;setting the digital port as output
MOV     BL, 09H                 ;digital value is 09H
INT     15H             ;
```

Digital Output is 1001b

Appendix

E

Watchdog Timer

NOTE:

The following discussion applies to DOS environment. Contact IEI support or visit the IEI website for specific drivers for other operating systems.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMIs or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table E-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

NOTE:

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

EXAMPLE PROGRAM:

```
; INITIAL TIMER PERIOD COUNTER

;
W_LOOP:
;

        MOV     AX, 6F02H       ;setting the time-out value
        MOV     BL, 30          ;time-out value is 48 seconds
        INT     15H

;
; ADD THE APPLICATION PROGRAM HERE
;

        CMP     EXIT_AP, 1      ;is the application over?
        JNE     W_LOOP          ;No, restart the application

        MOV     AX, 6F02H       ;disable Watchdog Timer
        MOV     BL, 0           ;
        INT     15H

;
; EXIT ;
```

Appendix

F

Hazardous Materials Disclosure

The details provided in this appendix are to ensure that the product is compliant with the Peoples Republic of China (China) RoHS standards. The table below acknowledges the presences of small quantities of certain materials in the product, and is applicable to China RoHS only.

A label will be placed on each product to indicate the estimated "Environmentally Friendly Use Period" (EFUP). This is an estimate of the number of years that these substances would "not leak out or undergo abrupt change." This product may contain replaceable sub-assemblies/components which have a shorter EFUP such as batteries and lamps. These components will be separately marked.

Please refer to the following table.

Part Name	Toxic or Hazardous Substances and Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
Housing	O	O	O	O	O	O
Display	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O
Battery	O	O	O	O	O	O

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in SJ/T11363-2006 (now replaced by GB/T 26572-2011).

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in SJ/T11363-2006 (now replaced by GB/T 26572-2011).

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有"环境友好使用期限"的标签，此期限是估算这些物质"不会有泄漏或突变"的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	O	O	O	O	O	O
显示	O	O	O	O	O	O
印刷电路板	O	O	O	O	O	O
金属螺帽	O	O	O	O	O	O
电缆组装	O	O	O	O	O	O
风扇组装	O	O	O	O	O	O
电力供应组装	O	O	O	O	O	O
电池	O	O	O	O	O	O

O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T 11363-2006 (现由 GB/T 26572-2011 取代) 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 (现由 GB/T 26572-2011 取代) 标准规定的限量要求。