

CET0 / conga-MEVAL

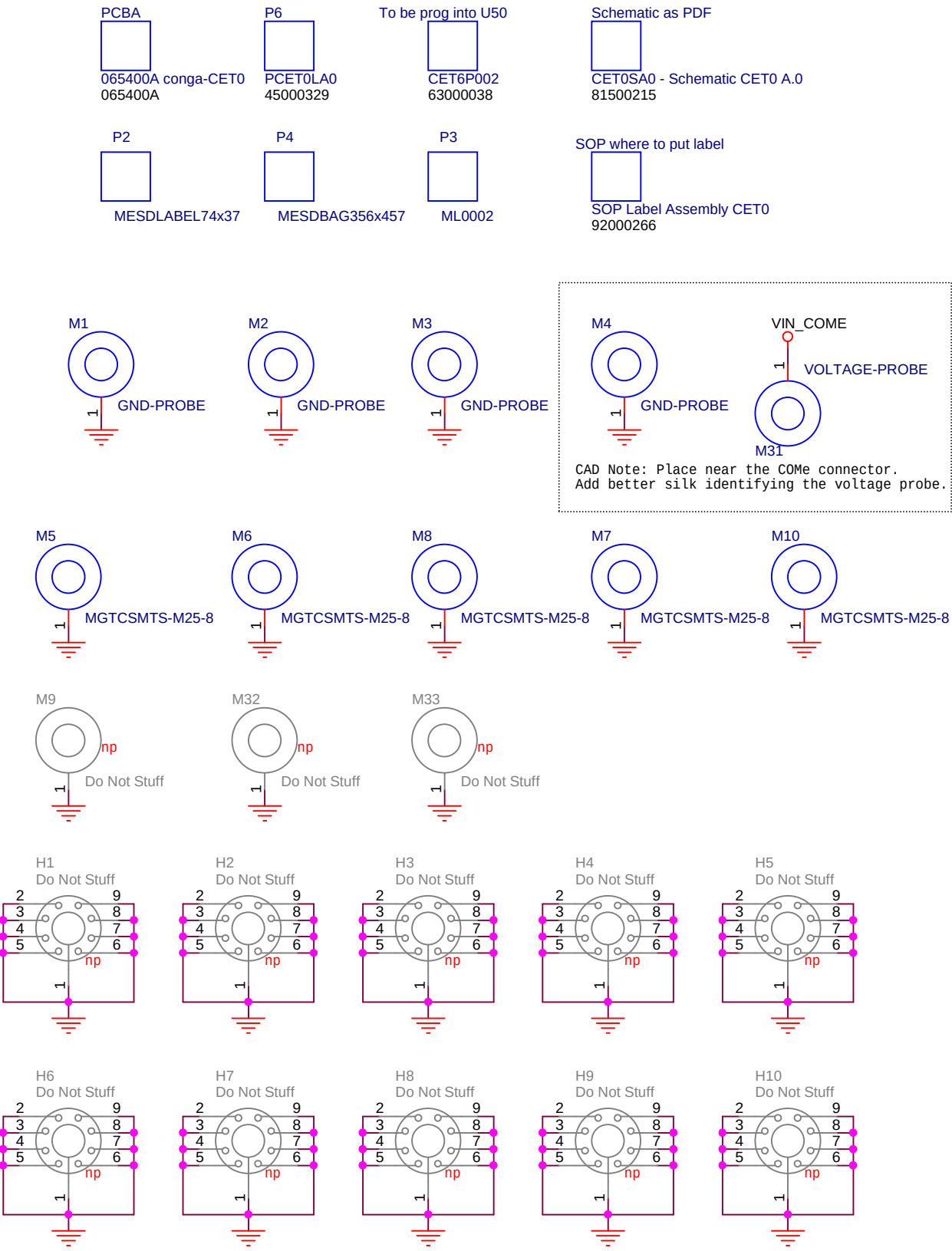
COM Express Type 10 Eval Board

Rev. A.2

Mini, Compact, & Basic

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Title

CET0 - COM Express Type 10 Evaluation Board

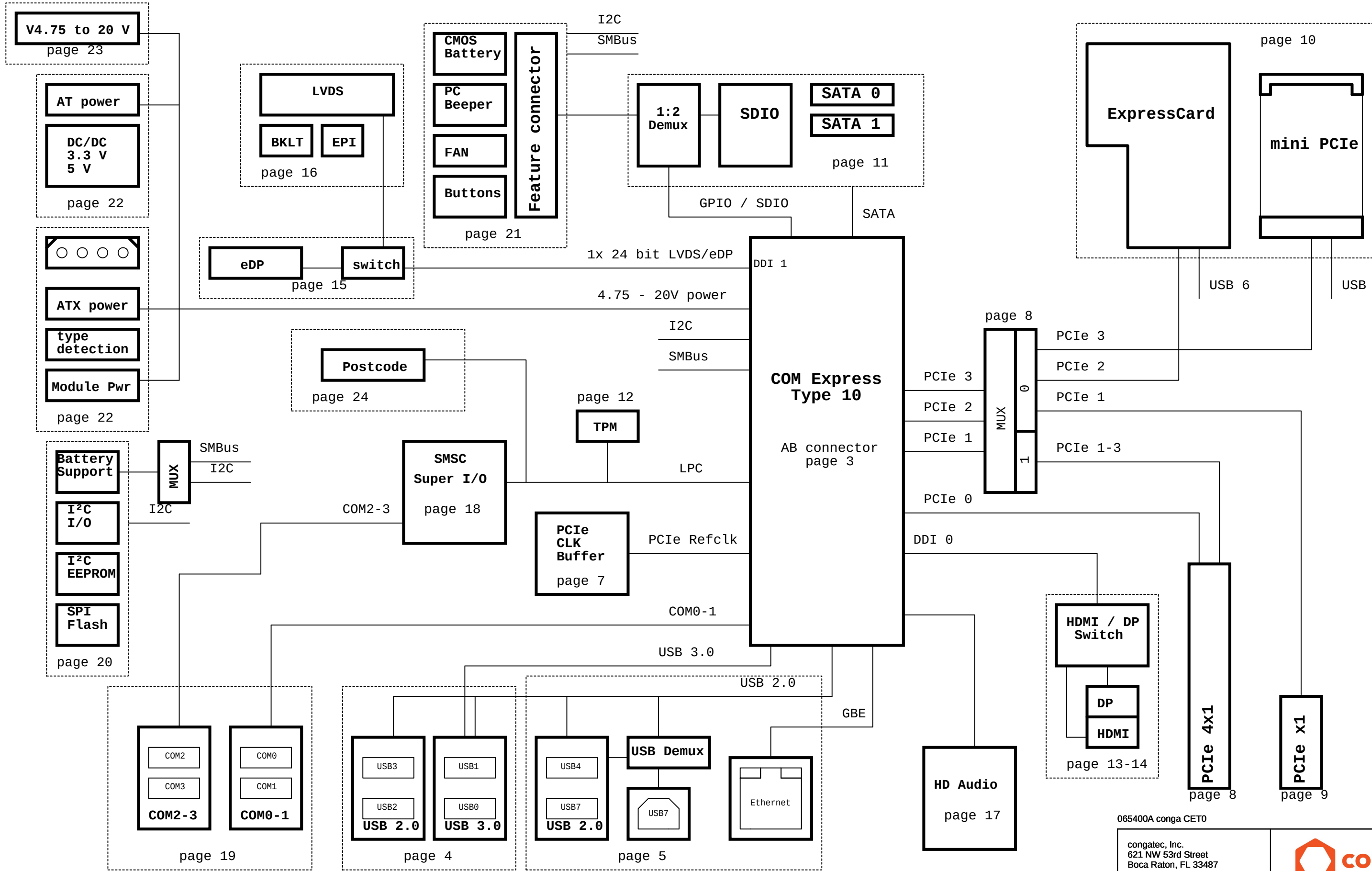
Size B

Document Number
CET0SA2

Created VRO

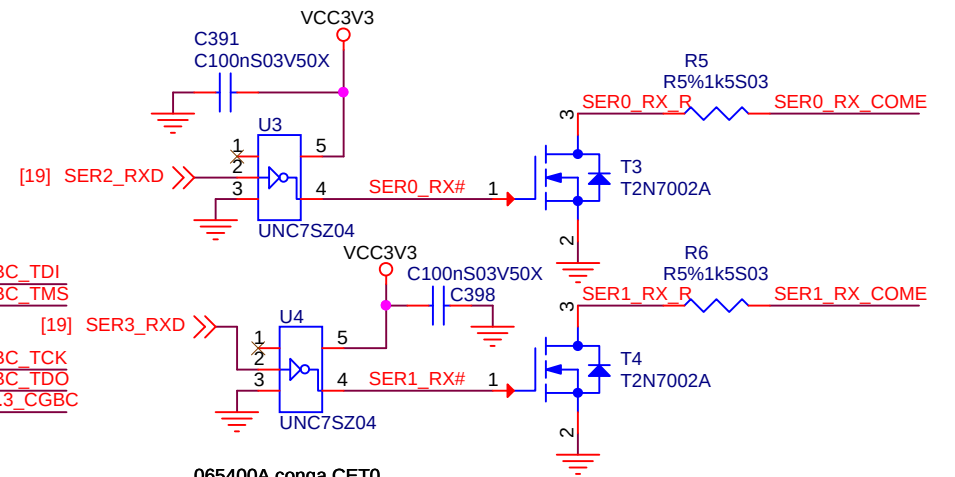
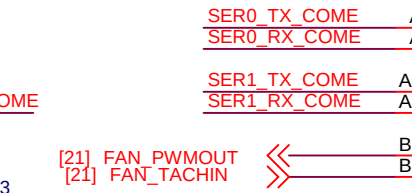
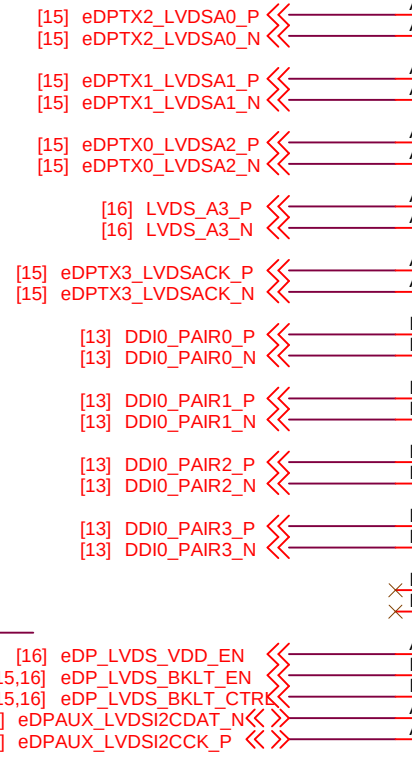
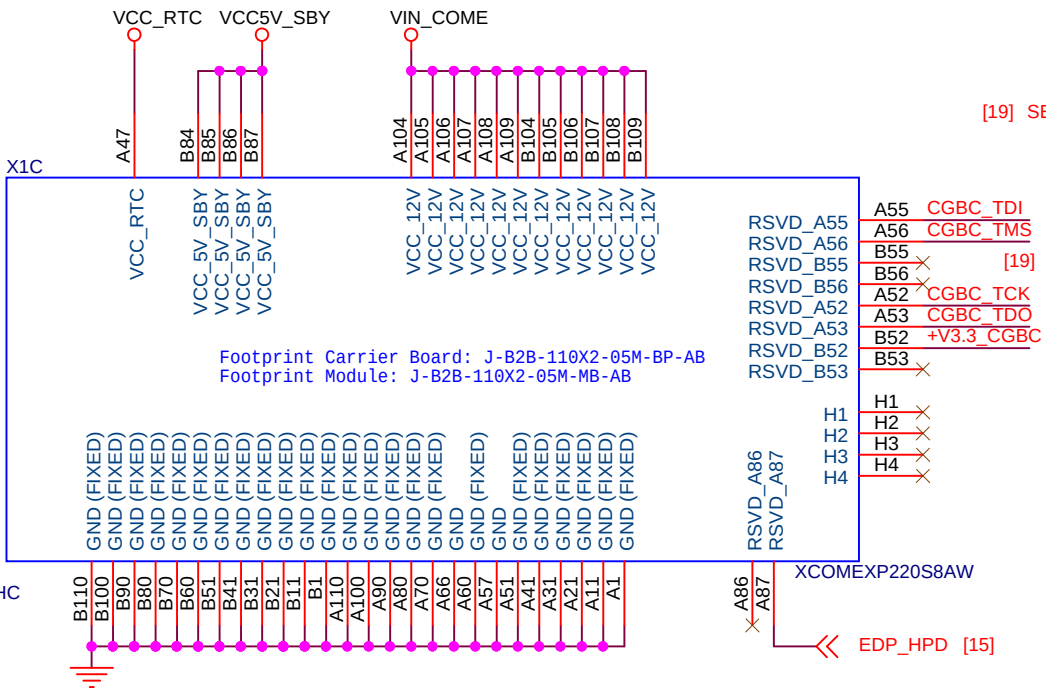
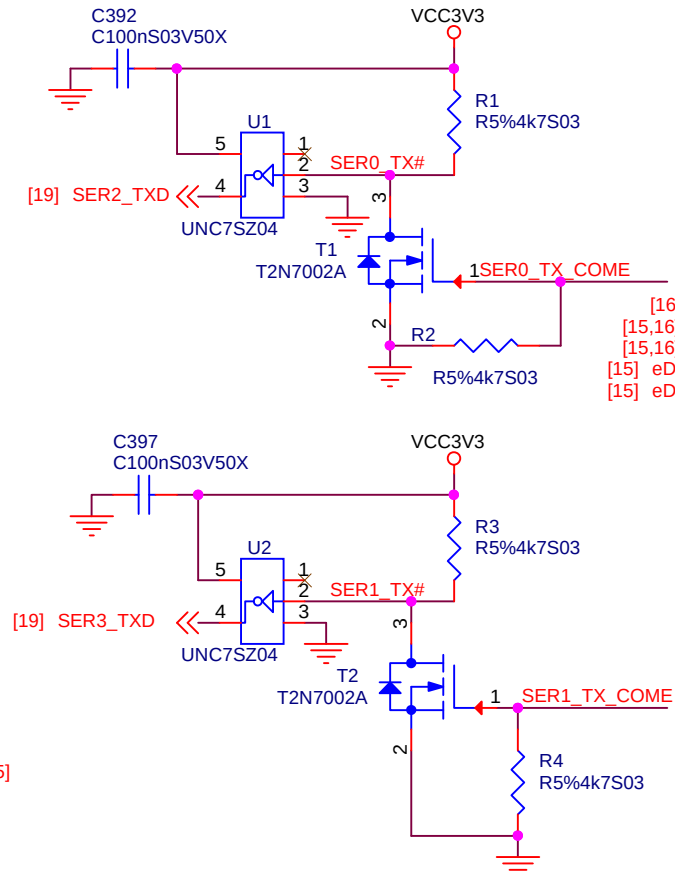
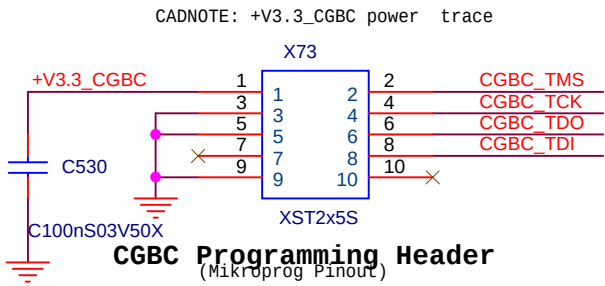
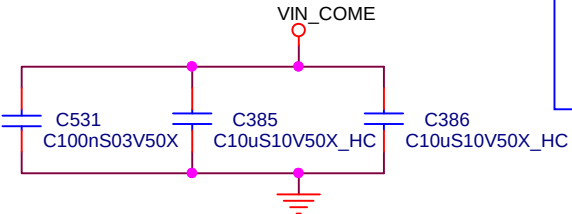
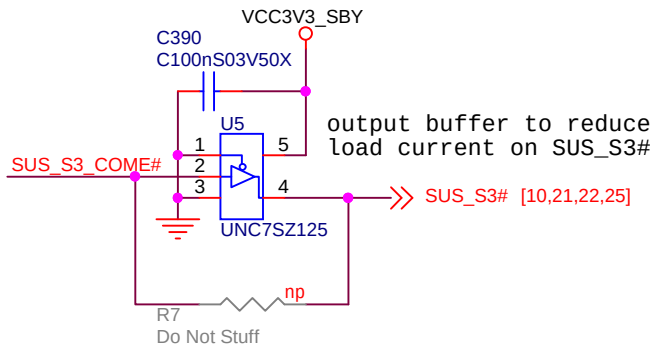
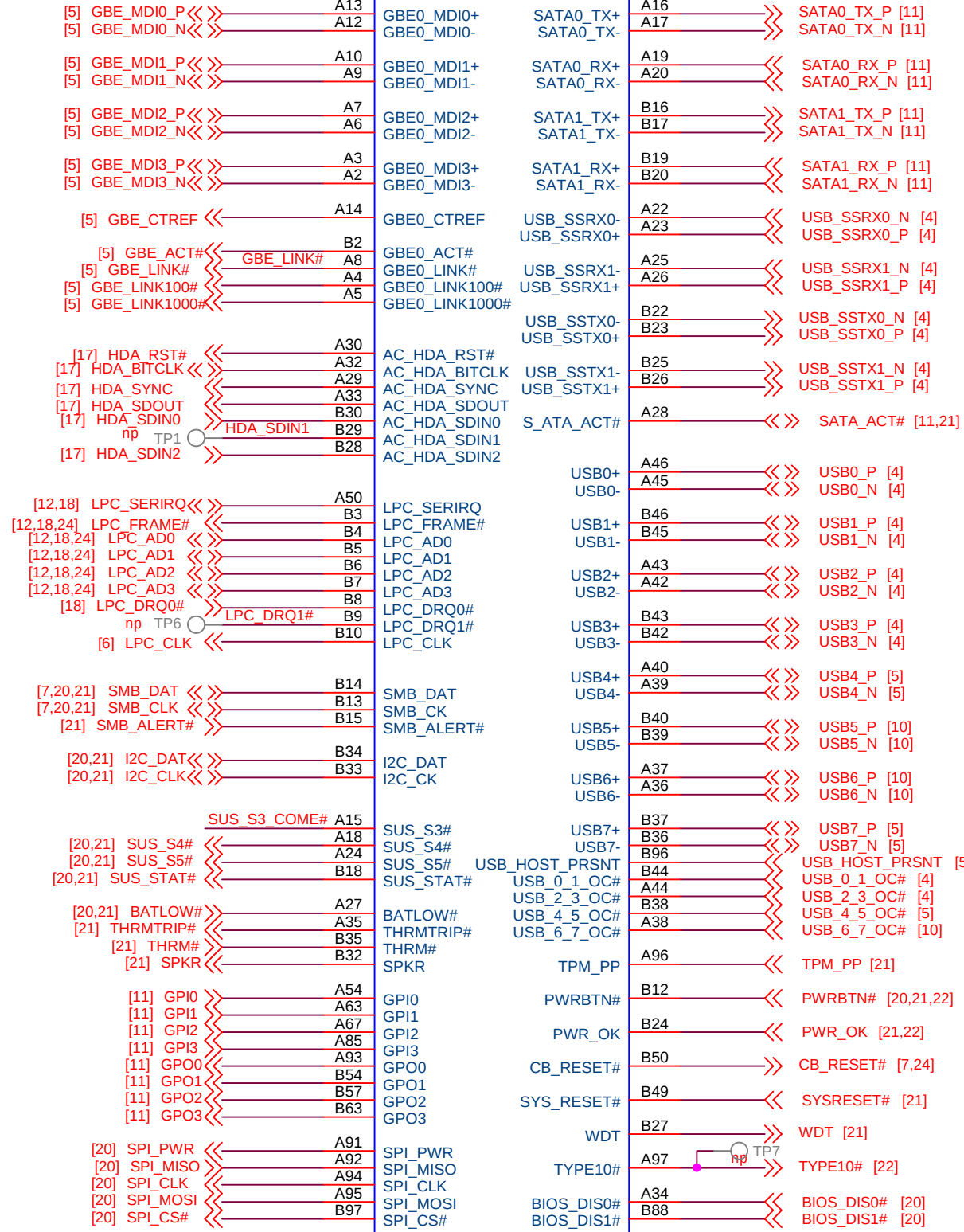
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**CET0 / conga-MEVAL COM Express Type 10
Basic, Compact, Mini Carrier Board**

COM Express Conn



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Title	COM Express Type 6 AB connector
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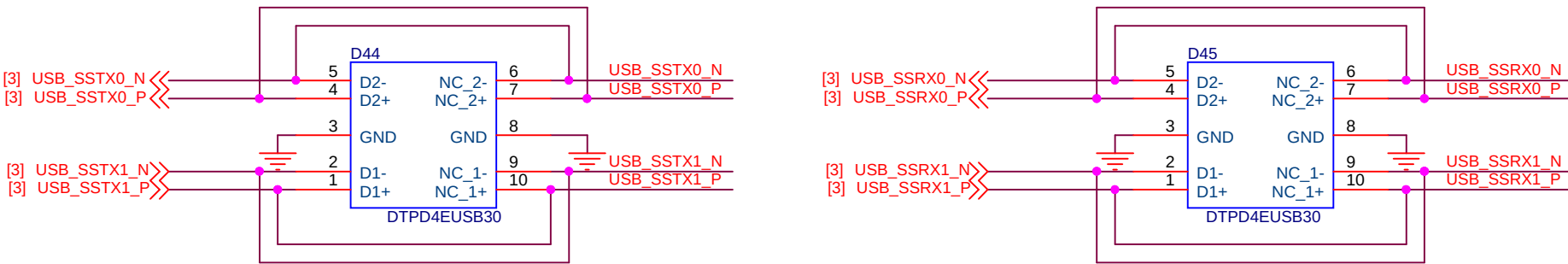
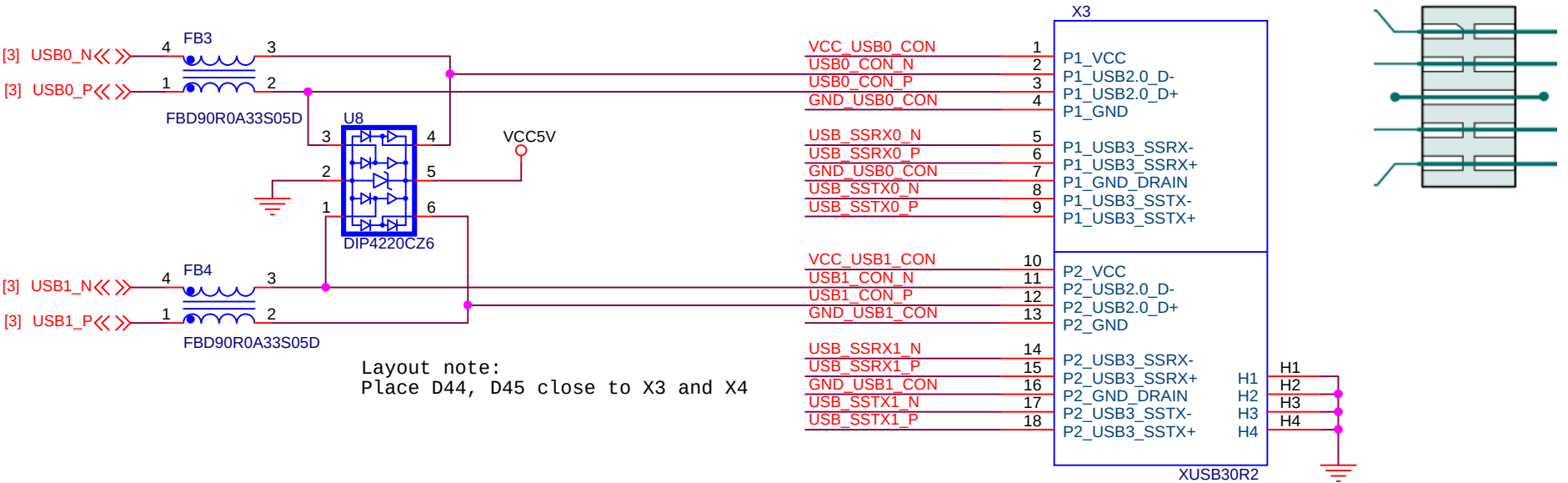
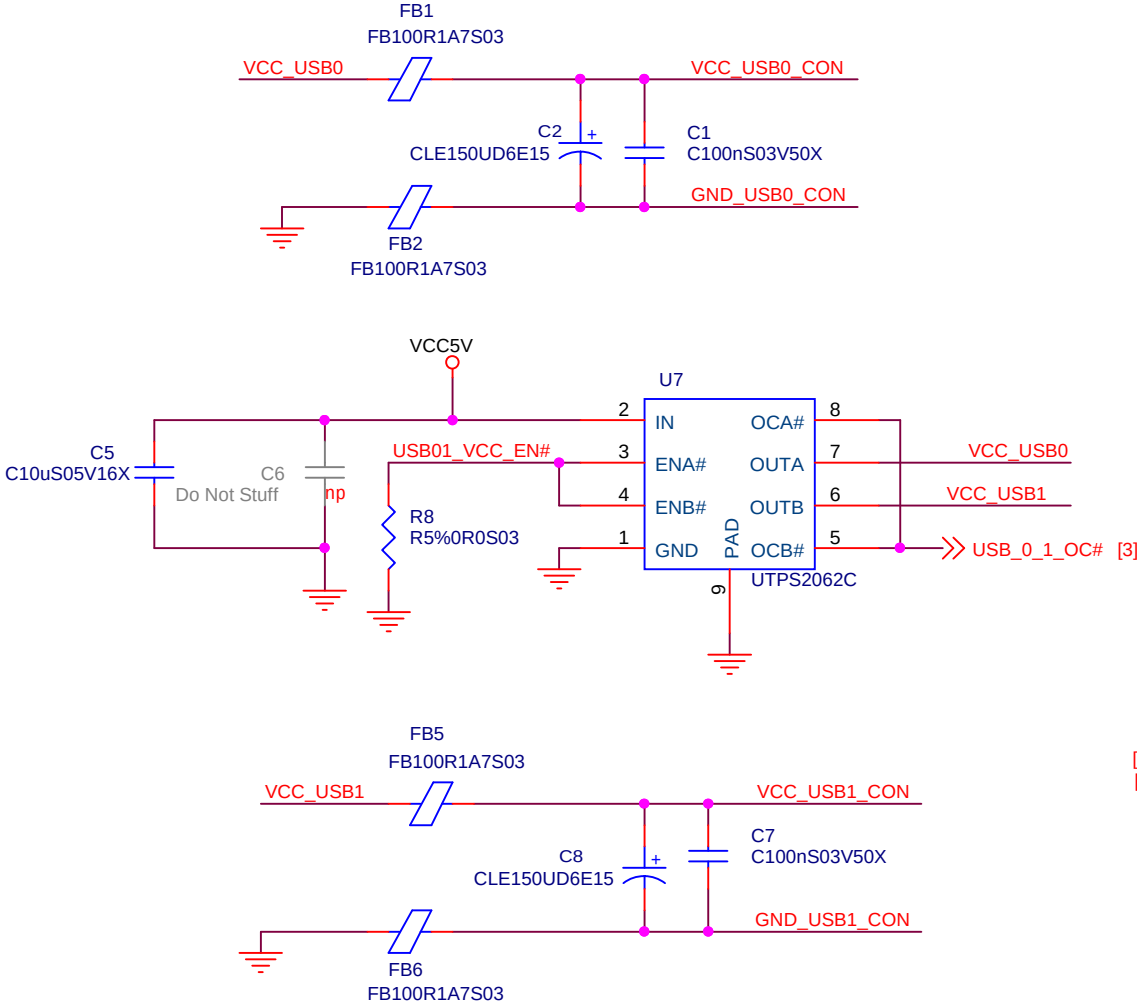
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USB0-2

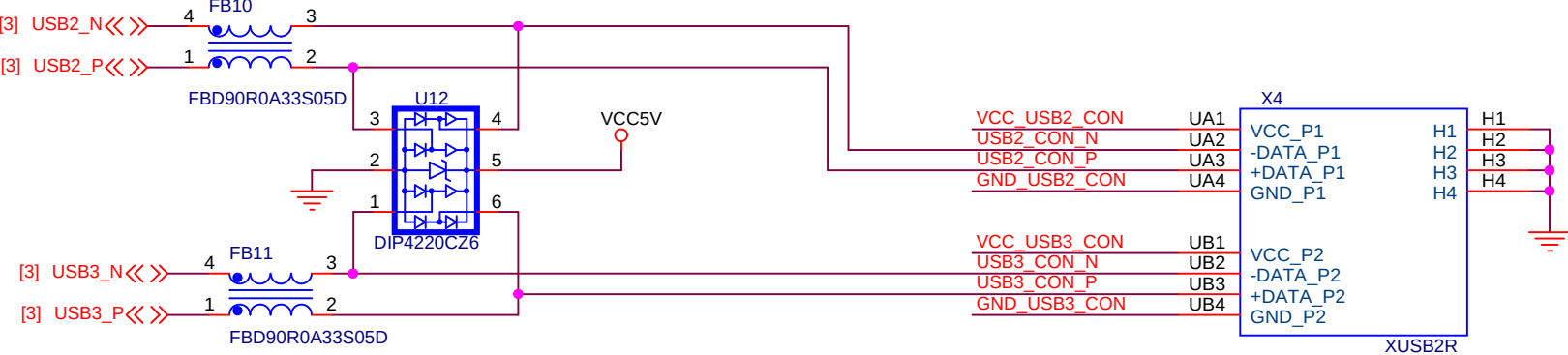
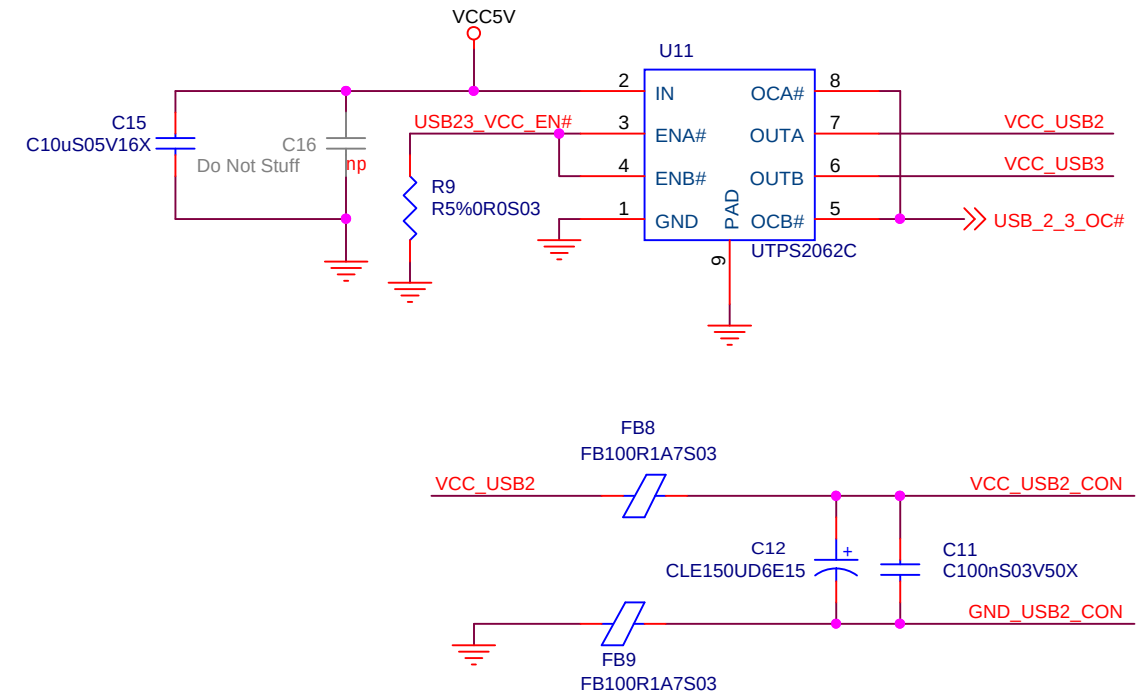
USB 3.0

USB 3.0 spec. requires
low ESR cap ($\geq 120\text{ uF}$)
directly connected to I/O connector

Layout Note: Route USB 3.0 signals through
D44, D45, D46, D47 in the following style



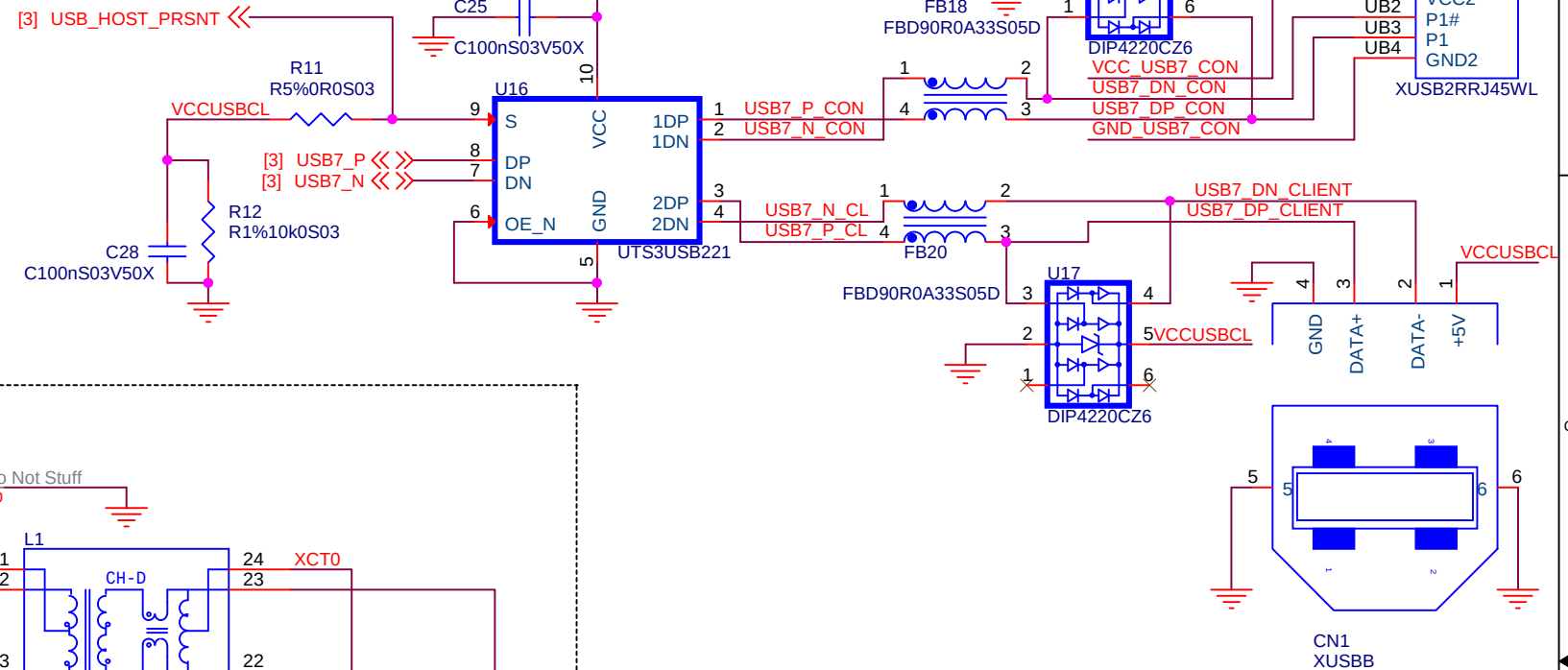
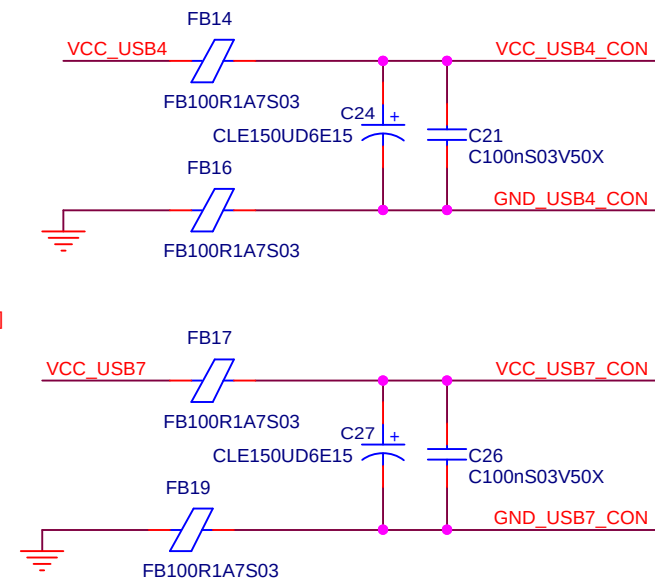
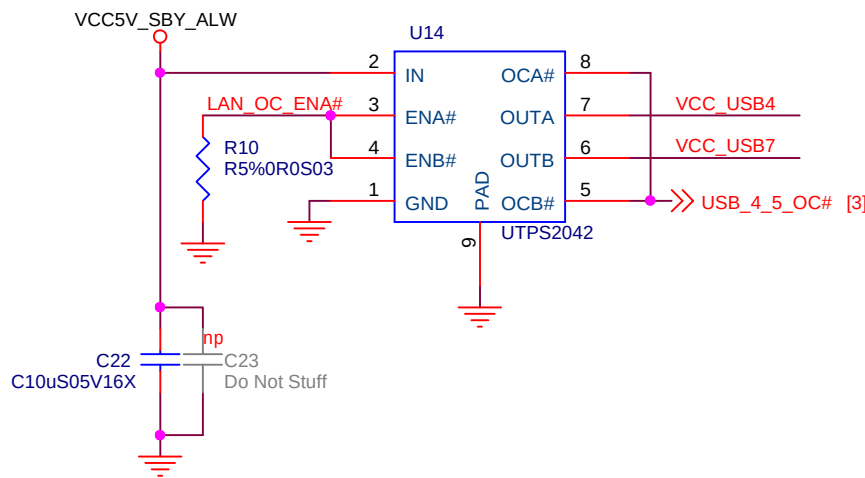
USB 2.0



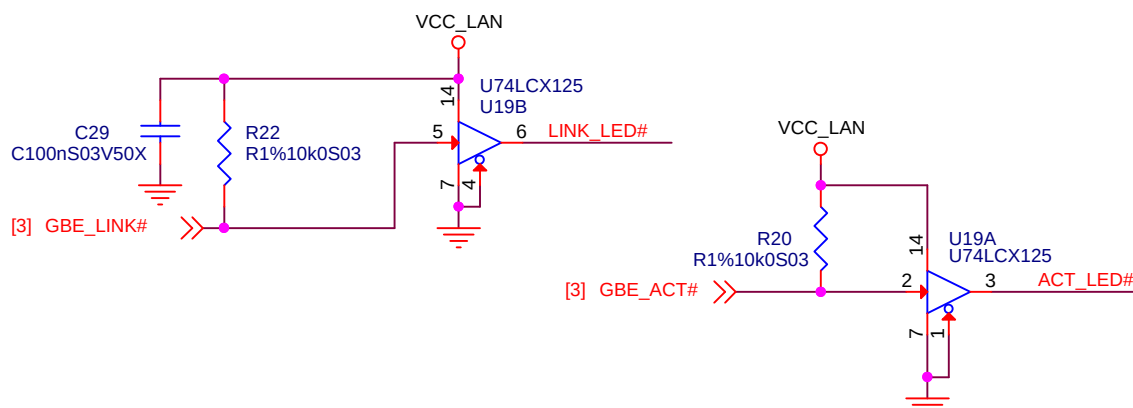
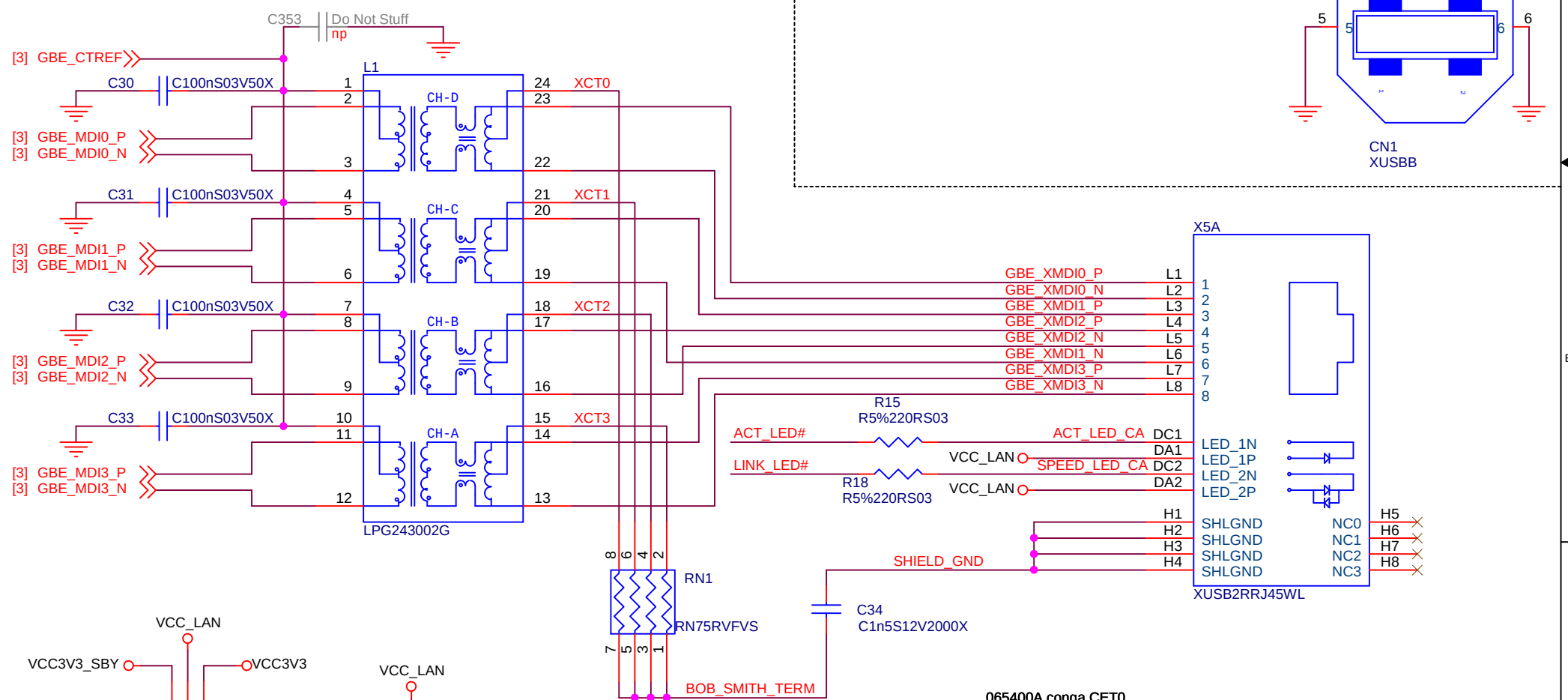
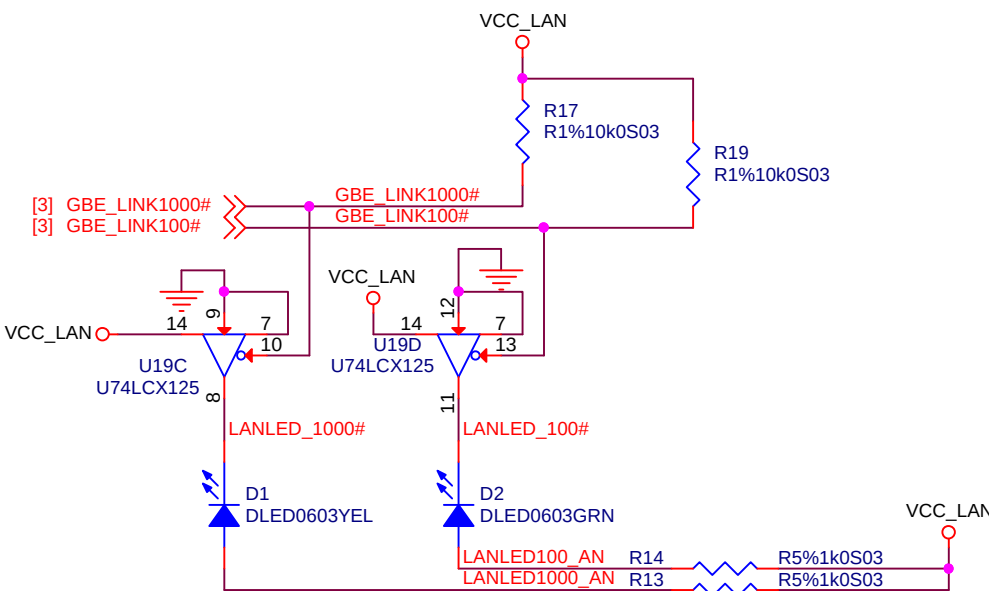
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Title USB 3.0				
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USB - LAN



Gigabit LAN



set jumper 1-2 if LAN Controller is powered from standby voltage (default)
set jumper 2-3 if LAN Controller is powered from S0 voltage

Layout note:
GND void under magnetics
See section 12.5.5 of I210 DG
for layout guidelines.

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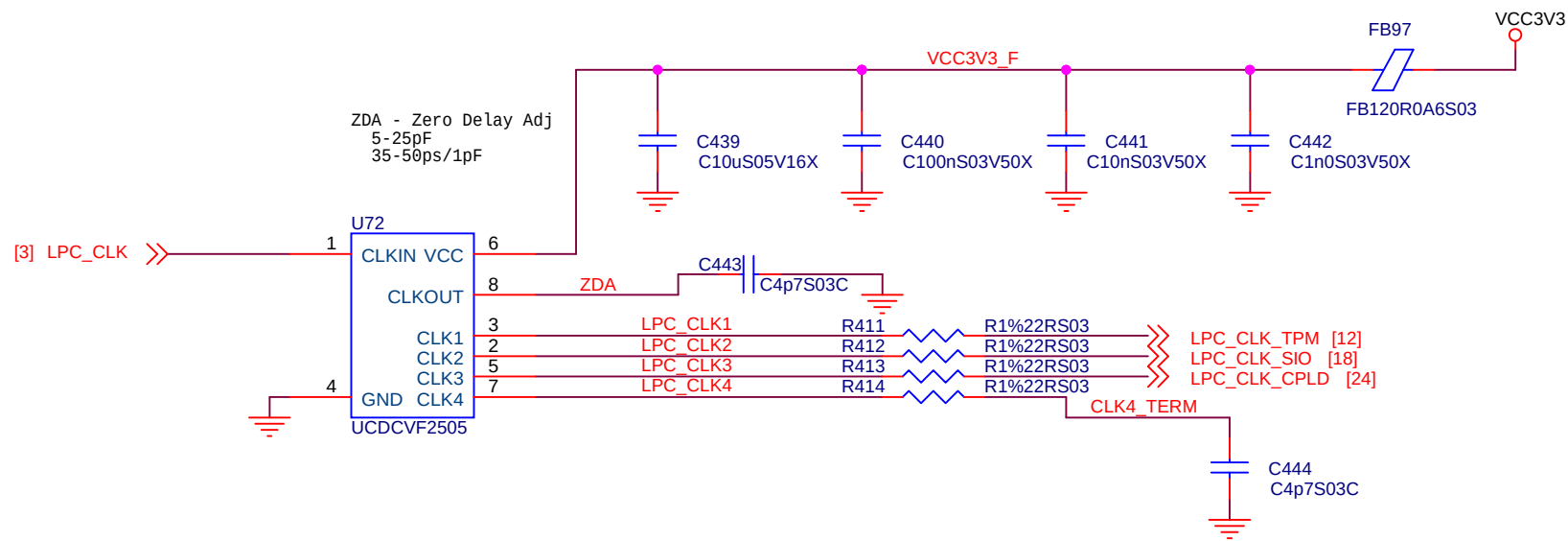
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USA



Title
USB 2.0, Gigabit Ethernet

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LPC CLK BUFFER



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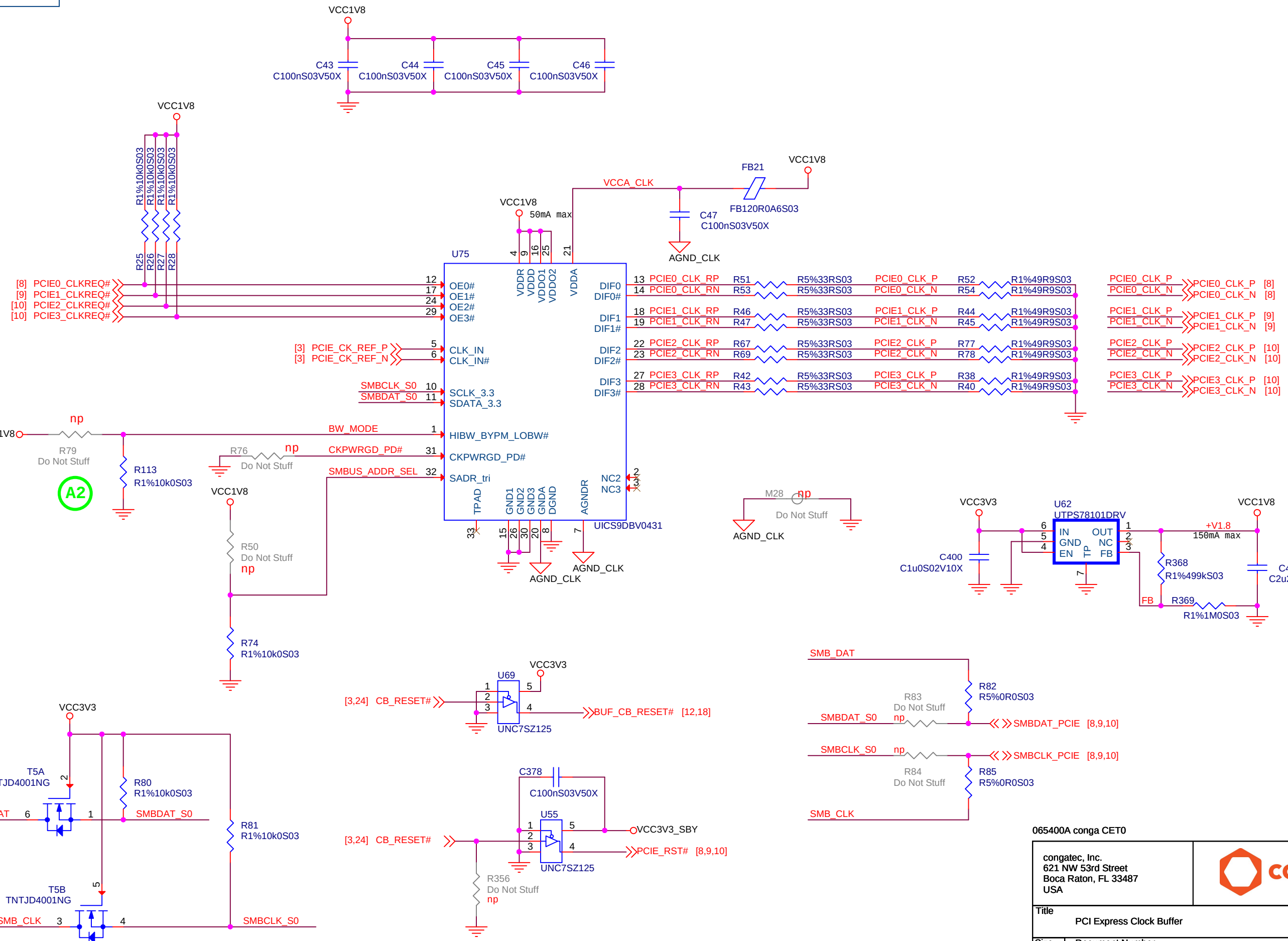
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Title
LPC CLOCK BUFFER

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PCIE CLK BUFFER



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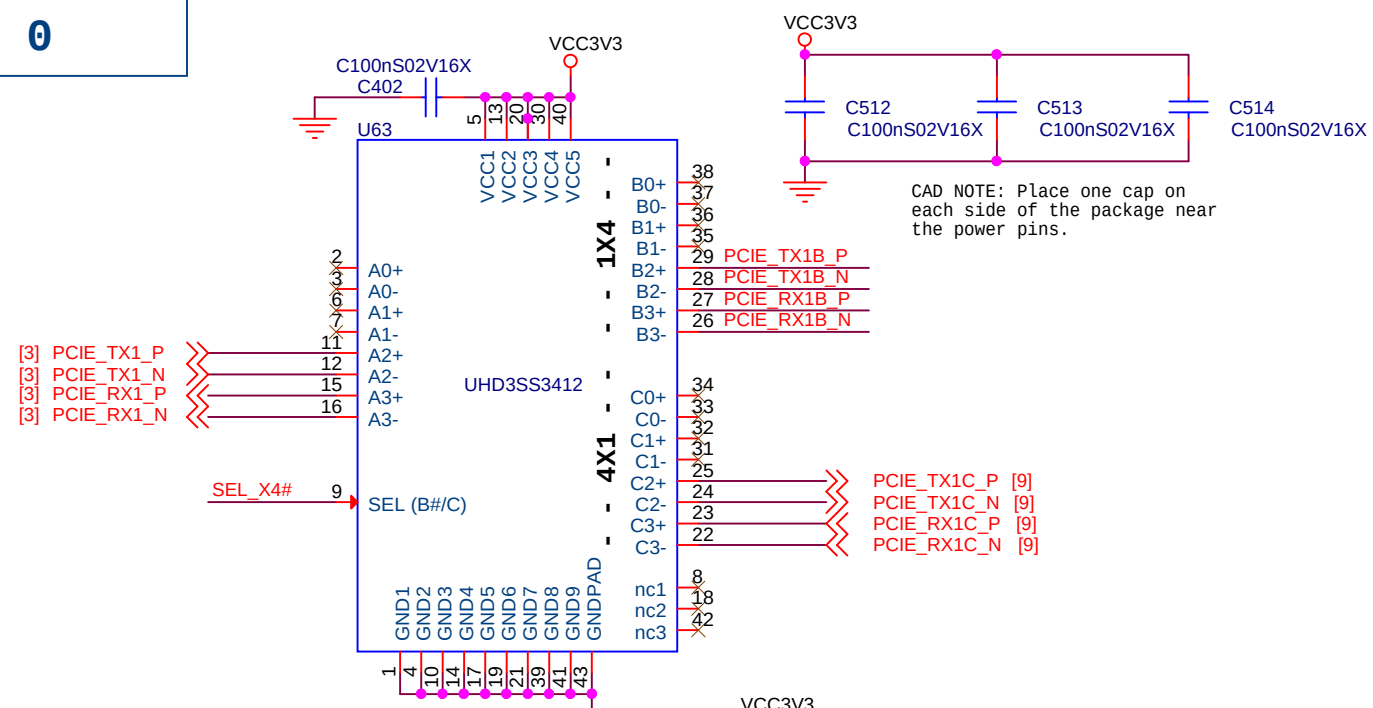
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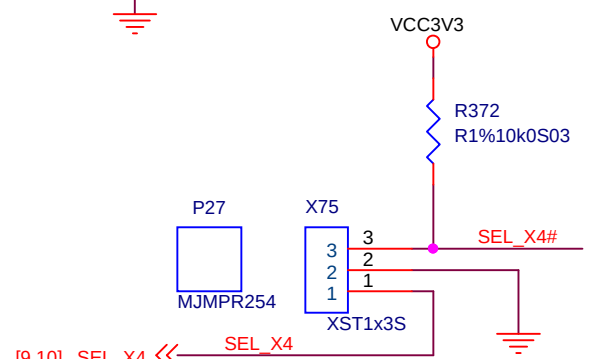
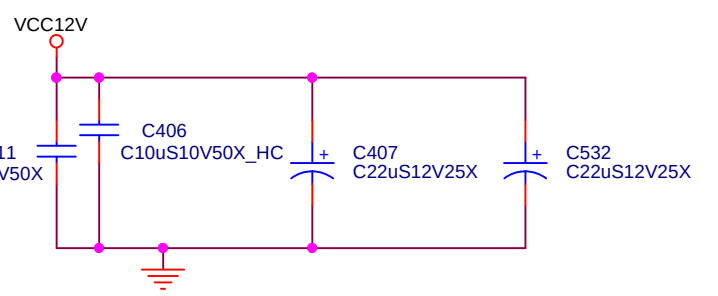
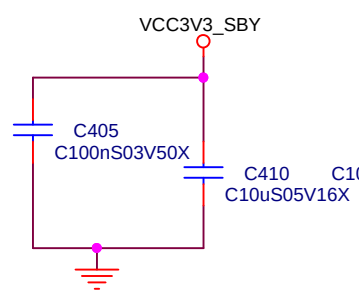
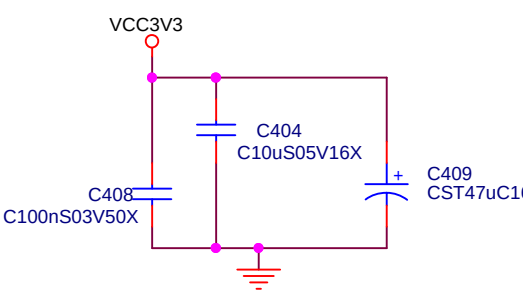
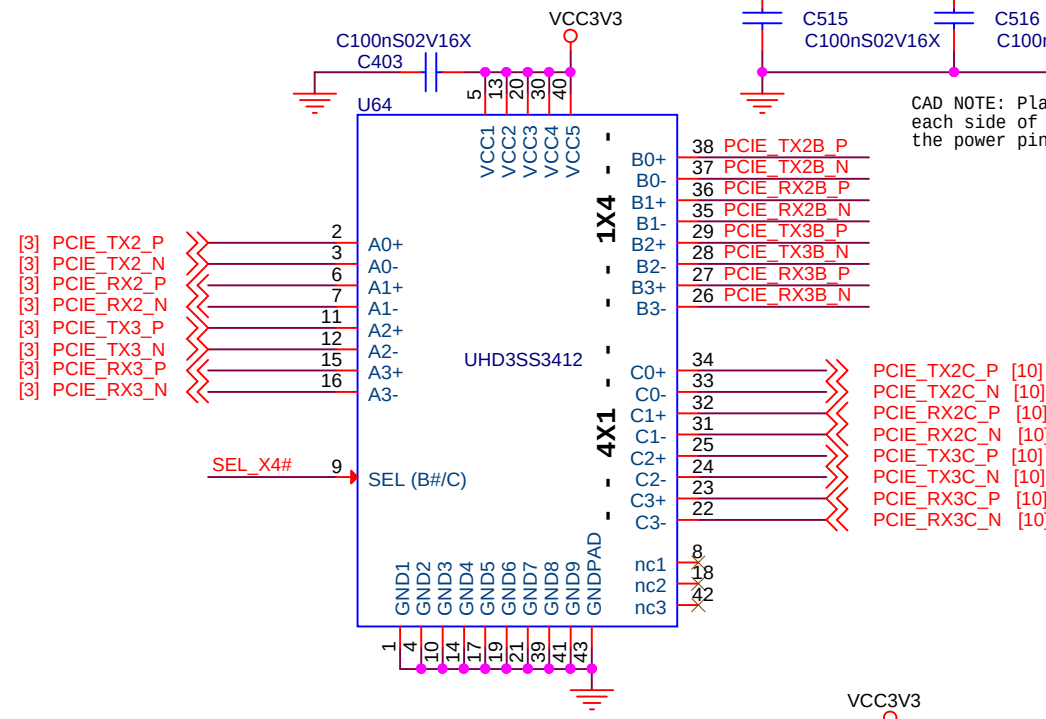
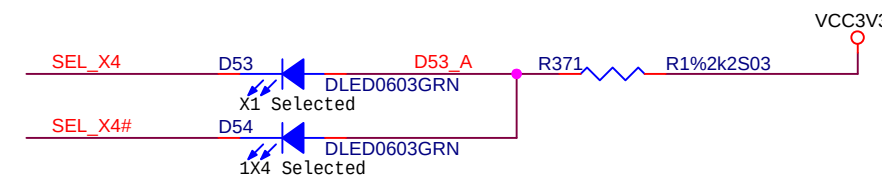
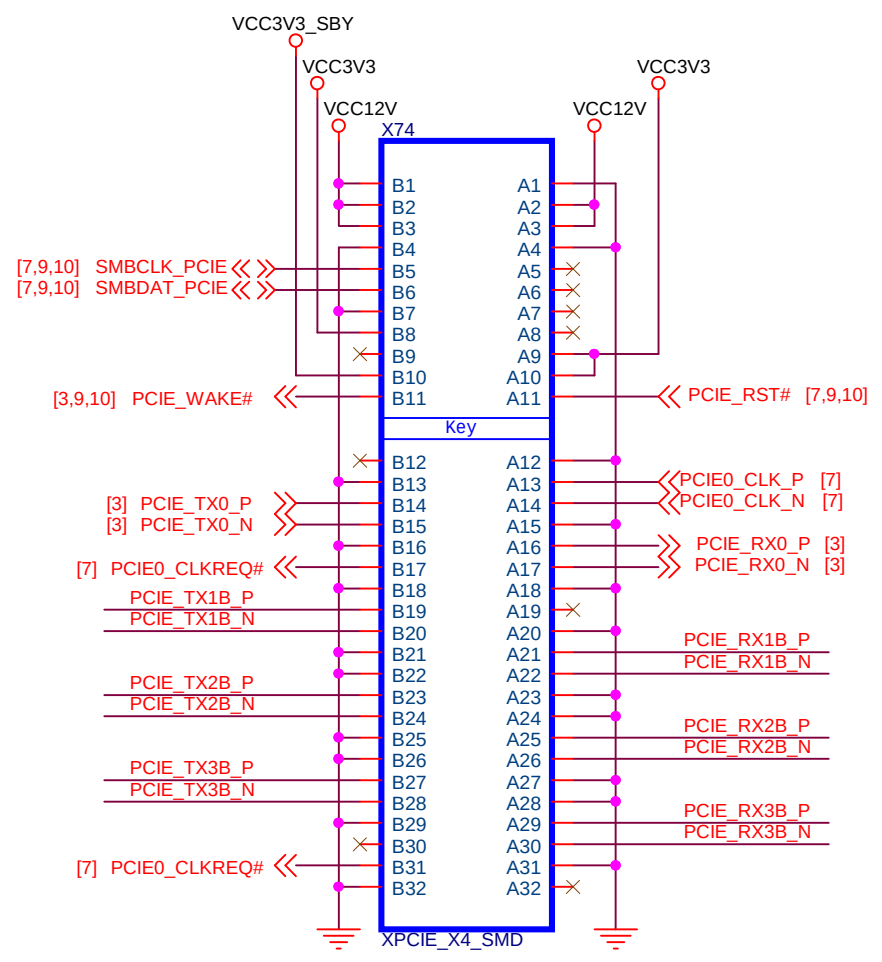
Title	PCI Express Clock Buffer
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PCIE SLOT 0



PCI Express SLOT 0 / Lane 0



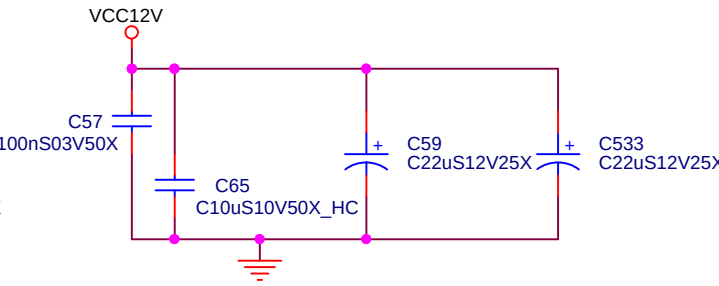
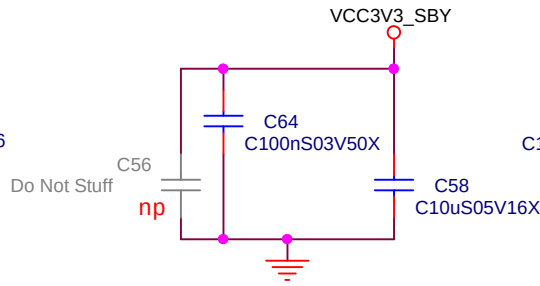
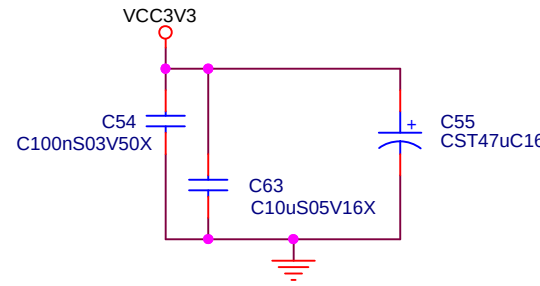
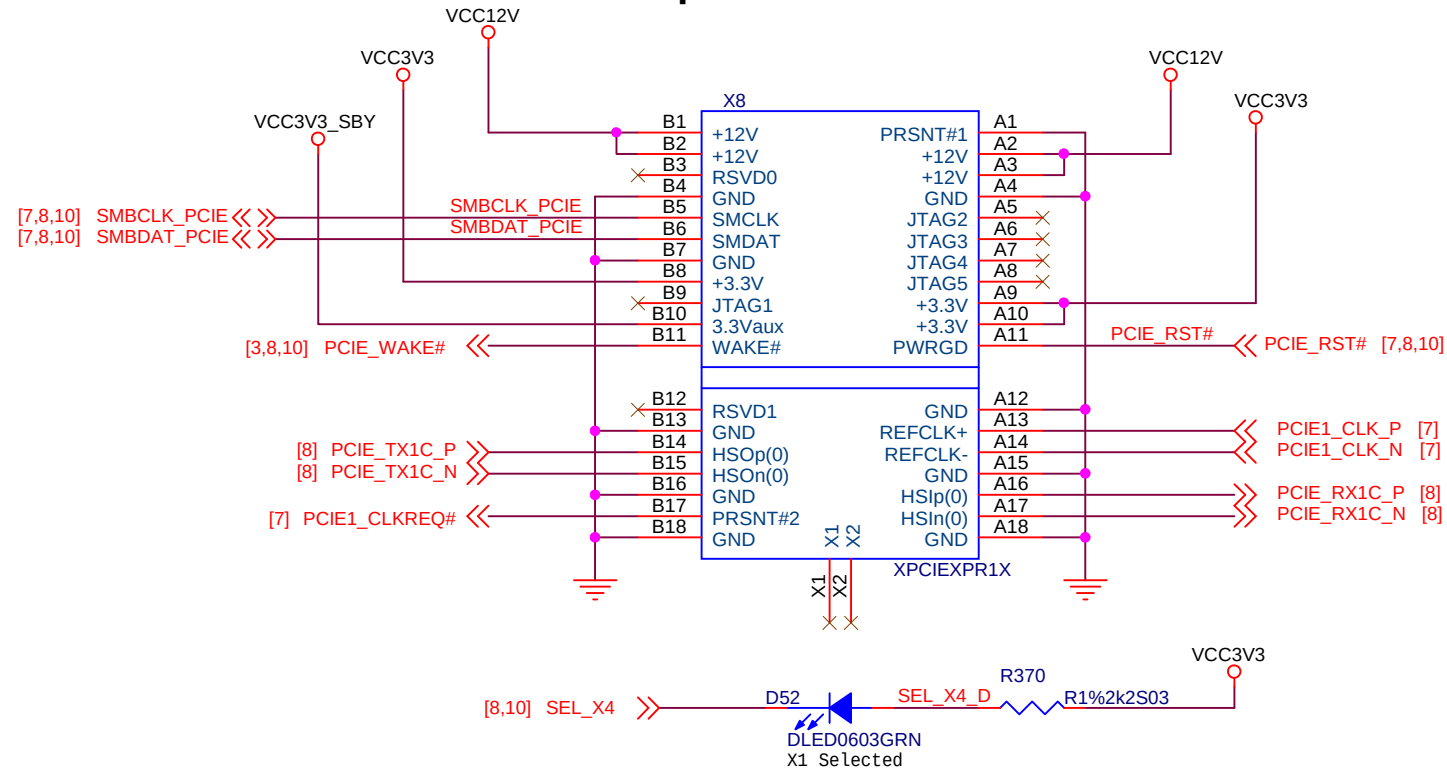
set jumper 1-2 for PCIe 4X1 (default)
set jumper 2-3 for PCIe 1X4

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Title PCI Express Slot 0			
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PCIE SLOT 1

PCI Express SLOT 1 / Lane 1



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Title PCI Express Slot 1				
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ExpressCard
Mini PCIe

ExpressCard

mini PCIe

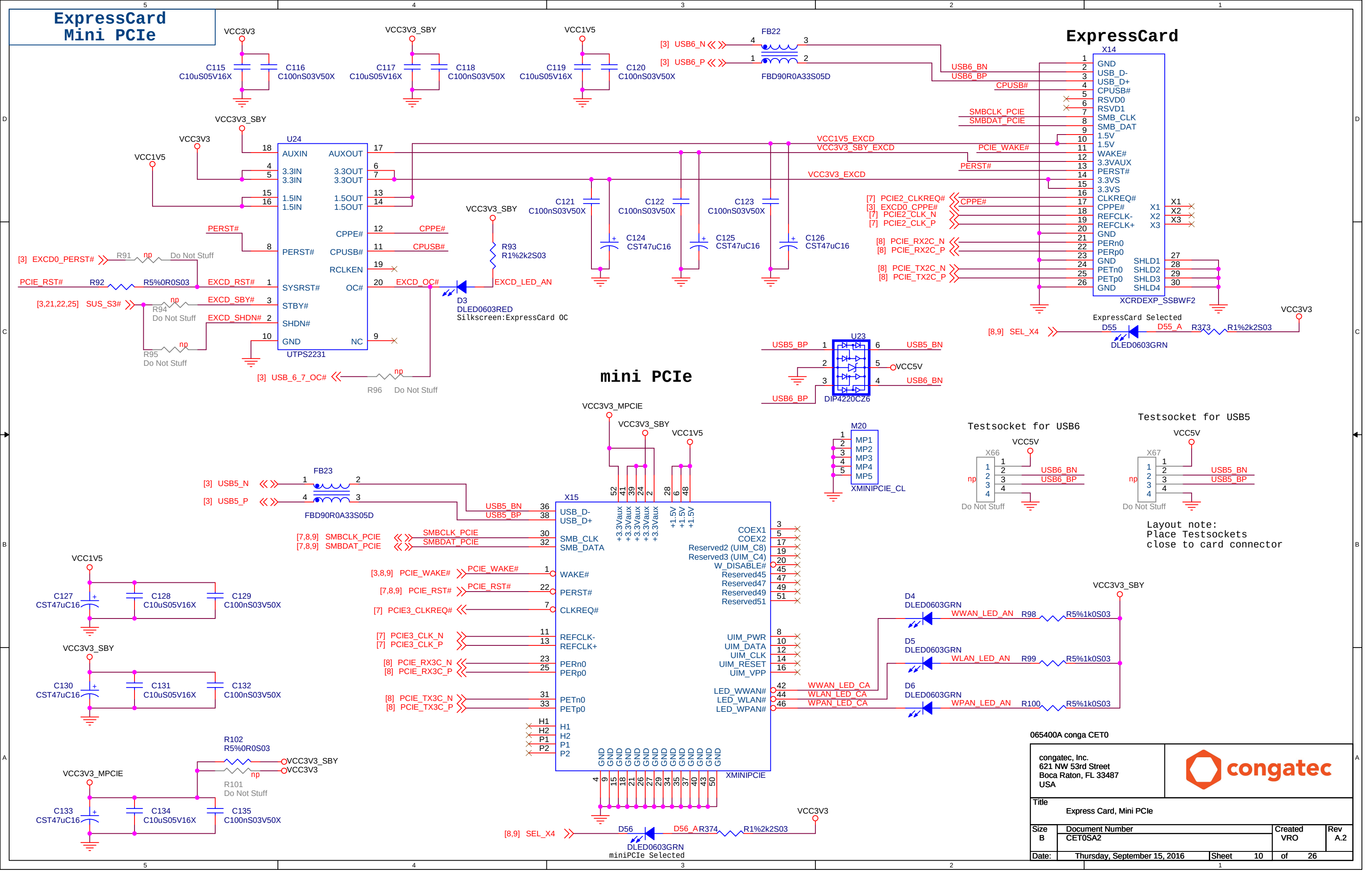
Testsocket for USB6

Testsocket for USB5

Layout note:
Place Testsockets
close to card connector

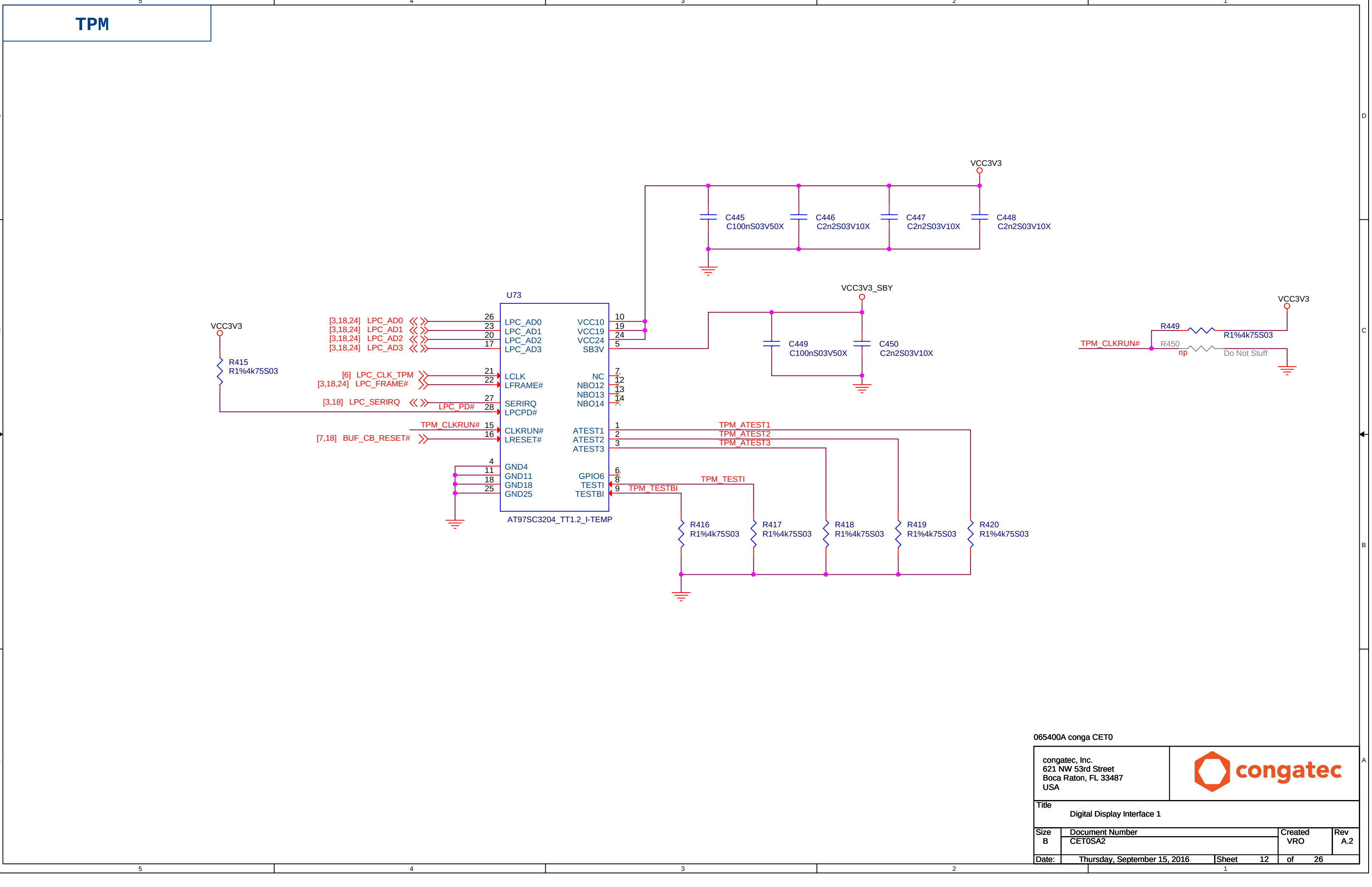
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Title Express Card, Mini PCIe			
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SATA

Title		SATA, SDIO	
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Title				
Digital Display Interface 1				
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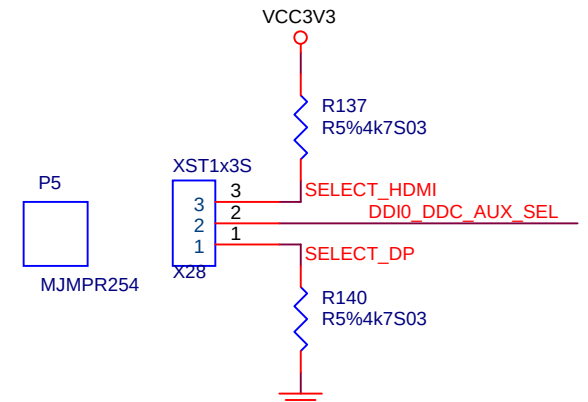
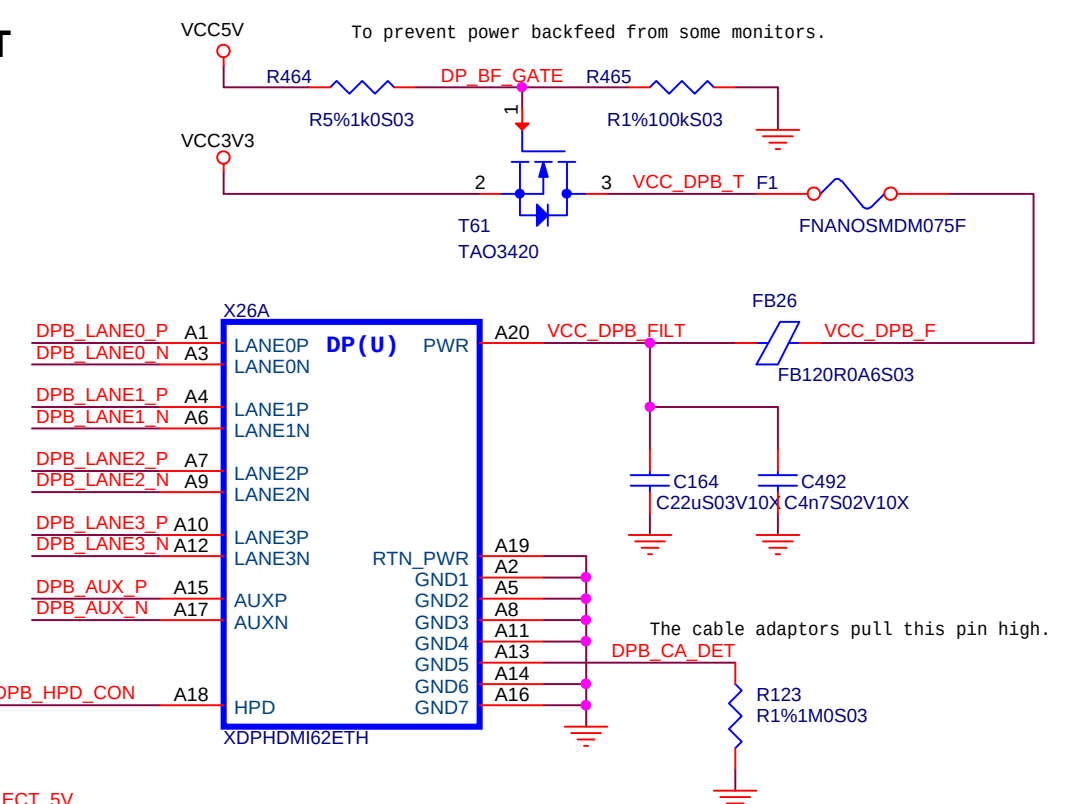
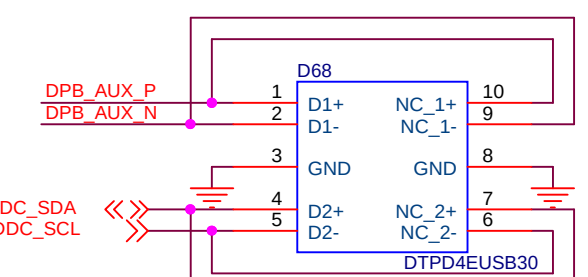
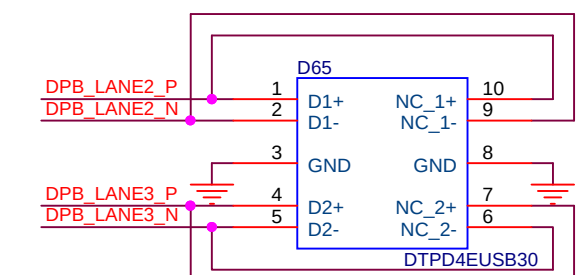
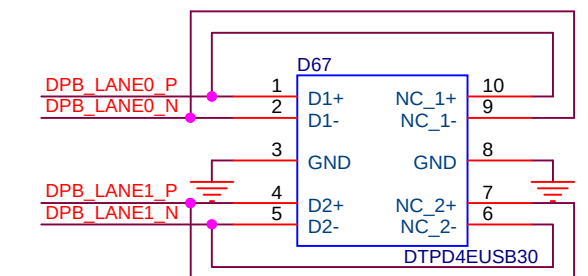
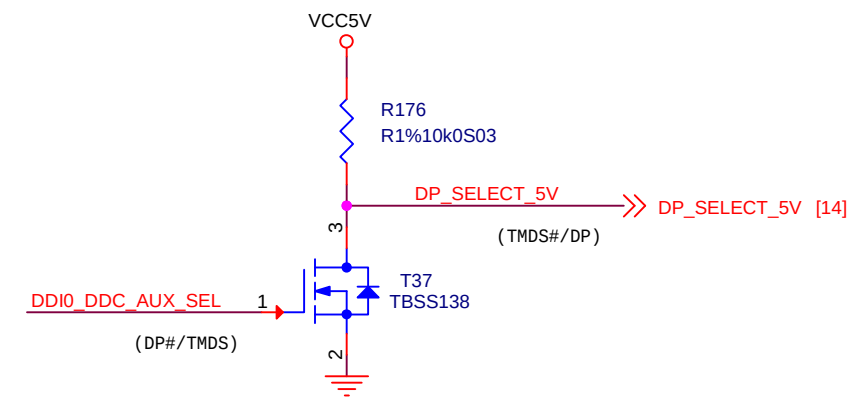
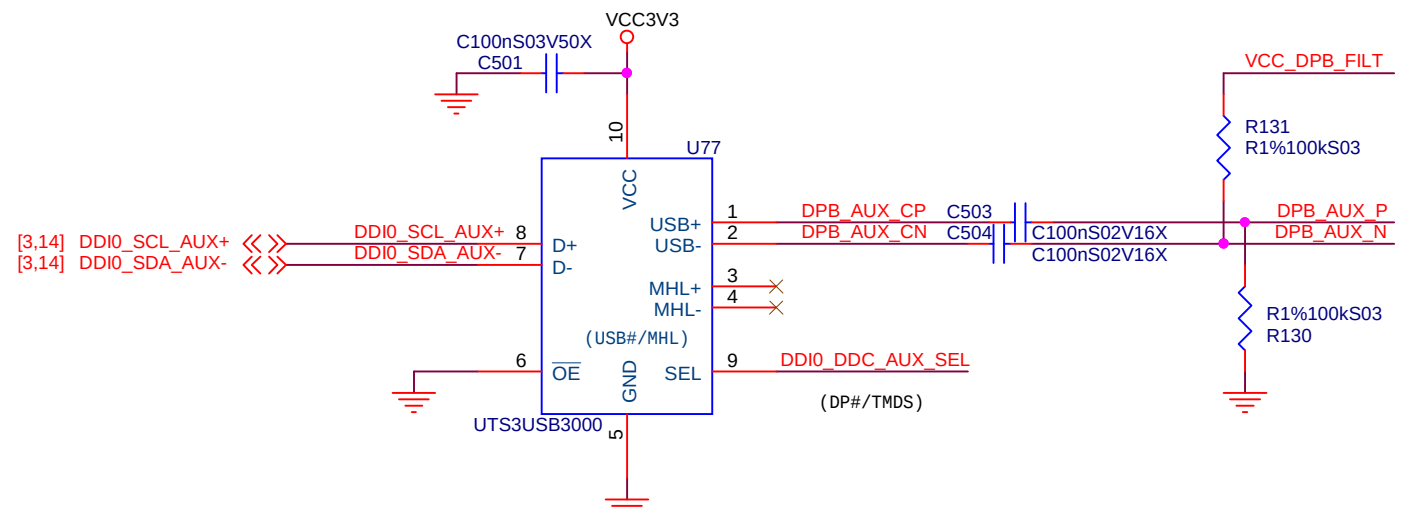
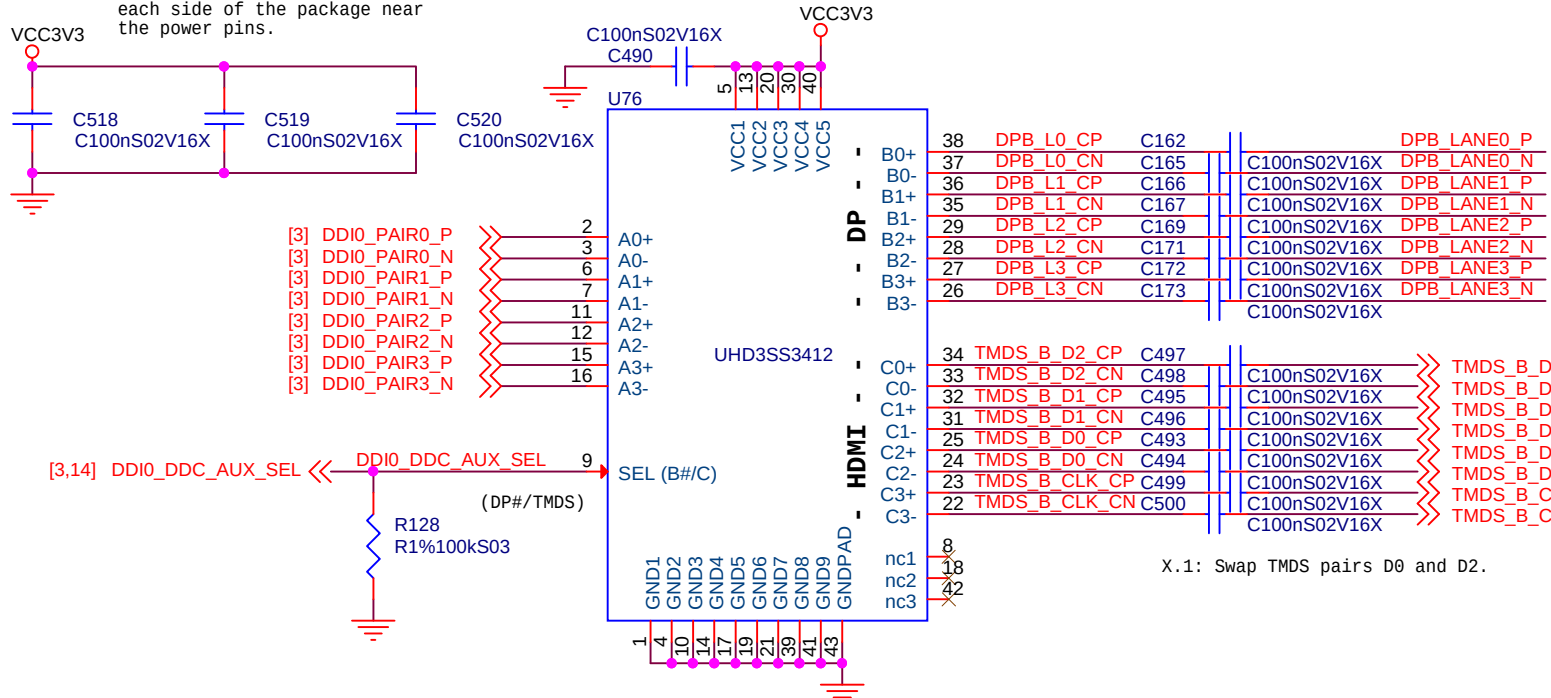
Digital Display Interface 0 to DISPLAY PORT

each side of the package near the power pins.

The diagram shows a power plane with three capacitors: C518, C519, and C520, all labeled C100nS02V16X. They are connected to a VCC3V3 supply and ground. Below this, a signal line DDI0_DDC_AUX_SEL is shown with a pull-down resistor R128 (R1%100kS03) to ground. The signal line is connected to a bus labeled [3,14] DDI0_DDC_AUX_SEL. To the right, a list of signals is shown with their respective widths:

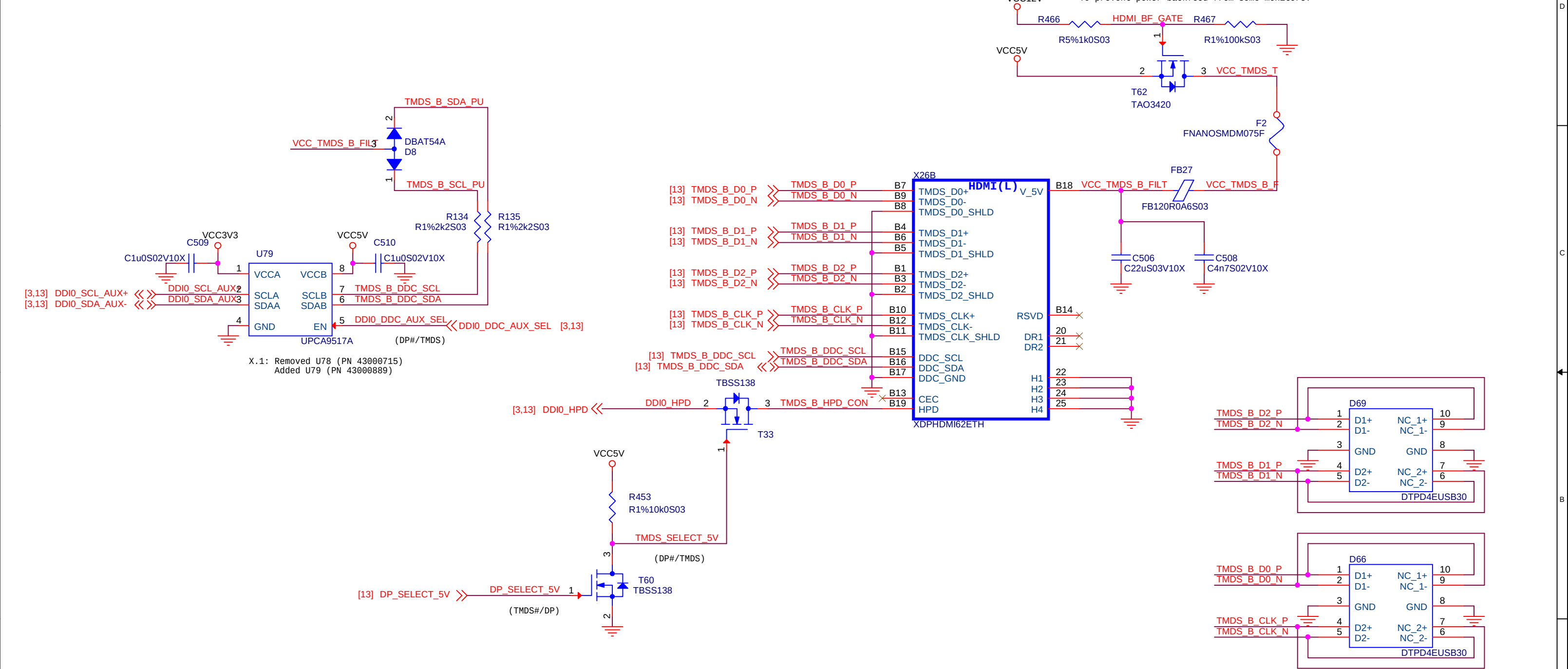
- [3] DDI0_PAIR0_P
- [3] DDI0_PAIR0_N
- [3] DDI0_PAIR1_P
- [3] DDI0_PAIR1_N
- [3] DDI0_PAIR2_P
- [3] DDI0_PAIR2_N
- [3] DDI0_PAIR3_P
- [3] DDI0_PAIR3_N

These signals are connected to a bus labeled (DP#/TMDS) with widths 2, 3, 6, 7, 11, 12, 15, and 16 respectively.



When using HDMI port:
 Jumper 1-2: Select Display Port (default)
 Jumper 2-3: Select HDMI

DDIO to HDMI



Design Note: The DDC TVS is on the DP page.

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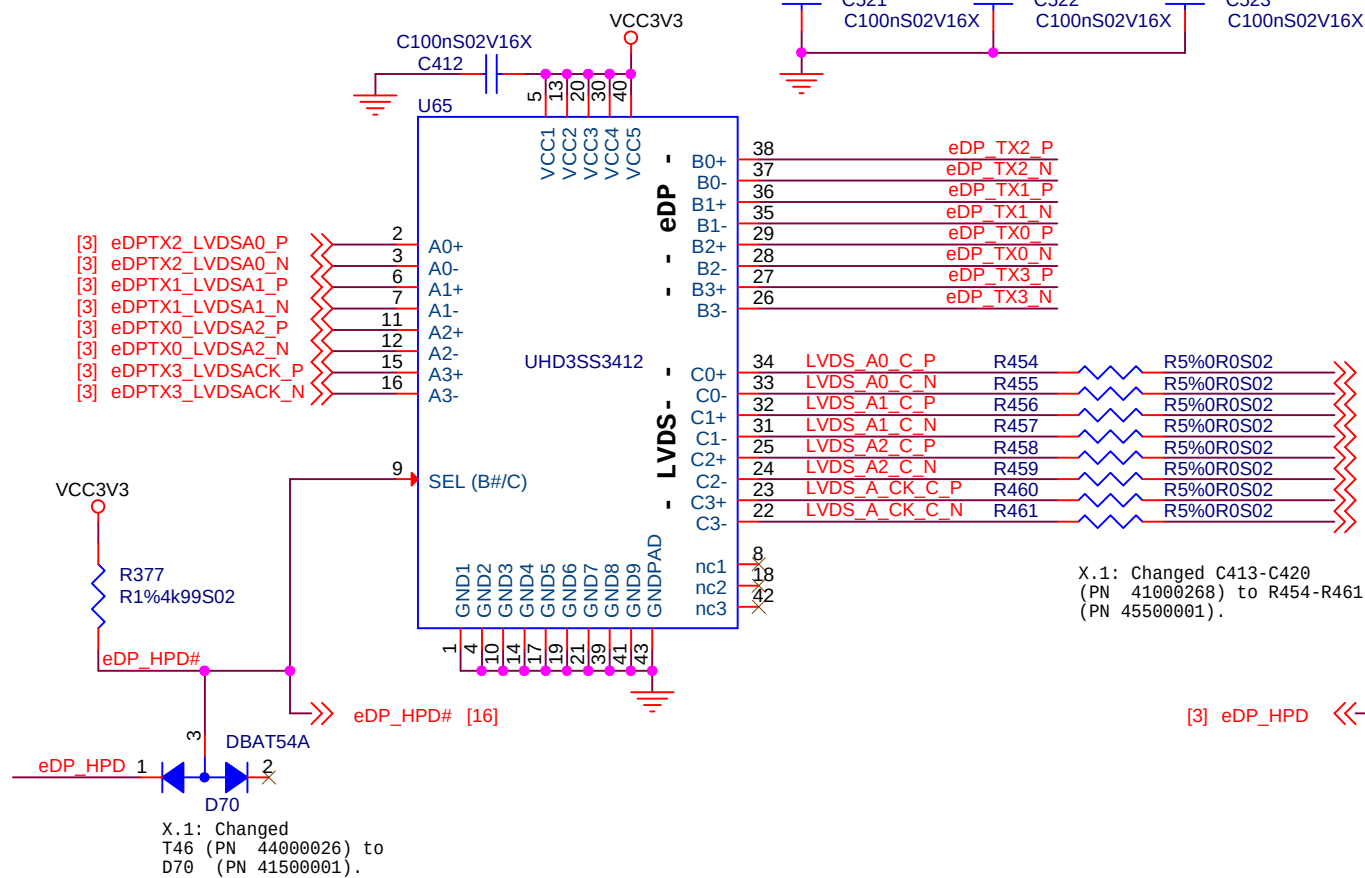
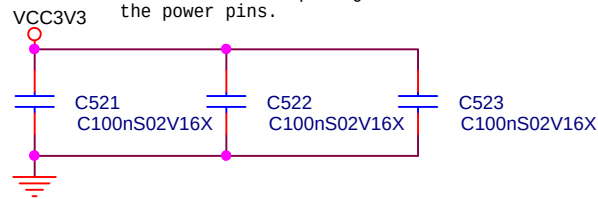
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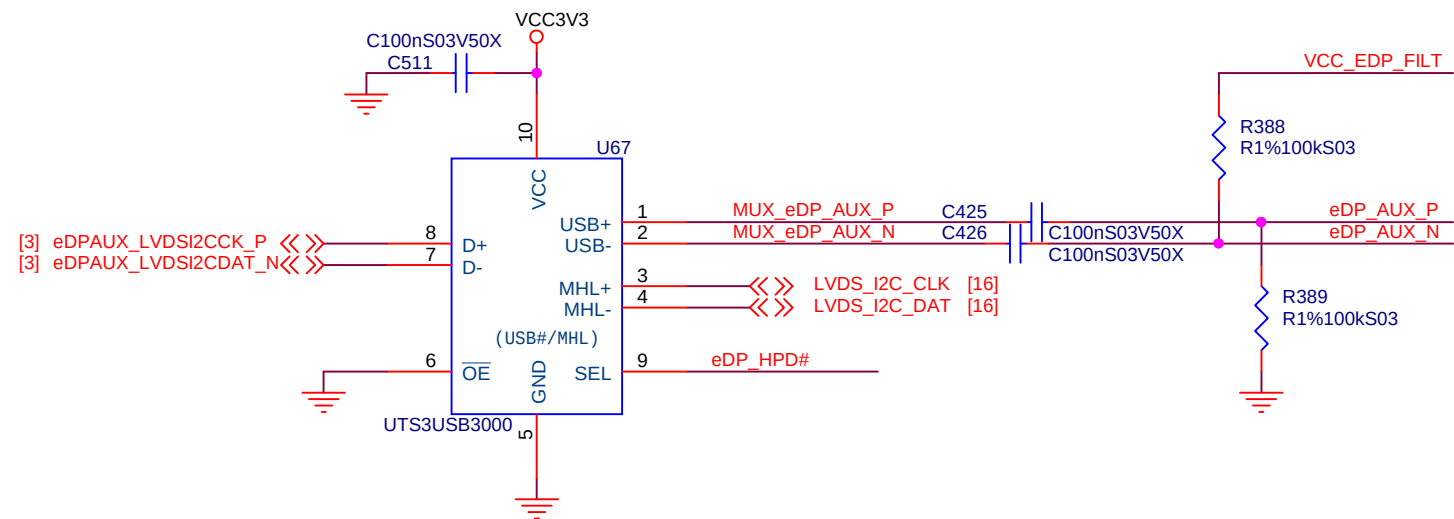
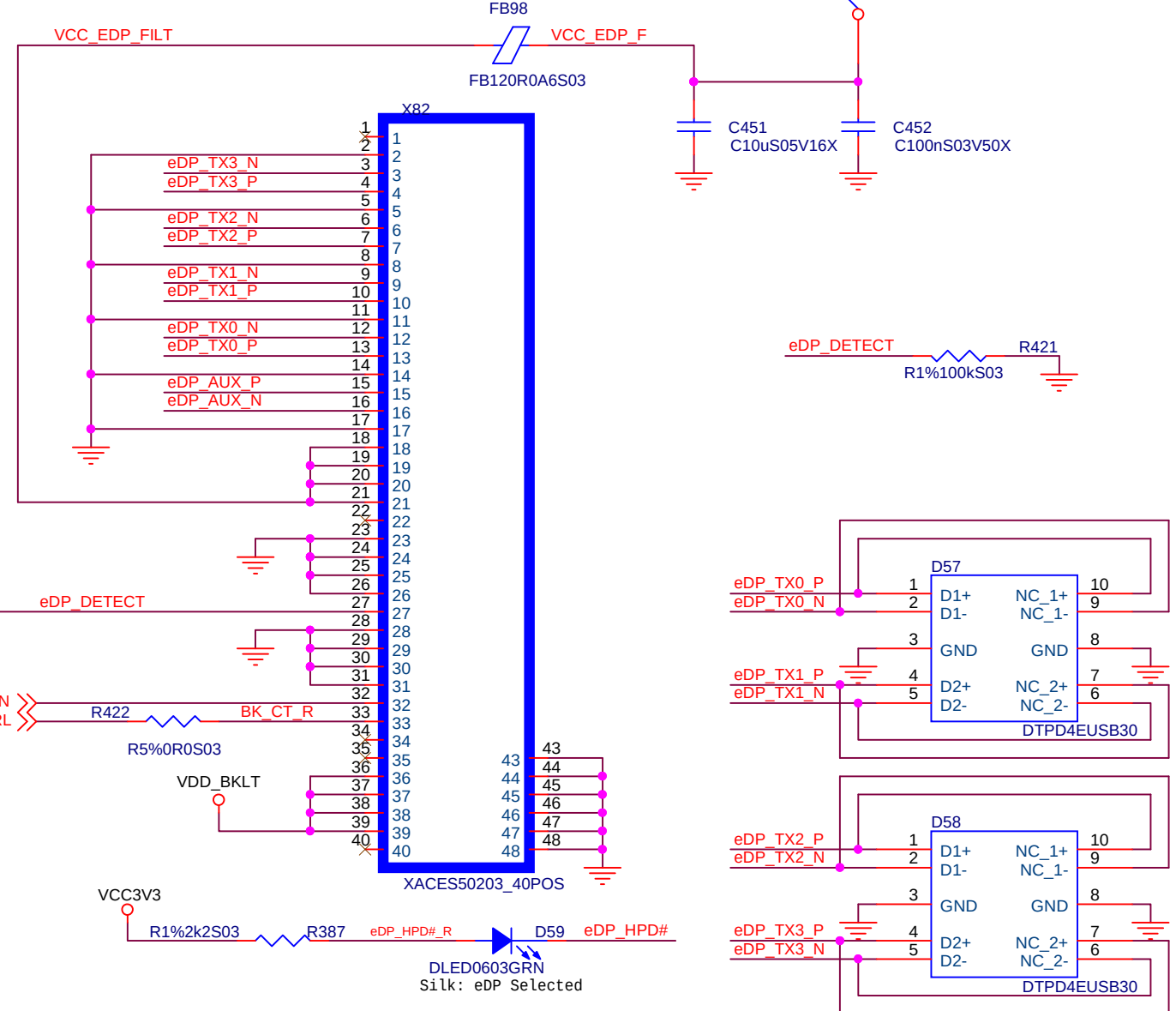
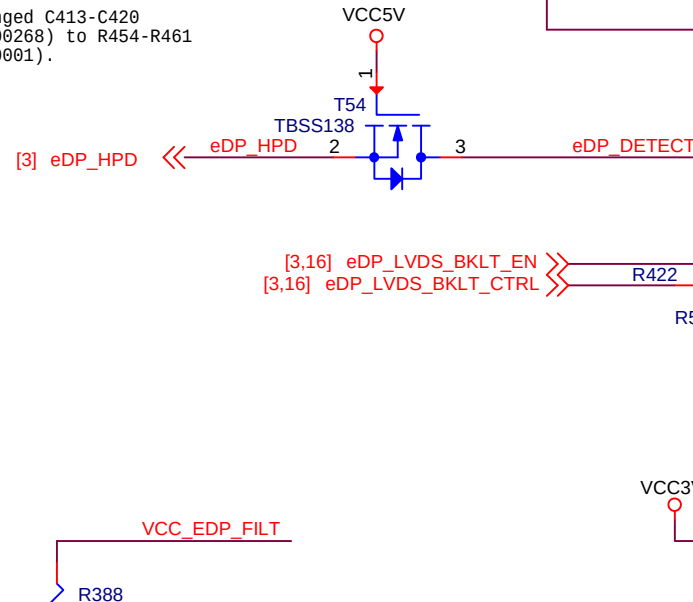
DDI1 to eDP

CAD NOTE: Place one cap on each side of the package near the power pins.

CAD NOTE: Place one cap on each side of the package near the power pins.



X.1: Changed C413-C420
(PN 41000268) to R454-R461
(PN 45500001).



PIN	eDP	Pin Name
A71	eDP_TX2+	LVDS_A0+
A72	eDP_TX2-	LVDS_A0-
A73	eDP_TX1+	LVDS_A1+
A74	eDP_TX1-	LVDS_A1-
A75	eDP_TX0+	LVDS_A2+
A76	eDP_TX0-	LVDS_A2-
A81	eDP_TX3+	LVDS_A_CK+
A82	eDP_TX3-	LVDS_A_CK-
A77	eDP_VDD_EN	LVDS_VDD_EN
B79	eDP_BKLT_EN	LVDS_BKLT_EN
A83	eDP_AUX+	LVDS_I2C_CK
A84	eDP_AUX-	LVDS_I2C_DAT
B83	eDP_BKLT_CTRL	LVDS_BKLT_CTRL
A87	eDP_HPD	RSVD

eDP Signal Mapping to COM Express T10 Connector

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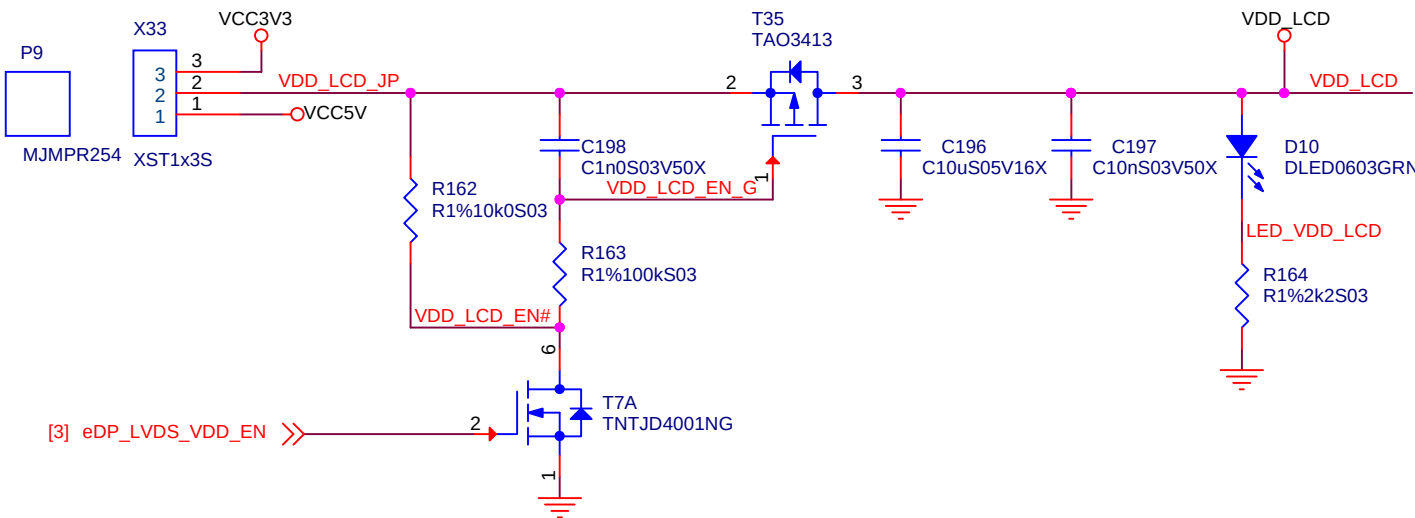


Title	eDP Interface
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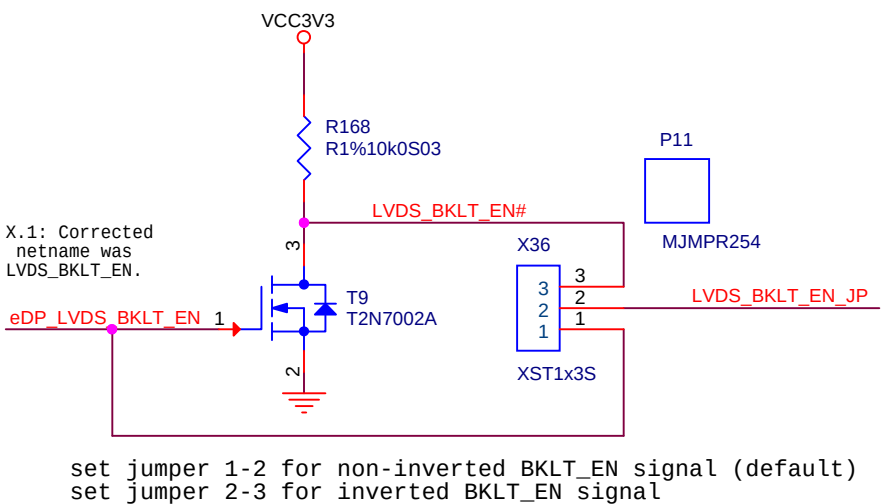
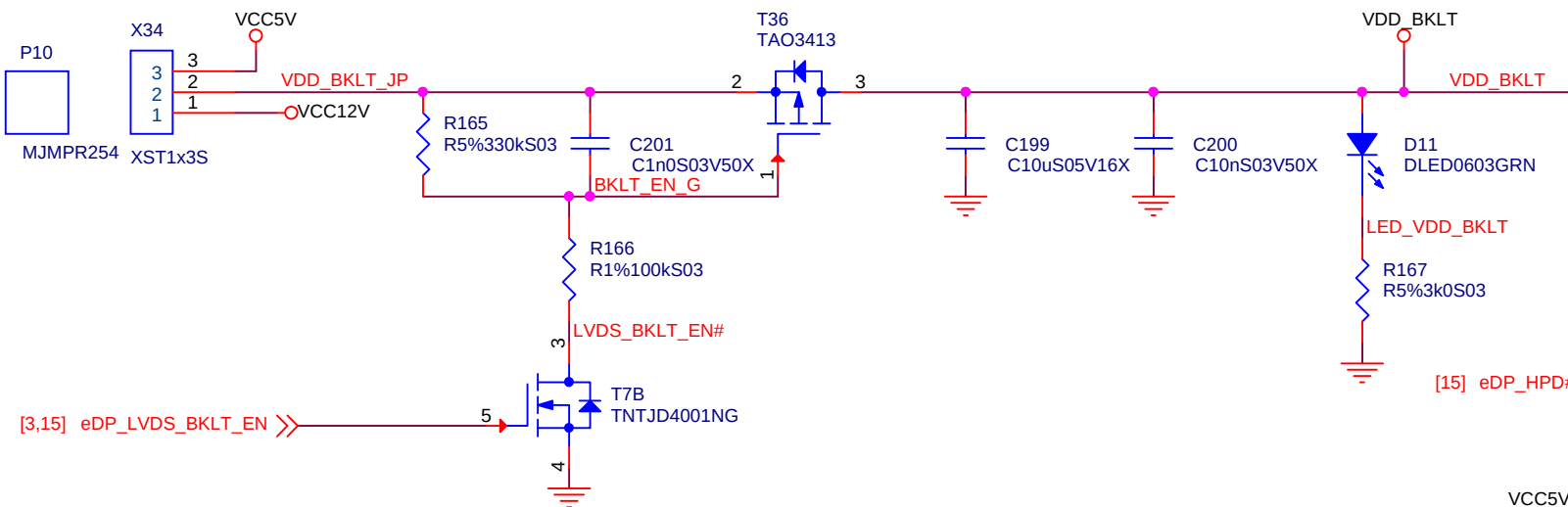
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DDI1 to LVDS

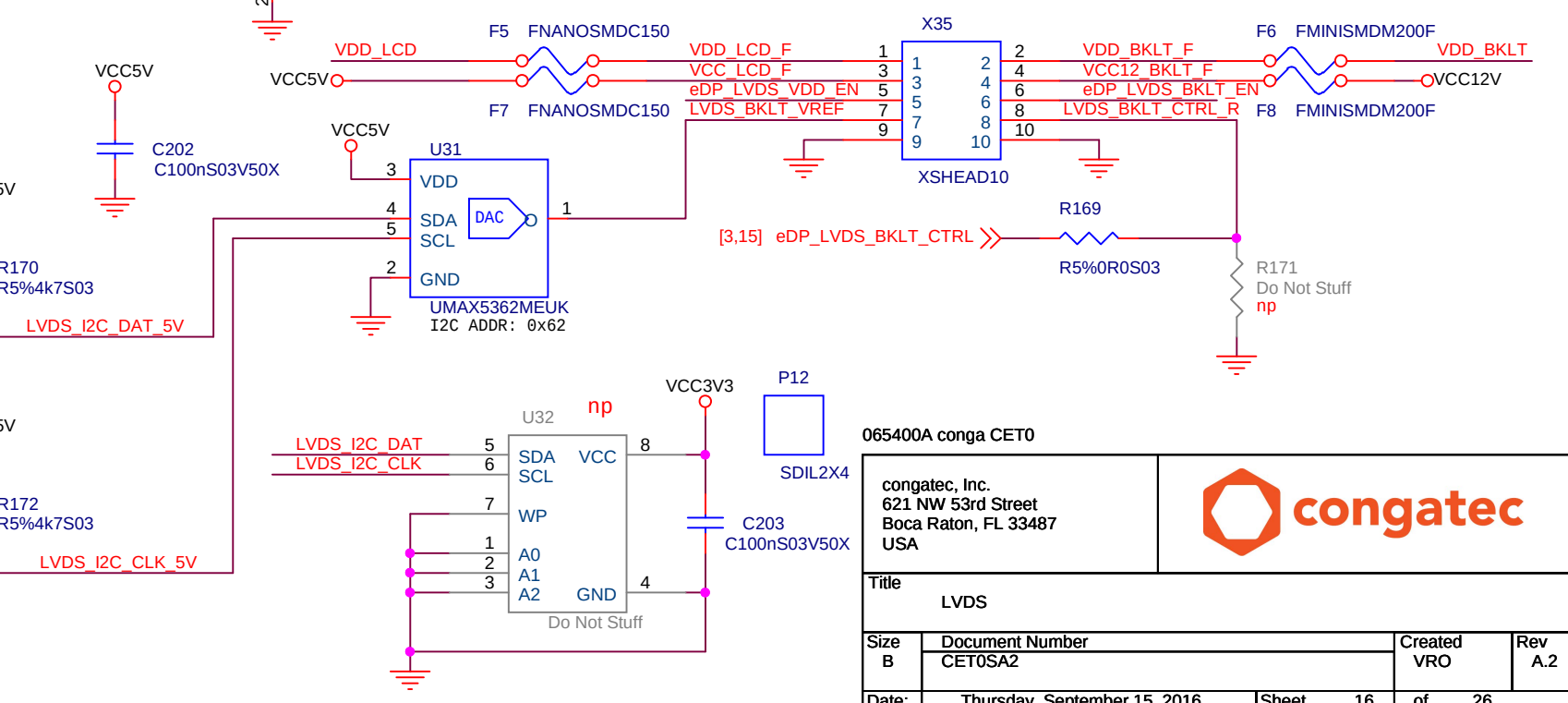
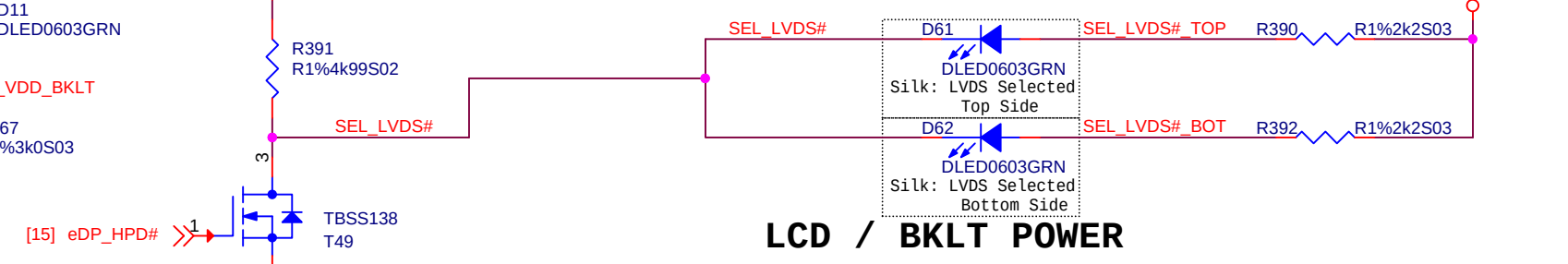
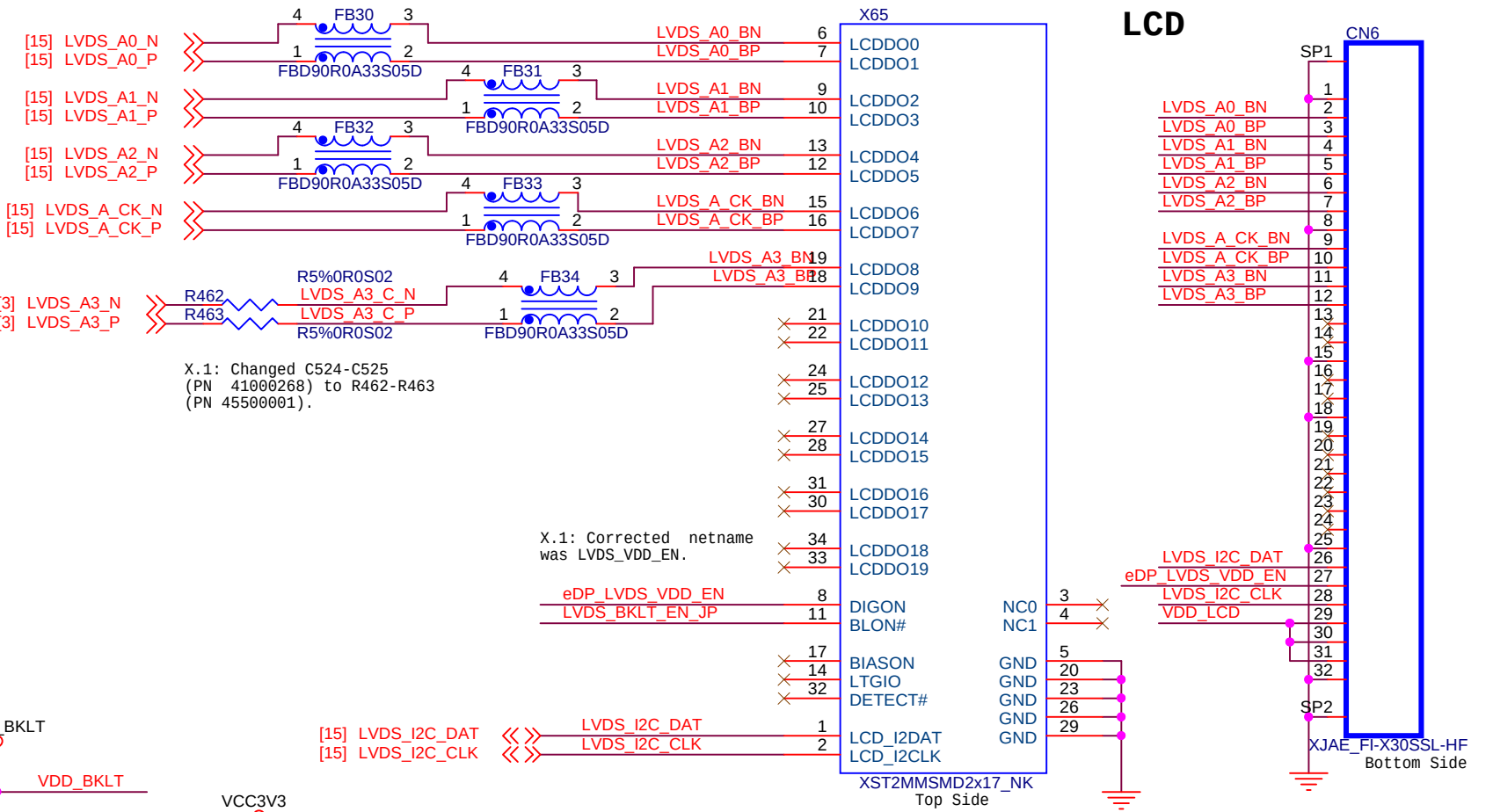
set jumper 1-2 for 5 V LCD supply voltage
set jumper 2-3 for 3.3 V LCD supply voltage (default)



set jumper 1-2 for 12 V backlight voltage (default)
set jumper 2-3 for 5 V backlight voltage



set jumper 1-2 for non-inverted BKLT_EN signal (default)
set jumper 2-3 for inverted BKLT_EN signal



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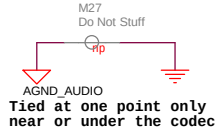
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Title
LVDS

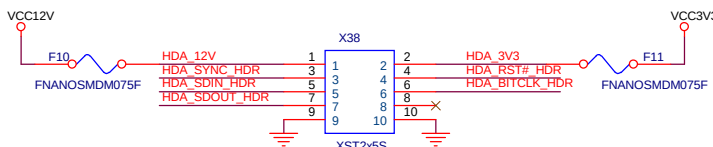
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HD AUDIO

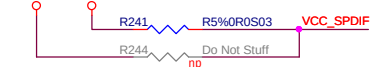
HD-Audio Codec



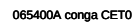
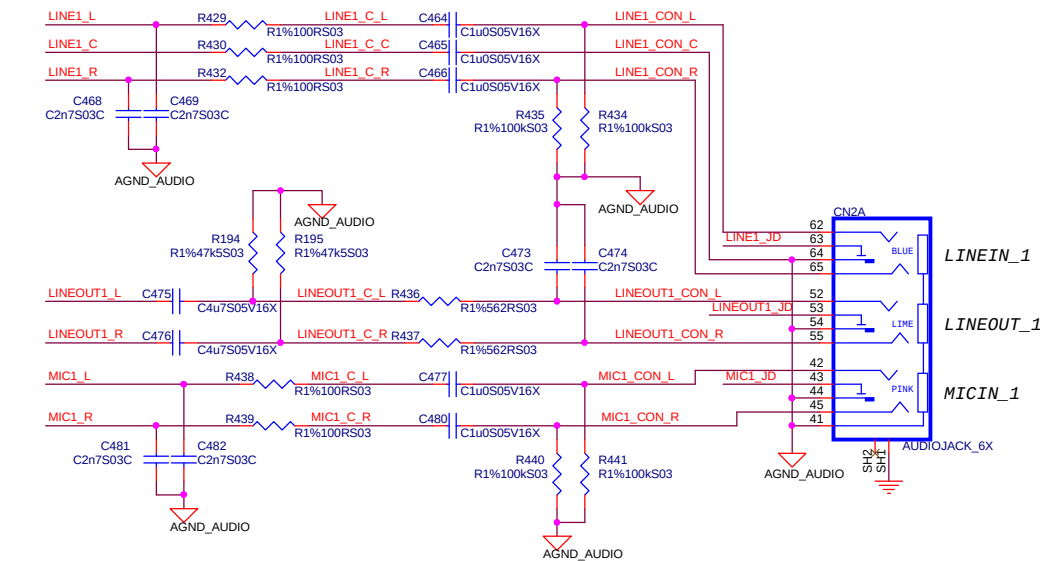
Debug and HDA Adapter



S/PDIF

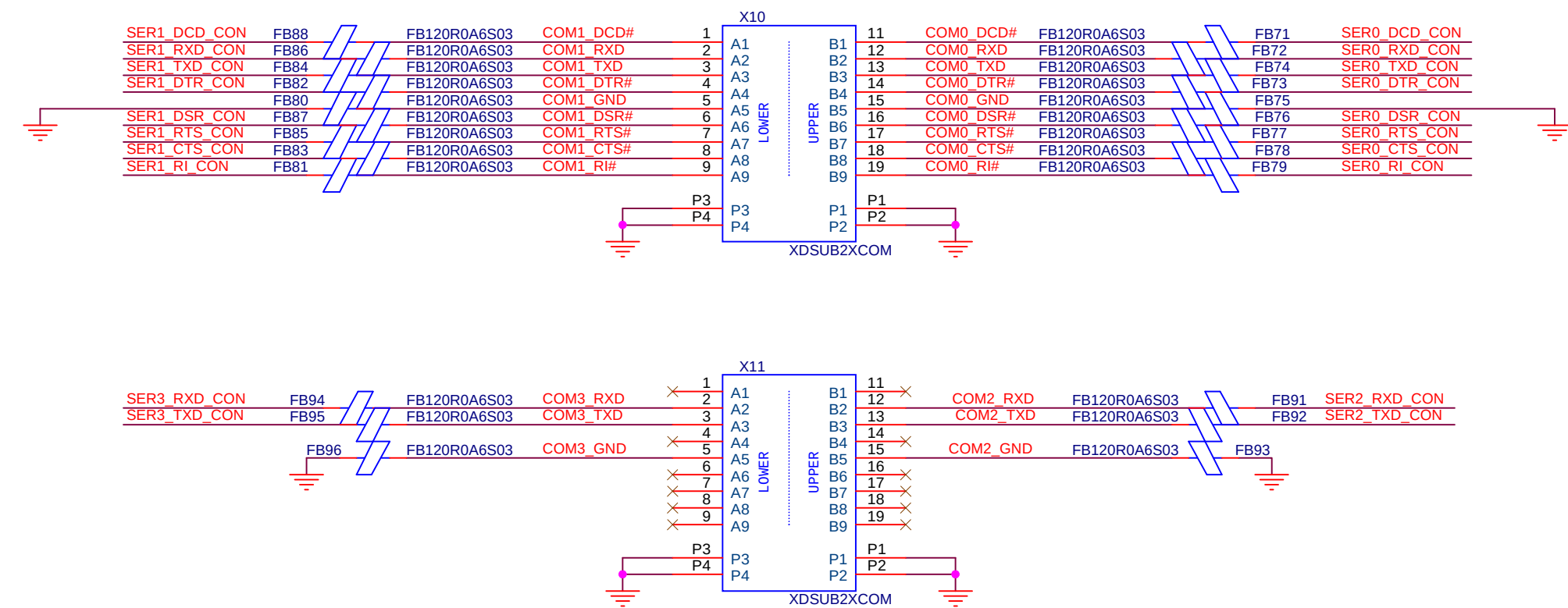
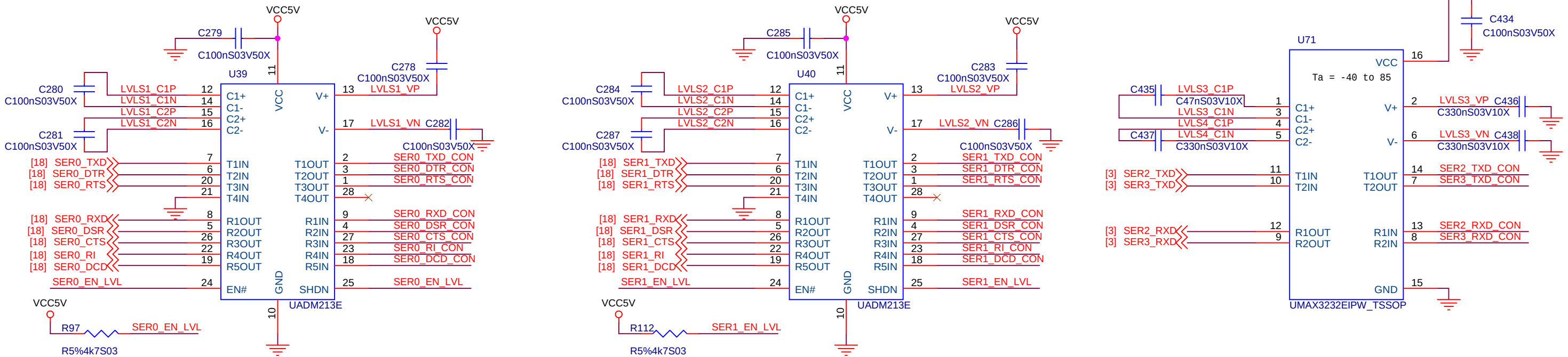


Audio Power



SIO Interface

Attention: U39, U40 shows UADM211E
UADM213E has high-active EN (pin 24)
and low-active SHDN# (pin 25)

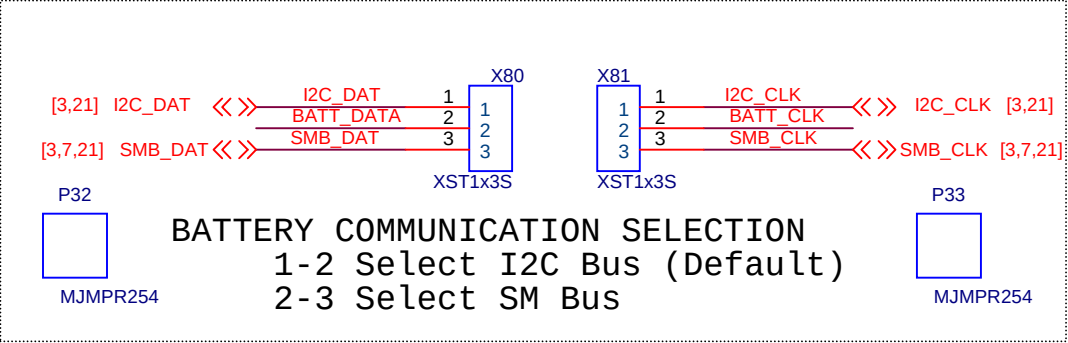
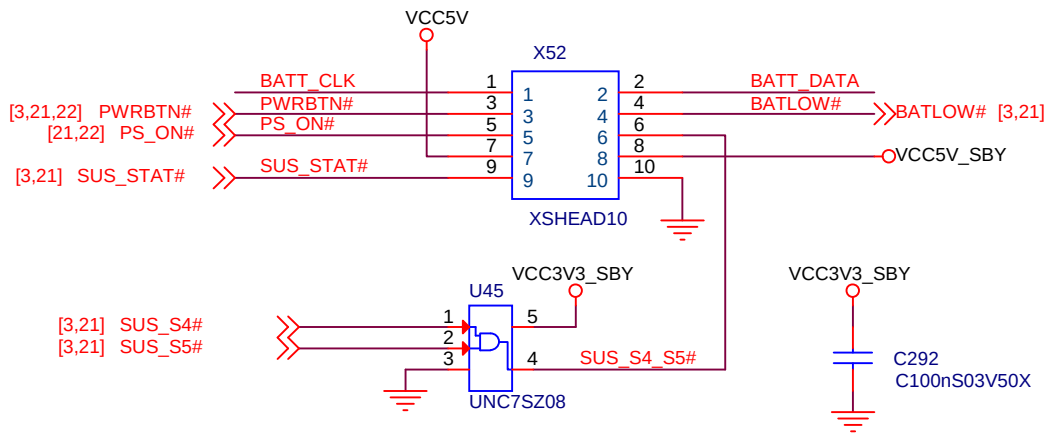


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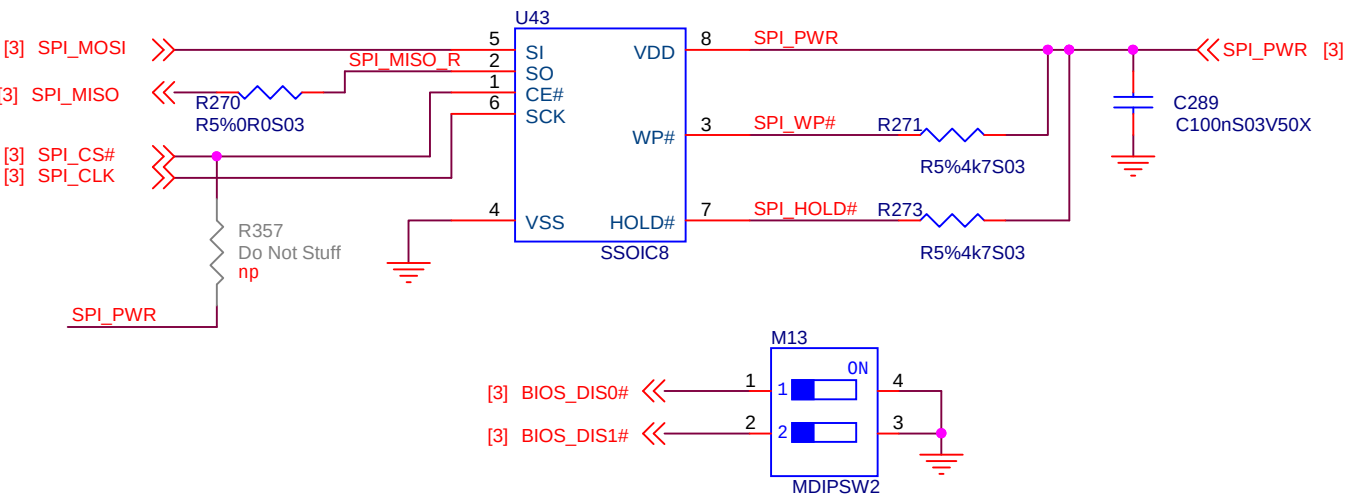
congatec, Inc. 621 NW 53rd Street Boca Raton, FL 33487 USA		 congatec	
Title RS-232, parallel port			
Size B	Document Number CET0SA2	Created VRO	Rev A.2
Date:	Thursday, September 15, 2016	Sheet 19	of 26

BATTERY, FWH, GPIO, EEPROM

Battery Support

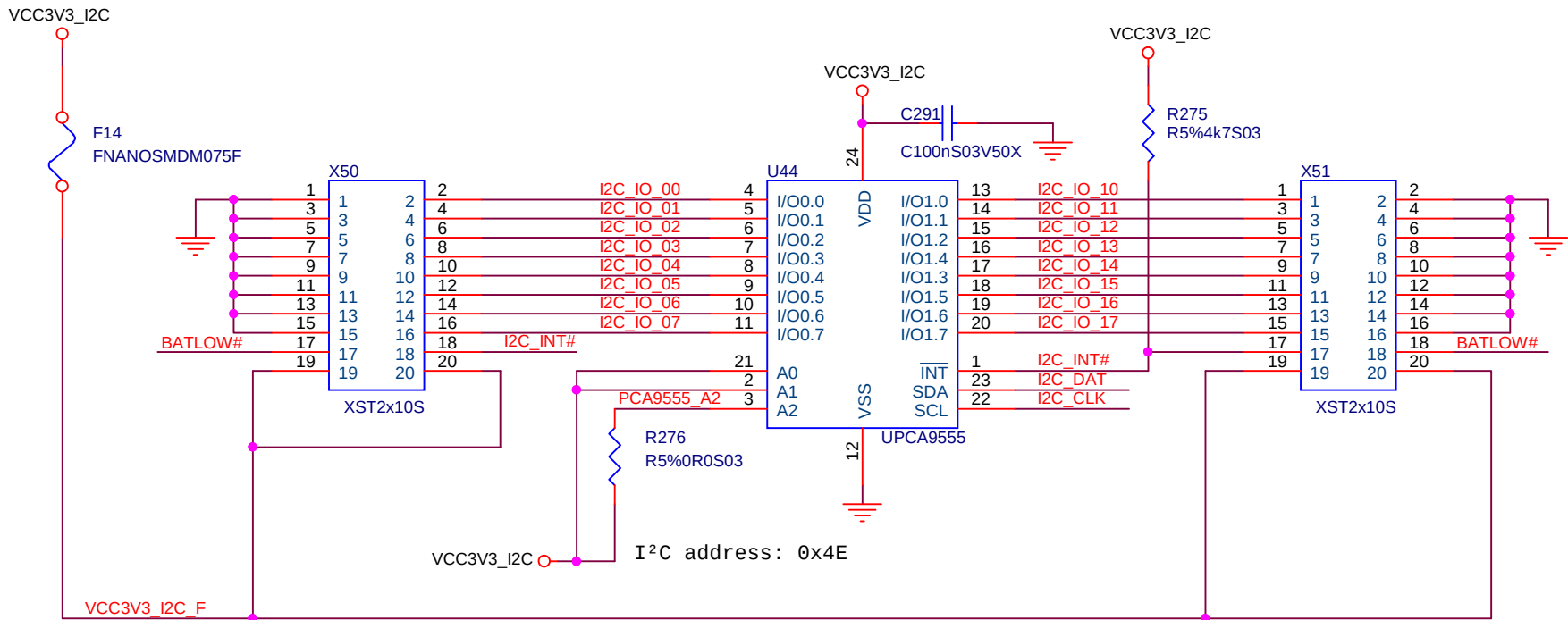


SPI BIOS Flash

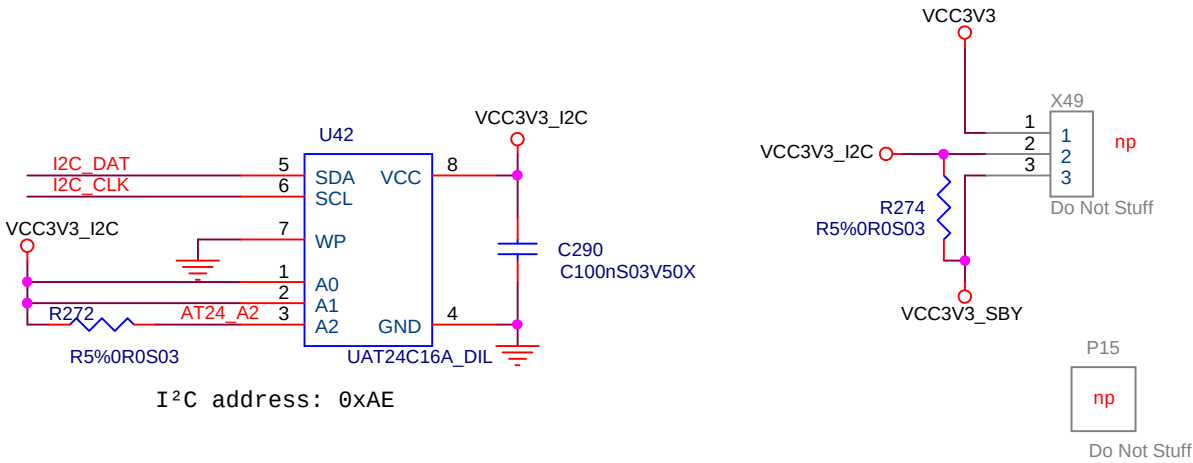


BIOS_DIS1#	BIOS_DIS0#	SPI Descriptor / BIOS Entry
OFF (1)	OFF (1)	Module / SPI0/SPI1 (default)
OFF (1)	ON (0)	Module / Carrier FWH (not supported)
ON (0)	OFF (1)	Carrier / SPI0/SPI1
ON (0)	ON (0)	Module / SPI0/SPI1

Digital IO over I2C



I²C EEPROM



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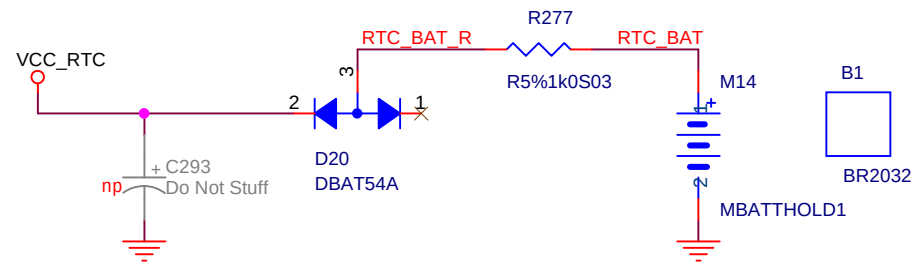
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USA



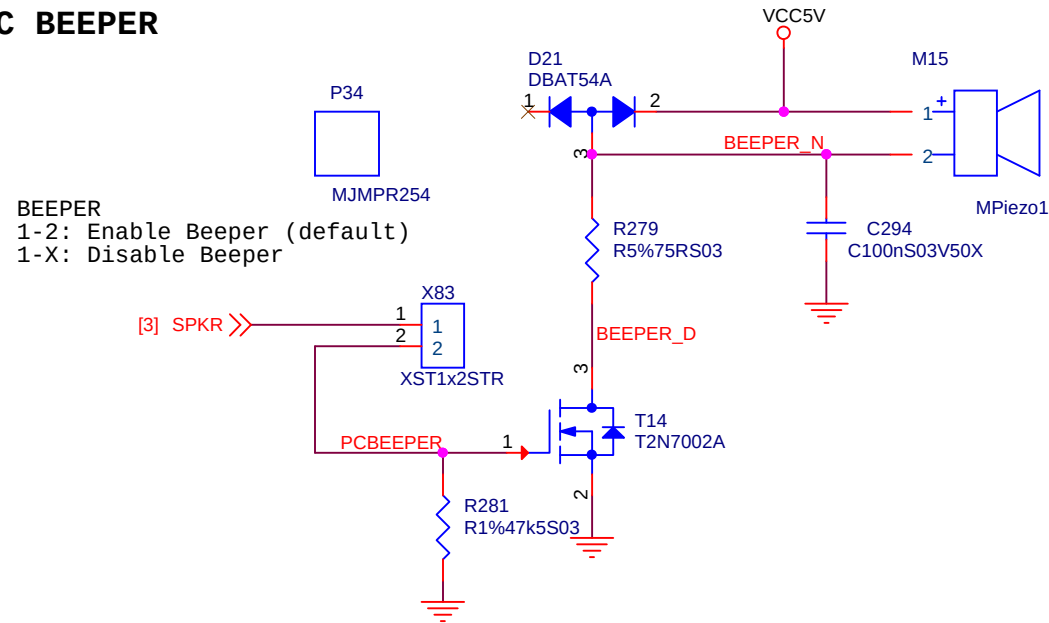
Title
SPI, I2C, Battery Support

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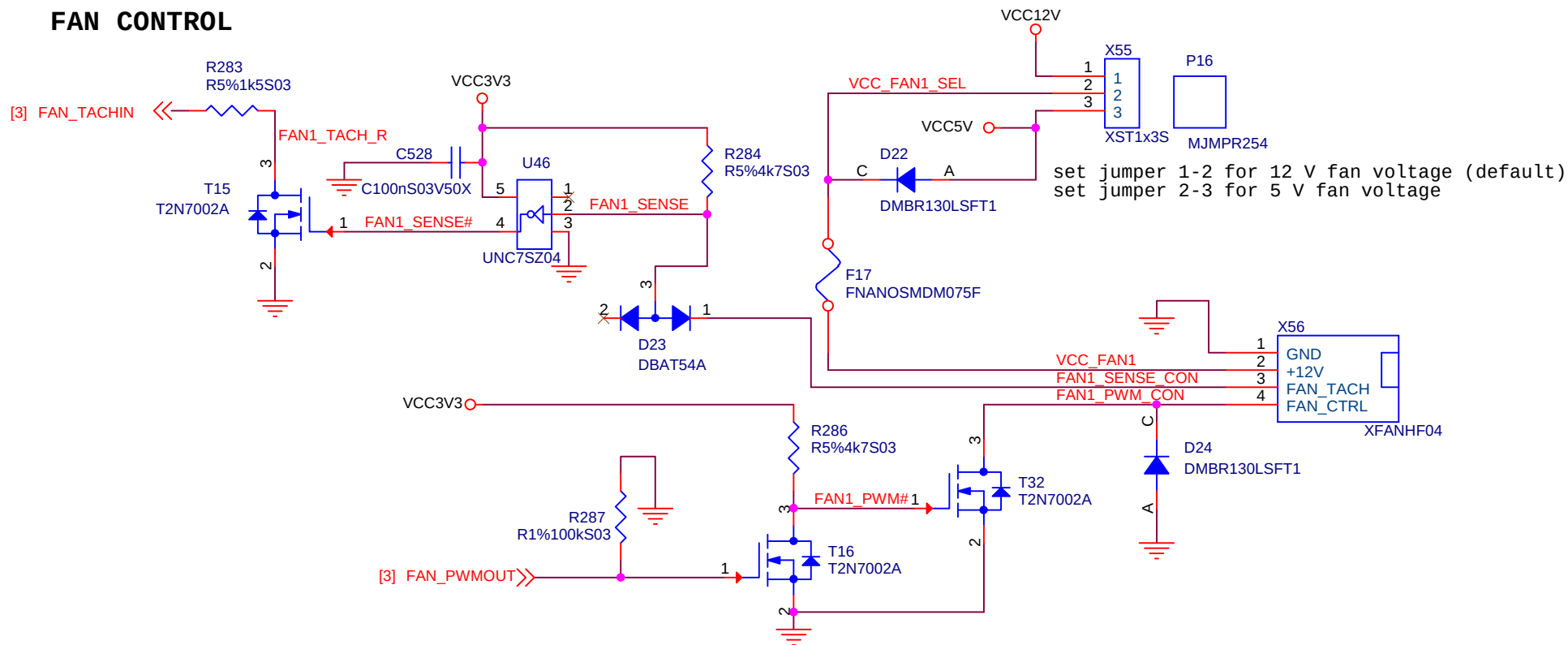
RTC / CMOS BATTERY



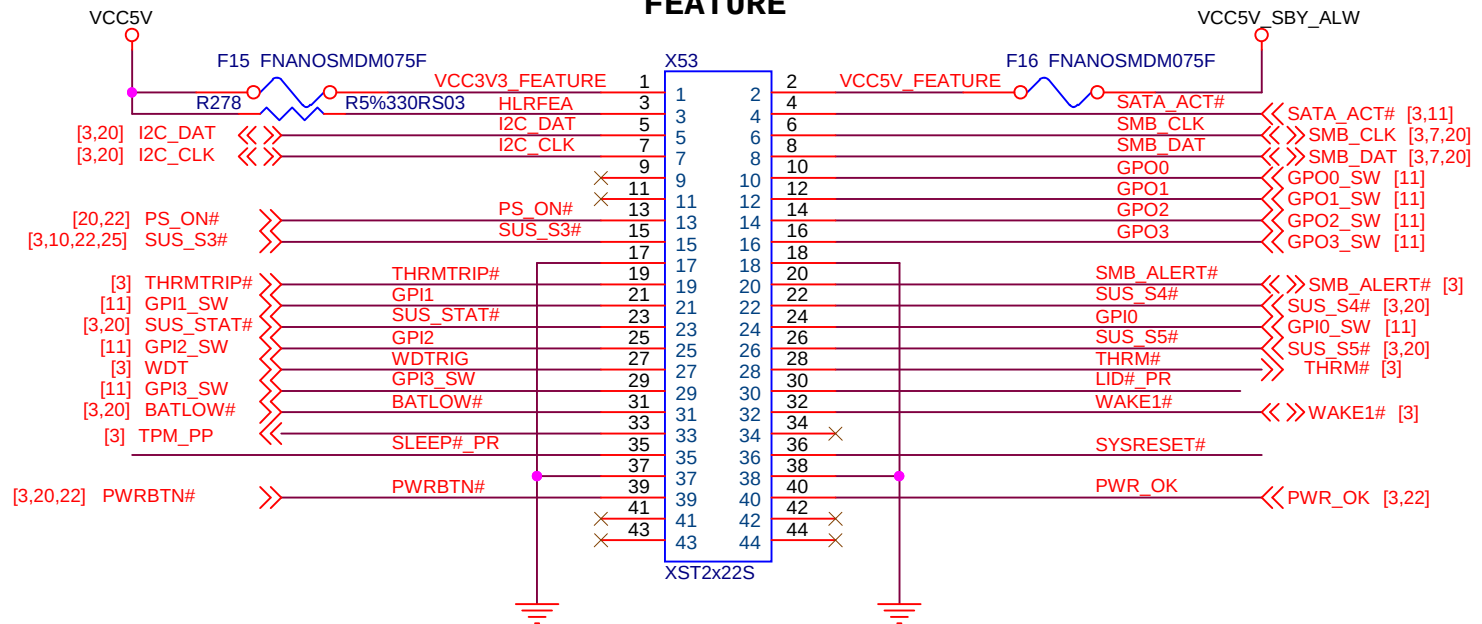
PC BEEPER



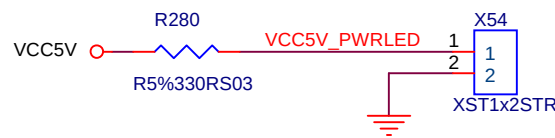
FAN CONTROL



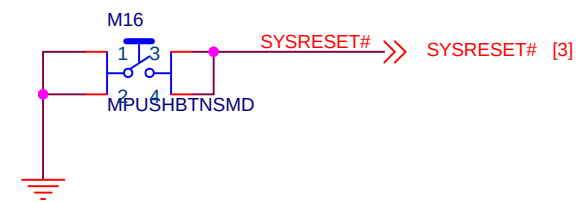
FEATURE



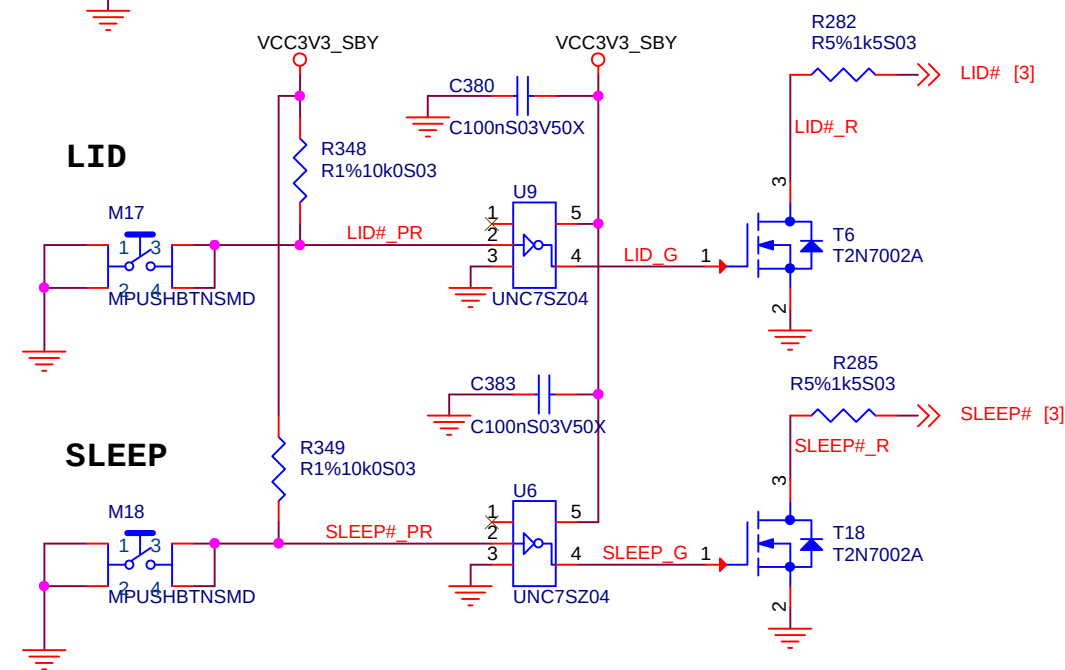
REMOTE POWER LED



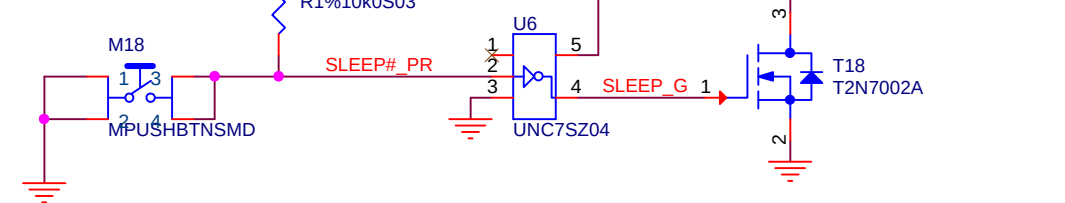
RESET



LID



SLEEP



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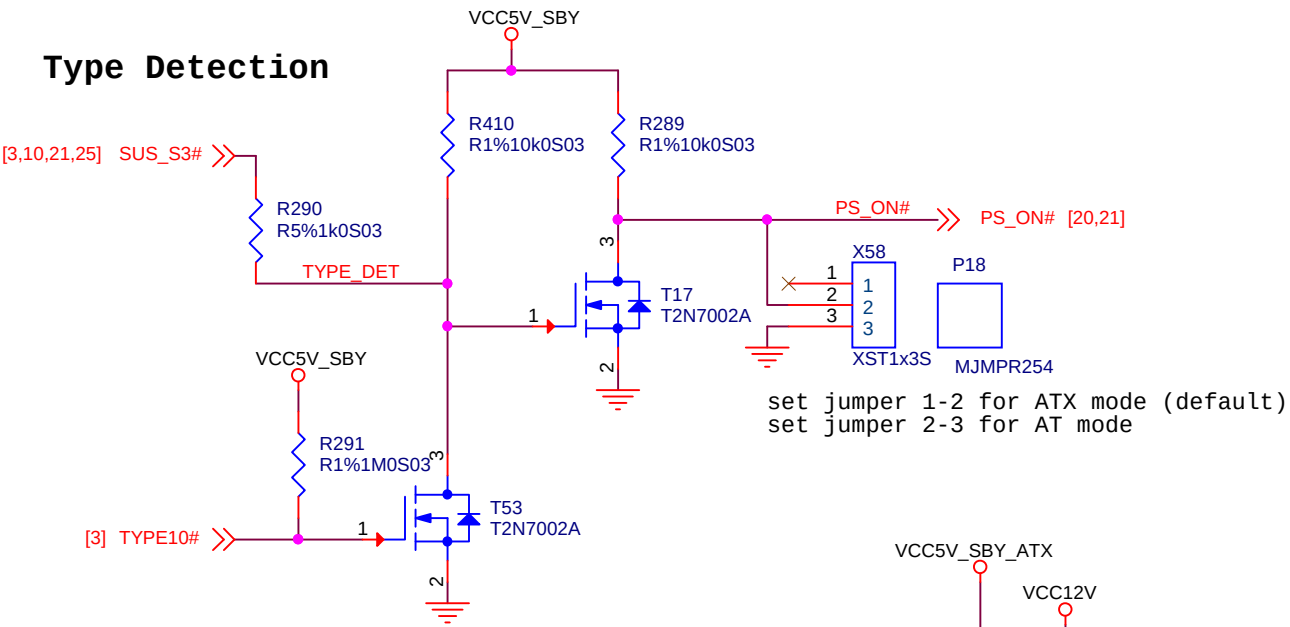


Title	CMOS Battery, Speaker, FAN, Feature Connector
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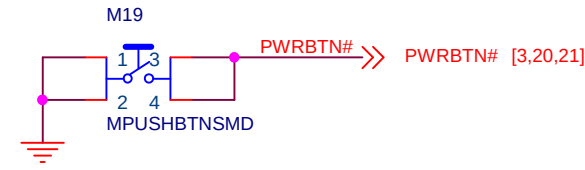
Size B	Document Number		Created VRO	Rev A.2
	CET0SA2			
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INPUT POWER

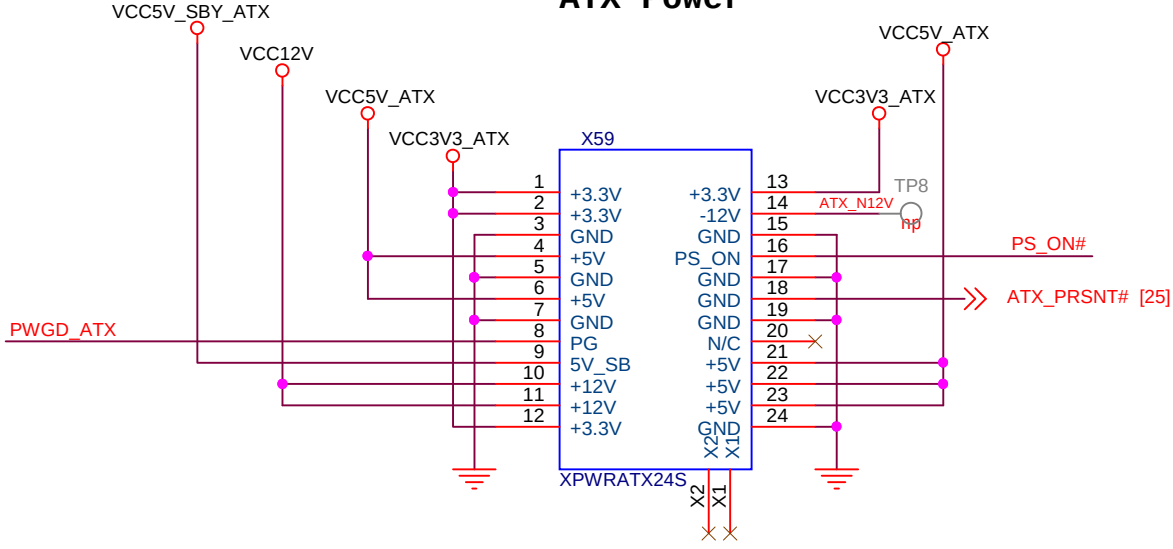
Type Detection



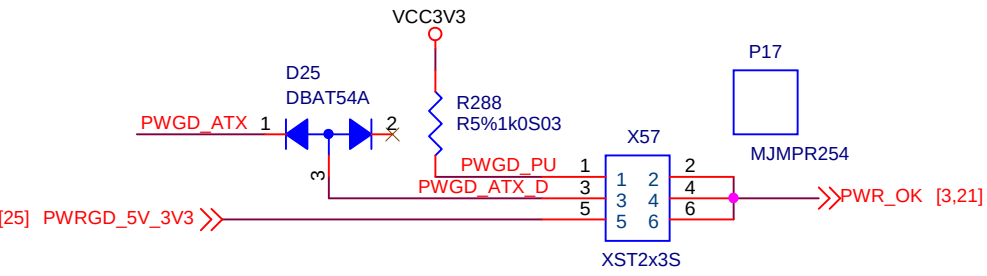
Power Button



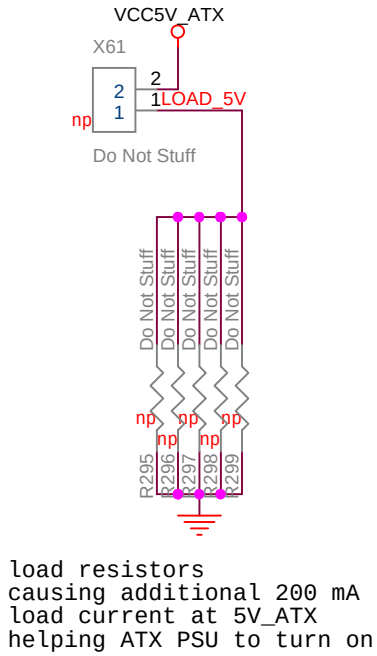
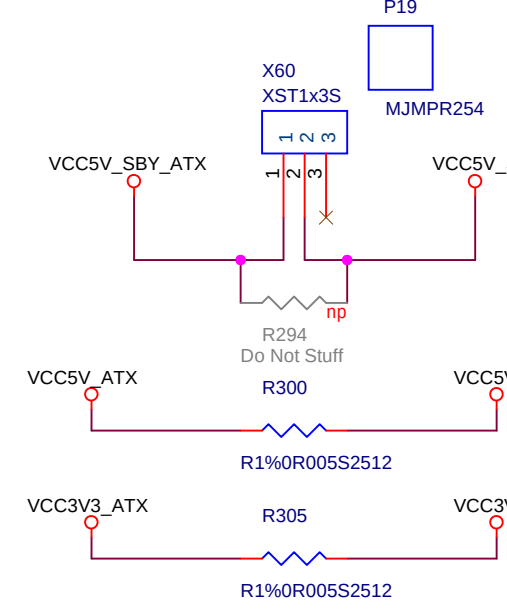
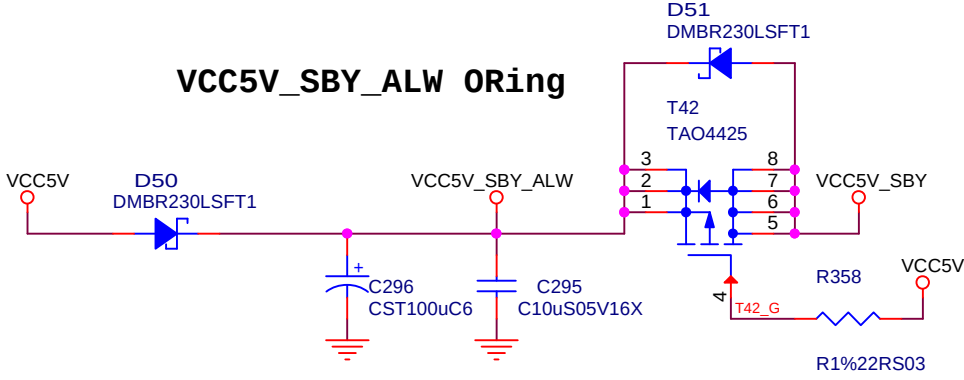
ATX Power



set jumper 1-2 for pull-up on PWR_OK; only for debug
set jumper 3-4 for PWR_OK from ATX supply (default)
set jumper 5-6 for PWR_OK from DC/DC (only in single 12 V mode)



VCC5V_SBY_ALW ORing



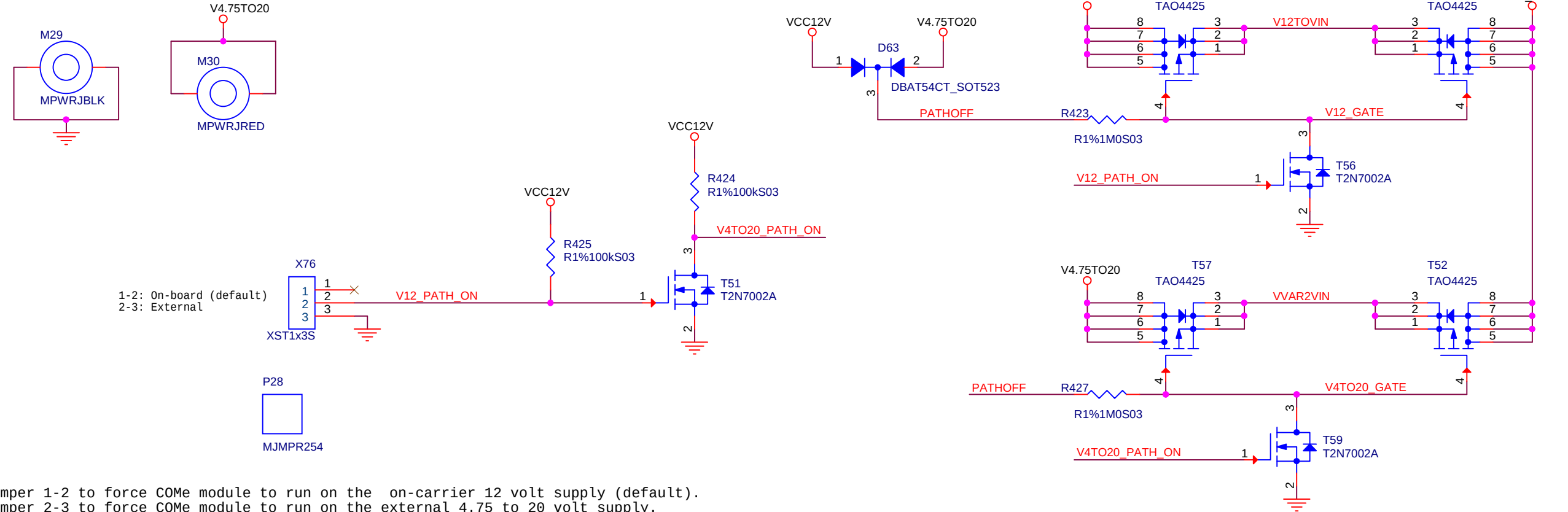
load resistors
causing additional 200 mA
load current at 5V_ATX
helping ATX PSU to turn on

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Title ATX Power, 5V Standby Always				
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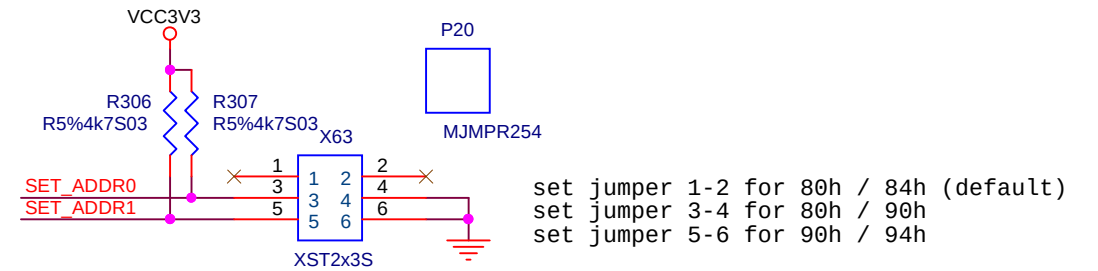
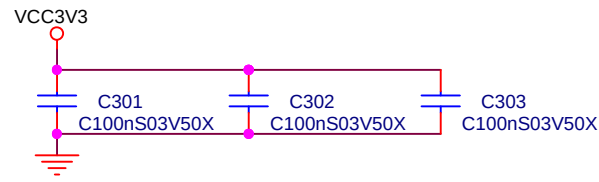
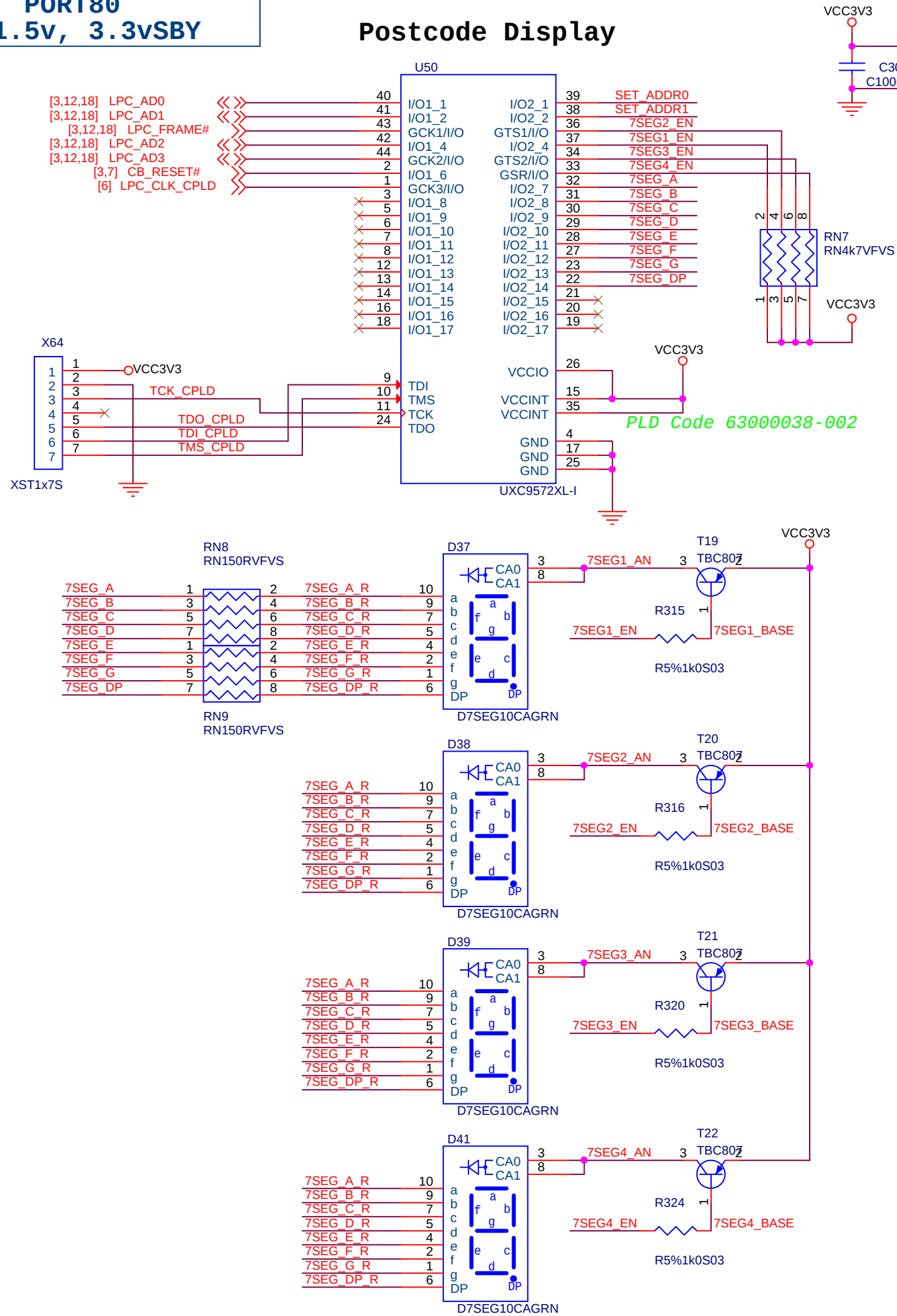
MODULE POWER PATH

COM Express Module
Variable Power In
Connectors

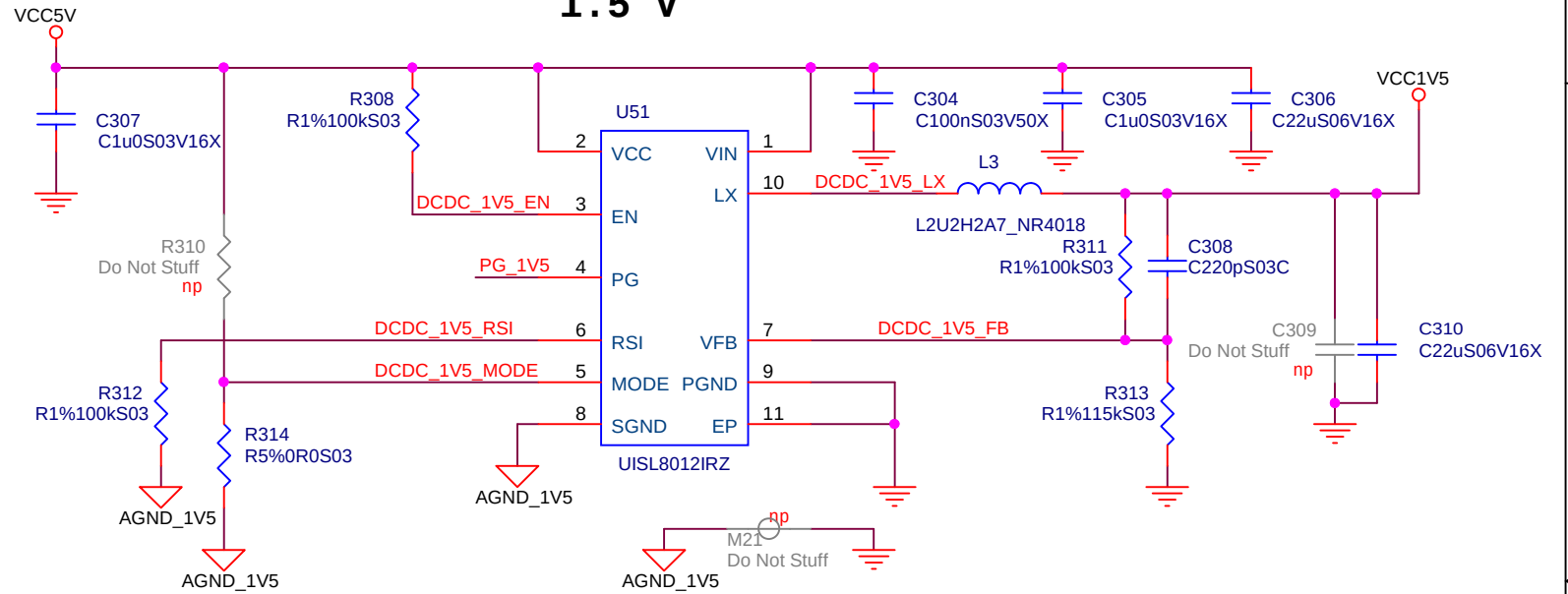


PORT80
1.5v, 3.3vSBY

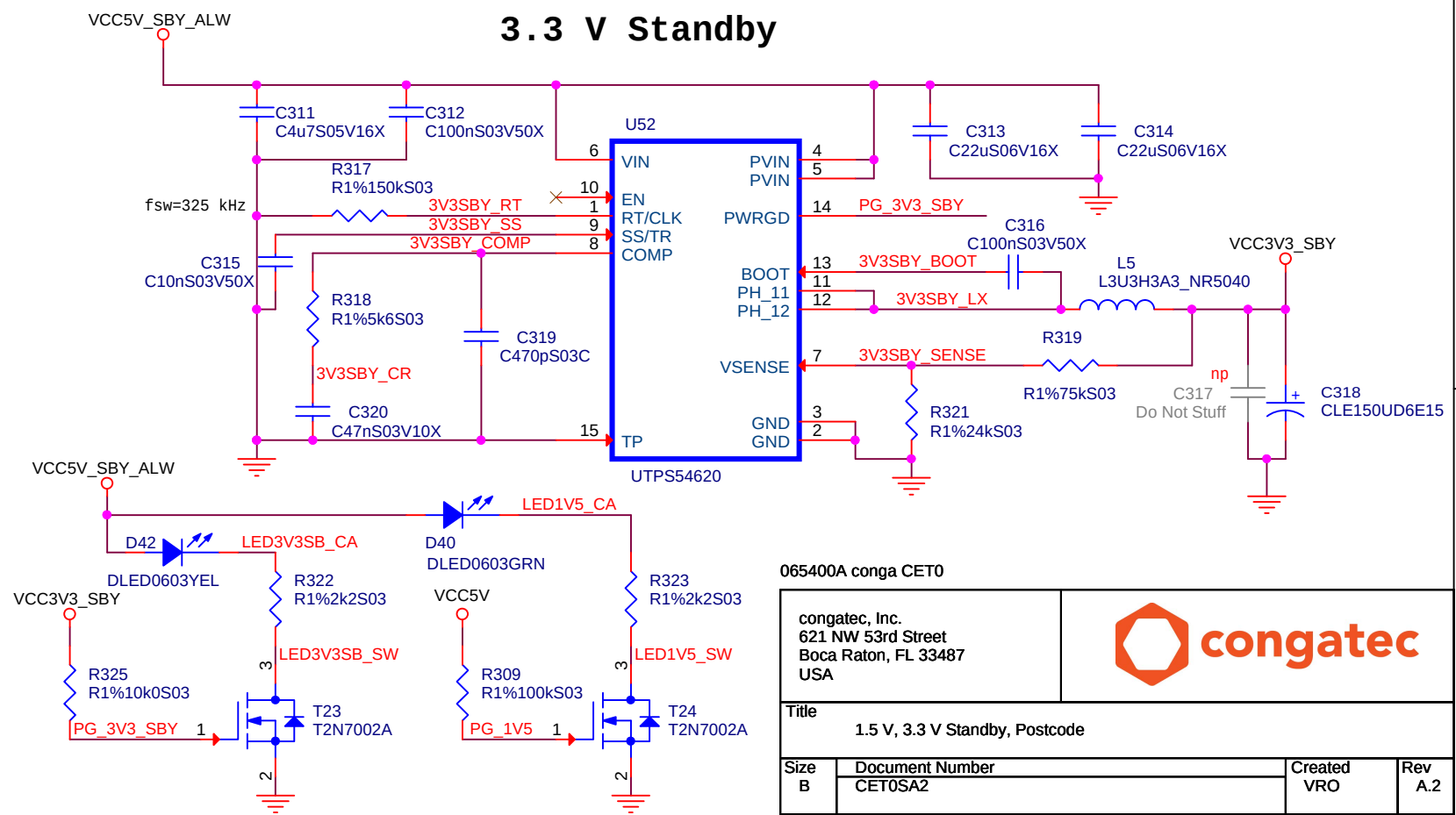
Postcode Display



1.5 V



3.3 V Standby



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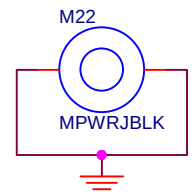
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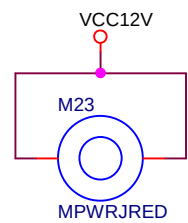
Title
1.5 V, 3.3 V Standby, Postcode

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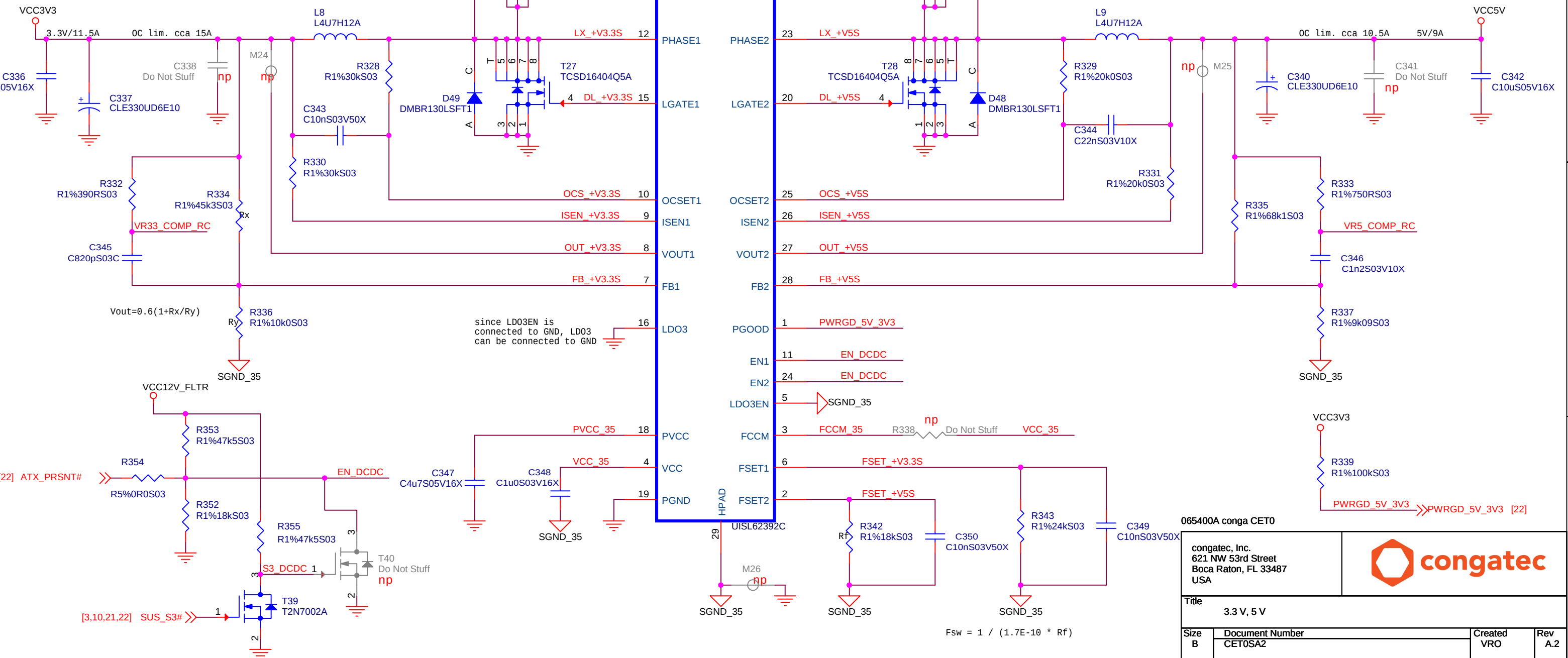
VRs 5V & 3.3V



Power In connectors BANANA JACK



3.3V



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Title	3.3 V, 5 V
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REV HISTORY

A2

15.09.2016 DMI U75 pin 1, NoStuff R79 PU, Stuff R113 PD
(to resolve PCIe 2.0 Clk jitter issue discovered in MA40 DVT by reducing the bandwidth of the U75 clk buffer)

NOTE: These was no A.1 revision of the CET0 schematics; MEVAL revision A.1 added non-schematic parts to BOM and modified other documentation

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Title

History

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B

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VRO

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A.2

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