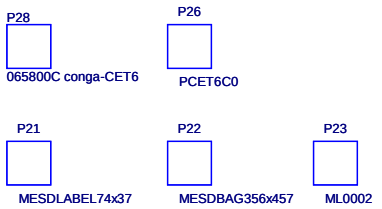
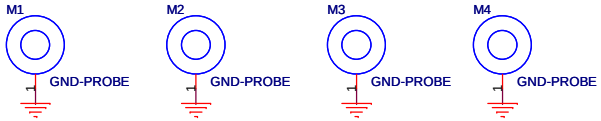
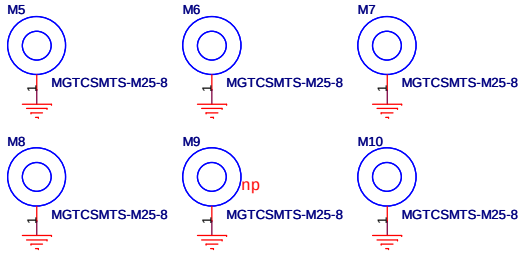
CET6

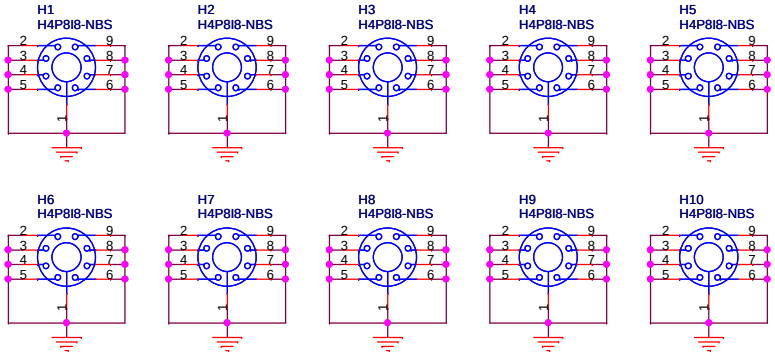
COM.0 Type 6 Evaluation Baseboard

Rev. C.0









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Variants

Base	Standard w/ SuperIO W83627-DHG-P

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Title: CET6 - COM Express Type 6 Evaluation Backplane			
Size: B	Document Number: CET6SC0	Created: SRO	Rev: C.0
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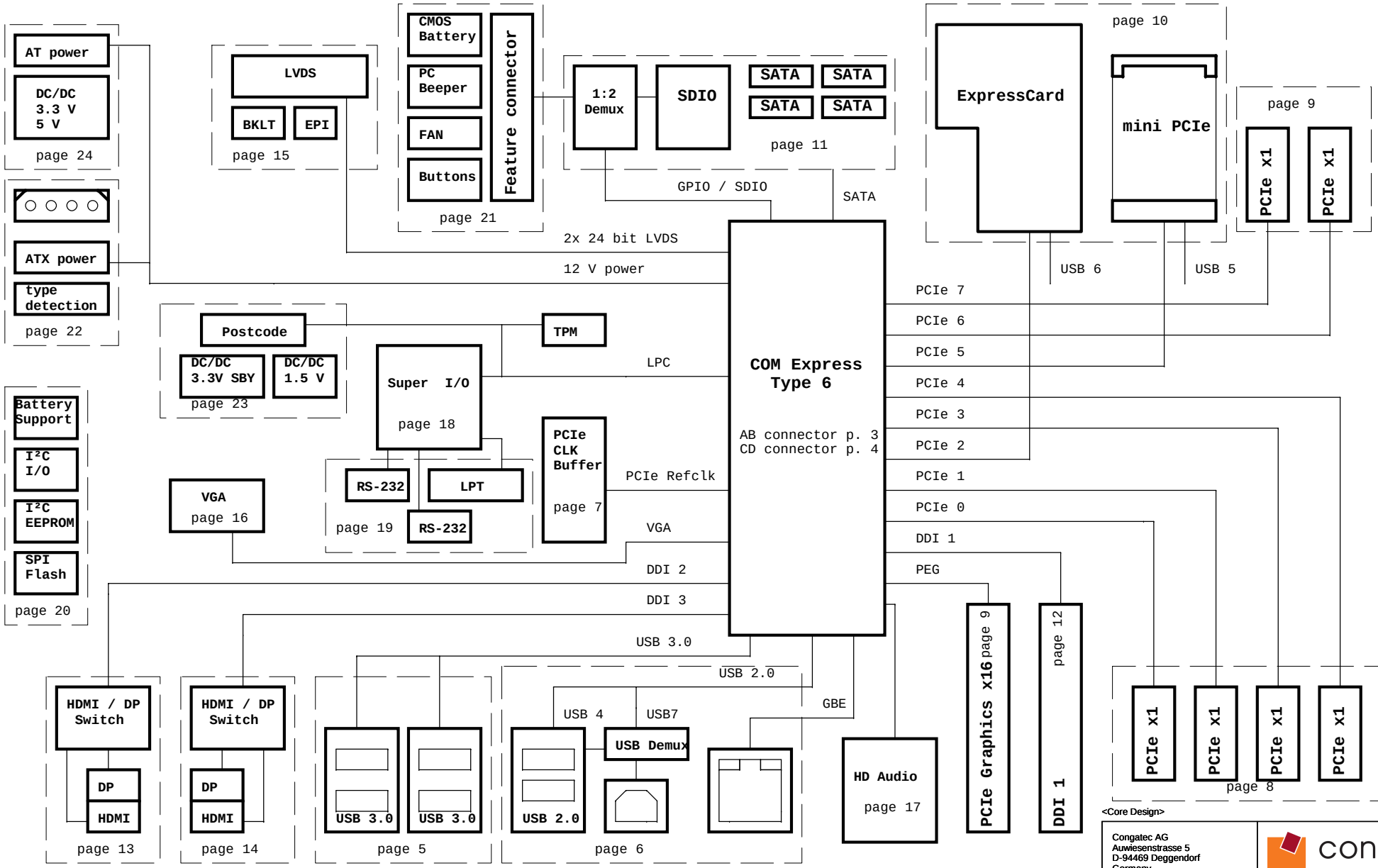

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Title: Block Diagram			
Size: B	Document Number: CET6SC0	Created: SRO, KLI	Rev: C.0
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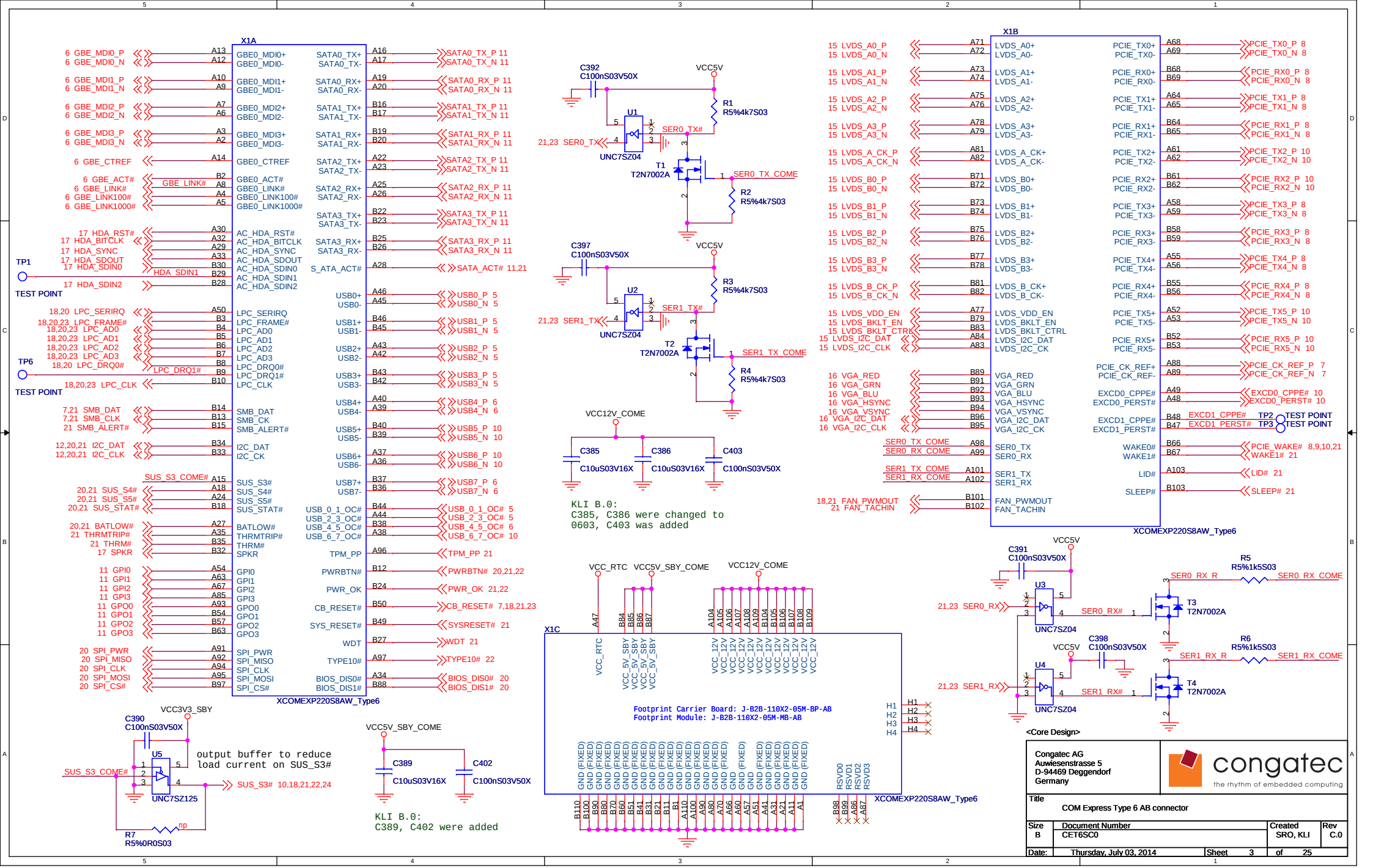
X1A
XCOMEXP220S8AW_Type6
TP1
TEST POINT
TP6
TEST POINT
C390
C100nS03V50X
U5
UNC7SZ125
R7
R5%0R0S03
output buffer to reduce
load current on SUS_S3#
C389
C10uS03V16X
C402
C100nS03V50X
KLI B.0:
C389, C402 were added
C392
C100nS03V50X
U1
UNC7SZ04
T1
T2N7002A
R1
R5%4k7S03
R2
R5%4k7S03
C397
C100nS03V50X
U2
UNC7SZ04
T2
T2N7002A
R3
R5%4k7S03
R4
R5%4k7S03
C385
C10uS03V16X
C386
C10uS03V16X
C403
C100nS03V50X
KLI B.0:
C385, C386 were changed to
0603, C403 was added
X1C
Footprint Carrier Board: J-B2B-110X2-05M-BP-AB
Footprint Module: J-B2B-110X2-05M-MB-AB
XCOMEXP220S8AW_Type6
X1B
XCOMEXP220S8AW_Type6
C391
C100nS03V50X
U3
UNC7SZ04
T3
T2N7002A
R5
R5%1k5S03
C398
C100nS03V50X
U4
UNC7SZ04
T4
T2N7002A
R6
R5%1k5S03
<Core Design>
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Title
COM Express Type 6 AB connector
Size B
Document Number CET6SC0
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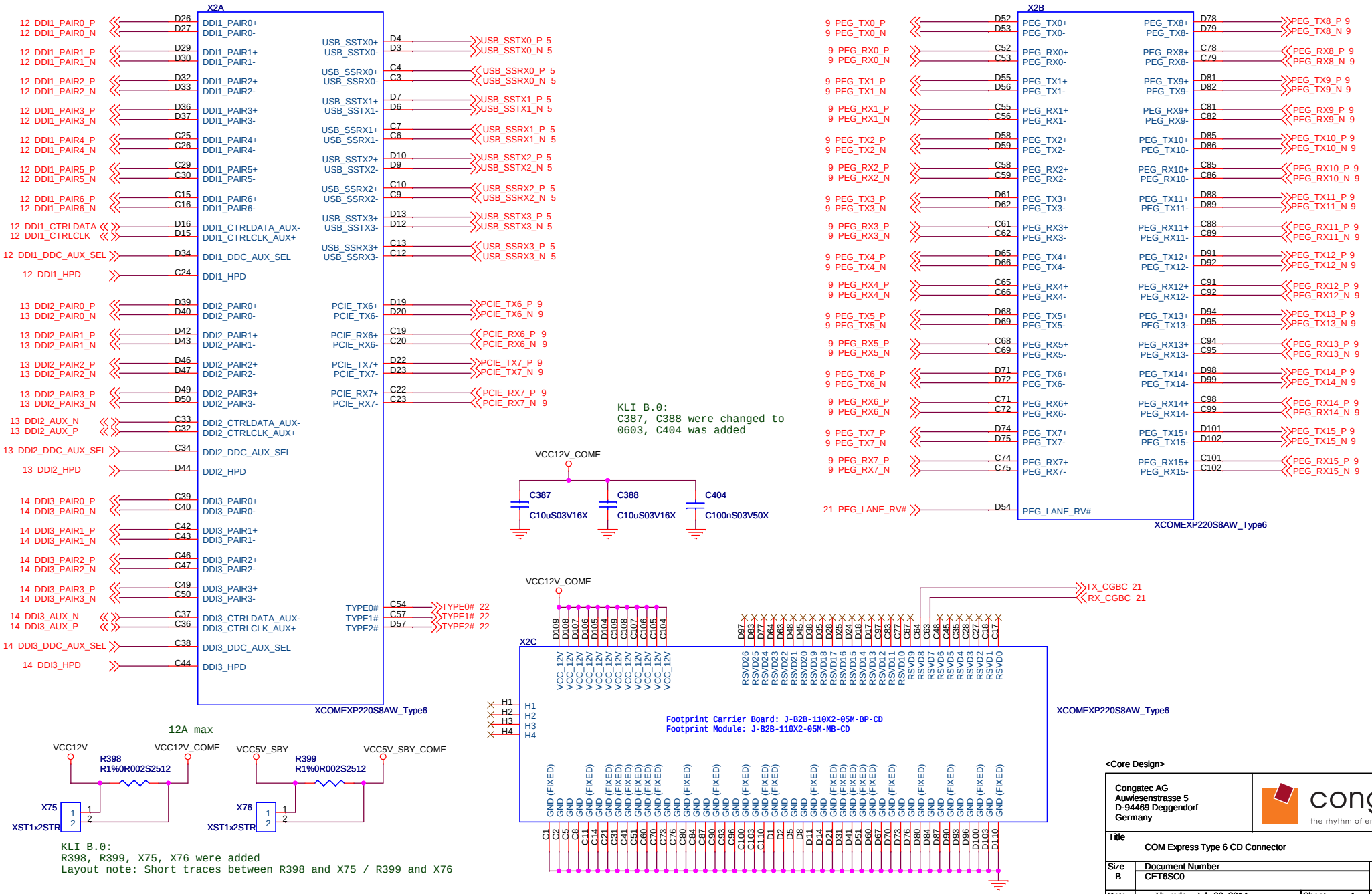
X2A
12 DDI1_PAIR0_P
12 DDI1_PAIR0_N
12 DDI1_PAIR1_P
12 DDI1_PAIR1_N
12 DDI1_PAIR2_P
12 DDI1_PAIR2_N
12 DDI1_PAIR3_P
12 DDI1_PAIR3_N
12 DDI1_PAIR4_P
12 DDI1_PAIR4_N
12 DDI1_PAIR5_P
12 DDI1_PAIR5_N
12 DDI1_PAIR6_P
12 DDI1_PAIR6_N
12 DDI1_CTRLDATA
12 DDI1_CTRLCLK
12 DDI1_DDC_AUX_SEL
12 DDI1_HPD
13 DDI2_PAIR0_P
13 DDI2_PAIR0_N
13 DDI2_PAIR1_P
13 DDI2_PAIR1_N
13 DDI2_PAIR2_P
13 DDI2_PAIR2_N
13 DDI2_PAIR3_P
13 DDI2_PAIR3_N
13 DDI2_AUX_N
13 DDI2_AUX_P
13 DDI2_DDC_AUX_SEL
13 DDI2_HPD
14 DDI3_PAIR0_P
14 DDI3_PAIR0_N
14 DDI3_PAIR1_P
14 DDI3_PAIR1_N
14 DDI3_PAIR2_P
14 DDI3_PAIR2_N
14 DDI3_PAIR3_P
14 DDI3_PAIR3_N
14 DDI3_AUX_N
14 DDI3_AUX_P
14 DDI3_DDC_AUX_SEL
14 DDI3_HPD
DDI1_PAIR0+
DDI1_PAIR0-
DDI1_PAIR1+
DDI1_PAIR1-
DDI1_PAIR2+
DDI1_PAIR2-
DDI1_PAIR3+
DDI1_PAIR3-
DDI1_PAIR4+
DDI1_PAIR4-
DDI1_PAIR5+
DDI1_PAIR5-
DDI1_PAIR6+
DDI1_PAIR6-
DDI1_CTRLDATA_AUX-
DDI1_CTRLCLK_AUX+
DDI1_DDC_AUX_SEL
DDI1_HPD
DDI2_PAIR0+
DDI2_PAIR0-
DDI2_PAIR1+
DDI2_PAIR1-
DDI2_PAIR2+
DDI2_PAIR2-
DDI2_PAIR3+
DDI2_PAIR3-
DDI2_CTRLDATA_AUX-
DDI2_CTRLCLK_AUX+
DDI2_DDC_AUX_SEL
DDI2_HPD
DDI3_PAIR0+
DDI3_PAIR0-
DDI3_PAIR1+
DDI3_PAIR1-
DDI3_PAIR2+
DDI3_PAIR2-
DDI3_PAIR3+
DDI3_PAIR3-
DDI3_CTRLDATA_AUX-
DDI3_CTRLCLK_AUX+
DDI3_DDC_AUX_SEL
DDI3_HPD
USB_SSTX0+
USB_SSTX0-
USB_SSRX0+
USB_SSRX0-
USB_SSTX1+
USB_SSTX1-
USB_SSRX1+
USB_SSRX1-
USB_SSTX2+
USB_SSTX2-
USB_SSRX2+
USB_SSRX2-
USB_SSTX3+
USB_SSTX3-
USB_SSRX3+
USB_SSRX3-
USB_SSTX0_P 5
USB_SSTX0_N 5
USB_SSRX0_P 5
USB_SSRX0_N 5
USB_SSTX1_P 5
USB_SSTX1_N 5
USB_SSRX1_P 5
USB_SSRX1_N 5
USB_SSTX2_P 5
USB_SSTX2_N 5
USB_SSRX2_P 5
USB_SSRX2_N 5
USB_SSTX3_P 5
USB_SSTX3_N 5
USB_SSRX3_P 5
USB_SSRX3_N 5
PCIE_TX6+
PCIE_TX6-
PCIE_RX6+
PCIE_RX6-
PCIE_TX7+
PCIE_TX7-
PCIE_RX7+
PCIE_RX7-
PCIE_TX6_P 9
PCIE_TX6_N 9
PCIE_RX6_P 9
PCIE_RX6_N 9
PCIE_TX7_P 9
PCIE_TX7_N 9
PCIE_RX7_P 9
PCIE_RX7_N 9
TYPE0#
TYPE1#
TYPE2#
TYPE0# 22
TYPE1# 22
TYPE2# 22
XCOMEXP220S8AW_Type6
X2B
9 PEG_TX0_P
9 PEG_TX0_N
9 PEG_RX0_P
9 PEG_RX0_N
9 PEG_TX1_P
9 PEG_TX1_N
9 PEG_RX1_P
9 PEG_RX1_N
9 PEG_TX2_P
9 PEG_TX2_N
9 PEG_RX2_P
9 PEG_RX2_N
9 PEG_TX3_P
9 PEG_TX3_N
9 PEG_RX3_P
9 PEG_RX3_N
9 PEG_TX4_P
9 PEG_TX4_N
9 PEG_RX4_P
9 PEG_RX4_N
9 PEG_TX5_P
9 PEG_TX5_N
9 PEG_RX5_P
9 PEG_RX5_N
9 PEG_TX6_P
9 PEG_TX6_N
9 PEG_RX6_P
9 PEG_RX6_N
9 PEG_TX7_P
9 PEG_TX7_N
9 PEG_RX7_P
9 PEG_RX7_N
21 PEG_LANE_RV#
PEG_TX0+
PEG_TX0-
PEG_RX0+
PEG_RX0-
PEG_TX1+
PEG_TX1-
PEG_RX1+
PEG_RX1-
PEG_TX2+
PEG_TX2-
PEG_RX2+
PEG_RX2-
PEG_TX3+
PEG_TX3-
PEG_RX3+
PEG_RX3-
PEG_TX4+
PEG_TX4-
PEG_RX4+
PEG_RX4-
PEG_TX5+
PEG_TX5-
PEG_RX5+
PEG_RX5-
PEG_TX6+
PEG_TX6-
PEG_RX6+
PEG_RX6-
PEG_TX7+
PEG_TX7-
PEG_RX7+
PEG_RX7-
PEG_LANE_RV#
PEG_TX8+
PEG_TX8-
PEG_RX8+
PEG_RX8-
PEG_TX9+
PEG_TX9-
PEG_RX9+
PEG_RX9-
PEG_TX10+
PEG_TX10-
PEG_RX10+
PEG_RX10-
PEG_TX11+
PEG_TX11-
PEG_RX11+
PEG_RX11-
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PEG_TX12-
PEG_RX12+
PEG_RX12-
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PEG_TX14+
PEG_TX14-
PEG_RX14+
PEG_RX14-
PEG_TX15+
PEG_TX15-
PEG_RX15+
PEG_RX15-
PEG_TX8_P 9
PEG_TX8_N 9
PEG_RX8_P 9
PEG_RX8_N 9
PEG_TX9_P 9
PEG_TX9_N 9
PEG_RX9_P 9
PEG_RX9_N 9
PEG_TX10_P 9
PEG_TX10_N 9
PEG_RX10_P 9
PEG_RX10_N 9
PEG_TX11_P 9
PEG_TX11_N 9
PEG_RX11_P 9
PEG_RX11_N 9
PEG_TX12_P 9
PEG_TX12_N 9
PEG_RX12_P 9
PEG_RX12_N 9
PEG_TX13_P 9
PEG_TX13_N 9
PEG_RX13_P 9
PEG_RX13_N 9
PEG_TX14_P 9
PEG_TX14_N 9
PEG_RX14_P 9
PEG_RX14_N 9
PEG_TX15_P 9
PEG_TX15_N 9
PEG_RX15_P 9
PEG_RX15_N 9
XCOMEXP220S8AW_Type6
KLI B.0:
C387, C388 were changed to
0603, C404 was added
VCC12V_COME
C387
C10uS03V16X
C388
C10uS03V16X
C404
C100nS03V50X
X2C
TX_CGBC 21
RX_CGBC 21
VCC_12V
RSVD
GND (FIXED)
H1
H2
H3
H4
Footprint Carrier Board: J-B2B-110X2-05M-BP-CD
Footprint Module: J-B2B-110X2-05M-MB-CD
XCOMEXP220S8AW_Type6
12A max
VCC12V
VCC12V_COME
R398
R1%0R002S2512
X75
XST1x2STR
VCC5V_SBY
VCC5V_SBY_COME
R399
R1%0R002S2512
X76
XST1x2STR
KLI B.0:
R398, R399, X75, X76 were added
Layout note: Short traces between R398 and X75 / R399 and X76
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Title
COM Express Type 6 CD Connector
Size
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Document Number
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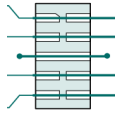
USB 3.0

Layout Note: Route USB 3.0 signals through
D44, D45, D46, D47 in the following style



USB 3.0 spec. requires
low ESR cap (>= 120 uF)
directly connected to I/O connector

FB1 FB100R1A7S03
VCC_USB0 — VCC_USB0_CON
C2 CLE150UD6E15 + C1 C100nS03V50X
GND_USB0_CON
FB2 FB100R1A7S03

FB3 FBD90R0A33S05D
3 USB0_N
3 USB0_P

U8 DIP4220C26
VCC5V

D44 DTPD4EUSB30
4 USB_SSTX0_N
4 USB_SSTX0_P
4 USB_SSTX1_N
4 USB_SSTX1_P
USB_SSTX0_N
USB_SSTX0_P
USB_SSTX1_N
USB_SSTX1_P

X3 XUSB30R2
VCC_USB0_CON
USB0_CON_N
USB0_CON_P
GND_USB0_CON
USB_SSRX0_N
USB_SSRX0_P
GND_USB0_CON
USB_SSTX0_N
USB_SSTX0_P
VCC_USB1_CON
USB1_CON_N
USB1_CON_P
GND_USB1_CON
USB_SSRX1_N
USB_SSRX1_P
GND_USB1_CON
USB_SSTX1_N
USB_SSTX1_P
P1_VCC
P1_USB2.0_D-
P1_USB2.0_D+
P1_GND
P1_USB3_SSRX-
P1_USB3_SSRX+
P1_GND_DRAIN
P1_USB3_SSTX-
P1_USB3_SSTX+
P2_VCC
P2_USB2.0_D-
P2_USB2.0_D+
P2_GND
P2_USB3_SSRX-
P2_USB3_SSRX+
P2_GND_DRAIN
P2_USB3_SSTX-
P2_USB3_SSTX+
H1 H2 H3 H4

FB4 FBD90R0A33S05D
3 USB1_N
3 USB1_P

U7 UTPS2062C
VCC5V
C5 C10uS05V16X
C6 C100nS03V50X np
USB01_VCC_EN#
R8 R5%0R0S03
IN OCA# ENA# OUTA ENB# OUTB GND OCB# PAD
VCC_USB0
VCC_USB1
USB_0_1_OC# 3

Layout note:
Place D44, D45 close to X3 and X4

KLI B.0:
U7, U11 were changed for TPS2062C

FB5 FB100R1A7S03
VCC_USB1 — VCC_USB1_CON
C8 CLE150UD6E15 + C7 C100nS03V50X
GND_USB1_CON
FB6 FB100R1A7S03

D45 DTPD4EUSB30
4 USB_SSRX0_N
4 USB_SSRX0_P
4 USB_SSRX1_N
4 USB_SSRX1_P
USB_SSRX0_N
USB_SSRX0_P
USB_SSRX1_N
USB_SSRX1_P

FB8 FB100R1A7S03
VCC_USB2 — VCC_USB2_CON
C12 CLE150UD6E15 + C11 C100nS03V50X
GND_USB2_CON
FB9 FB100R1A7S03

FB10 FBD90R0A33S05D
3 USB2_N
3 USB2_P

U12 DIP4220C26
VCC5V

D46 DTPD4EUSB30
4 USB_SSTX2_N
4 USB_SSTX2_P
4 USB_SSTX3_N
4 USB_SSTX3_P
USB_SSTX2_N
USB_SSTX2_P
USB_SSTX3_N
USB_SSTX3_P

X4 XUSB30R2
VCC_USB2_CON
USB2_CON_N
USB2_CON_P
GND_USB2_CON
USB_SSRX2_N
USB_SSRX2_P
GND_USB2_CON
USB_SSTX2_N
USB_SSTX2_P
VCC_USB3_CON
USB3_CON_N
USB3_CON_P
GND_USB3_CON
USB_SSRX3_N
USB_SSRX3_P
GND_USB3_CON
USB_SSTX3_N
USB_SSTX3_P
P1_VCC
P1_USB2.0_D-
P1_USB2.0_D+
P1_GND
P1_USB3_SSRX-
P1_USB3_SSRX+
P1_GND_DRAIN
P1_USB3_SSTX-
P1_USB3_SSTX+
P2_VCC
P2_USB2.0_D-
P2_USB2.0_D+
P2_GND
P2_USB3_SSRX-
P2_USB3_SSRX+
P2_GND_DRAIN
P2_USB3_SSTX-
P2_USB3_SSTX+
H1 H2 H3 H4

FB11 FBD90R0A33S05D
3 USB3_N
3 USB3_P

U11 UTPS2062C
VCC5V
C15 C10uS05V16X
C16 C100nS03V50X np
USB23_VCC_EN#
R9 R5%0R0S03
IN OCA# ENA# OUTA ENB# OUTB GND OCB# PAD
VCC_USB2
VCC_USB3
USB_2_3_OC# 3

D47 DTPD4EUSB30
4 USB_SSRX2_N
4 USB_SSRX2_P
4 USB_SSRX3_N
4 USB_SSRX3_P
USB_SSRX2_N
USB_SSRX2_P
USB_SSRX3_N
USB_SSRX3_P

Layout note:
Place D46, D47 close to X3 and X4

FB12 FB100R1A7S03
VCC_USB3 — VCC_USB3_CON
C20 CLE150UD6E15 + C19 C100nS03V50X
GND_USB3_CON
FB13 FB100R1A7S03

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Title: USB 3.0			
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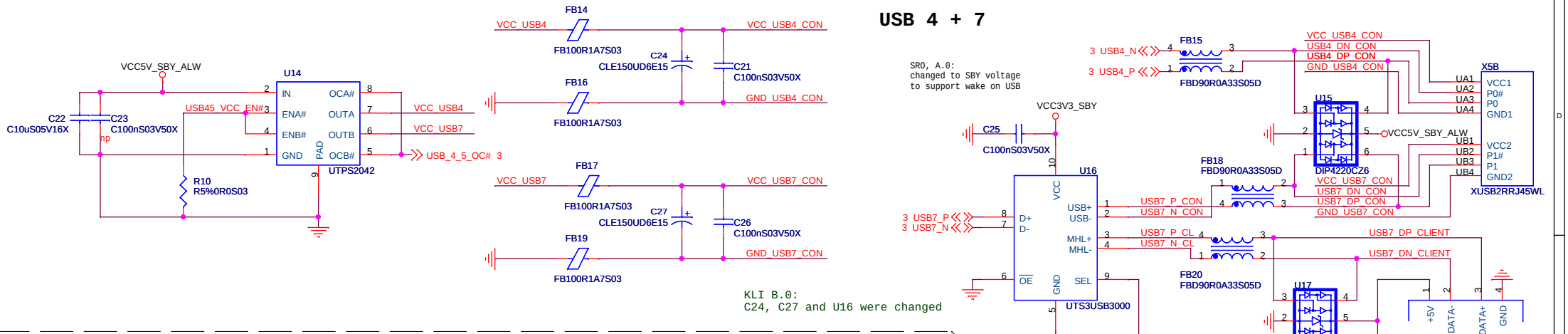
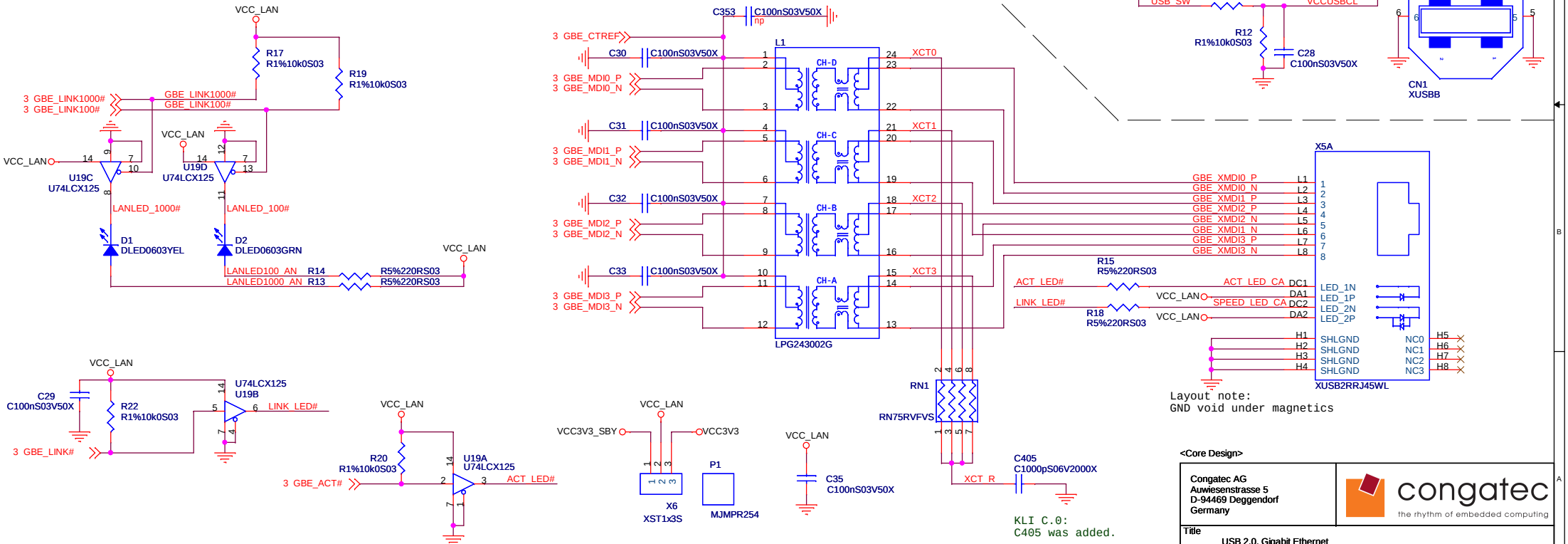
USB 4 + 7



KLI B.0:
C24, C27 and U16 were changed

Gigabit LAN



Layout note:
GND void under magnetics

KLI C.0:
C405 was added.

set jumper 1-2 if LAN Controller is powered from standby voltage (default)
set jumper 2-3 if LAN Controller is powered from S0 voltage

<Core Design>

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Title: USB 2.0, Gigabit Ethernet	
Size: B	Document Number: CET6SC0
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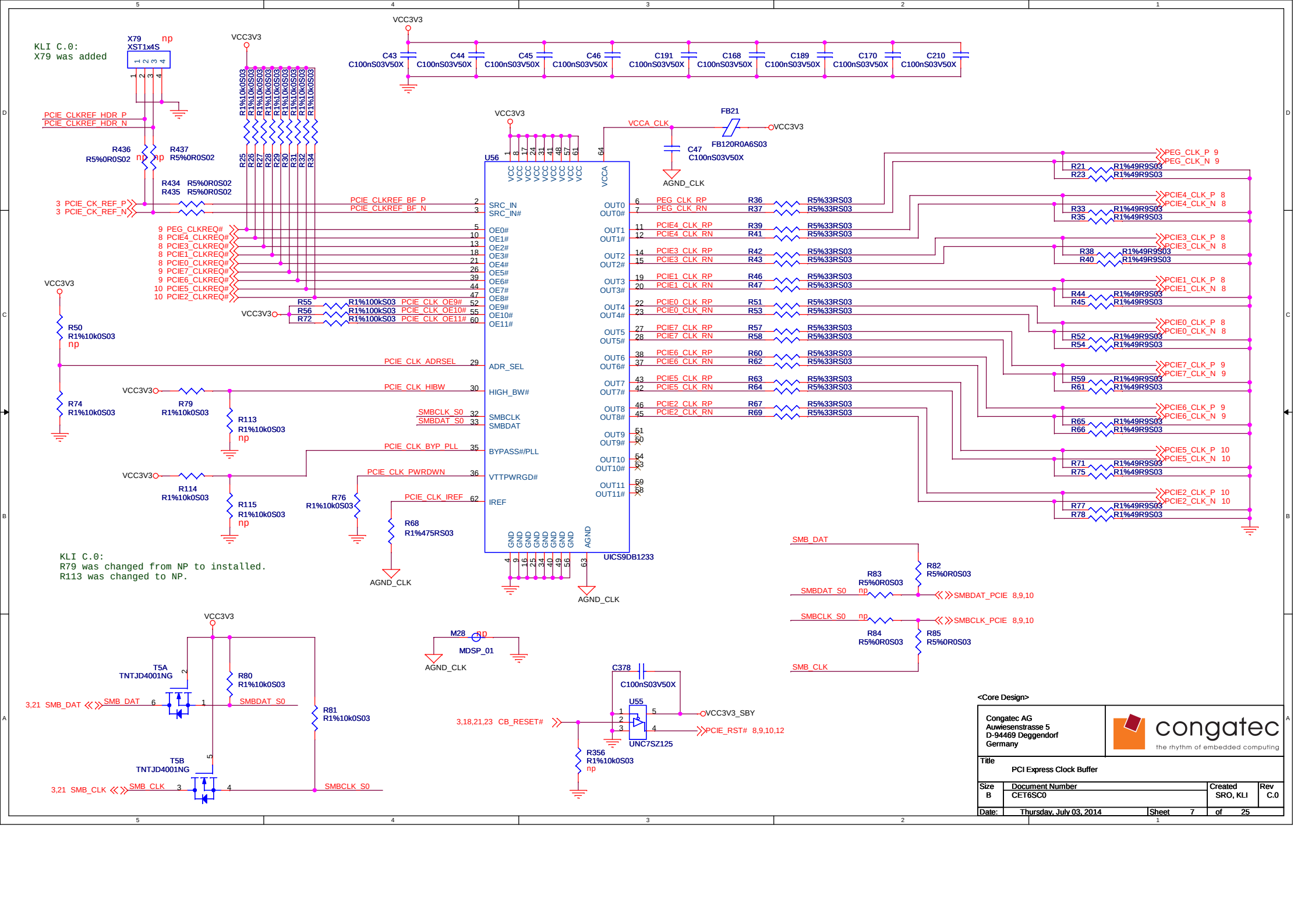
KLI C.0:
X79 was added
X79
XST1x4S
np
VCC3V3
C43 C100nS03V50X
C44 C100nS03V50X
C45 C100nS03V50X
C46 C100nS03V50X
C191 C100nS03V50X
C168 C100nS03V50X
C189 C100nS03V50X
C170 C100nS03V50X
C210 C100nS03V50X
R1%10k0S03
PCIE_CLKREF_HDR_P
PCIE_CLKREF_HDR_N
R436 R5%0R0S02
R437 R5%0R0S02
R434 R5%0R0S02
R435 R5%0R0S02
3 PCIE_CK_REF_P
3 PCIE_CK_REF_N
PCIE_CLKREF_BF_P
PCIE_CLKREF_BF_N
U56
SRC_IN
SRC_IN#
OE0#
OE1#
OE2#
OE3#
OE4#
OE5#
OE6#
OE7#
OE8#
OE9#
OE10#
OE11#
9 PEG_CLKREQ#
8 PCIE4_CLKREQ#
8 PCIE3_CLKREQ#
8 PCIE1_CLKREQ#
8 PCIE0_CLKREQ#
9 PCIE7_CLKREQ#
9 PCIE6_CLKREQ#
10 PCIE5_CLKREQ#
10 PCIE2_CLKREQ#
R55 R1%100kS03 PCIE_CLK_OE9#
R56 R1%100kS03 PCIE_CLK_OE10#
R72 R1%100kS03 PCIE_CLK_OE11#
VCCA_CLK
FB21
FB120R0A6S03
C47 C100nS03V50X
AGND_CLK
VCCA
OUT0 OUT0#
OUT1 OUT1#
OUT2 OUT2#
OUT3 OUT3#
OUT4 OUT4#
OUT5 OUT5#
OUT6 OUT6#
OUT7 OUT7#
OUT8 OUT8#
OUT9 OUT9#
OUT10 OUT10#
OUT11 OUT11#
PEG_CLK_RP
PEG_CLK_RN
PCIE4_CLK_RP
PCIE4_CLK_RN
PCIE3_CLK_RP
PCIE3_CLK_RN
PCIE1_CLK_RP
PCIE1_CLK_RN
PCIE0_CLK_RP
PCIE0_CLK_RN
PCIE7_CLK_RP
PCIE7_CLK_RN
PCIE6_CLK_RP
PCIE6_CLK_RN
PCIE5_CLK_RP
PCIE5_CLK_RN
PCIE2_CLK_RP
PCIE2_CLK_RN
R36 R5%33RS03
R37 R5%33RS03
R39 R5%33RS03
R41 R5%33RS03
R42 R5%33RS03
R43 R5%33RS03
R46 R5%33RS03
R47 R5%33RS03
R51 R5%33RS03
R53 R5%33RS03
R57 R5%33RS03
R58 R5%33RS03
R60 R5%33RS03
R62 R5%33RS03
R63 R5%33RS03
R64 R5%33RS03
R67 R5%33RS03
R69 R5%33RS03
PEG_CLK_P 9
PEG_CLK_N 9
R21 R1%49R9S03
R23 R1%49R9S03
PCIE4_CLK_P 8
PCIE4_CLK_N 8
R33 R1%49R9S03
R35 R1%49R9S03
PCIE3_CLK_P 8
PCIE3_CLK_N 8
R38 R1%49R9S03
R40 R1%49R9S03
PCIE1_CLK_P 8
PCIE1_CLK_N 8
R44 R1%49R9S03
R45 R1%49R9S03
PCIE0_CLK_P 8
PCIE0_CLK_N 8
R52 R1%49R9S03
R54 R1%49R9S03
PCIE7_CLK_P 9
PCIE7_CLK_N 9
R59 R1%49R9S03
R61 R1%49R9S03
PCIE6_CLK_P 9
PCIE6_CLK_N 9
R65 R1%49R9S03
R66 R1%49R9S03
PCIE5_CLK_P 10
PCIE5_CLK_N 10
R71 R1%49R9S03
R75 R1%49R9S03
PCIE2_CLK_P 10
PCIE2_CLK_N 10
R77 R1%49R9S03
R78 R1%49R9S03
R50 R1%10k0S03 np
PCIE_CLK_ADRSEL
PCIE_CLK_HIBW
R74 R1%10k0S03
R79 R1%10k0S03
R113 R1%10k0S03 np
SMBCLK_S0
SMBDAT_S0
SMBCLK
SMBDAT
PCIE_CLK_BYP_PLL
BYPASS#/PLL
PCIE_CLK_PWRDWN
VTTPWRGD#
R114 R1%10k0S03
R115 R1%10k0S03 np
R76 R1%10k0S03
PCIE_CLK_IREF
IREF
R68 R1%475RS03
AGND_CLK
GND
AGND
UICS9DB1233
KLI C.0:
R79 was changed from NP to installed.
R113 was changed to NP.
SMB_DAT
SMBDAT_S0
SMBCLK_S0
SMB_CLK
R82 R5%0R0S03
R83 R5%0R0S03 np
R84 R5%0R0S03
R85 R5%0R0S03
SMBDAT_PCIE 8,9,10
SMBCLK_PCIE 8,9,10
T5A TNTJD4001NG
T5B TNTJD4001NG
R80 R1%10k0S03
R81 R1%10k0S03
3,21 SMB_DAT
3,21 SMB_CLK
M28 np
MDSP_01
C378 C100nS03V50X
U55
UNC7SZ125
3,18,21,23 CB_RESET#
VCC3V3_SBY
PCIE_RST# 8,9,10,12
R356 R1%10k0S03 np
<Core Design>
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Title
PCI Express Clock Buffer
Size B
Document Number CET6SC0
Created SRO, KLI
Rev C.0
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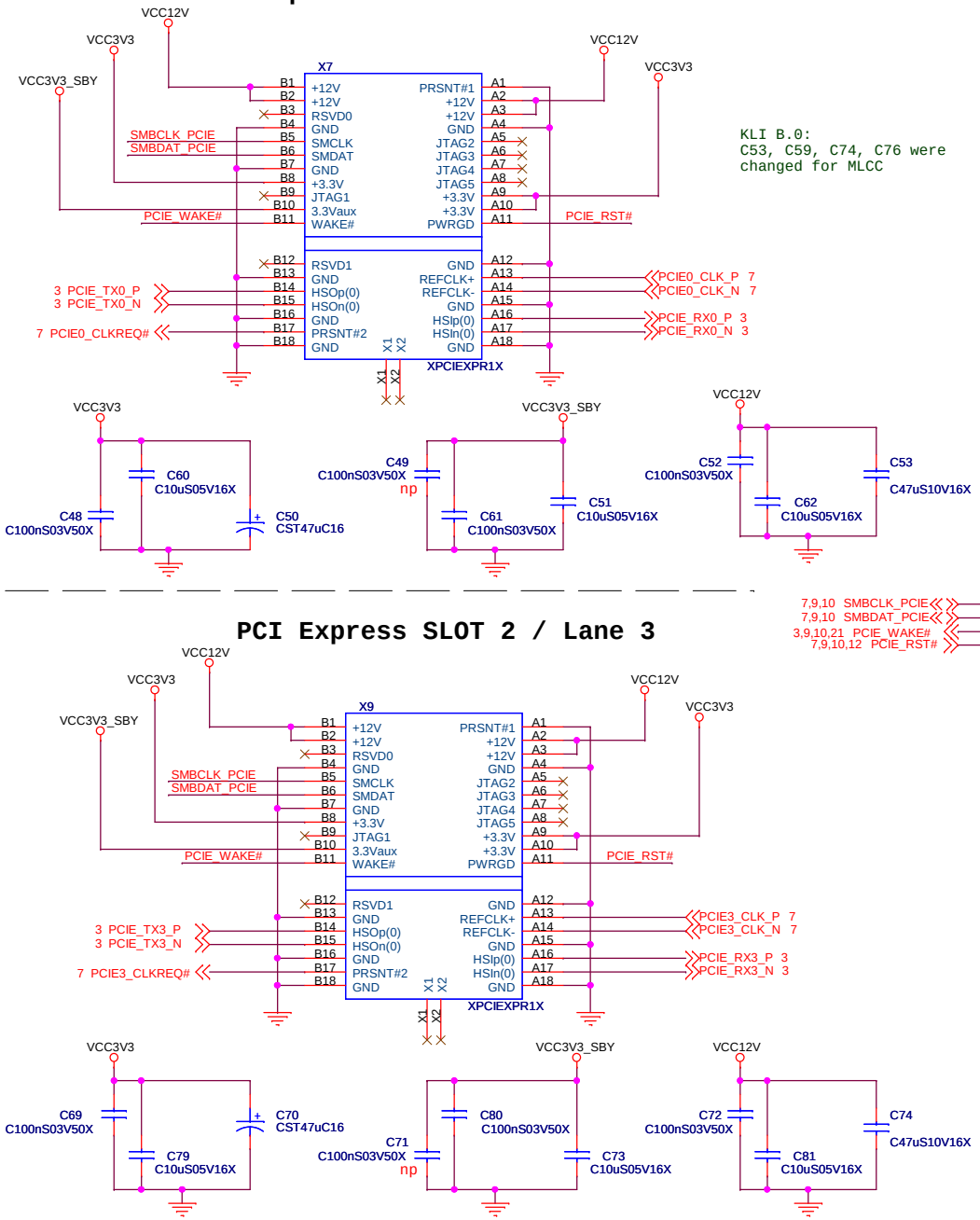
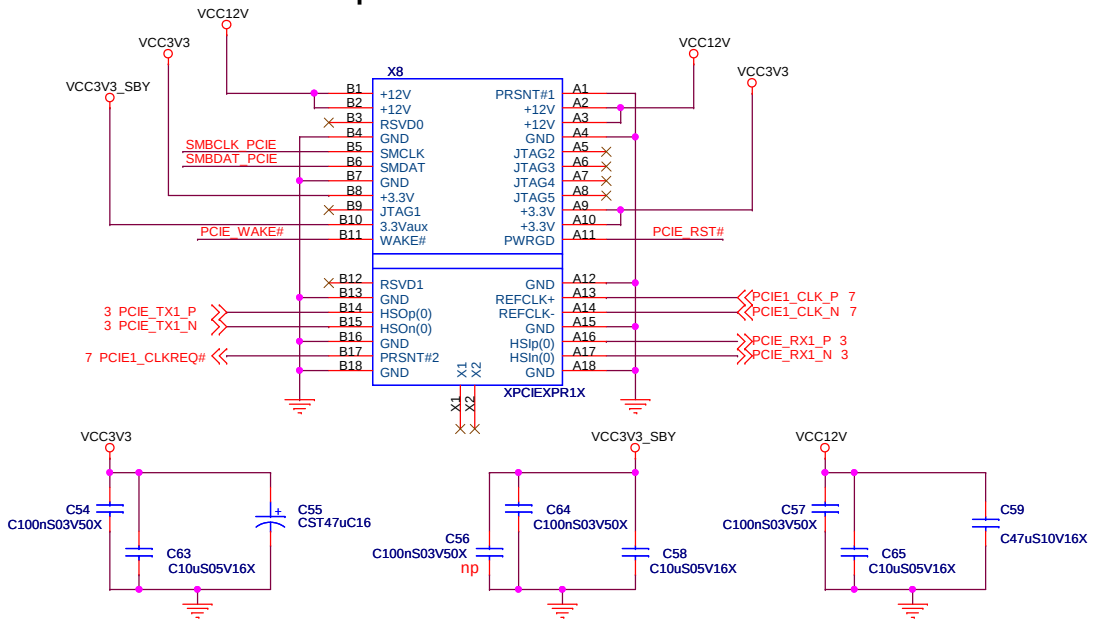
Sheet 7 of 25

PCI Express SLOT 0 / Lane 0



KLI B.0:
C53, C59, C74, C76 were
changed for MLCC

PCI Express SLOT 1 / Lane 1

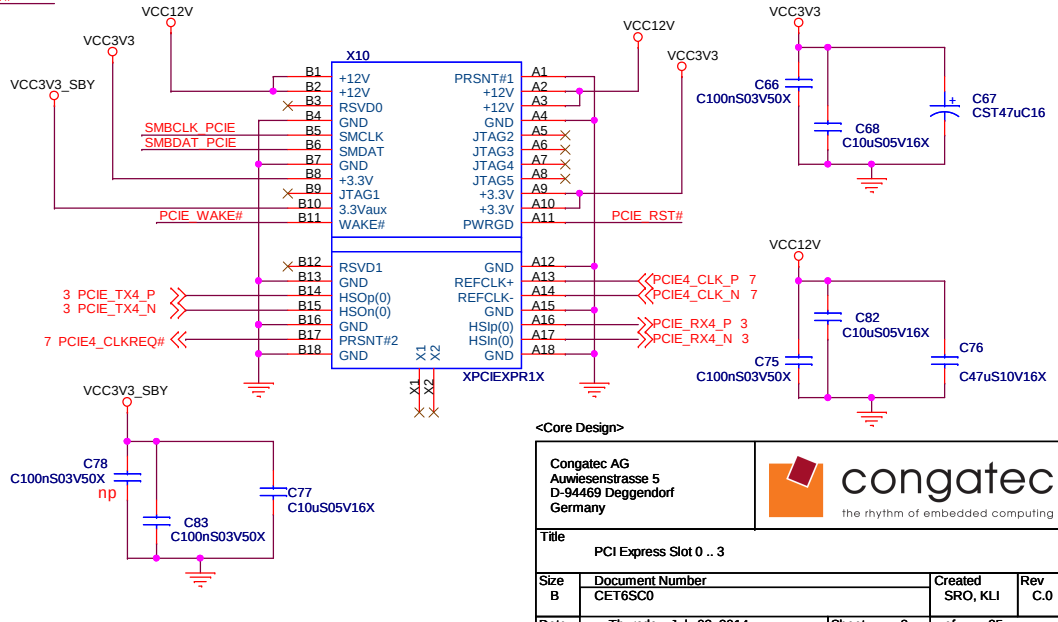


7,9,10 SMBCLK_PCIE
7,9,10 SMBDAT_PCIE
3,9,10,21 PCIE_WAKE#
7,9,10,12 PCIE_RST#

SMBCLK_PCIE
SMBDAT_PCIE
PCIE_WAKE#
PCIE_RST#

PCI Express SLOT 2 / Lane 3

PCI Express SLOT 3 / Lane 4



<Core Design>

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Title: PCI Express Slot 0 .. 3			
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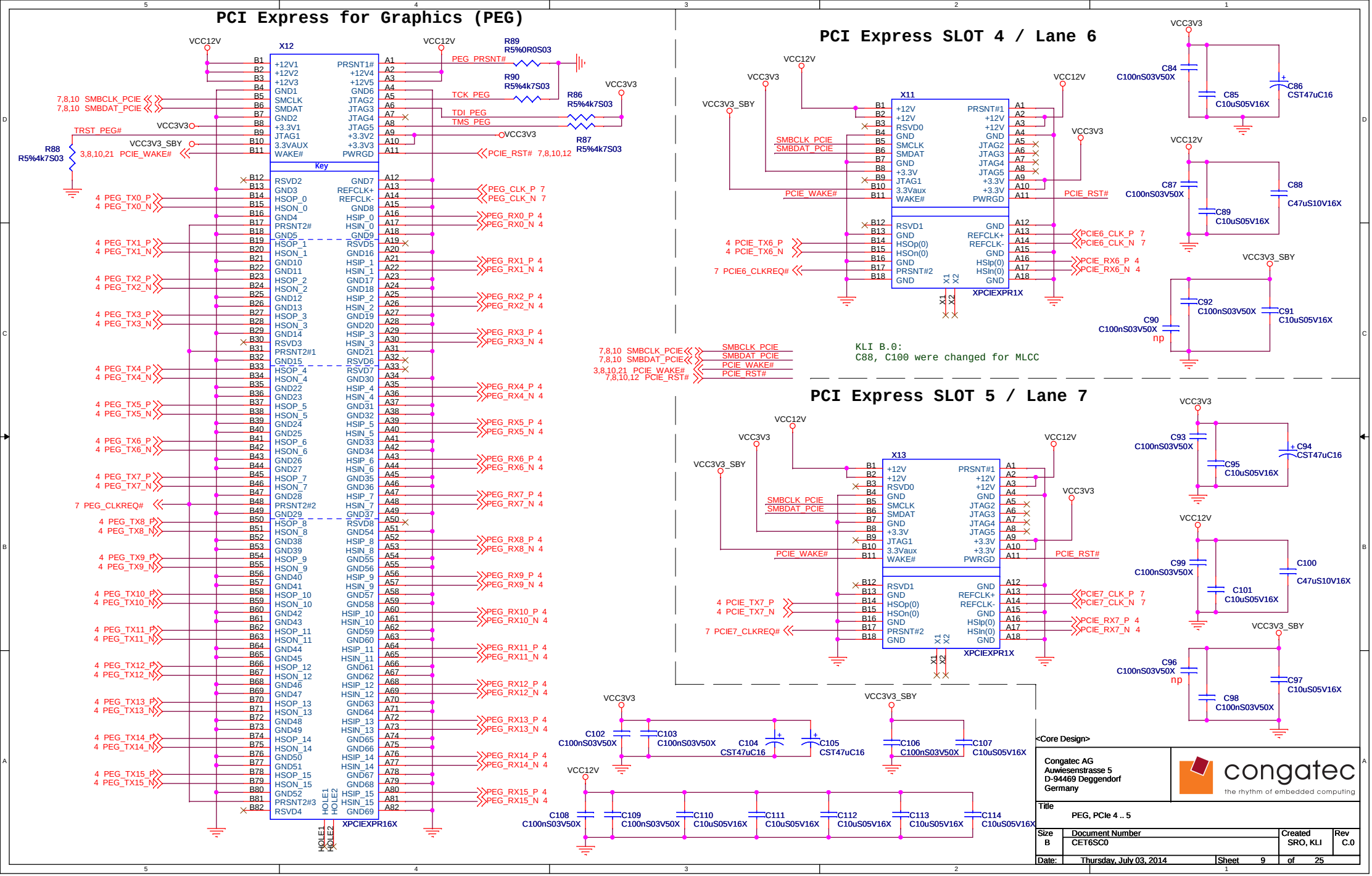
PCI Express for Graphics (PEG)



PCI Express SLOT 4 / Lane 6

KLI B.0:
C88, C100 were changed for MLCC

PCI Express SLOT 5 / Lane 7

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Title: PEG, PCIe 4 .. 5			
Size: B	Document Number: CET6SC0	Created: SRO, KLI	Rev: C.0
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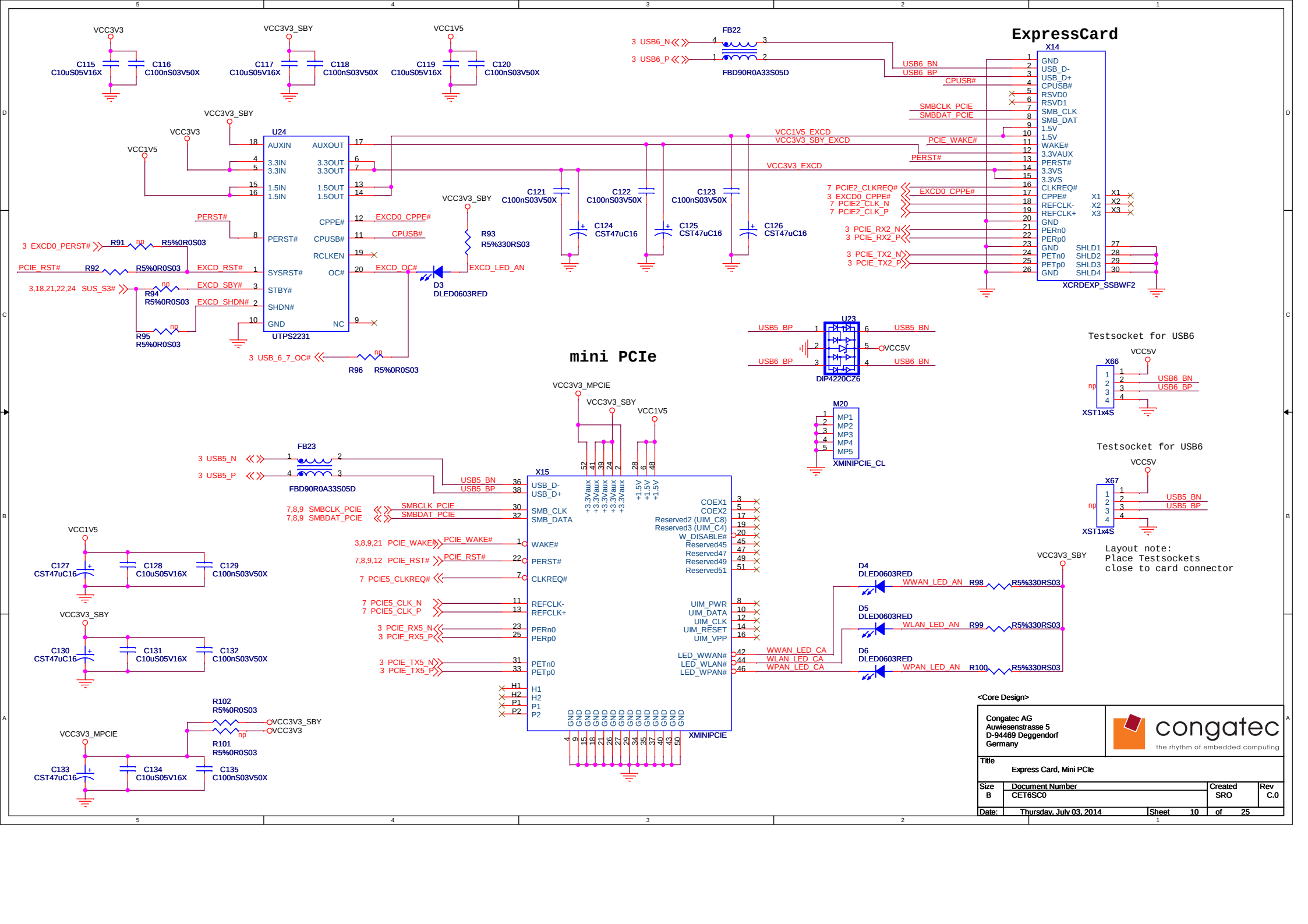
ExpressCard
mini PCIe
VCC3V3
VCC3V3_SBY
VCC1V5
VCC3V3_MPCIE
C115 C10uS05V16X
C116 C100nS03V50X
C117 C10uS05V16X
C118 C100nS03V50X
C119 C10uS05V16X
C120 C100nS03V50X
FB22
FBD90R0A33S05D
X14
XCRDEXP_SSBWF2
U24
UTPS2231
C121 C100nS03V50X
C122 C100nS03V50X
C123 C100nS03V50X
C124 CST47uC16
C125 CST47uC16
C126 CST47uC16
R91 R5%0R0S03
R92 R5%0R0S03
R93 R5%330RS03
R94 R5%0R0S03
R95 R5%0R0S03
R96 R5%0R0S03
D3 DLED0603RED
U23
DIP4220CZ6
Testsocket for USB6
X66
XST1x4S
M20
XMINIPICIE_CL
FB23
FBD90R0A33S05D
X15
XMINIPICIE
Testsocket for USB6
X67
XST1x4S
Layout note:
Place Testsockets
close to card connector
C127 CST47uC16
C128 C10uS05V16X
C129 C100nS03V50X
C130 CST47uC16
C131 C10uS05V16X
C132 C100nS03V50X
C133 CST47uC16
C134 C10uS05V16X
C135 C100nS03V50X
R101 R5%0R0S03
R102 R5%0R0S03
D4 DLED0603RED
D5 DLED0603RED
D6 DLED0603RED
R98 R5%330RS03
R99 R5%330RS03
R100 R5%330RS03
<Core Design>
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Express Card, Mini PCIe
Size B
Document Number CET6SC0
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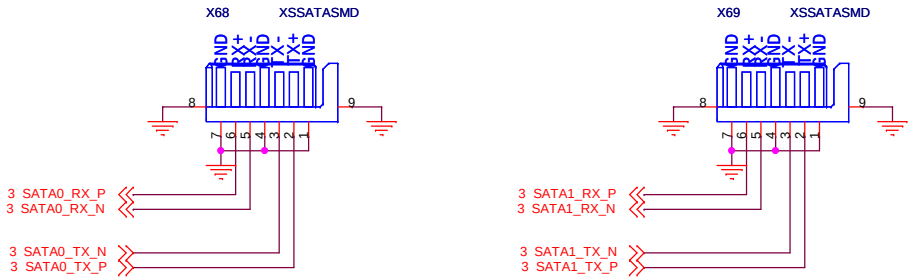
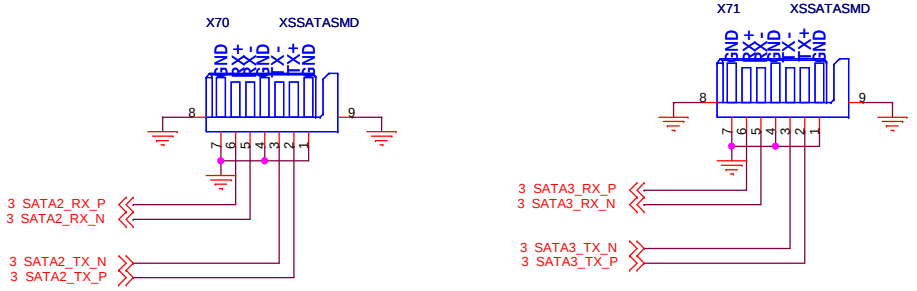
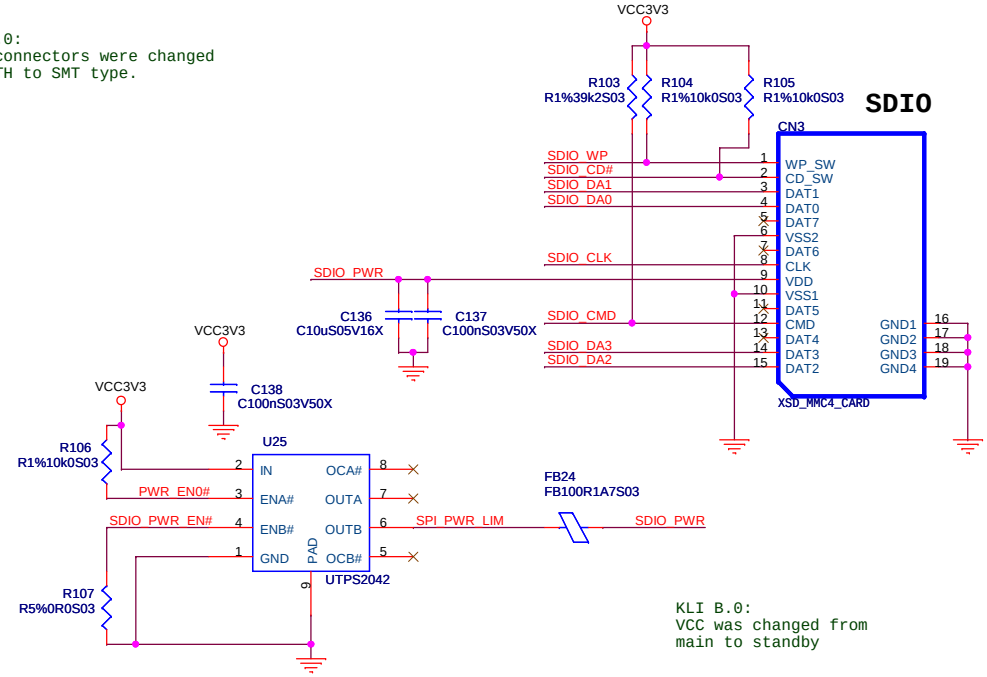
SATA

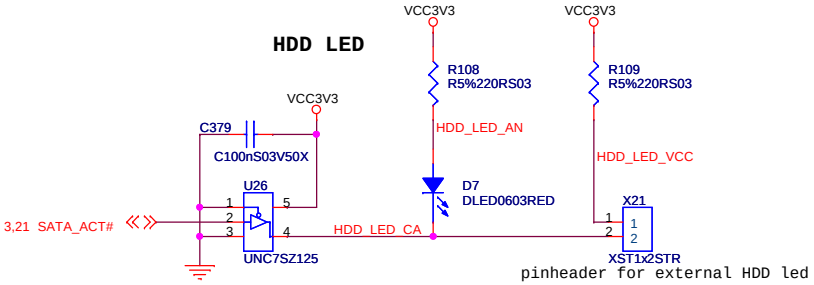




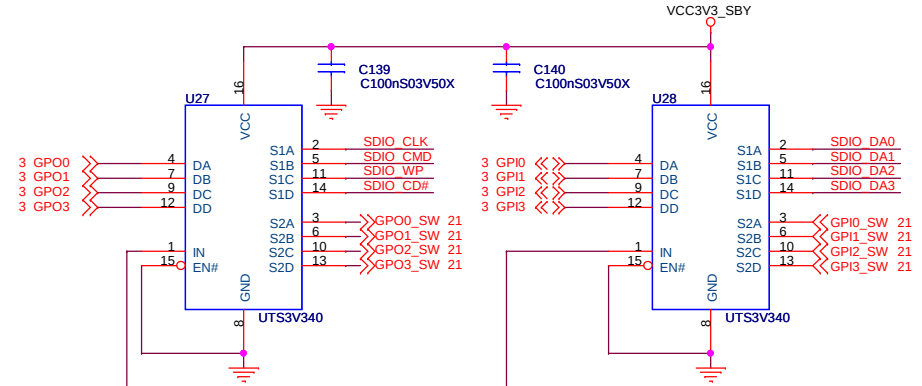
KLI B.0:
SATA connectors were changed
from TH to SMT type.

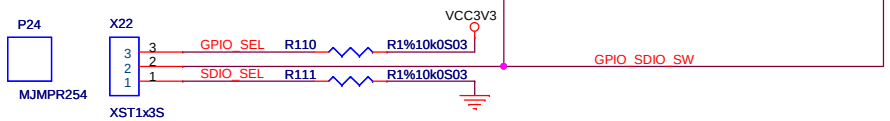


KLI B.0:
VCC was changed from
main to standby



pinheader for external HDD led





set jumper 1-2 for SDIO
set jumper 2-3 for GPIO (default)

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Title: SATA, SDIO			
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Date: Thursday, July 03, 2014	Sheet 11 of 25		

KLI B.0:
I2C bus is connected to X23

KLI B.0:
AC coupling capacitors
were changed from 0603
to 0402

KLI B.0:
I2C bus for S0 only

DDI1 AUX SEL:
Set Jumper to 1-2 for DP
Set Jumper to 2-3 for HDMI / DVI / SDVO (default)

KLI B.0:
C146 was changed for MLCC
C151 was changed for a higher value
C153 was deleted
Layout note: place C146 close to X12 (PEG),
place C151 between X12 and X23 (PEG and DDI1)

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Title: Digital Display Interface 1

Size	Document Number	Created	Rev
B	CET6SC0	SRO, KLI	C.0

Date: Thursday, July 03, 2014 Sheet 12 of 25

Digital Display Interface 2 to HDMI / DISPLAY PORT

240mA max
(4 DP Lanes)

KLI B.0:
DisplayPort re-driver switch with TMDS translator was changed for a new type SN75DP126

U29 USN75DP126SS

HPD_SNK are 5V tolerant with 130k pull-down

2kV ESD HBM

VSadj = 4k7 +/- 1k
4k7 ... 1000mV

DDIx_AUX is AC coupled on module

I2C 100kb/s, disabled by default
I2C_CTL_EN:
MID ... I2C enabled, 0x58h write, 0x59h read
HIGH ... I2C enabled, 0x5Ah write, 0x5Bh read

Default setting:
I2C disabled, PRE = 0 dB, lowest EQ

U60 U7WBD3306

connects PU only in TMDS mode

NOTE: CAD
DisplayPort is selected: CAD_SRC = CAD_SNK
(active high as default)
HDMI/DVI is selected: CAD_SRC is driven high

when the HDMI/DVI sink is selected:
jumper 1-2: output is DVI 1.0 compilant
jumper 2-3: output is HDMI 1.4b compilant (default)

DDC input/output buffer control
(default is lowest input threshold)

the DisplayPort sink has priority

TMDS slew rate control - transition rise and fall time at 20% and 80% (default is 85ps ... 160ps)

U20 UTPS2042

U18 UTPS2042

X26A DP(U) XDPHDMI62ETH

X26B HDMI(L) XDPHDMI62ETH

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Title: Digital Display Interface 2			
Size: B	Document Number: CET6SC0	Created: KLI	Rev: C.0
Date: Thursday, July 03, 2014	Sheet 13 of 25		

Digital Display Interface 3 to HDMI / DISPLAY PORT

240mA max
(4 DP Lanes)

KLI B.0:
DisplayPort re-driver switch with TMDS translator was changed for a new type SN75DP126

U30 USN75DP126SS

HPD_SNK are 5V tolerant with 130k pull-down

2kV ESD HBM

VSadj = 4k7 +/- 1k
4k7 ... 1000mV

DDIx_AUX is AC coupled on module

I2C 100kb/s, disabled by default
I2C_CTL_EN:
MID ... I2C enabled, 0x58h write, 0x59h read
HIGH ... I2C enabled, 0x5Ah write, 0x5Bh read

Default setting:
I2C disabled, PRE = 0 dB, lowest EQ

DDC input/output buffer control
(default is lowest input threshold)

the DisplayPort sink has priority

TMDS slew rate control - transition rise and fall time at 20% and 80% (default is 85ps ... 160ps)

connects PU only in TMDS mode

NOTE: CAD
DisplayPort is selected: CAD_SRC = CAD_SNK
(active high as default)
HDMI/DVI is selected: CAD_SRC is driven high

when the HDMI/DVI sink is selected:
jumper 1-2: output is DVI 1.0 compilant
jumper 2-3: output is HDMI 1.4b compilant (default)

X74A XDPHDMI62ETH

X74B XDPHDMI62ETH

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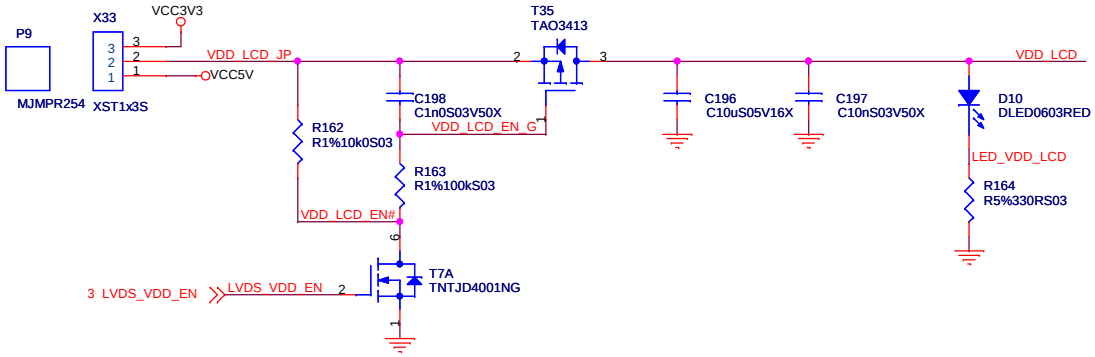
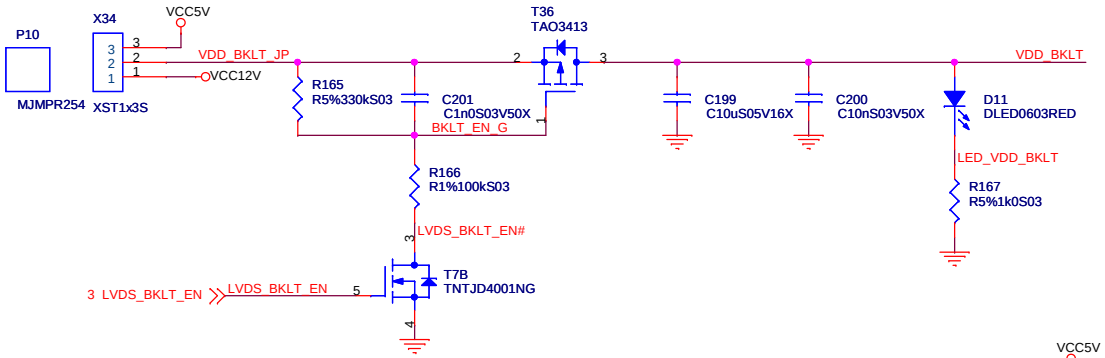
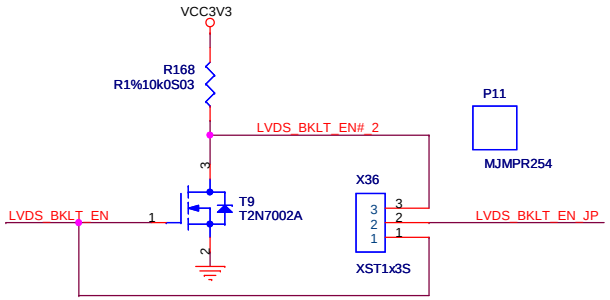
Title: Digital Display Interface 3			
Size: B	Document Number: CET6SC0	Created: KLI	Rev: C.0
Date: Thursday, July 03, 2014	Sheet 14 of 25		

set jumper 1-2 for 5 V LCD supply voltage (default)
set jumper 2-3 for 3.3 V LCD supply voltage



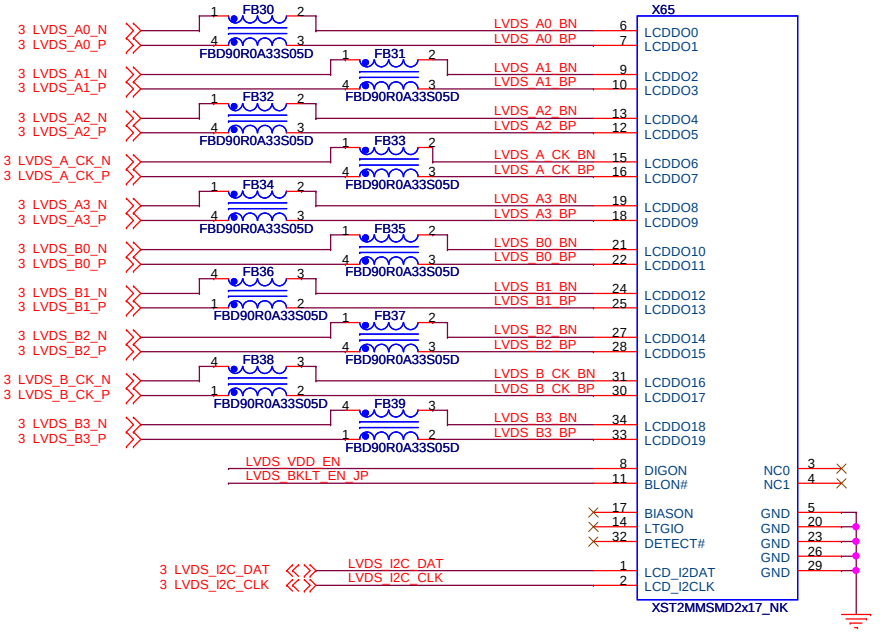
set jumper 1-2 for 12 V backlight voltage (default)
set jumper 2-3 for 5 V backlight voltage





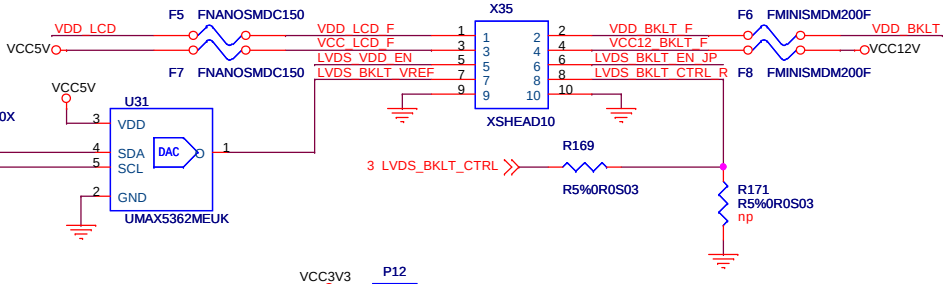
set jumper 1-2 for non-inverted BKLT_EN signal (default)
set jumper 2-3 for inverted BKLT_EN signal

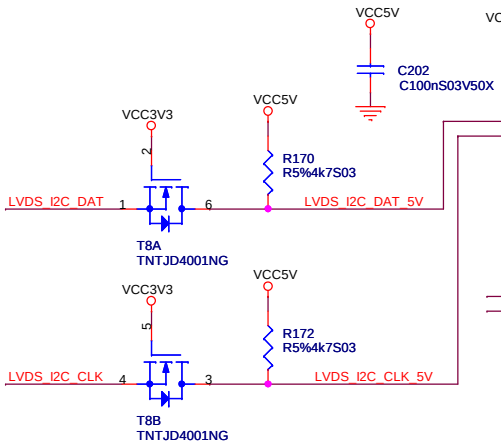
LCD

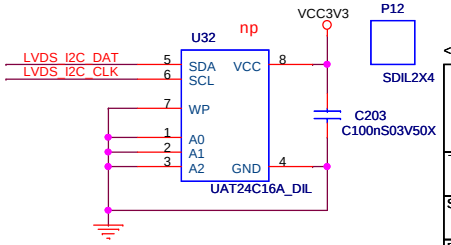


LCD / BKLT POWER

KLI B.0:
X35.6 is connected
to LVDS_BKLT_EN_JP







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Title: LVDS			
Size: B	Document Number: CET6SC0	Created: SRO, KLI	Rev: C.0
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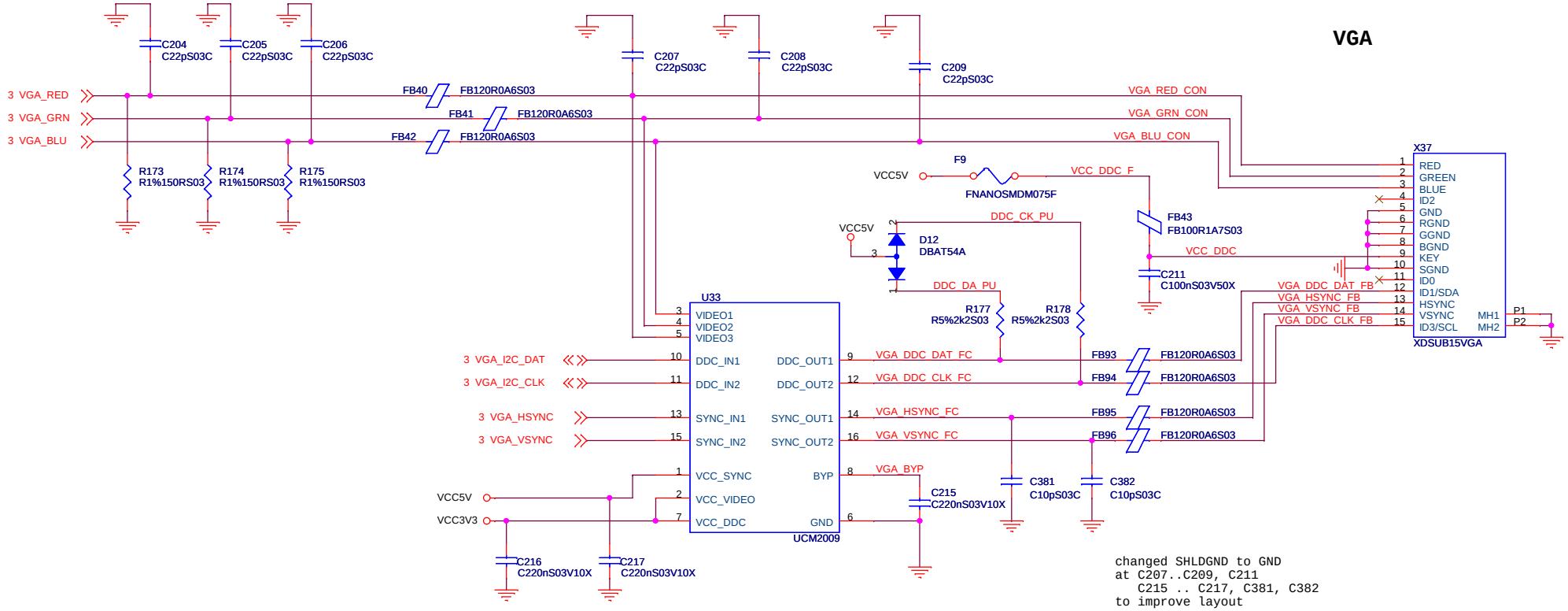
VGA



changed SHLDGND to GND
at C207..C209, C211
C215 .. C217, C381, C382
to improve layout

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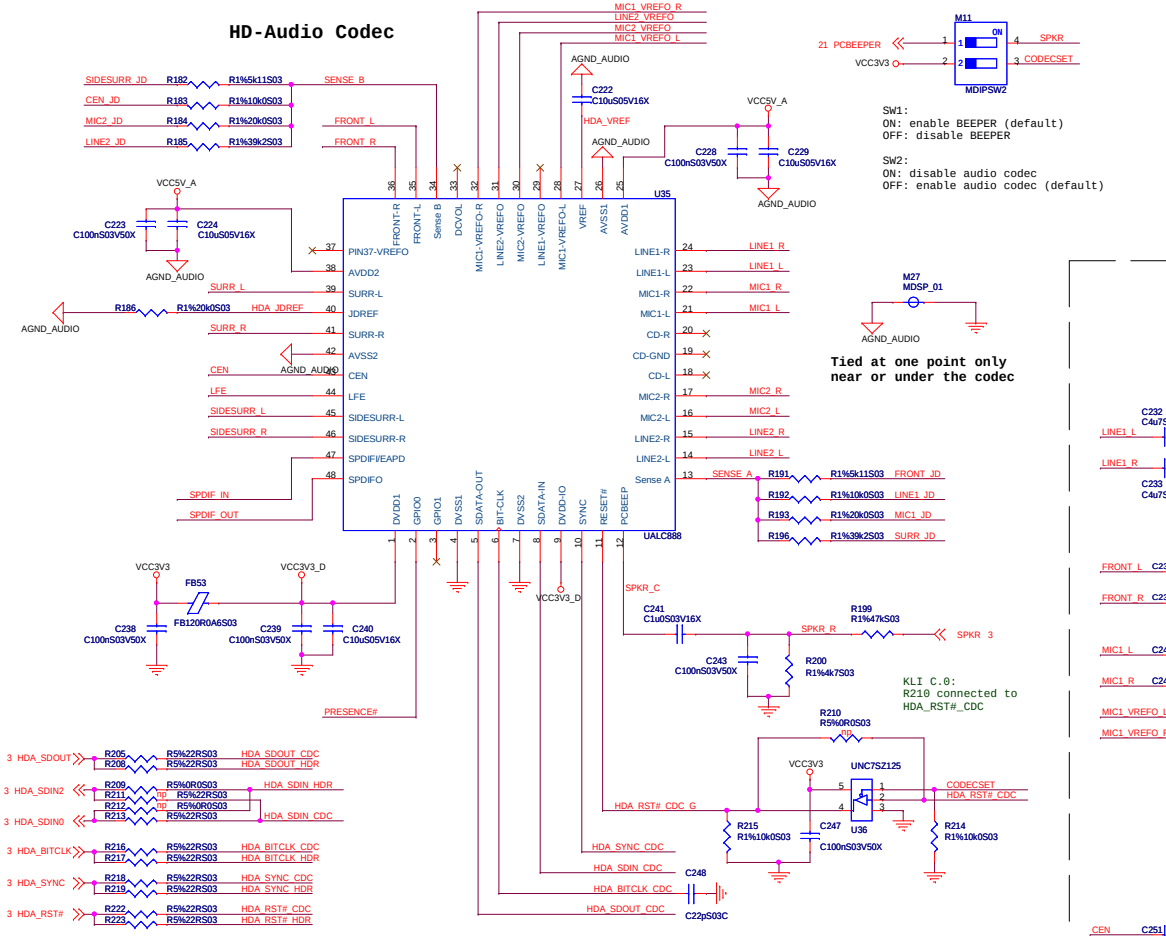
Title: VGA	
Size: B	Document Number: CET6SC0
Created: SRO	Rev: C.0
Date: Thursday, July 03, 2014	Sheet 16 of 25

HD-Audio Codec



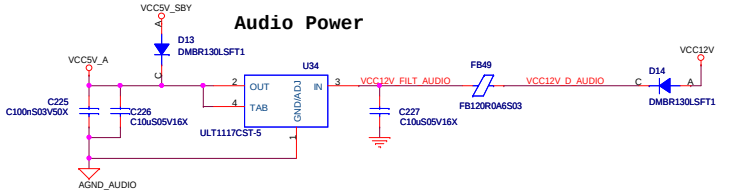
SW1:
ON: enable BEEPER (default)
OFF: disable BEEPER

SW2:
ON: disable audio codec
OFF: enable audio codec (default)

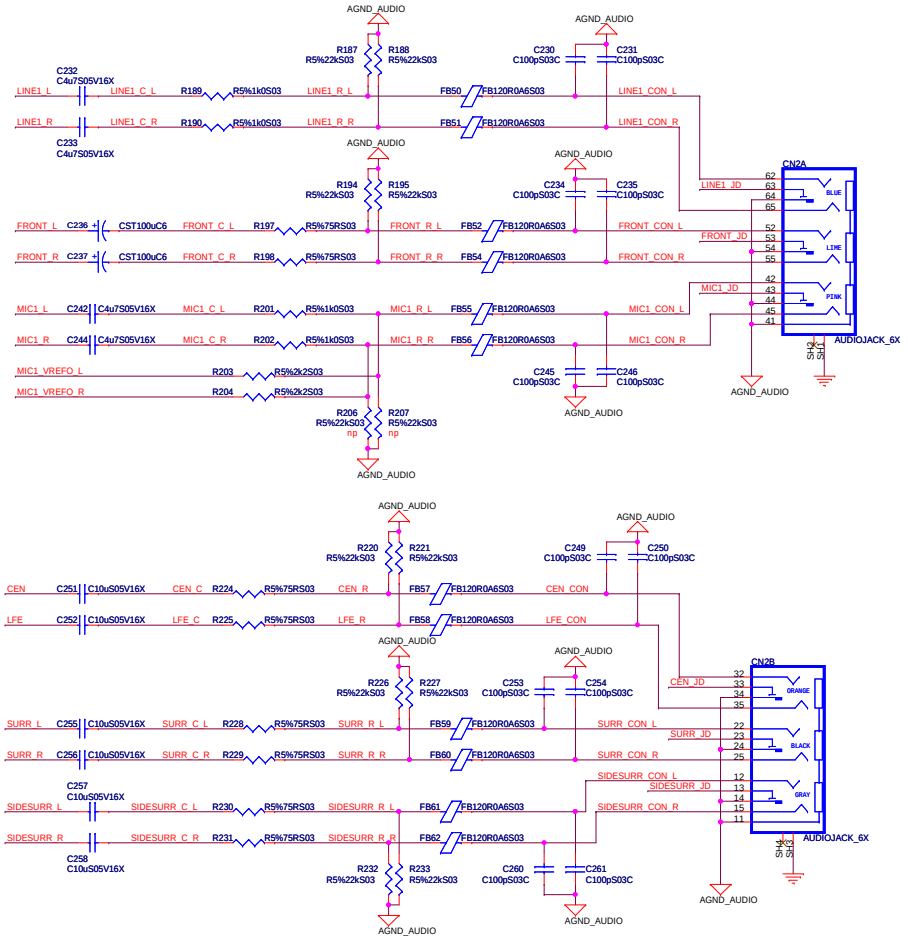
Tied at one point only
near or under the codec

KLI C.0:
R210 connected to
HDA_RST#_CDC

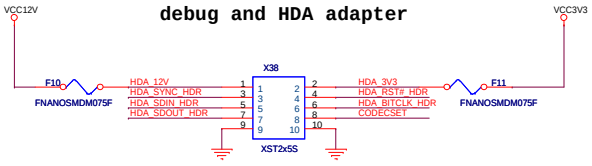
Audio Power



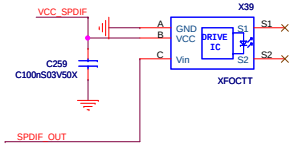
Rear Panel 7.1



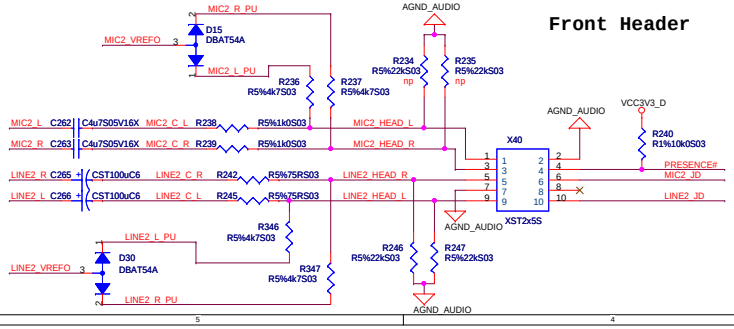
debug and HDA adapter

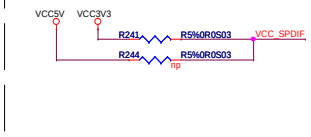


S/PDIF out

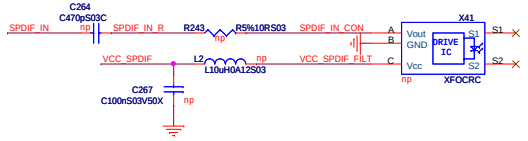


Front Header





in



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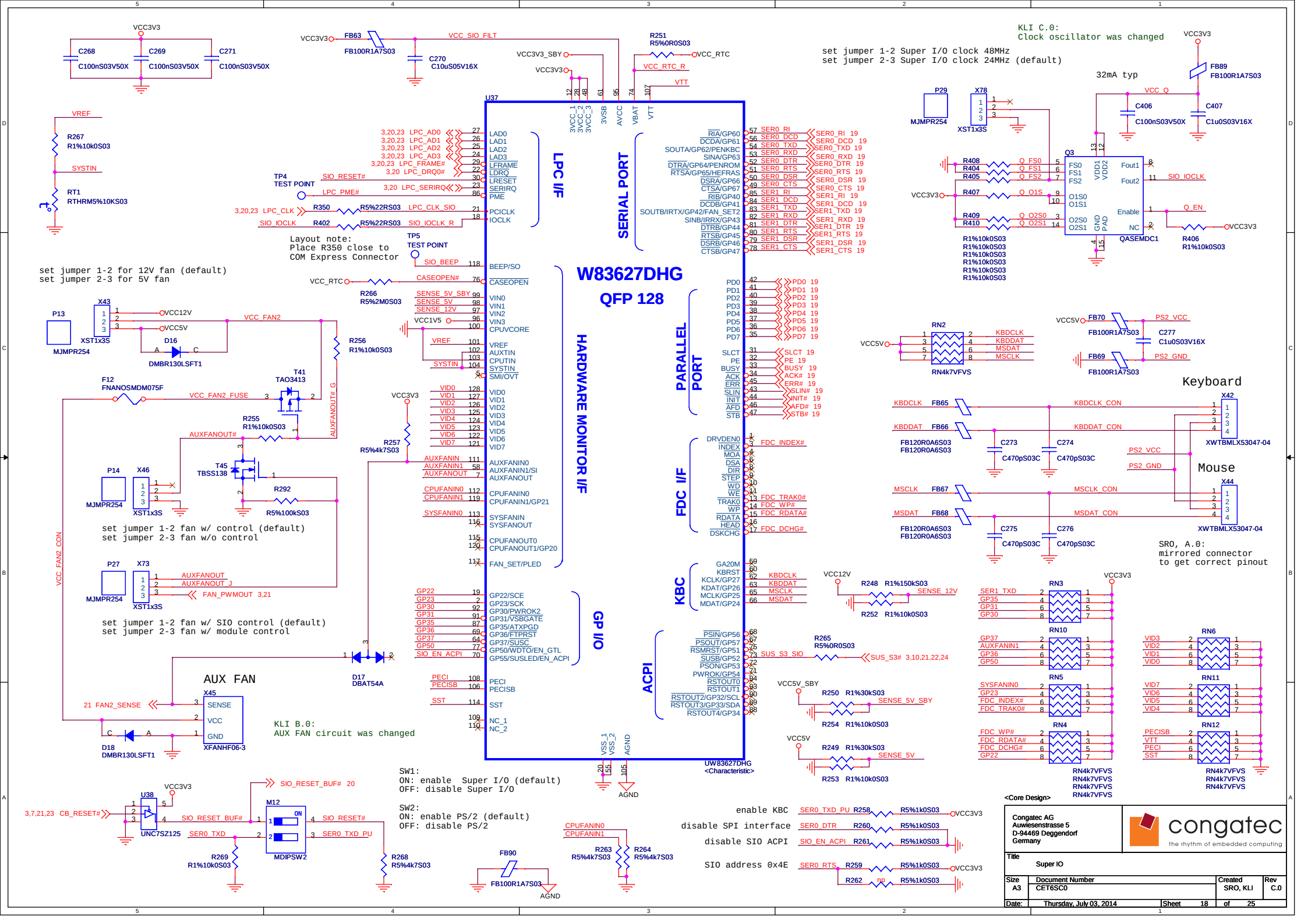
Title: HD Audio			
Size: C	Document Number: CET6SC0	Created: SRO, KLI	Rev: C.0
Date: Thursday, July 03, 2014	Sheet 17 of 25		


W83627DHG
QFP 128
U37
UW83627DHG
<Characteristic>
LPC I/F
SERIAL PORT
PARALLEL PORT
HARDWARE MONITOR I/F
FDC I/F
KBC
GP I/O
ACPI
KLI C.0:
Clock oscillator was changed
set jumper 1-2 Super I/O clock 48MHz
set jumper 2-3 Super I/O clock 24MHz (default)
32mA typ
Q3
QASEMDC1
XST1x3S
MJMPR254
set jumper 1-2 for 12V fan (default)
set jumper 2-3 for 5V fan
set jumper 1-2 fan w/ control (default)
set jumper 2-3 fan w/o control
set jumper 1-2 fan w/ SIO control (default)
set jumper 2-3 fan w/ module control
AUX FAN
XFANHF06-3
KLI B.0:
AUX FAN circuit was changed
Layout note:
Place R350 close to
COM Express Connector
SW1:
ON: enable Super I/O (default)
OFF: disable Super I/O
SW2:
ON: enable PS/2 (default)
OFF: disable PS/2
Keyboard
Mouse
SRO, A.0:
mirrored connector
to get correct pinout
enable KBC
disable SPI interface
disable SIO ACPI
SIO address 0x4E
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Super IO
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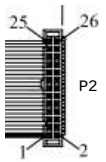
KLI B.0:
FB75, FB80 were changed for 100R/1.7A

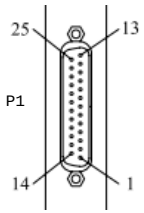
SRO, A.0:
swapped X62.5 <-> X62.7

SRO, A.0:
swapped X47.5 <-> X47.7

Attention: U39, U40 shows UADM211E UADM213E has high-active EN (pin 24) and low-active SHDN# (pin 25)



26P FC(F)



P1	1	14	2	15	3	16	4	17	5	18	6	19	
P2	1	2	3	4	5	6	7	8	9	10	11	12	

P1	7	20	8	21	9	22	10	23	11	24	12	25	13
P2	13	14	15	16	17	18	19	20	21	22	23	24	25

for use with I/O cables (e.g. AK 664 from reichelt)

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Title: RS-232, parallel port			
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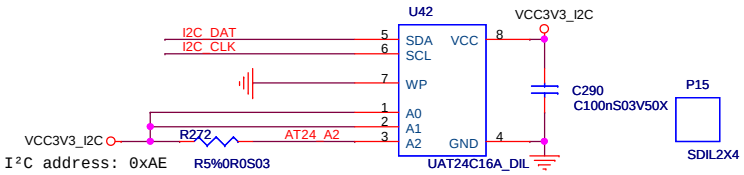
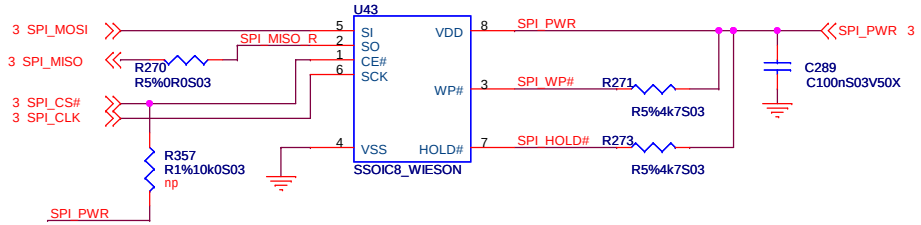
I²C EEPROM

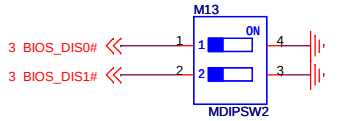


I²C address: 0xAE

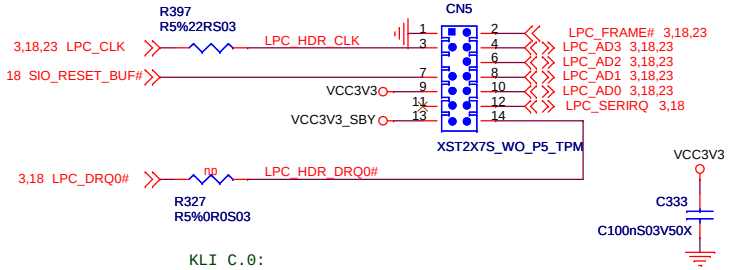
SPI BIOS Flash

KLI B.0:
SPI socket was changed
for a different type





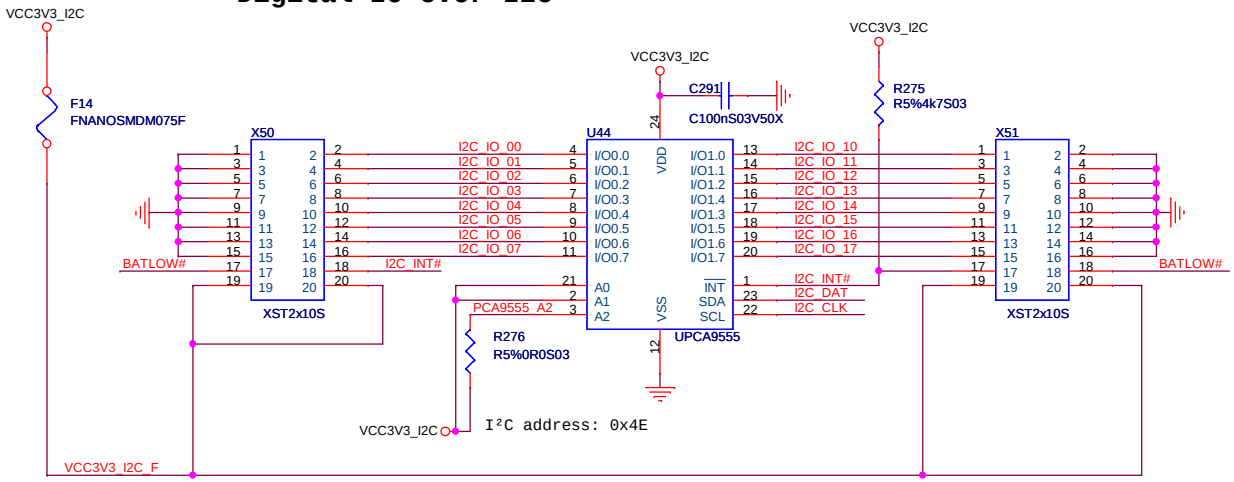
TPM header



KLI C.0:
LPC header was changed for TPM header

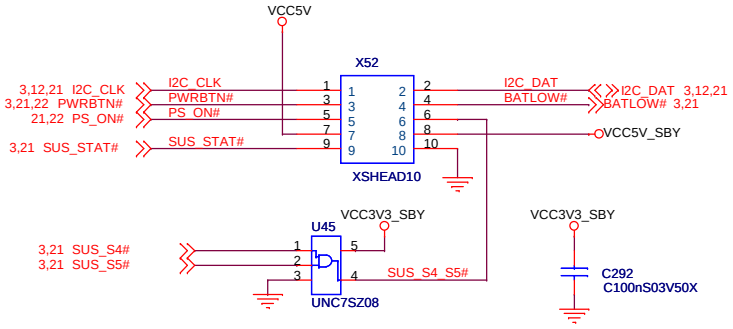
BIOS_DIS1#	BIOS_DIS0#	BIOS ENTRY / SPI_CS#
OFF	OFF	on-module firmware (default)
OFF	ON	carrier FWH (not supported)
ON	OFF	carrier firmware from SPI
ON	ON	on-module firmware, carrier SPI contains management data

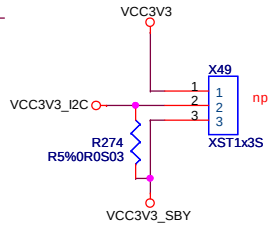
Digital IO over I2C



I²C address: 0x4E

Battery Support





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Title: SPI, I2C, Battery Support			
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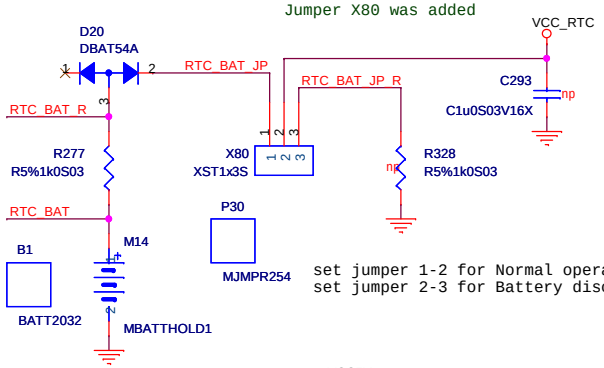
RTC / CMOS Battery

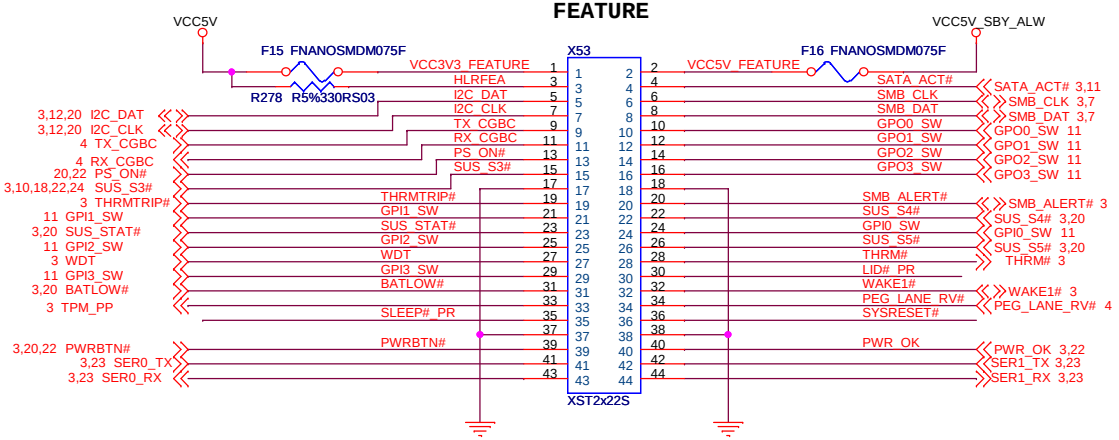
KLI C.0:
Jumper X80 was added



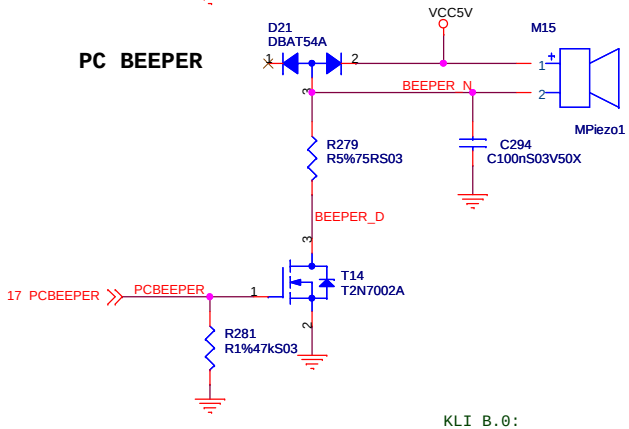
set jumper 1-2 for Normal operation (default)
set jumper 2-3 for Battery disconnected

SRO, A.0:
changed to 5V to be compatible to previous platforms

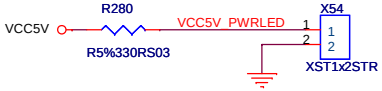
FEATURE



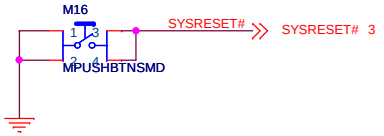
PC BEEPER



PWR LED



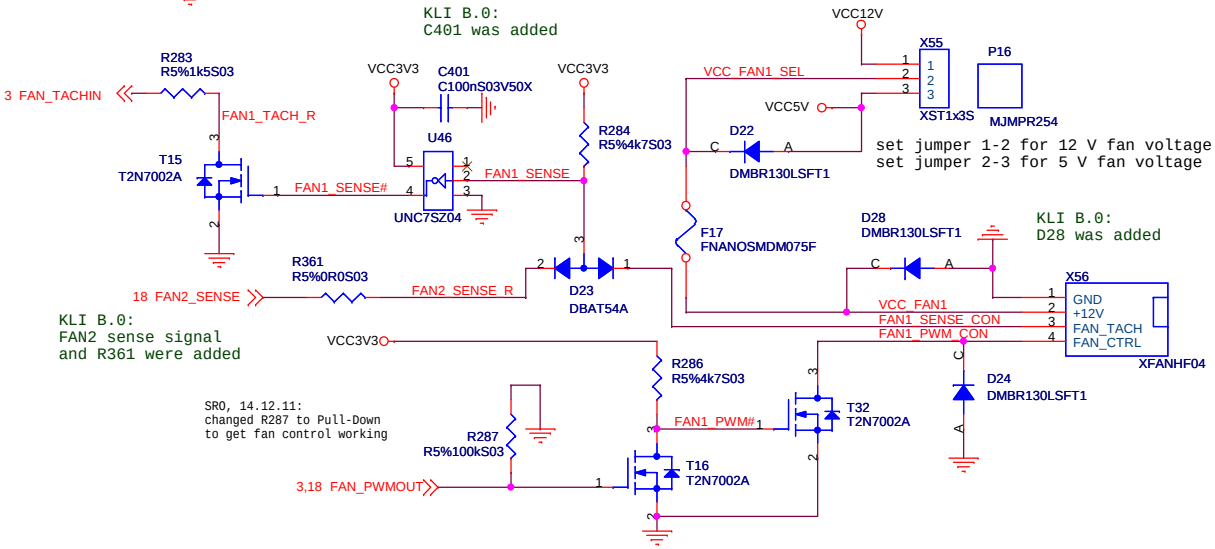
RESET



KLI B.0:
X77 was added

FAN Control

KLI B.0:
C401 was added



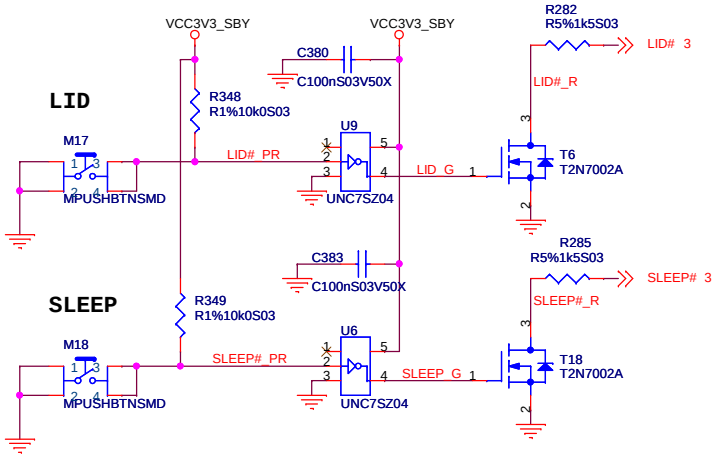
KLI B.0:
D28 was added

KLI B.0:
FAN2 sense signal
and R361 were added

SRO, 14.12.11:
changed R287 to Pull-Down
to get fan control working

set jumper 1-2 for 12 V fan voltage (default)
set jumper 2-3 for 5 V fan voltage

LID



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Title: CMOS Battery, Speaker, FAN, Feature Connector			
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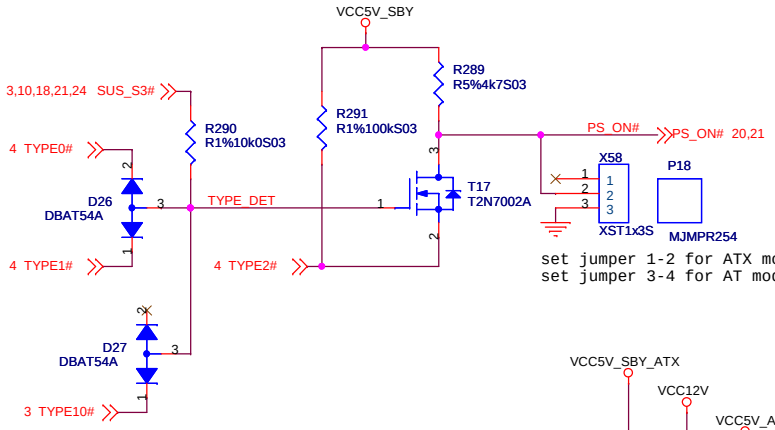
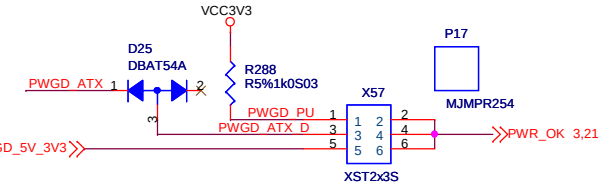
Type detection



set jumper 1-2 for ATX mode (default)
set jumper 3-4 for AT mode

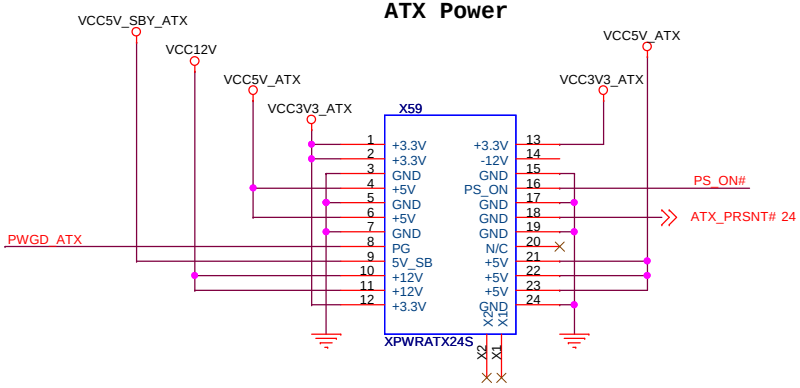
	Type10#	Type2#	Type1#	Type0#
Type 2 Rev 1.0:	12 V	N.C.	N.C.	N.C.
Type 2 Rev 2.0:	N.C.	N.C.	N.C.	N.C.
Type 6:	N.C.	GND	N.C.	N.C.



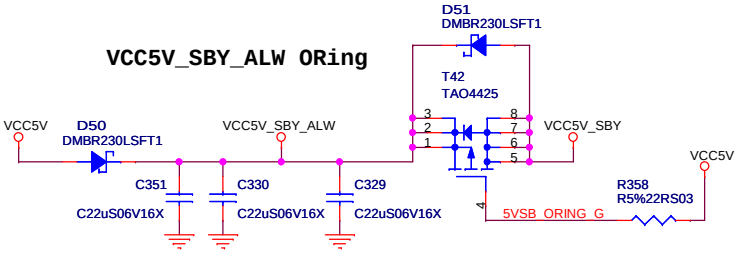
set jumper 1-2 for pull-up on PWR_OK; only for debug
set jumper 3-4 for PWR_OK from ATX supply (default)
set jumper 5-6 for PWR_OK from DC/DC (only in single 12 V mode)

KLI B.0:
C295, C296 were changed for C329, C330, C351

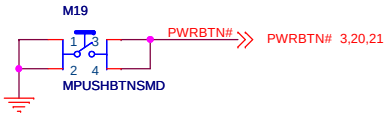
ATX Power



VCC5V_SBY_ALW ORing

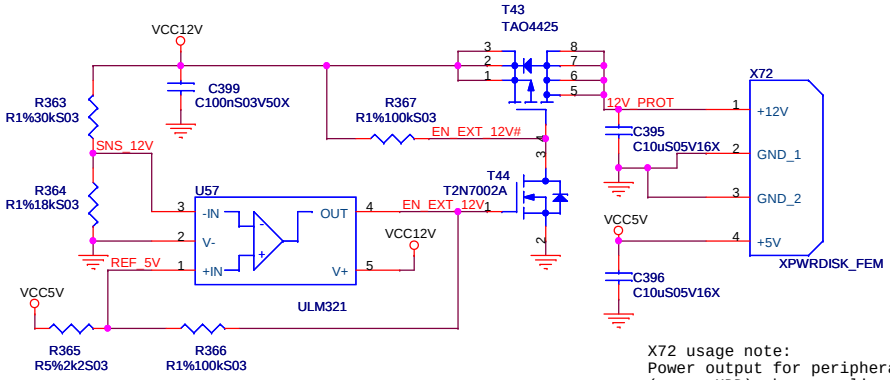


Power Button

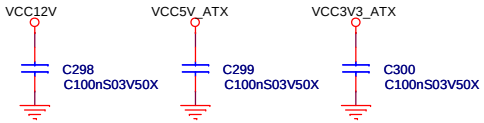


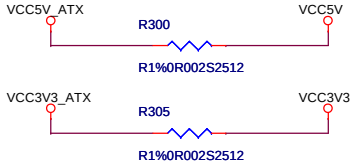
SRO, A.0: overvoltage protection:
disables +12V at X72 at about 13.6V

Disk Drive Power

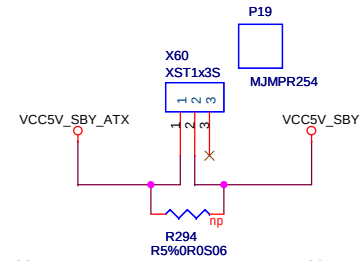


X72 usage note:
Power output for peripherals
(e. g. HDD) when suppling
the system with 12 V only

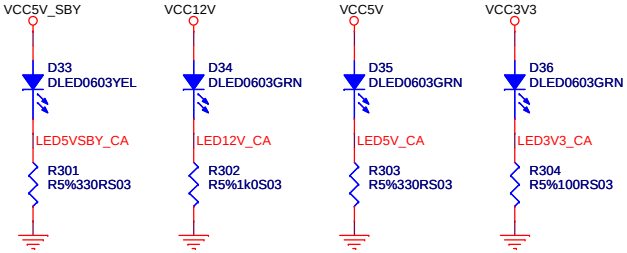




KLI B.0:
R300, R305 were change
(simplification of BOM)



load resistors
causing additional 200 mA
load current at 5V_ATX
helping ATX PSU to turn on



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Title: ATX Power, 5V Standby Always			
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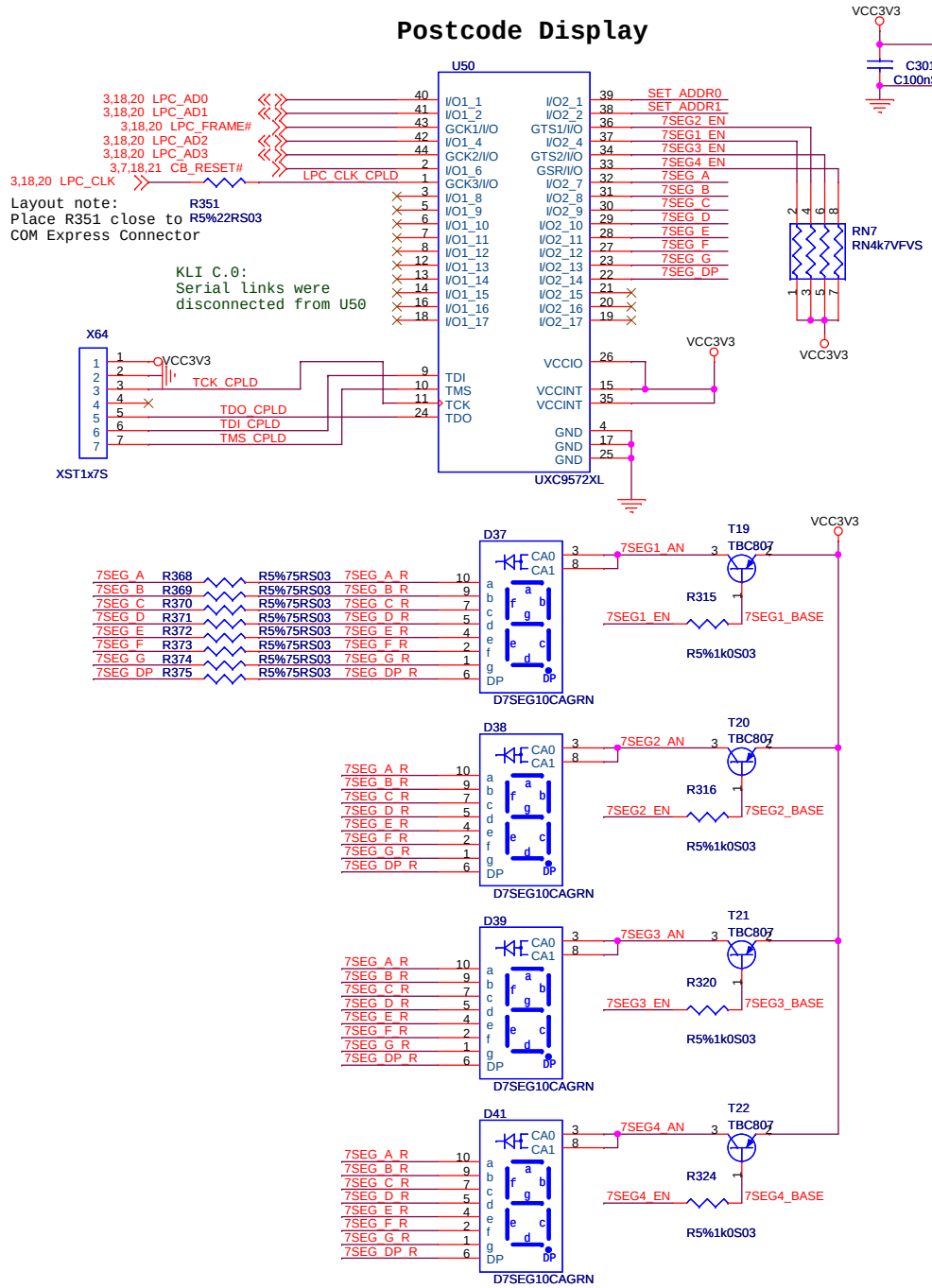
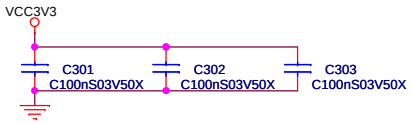
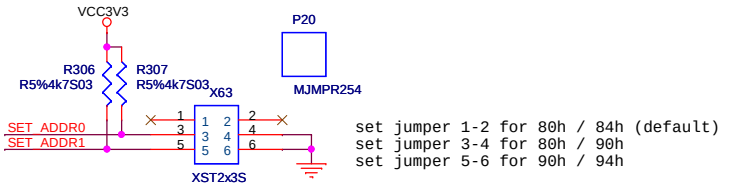
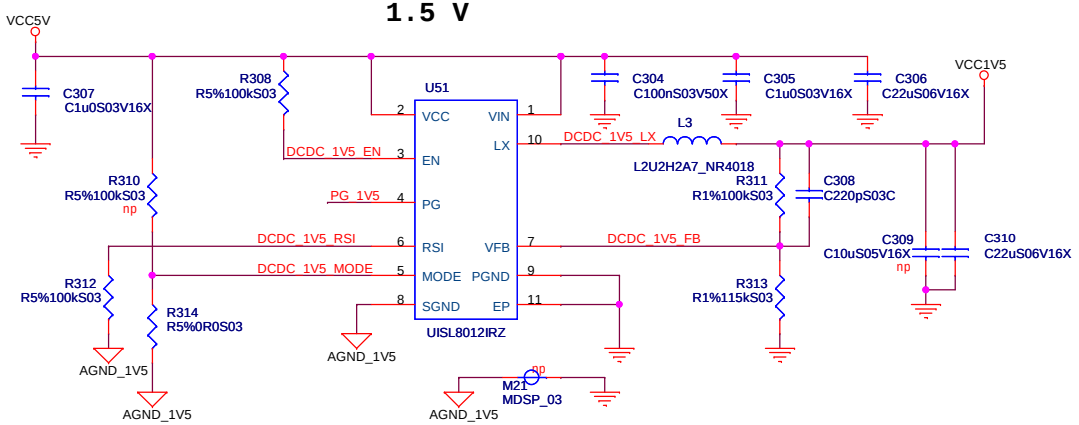
Postcode Display



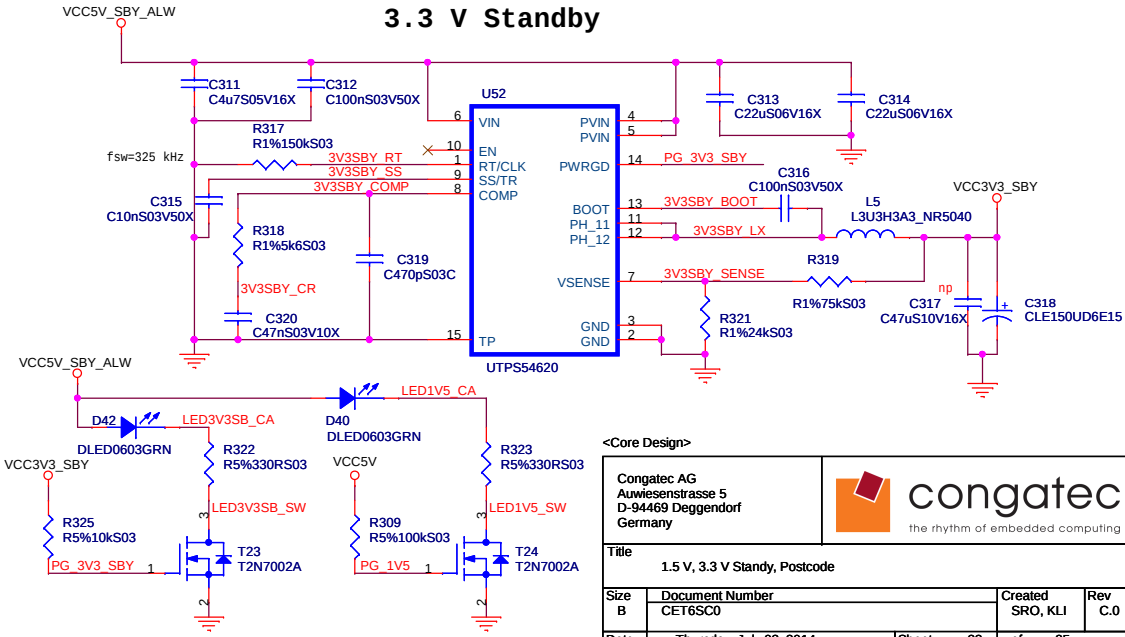




1.5 V



3.3 V Standby



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Title: 1.5 V, 3.3 V Standy, Postcode	
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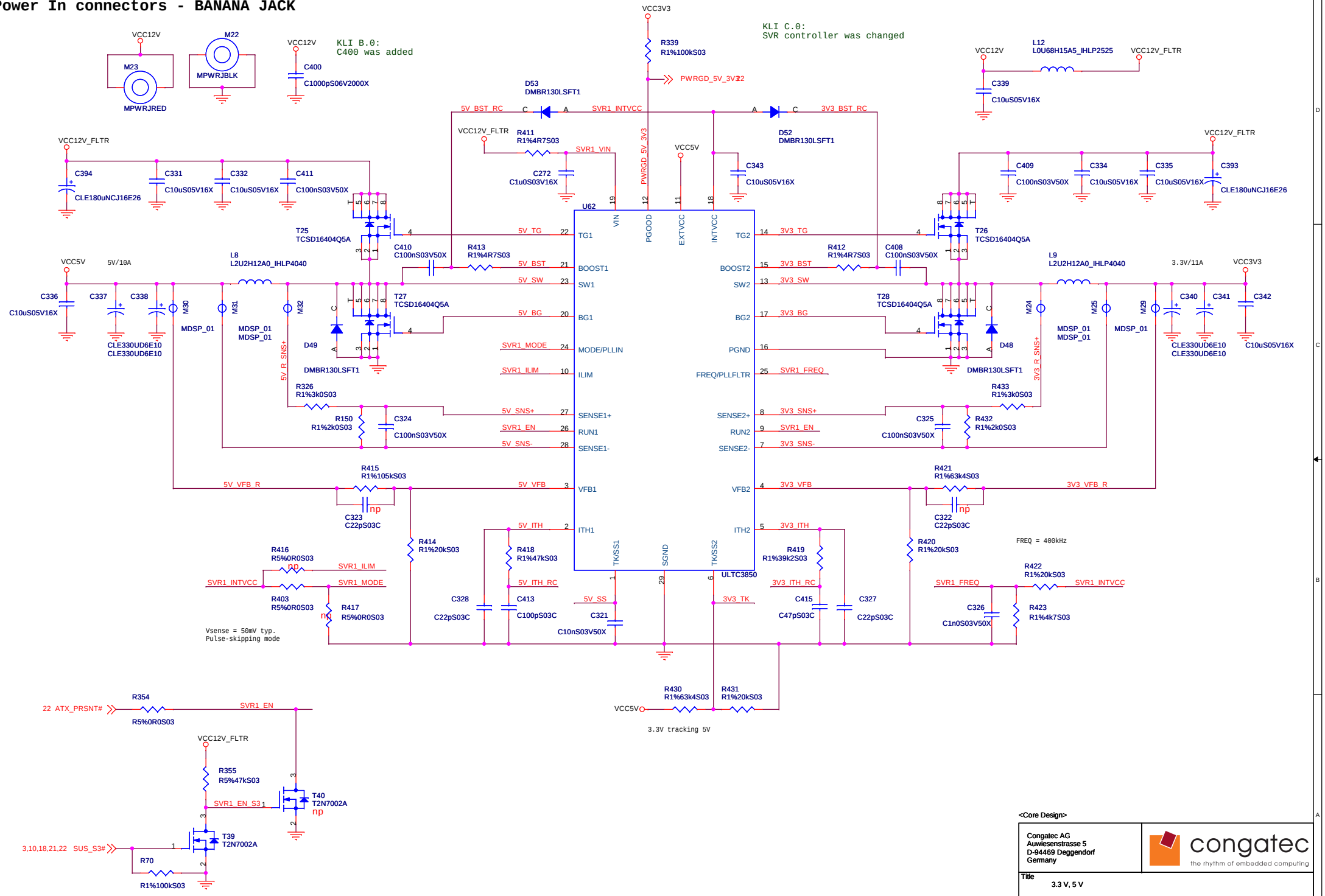
Power In connectors - BANANA JACK



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Title: 3.3 V, 5 V			
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HISTORY

10.01.2011 SRO design created

19.08.2011 SRO
page 3: set SUS_S3# buffer to be populated
page 4: swapped connection of DDI2_AUX, DDI3_AUX
page 6: changed SHLDGND - GND connection
page 7: exchanged UPI6C21200 by UICS9DB1233 (PCIe Gen. 3 compatible Clock Buffer)
page 9: connected X12.B17, B31, B81 to B48, to enable PCIe RefClk also with x1, x4 and x16 cards
page 11: exchanged SATA connectors
page 13, 14: swapped connection of TMDS_B_CLK and TMDS_C_CLK at U29, U30,
added circuitry to connect DDC-PU only in TMDS mode
page 18: changed oscillator at Super I/O from 48 MHz to 24 MHz
mirrored X42, X44 to be compatible to conga-adapPS2
page 19: connected U39.24, U39.25, U40.24, U40.25 to VCC5V to enable RS232 Levelshifter
swapped DTR and TXD signals at X47, X62 to maintain compatibility to conga-CEVAL
page 20: added PU at SPI_CS# to ensure stable level at SPI flash
page 21: changed connection of X53.1 and X53.3 from 3.3V to 5V
page 22: changed VCC5V_SBY_ALW Oring circuit
added overvoltage protection circuit to Disk Drive Power Connector

General: changed connection of I/O connector's shield from SHLDGND to GND
General: changed CLE150UC6E25 to CLE150UD6E15

7.8.2013 KLI
page 3: C389, C402, C403 were added. C385, C386 were changed from 0805 to 0603 (0805 too high to place under module).
page 4: R398, R399, X75, X76 were added (power consumption measurement). C404 was added. C387, C388 were changed from 0805 to 0603.
page 5: TPS2062 were changed for TPS2062C (previous chip has a bug).
page 6: C24, C27 were changed from 100u (tantalum) to 150u (polymer). U16 was changed to a new type for better signal quality
page 8, 9: C53, C59, C74, C76, C88, C100 were changed for 47u MLCC (recommended operating voltage for tantalum capacitors is 8V and they are sensitive for high ripple current, not recommended for 12V).
page 11: VCC for U27 and U28 was changed from VCC3V3 to VCC3V3_SBY. SATA connectors were changed from TH to SMT type (X68-X71) for better signal integrity.
page 12: AC coupling capacitors C370-C377 were changed from 0603 to 0402. C146, C151 were changed (new DC blocking capacitors for 12V). C153 was deleted.
page 13, 14: SN75DP122 was changed for SN75DP126 (new type, higher bandwidth).
page 15: New connection for X35.6, pin is connected to LVDS_BKLT_EN_JP
page 18: AUX FAN circuit was changed (new option for driving 3pin FAN by COMe module)
page 19: FB75, FB80 were changed for 100R/1.7A
page 20: SPI socket (U43) was changed for a different type. LPC header was added for different types of LPC devices.
page 21: FAN2_SENSE signal was connected to D2. C401 and D28 were added. X77 was added for connection to a probe.
page 22: C295, C296 (100u tantalum, 10u MLCC) were changed for C329, 330 and C351 (3x 22u MLCC)
page 23: RN8, RN9 were changed for R368-R375 (from 150R to 75R)
page 24: C400 was added (high voltage MLCC)

27.6.2014 KLI
page 6: C405 was added.
page 7: R79 was changed to installed, R113 was changed to NP (PLL bandwidth of PCIe clock buffer is set to Low, better signal integrity).
X79, R434-R437 were added for measuring PCIe CLK signal from COMe module.
page 17: Connection of R210 was changed, R210 is connected to U36 pin 2 (signal HDA_RST#_CDC).
page 18: Clock oscillator for Super I/O was changed. New oscillator can provide 24MHz or 48MHz (selectable by jumper).
page 20: LPC header was changed for TPM header, requested to have the connector for TPM module from Fujitsu.
page 21: Jumper X80 was added to have an option to disconnect RTC battery.
page 23: SER0_TX/RX and SER1_TX/RX were disconnected from U50 (not used by U50)
page 24: SVR was changed, previous controller has output discharge (unwanted when using ATX PSU). ISL62392 was replaced by LTC3850.

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Title: History			
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