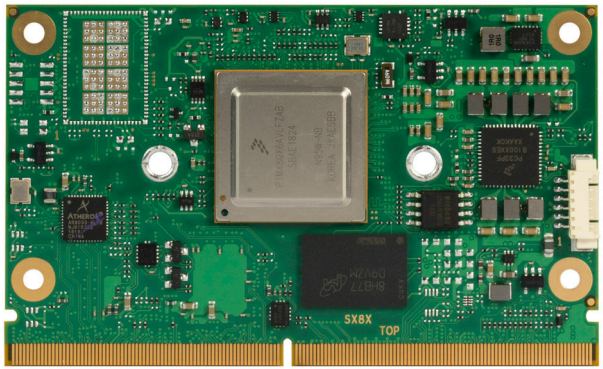


SMARC® conga-SMX8X

SMARC 2.0 module based on NXP® i.MX 8QuadXPlus, 8DualXPlus, and 8DualX

Short Description

Revision 1.1

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
1.0	2019-01-24	BEU	• Final release
1.1	2019-03-25	BEU	• Unified processor names in table 1 and 2 • Corrected CSI routing in section 3 “Block Diagram”

1 Introduction

1.1 SMARC® Concept

The Standardization Group for Embedded Technologies e.V (SGET) defined the SMARC standard for small form factor computer modules that target applications with ultra low power, low cost and high performance. The SMARC connector and interfaces are optimized for high-speed communication, and are suitable for ARM SoCs and low power x86 SoCs.

The SMARC standard bridges the gap between the COM Express standard and the Qseven standard by offering most of the interfaces defined in the COM Express specification at a lower power. With a footprint of 82 mm x 50 mm or 82 mm x 80 mm, the SMARC standard promotes the design of highly integrated, energy efficient systems.

Due to its small size and lower power demands, PC appliance designers can design low cost devices as well as explore a huge variety of product development options—from compact space-saving designs to fully functional systems. This solution allows scalability, product diversification and faster time to market.

1.2 conga-SMX8X Options Information

The conga-SMX8X is designed based on the SMARC 2.0 specification. The conga-SMX8X features the NXP i.MX 8X processor family. The conga-SMX8X offers Ultra Low Power boards with high computing performance and outstanding graphics. Additionally, the conga-SMX8X supports dual channel LPDDR4 memory with up to 4 GB capacity and data rates up to 2400 MTps, multiple I/O interfaces, up to two independent displays and various congatec embedded features.

By offering most of the functional requirement for any SMARC application, the conga-SMX8X provides manufacturers and developers with a platform to jump-start the development of systems and applications based on SMARC specification. Its features and capabilities make it an ideal platform for designing compact, energy-efficient, performance-oriented embedded systems.

1.2.1 Options Information

The conga-SMX8X is available in eight variants (four commercial and four industrial). The tables below show the different configurations available.

Table 1 conga-SMX8X (Commercial Variants)

Part-No	051100	051101	051102	051103
Processor	i.MX 8QuadXPlus	i.MX 8DualXPlus	i.MX 8DualX	i.MX 8QuadXPlus
Core Complex	4x Cortex®-A35 1x Cortex®-M4F	2x Cortex®-A35 1x Cortex®-M4F	2x Cortex®-A35 1x Cortex®-M4F	4x Cortex®-A35 1x Cortex®-M4F
Graphics	GC7000Lite Performance Optimized	GC7000Lite Performance Optimized	GC7000Lite Power Optimized	GC7000Lite Performance Optimized
Onboard Memory	4 GB LPDDR4	2 GB LPDDR4	2 GB LPDDR4	2 GB LPDDR4
Ethernet	2x 1 GbE with AVB	2x 1 GbE with AVB	1x 1 GbE with AVB 1x 10/100 Mbps	2x 1 GbE with AVB
USB	5x USB 2.0 (1x OTG) 2x USB 3.0	5x USB 2.0 (1x OTG) 2x USB 3.0	5x USB 2.0 (1x OTG)	5x USB 2.0 (1x OTG) 2x USB 3.0
eMMC	16 GB	16 GB	16 GB	16 GB

Table 2 conga-SMX8X (Industrial Variants)

Part-No	051110	051111	051112	051113
Processor	i.MX 8QuadXPlus	i.MX 8DualXPlus	i.MX 8DualX	i.MX 8QuadXPlus
Core Complex	4x Cortex®-A35 1x Cortex®-M4F	2x Cortex®-A35 1x Cortex®-M4F	2x Cortex®-A35 1x Cortex®-M4F	4x Cortex®-A35 1x Cortex®-M4F
Graphics	GC7000Lite Performance Optimized	GC7000Lite Performance Optimized	GC7000Lite Power Optimized	GC7000Lite Performance Optimized
Onboard Memory	4 GB LPDDR4	2 GB LPDDR4	2 GB LPDDR4	2 GB LPDDR4
Ethernet	2x 1 GbE	2x 1 GbE	1x 1 GbE 1x 10/100 Mbps	2x 1 GbE
USB	5x USB 2.0 (1x OTG) 2x USB 3.0	5x USB 2.0 (1x OTG) 2x USB 3.0	5x USB 2.0 (1x OTG)	5x USB 2.0 (1x OTG) 2x USB 3.0
eMMC	16 GB	16 GB	16 GB	16 GB

1.2.2 Cooling Solutions

Table 3 conga-SMX8X Cooling Solutions

Part-No	051052	051053	050060
Product	SMX8/CSP-B	SMX8/HSP-B	conga-SMARC/CSA Adapter
Description	Passive cooling solution for commercial (open-die) conga-SMX8X variants. All standoffs are with M2.5 mm thread.	Heatspreader solution for commercial (open-die) conga-SMX8X variants. All standoffs are with 2.7 mm bore hole.	SMARC CSA Adapter suitable for all SMARC 2.0 heatspreaders. PWM controlled fan.

Part-No	051050	051051
Product	SMX8/i-CSP-B	SMX8/i-HSP-B
Description	Passive cooling solution for industrial (lidded) conga-SMX8X variants. All standoffs are with M2.5 mm thread.	Heatspreader solution for industrial (lidded) conga-SMX8X variants. All standoffs are with 2.7 mm bore hole.

1.2.3 Accessories

Table 4 conga-SMX8X Adapters

Part-No	48000023
Product	RS-232 adapter cable for conga-ARM modules
Description	Adapter cable for ARM console. MOLEX 6Pin PicoBlade to 2x D-SUB 9.

2 Specifications

2.1 Feature List

Table 5 Feature Summary

Form Factor	Based on SMARC 2.0 Specification (82 mm x 50 mm)	
SoC	NXP i.MX 8X ARM® Cortex®-A35/M4F processor	
Onboard Memory	Up to 4 GB, 2400 MTps LPDDR4	
Onboard Storage	eMMC 5.1 up to 64 GByte	
Audio	2x I²S	
Ethernet	Up to 2x 1 GbE with IEEE 1588 and Audio Video Bridging (AVB) support	
Graphics	Integrated in NXP i.MX 8X Series single GT7000Lite multimedia GPU VPU up to 4K h.265 dec / 1080p h.264 enc/dec, 3D Graphics with up to 4 high performance vec4 shaders and 16 execution, OpenGL ES 3.1, Vulcan VX extensions, OpenCL 1.2 EP, OpenVG 1.1i	
	The conga-SMX8X supports up to two independent displays: 2x Single channel LVDS 24 bit (default) or 1x Dual channel LVDS 24 bit (optional) or 1x Single channel LVDS 24 bit and 1x HDMI® 1.3 (optional)	**NOTE:** HDMI is not available for industrial variants.
I/O Interfaces	1x PCIe 3.0 5x USB 2.0 (1x OTG) Up to 2x USB 3.0 1x SDIO 3.0 4x UARTs (2x RX/TX with handshake; 2x RX/TX without handshake) 2x UARTs via onboard connector 1x MIPI CSI-2 x4	2x FlexCAN WiFi and Bluetooth (optional) I²C Bus SPI QSPI GPIOs
Features	Watchdog timer JTAG debug interface	
Bootloader	U-Boot	
Virtualization	Multiple domains with hardware virtualization Multiple Operating Systems	System MMU Resource partitioning and split GPU
Security	High Assurance Boot Encryption Engine (AES-128, AES-256, 3DES, ARC4, SHA-1, SHA-2, SHA-256, MD-5, RSA-1024, RSA-2048, RSA-3072, RSA-4096)	

Note

Some of the listed features are not available on all conga-SMX8X variants. Check the article number of your module and compare it to the options information table on page 4 to determine the available features on your module variant.

2.2 Supported Operating Systems

The conga-SMX8X supports the following operating systems:

- Linux®
- Yocto Project®
- Android™

2.3 Environmental Specifications

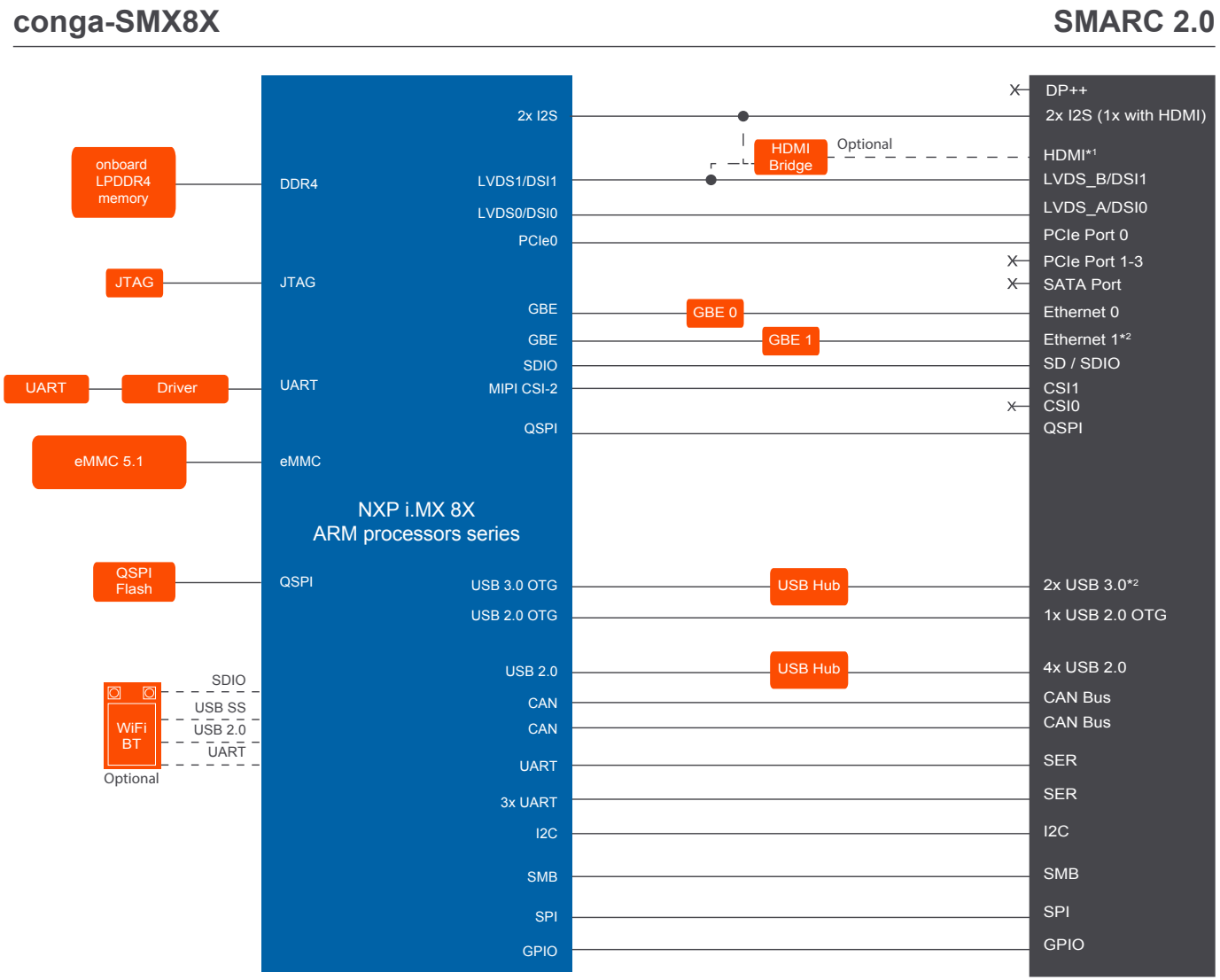
Temperature	Operation: 0° to 60°C	Storage: -20° to 80°C (Commercial)
Tempererature	Operation: -40° to 85°C	Storage: -40° to 85°C (Industrial)
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



*1 HDMI is not available for industrial variants.
*2 i.MX 8DualX variants only support 10/100 Mbps on Ethernet 1 and do not support USB 3.0 signals.

4 Connector Rows

Table 6 SMARC Edge Finger Pinout

P-PIN	Primary (Top) Side	Description	S-Pin	Secondary (Bottom) Side	Description
			S1	I2C_CAM1_CK	I2C clock (serial camera support link for serial cameras)
P1	N.C		S2	I2C_CAM1_DAT	I2C data (serial camera support link for serial cameras)
P2	GND	Ground	S3	GND	Ground
P3	CSI1_CK+	CSI1 differential clock pair	S4	N.C	
P4	CSI1_CK-		S5	CSI0_TX- / I2C_CAM0_CK	I2C clock
P5	GBE1_SDP	IEEE 1588 PPS signal	S6	CAM_MCK	Master clock output for CSI camera support. May be used for CSI0 or CSI1 or both
P6	GBE0_SDP		S7	CSI0_TX+ / I2C_CAM0_DAT	I2C data
P7	CSI1_RX0+	CSI1 differential data pair 0	S8	N.C	CSI0 differential clock pair
P8	CSI1_RX0-		S9	N.C	
P9	GND	Ground	S10	GND	Ground
P10	CSI1_RX1+	CSI1 differential data pair 1	S11	N.C	CSI0 differential data pair 0
P11	CSI1_RX1-		S12	N.C	
P12	GND	Ground	S13	GND	Ground
P13	CSI1_RX2+	CSI1 differential data pair 2	S14	N.C	CSI0 differential data pair 1
P14	CSI1_RX2-		S15	N.C	
P15	GND	Ground	S16	GND	Ground
P16	CSI1_RX3+	CSI1 differential data pair 3	S17	GBE1_MDI0+	Bidirectional transmit/receive pair 0 **NOTE:** Only 10/100 Mbps on DualX variants.
P17	CSI1_RX3-		S18	GBE1_MDI0-	
P18	GND	Ground	S19	GBE1_LINK100#	Link speed indication LED for 100 Mbps
P19	GBE0_MDI3-	Bidirectional transmit/receive pair 3	S20	GBE1_MDI1+	Bidirectional transmit/receive pair 1 **NOTE:** Only 10/100 Mbps on DualX variants.
P20	GBE0_MDI3+		S21	GBE1_MDI1-	
P21	GBE0_LINK100#	Link speed indication LED for 100 Mbps	S22	GBE1_LINK1000#	Link speed indication LED for 1000 Mbps
P22	GBE0_LINK1000#	Link speed indication LED for 1000 Mbps	S23	GBE1_MDI2+	Bidirectional transmit/receive pair 2 **NOTE:** Only 10/100 Mbps on DualX variants.
P23	GBE0_MDI2-	Bidirectional transmit/receive pair 2	S24	GBE1_MDI2-	
P24	GBE0_MDI2+		S25	GND	Ground
P25	GBE0_LINK_ACT#	Link and activity indication LED	S26	GBE1_MDI3+	Bidirectional transmit/receive pair 3 **NOTE:** Only 10/100 Mbps on DualX variants.
P26	GBE0_MDI1-	Bidirectional transmit/receive pair 1	S27	GBE1_MDI3-	
P27	GBE0_MDI1+		S28	GBE1_CTREF	Center-tap reference voltage output

P-PIN	Primary (Top) Side	Description	S-Pin	Secondary (Bottom) Side	Description
P28	GBE0_CTREF	Center-tap reference voltage output	S29	N.C	
P29	GBE0_MDI0-	Bidirectional transmit/receive pair 0	S30	N.C	
P30	GBE0_MDI0+		S31	GBE1_LINK_ACT#	Link or activity indication LED
P31	SPI0_CS1#	SPI0 master chip select 1	S32	N.C	
P32	GND	Ground	S33	N.C	
P33	SDIO_WP	SDIO write protect input to module	S34	GND	Ground
P34	SDIO_CMD	SDIO command/response	S35	USB4+	
P35	SDIO_CD#	SDIO card detect input to module	S36	USB4-	
P36	SDIO_CK	SDIO Clock	S37	N.C	
P37	SDIO_PWR_EN	SDIO power enable output	S38	AUDIO_MCK	Master clock output from module
P38	GND	Ground	S39	I2S0_LRCK	Left and right audio synchronization clock
P39	SDIO_D0	SDIO data lines	S40	I2S0_SDOUT	Digital audio output
P40	SDIO_D1		S41	I2S0_SDIN	Digital audio input
P41	SDIO_D2		S42	I2S0_CK	Digital audio clock
P42	SDIO_D3		S43	ESPI_ALERT0#	Connected to GPIO
P43	SPI0_CS0#	SPI0 master chip select 0	S44	ESPI_ALERT1#	
P44	SPI0_CK	SPI0 master clock output	S45	N.C	
P45	SPI0_DIN	SPI0 master data input	S46	N.C	
P46	SPI0_DO	SPI0 master data output	S47	GND	Ground
P47	GND	Ground	S48	I2C_GP_CK	I2C general purpose clock signal
P48	N.C		S49	I2C_GP_DAT	I2C general purpose data signal
P49	N.C		S50	I2S2_LRCK	I2S2 left and right synchronization clock
P50	GND	Ground	S51	I2S2_SDOUT	I2S2 digital audio output
P51	N.C		S52	I2S2_SDIN	I2S2 digital audio input
P52	N.C		S53	I2S2_CK	I2S2 digital audio clock
P53	GND	Ground	S54	N.C	
P54	ESPI_CS0#	Quad-IO SPI master chip select output	S55	USB5_EN_OC#	USB5 over-current enable signal
P55	ESPI_CS1#		S56	ESPI_IO_2	Quad-IO SPI master data input/output
P56	ESPI_CK	Quad-IO SPI master clock output	S57	ESPI_IO_3	
P57	ESPI_IO_0	Quad-IO SPI master data input/output	S58	ESPI_RESET#	Quad-IO SPI reset signal output from module
P58	ESPI_IO_1		S59	N.C	
P59	GND	Ground	S60	N.C	

P-PIN	Primary (Top) Side	Description	S-Pin	Secondary (Bottom) Side	Description
P60	USB0+	USB differential data pairs 0	S61	GND	Ground
P61	USB0-		S62	USB3_SSTX+	SuperSpeed USB differential transmit data pair **NOTE:** Not available on DualX variants.
P62	USB0_EN_OC#	USB0 over-current enable signal	S63	USB3_SSTX-	
P63	USB0_VBUS_DET	USB host power detection	S64	GND	Ground
P64	USB0_OTG_ID	USB OTG ID input	S65	USB3_SSRX+	SuperSpeed USB differential receive data pair **NOTE:** Not available on DualX variants.
P65	USB1+	USB differential data pairs 1	S66	USB3_SSRX-	
P66	USB1-		S67	GND	Ground
P67	USB1_EN_OC#	USB1 over-current enable signal	S68	USB3+	USB differential data pairs 3 **NOTE:** Not available on DualX variants.
P68	GND	Ground	S69	USB3-	
P69	USB2+	USB differential data pairs 2	S70	GND	Ground
P70	USB2-		S71	USB2_SSTX+	SuperSpeed USB differential transmit data pair **NOTE:** Not available on DualX variants.
P71	USB2_EN_OC#	USB2 over-current enable signal	S72	USB2_SSTX-	
P72	N.C		S73	GND	Ground
P73	N.C		S74	USB2_SSRX+	SuperSpeed USB differential receive data pair **NOTE:** Not available on DualX variants.
P74	N.C		S75	USB2_SSRX-	
	Key			Key	
P75	PCIE_A_RST#	PCIe port reset output	S76	N.C	
P76	USB4_EN_OC#		S77	N.C	
P77	N.C		S78	N.C	
P78	N.C		S79	N.C	
P79	GND	Ground	S80	GND	Ground
P80	N.C		S81	N.C	
P81	N.C		S82	N.C	
P82	GND	Ground	S83	GND	Ground
P83	PCIE_A_REFCK+	Differential link reference clock output	S84	N.C	
P84	PCIE_A_REFCK-		S85	N.C	
P85	GND	Ground	S86	GND	Ground
P86	PCIE_A_RX+	PCIe link A differential receive data pair	S87	N.C	
P87	PCIE_A_RX-		S88	N.C	
P88	GND	Ground	S89	GND	Ground

P-PIN	Primary (Top) Side	Description	S-Pin	Secondary (Bottom) Side	Description
P89	PCIE_A_TX+	PCIe link A differential transmit data pair	S90	N.C	
P90	PCIE_A_TX-		S91	N.C	
P91	GND	Ground	S92	GND	Ground
P92	N.C	Optional HDMI differential data pair 2	S93	N.C	
P93	N.C		S94	N.C	
P94	GND	Ground	S95	N.C	
P95	N.C	Optional HDMI differential data pair 1	S96	N.C	
P96	N.C		S97	N.C	
P97	GND	Ground	S98	N.C	
P98	N.C	Optional HDMI differential data pair 0	S99	N.C	
P99	N.C		S100	N.C	
P100	GND	Ground	S101	GND	Ground
P101	N.C	Optional HDMI differential clock pair	S102	N.C	
P102	N.C		S103	N.C	
P103	GND	Ground	S104	N.C	
P104	N.C	Optional HDMI hot plug detect	S105	N.C	
P105	N.C	Optional HDMI I2C clock line	S106	N.C	
P106	N.C	Optional HDMI I2C data line	S107	LCD1_BKLT_EN	Panel 1 backlight enable control
P107	N.C	Optional HDMI_CEC	S108	LVDS1_CLK+ / DSI1_CLK+	Secondary LVDS data channel differential clock pair / optionally DSI-CLK
P108	GPIO0 / JTAG_TDO	GPIO0 or JTAG_TDO. See pin S157.	S109	LVDS1_CLK- / DSI1_CLK-	
P109	CAM1_PWR# / JTAG_TDI	Camera 1 power enable or JTAG_TDI. See pin S157.	S110	GND	Ground
P110	GPIO2 / JTAG_TCK	GPIO2 or JTAG_TCK. See pin S157.	S111	LVDS1_0+ / DSI1_D0+	LVDS1 or DSI1 secondary data channel, differential pair 0
P111	CAM1_RST# / JTAG_TMS	Camera 1 reset or JTAG_TMS. See pin S157.	S112	LVDS1_0- / DSI1_D0-	
P112	I2S2_RST#	I2S2_RST# instead of HDA_RST#	S113	N.C	
P113	GPIO5 / PWM_OUT	GPIO5 or PWM_OUT	S114	LVDS1_1+ / DSI1_D1+	LVDS1 or DSI1 secondary data channel, differential pair 1
P114	GPIO6 / TACHIN	GPIO6 or TACHIN	S115	LVDS1_1- / DSI1_D1-	
P115	GPIO7		S116	LCD1_VDD_EN	Panel 1 power enable
P116	GPIO8		S117	LVDS1_2+ / DSI1_D2+	LVDS1 or DSI1 secondary data channel, differential pair 2
P117	GPIO9		S118	LVDS1_2- / DSI1_D2-	
P118	GPIO10		S119	GND	Ground
P119	GPIO11		S120	LVDS1_3+ / DSI1_D3+	LVDS1 or DSI1 secondary data channel, differential pair 3
P120	GND	Ground	S121	LVDS1_3- / DSI1_D3-	

P-PIN	Primary (Top) Side	Description	S-Pin	Secondary (Bottom) Side	Description
P121	I2C_PM_CK	Power management I2C clock	S122	LCD1_BKLT_PWM	Panel 1 backlight PWM control
P122	I2C_PM_DAT	Power management I2C data	S123	N.C	
P123	BOOT_SEL0#	Input straps to determine the module's boot device. **NOTE:** Module will start to boot from on-module SPI flash by default.	S124	GND	Ground
P124	BOOT_SEL1#		S125	LVDS0_0+ / DSI0_D0+	LVDS0 primary data channel, differential pair 0
P125	BOOT_SEL2#		S126	LVDS0_0- / DSI0_D0-	
P126	RESET_OUT#	Reset output to carrier board	S127	LCD0_BKLT_EN	Panel 0 backlight enable control
P127	RESET_IN#	Reset input from carrier board	S128	LVDS0_1+ / DSI0_D1+	LVDS0 primary data channel, differential pair 1
P128	POWER_BTN#	Power-button input from carrier board	S129	LVDS0_1- / DSI0_D1-	
P129	SER0_TX	Serial port 0 data output	S130	GND	Ground
P130	SER0_RX	Serial port 0 data input	S131	LVDS0_2+ / DSI0_D2+	LVDS0 primary data channel, differential pair 2
P131	SER0_RTS#	Serial port 0 Request to Send handshake	S132	LVDS0_2- / DSI0_D2-	
P132	SER0_CTS#	Serial port 0 Clear to Send handshake	S133	LCD0_VDD_EN	Panel 0 power enable
P133	GND	Ground	S134	LVDS0_CLK+ / DSI0_CLK+	LVDS0 primary data channel, differential clock pair
P134	SER1_TX	Serial port 1 data output	S135	LVDS0_CLK- / DSI0_CLK-	
P135	SER1_RX	Serial port 1 data input	S136	GND	Ground
P136	SER2_TX	Serial port 2 data output	S137	LVDS0_3+ / DSI0_D3+	LVDS or DSI0 primary data channel, differential pair 3
P137	SER2_RX	Serial port 2 data input	S138	LVDS0_3- / DSI0_D3-	
P138	SER2_RTS#	Serial port 2 Request to Send handshake	S139	I2C_LCD_CK	LCD I2C clock
P139	SER2_CTS#	Serial port 2 Clear to Send handshake	S140	I2C_LCD_DAT	LCD I2C data
P140	SER3_TX	Serial port 1 data input	S141	LCD0_BKLT_PWM	Panel 0 backlight PWM control
P141	SER3_RX	Serial port 3 data input	S142	N.C	
P142	GND	Ground	S143	GND	Ground
P143	CAN0_TX		S144	N.C	
P144	CAN0_RX		S145	WDT_TIME_OUT#	Watchdog timer output from module
P145	CAN1_TX		S146	PCIE_WAKE#	PCIe wake input to module
P146	CAN1_RX		S147	VDD_RTC	Low current RTC circuit backup power

P-PIN	Primary (Top) Side	Description	S-Pin	Secondary (Bottom) Side	Description
P147	VDD_IN	Module power input voltage (5V only)	S148	LID#	Lid open/close indication to module
P148	VDD_IN		S149	SLEEP#	Sleep indicator from carrier board
P149	VDD_IN		S150	VIN_PWR_BAD#	Power bad input to module
P150	VDD_IN		S151	CHARGING#	Battery charging input to the module
P151	VDD_IN		S152	CHARGER_PRSNT#	Battery charger present input to the module
P152	VDD_IN		S153	CARRIER_STBY#	Carrier standby power output from module
P153	VDD_IN		S154	CARRIER_PWR_ON	Carrier power on output from module
P154	VDD_IN		S155	BOOT_ALT#	Set low for serial-download mode
P155	VDD_IN		S156	BATLOW#	Battery low input to the module
P156	VDD_IN		S157	TEST#	Set low to enable JTAG on shared pins
			S158	GND	Ground

5 Software

In order to build the root filesystem image, kernel and bootloader for conga-SMX8X, the complete kernel source, bootloader source and individual patches can be obtained from the congatec source code repository:
https://git.congatec.com/imx8x_early_access

The software documentation can be found here:
https://git.congatec.com/imx8x_early_access/meta-fsl-bsp-release

Note

Contact congatec technical support to get access to the repositories.