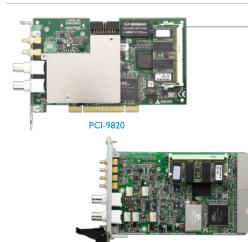
PCI/PXI-9820

2-CH 14-Bit 65 MS/s PCI/PXI Digitizers with SDRAM



PXI-9820

Features

- Supports a 32-bit 3.3 V or 5 V PCI bus
- PXI specifications Rev.2.2 compliant (PXI-9820)
- I4-bit A/D resolution
- Up to 60 MS/s sampling rate per channel with internal timebase
- Up to 65 MS/s sampling rate per channel with external timebase
- Up to 130 MS/s sampling rate in "ping pong" mode
- 2-CH single-ended bipolar inputs
- >30 MHz -3 dB bandwidth
- Up to 512 MB onboard SODIMM SDRAM
- Programmable ranges of ± I V and ±5 V
- User-configurable input impedance of 50 Ω or high input impedance
- Scatter-gather DMA
- Analog and digital triggering
- 2-CH synchronous digital inputs (PXI-9820)
- Fully auto calibration
- Multiple modules synchronization capability

Operating Systems

- Windows 2000/XP/Vista/7
- Linux
- · Windows CE (call for availability)

Recommended Software

- AD-Logger
- VB.NET/VC.NET/VB/VC++/BCB/Delphi
- DAQBench

Driver Support

- DAQPilot for Windows
- DAQPilot for LabVIEW™
- DAQ-MTLB for MATLAB®
- WD-DASK for Windows
- WD-DASK/X for Linux

Introduction

ADLINK's PCI/PXI-9820 is a 65 MS/s, high-resolution PXI digitizer with deep SODIMM SDRAM memory. The device features flexible input configurations, including programmable input ranges and user-configurable input impedance. With the deep onboard acquisition memory, the PCI-9820/PXI-9820 is not limited by the 132 MB/s bandwidth of PCI bus and can record the waveform for a long period of time. The PCI-9820/PXI-9820 is ideal for high-speed waveform capturing, such as radar and ultrasound applications, as well as software radio applications, or those signal digitizing applications which need deep memory for data storage.

Analog Input

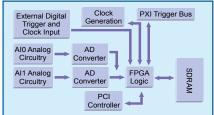
The PCI/PXI-9820 device features two analog input channels. The small signal bandwidth of each channel exceeds 30 MHz. The input ranges are programmable as either ± 5 V or ± 1 V. The I4-bit A/D resolution makes the PCI/PXI-9820 ideal both for time-domain and frequencydomain applications.

Acquisition System

ADLINK PCI/PXI-9820 device uses a pair of 65 MS/s, 14-bit pipeline ADCs to digitize the input signals, and the device provides an internal 60 MHz timebase for data acquisition. The maximum real-time sampling rate is 60 MS/s with internal timebase, and is up to 65 MS/s with external timebase. By using a "ping pong" mode, the sampling rate is up to 120 MS/s with internal timebase or 130 MS/s with external timebase.

Acquisition Memory

The PCI/PXI-9820 device supports 512 MB SODIMM SDRAM. The digitized data are stored in the onboard SDRAM before being transferred to the host memory. The PCI/PXI-9820 device uses the scatter-gather bus-mastering DMA to move data to the host memory. If the data throughput from the PCI/ PXI-9820 is less than the available PCI bus bandwidth, the PCI/ PXI-9820 also features onboard 3 k-sample FIFO to achieve real-time transfer bypassing the SDRAM, directly to the host memory.



۶Xi

DCI

Triggering

The PCI/PXI-9820 device features flexible triggering functionalities, such as analog and digital triggering. The analog trigger features programmable trigger thresholds on rising or falling edges on both input channels. The 5 V/TTL digital trigger comes from PXI trigger bus or the external SMB connector for synchronizing multiple devices.

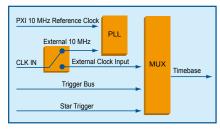
Post-trigger, pre-trigger, delay-trigger and middletrigger modes are available to acquire data around the trigger event. The PCI/PXI-9820 also features repeated trigger acquisition, so you can acquire data in multiple segments coming with successive trigger events at extremely short rearming interval.

Multiple-Module Synchronization

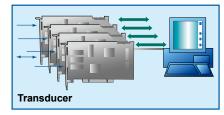
For PCI/PXI-9820, a proprietary bus named SSI (System Synchronization Interface) is designed to synchronize multiple PCI/PXI-9820 devices. SSI provides the timing and trigger synchronization between multiple cards by using a special ribbon cable to all the cards in a daisy-chain configuration. The PCI/PXI-9820 implements star trigger and trigger bus to route timing and trigger signals between one or more PCI/PXI-9820 and other PXI modules. These interfaces allow users to synchronize multiple PXI modules into a system easily. Timebase is also selectable. Users can choose to use the internal clock or the output of the onboard PLL with the reference clock from external clock input, or the PXI 10 MHz reference clock .

Calibration

The auto-calibration function of the PCI/PXI-9820 is performed with trim DACs to calibrate the offset and gain errors of the analog input channels. Once the calibration process is done, the calibration constant will be stored in EEPROM such that these values can be loaded and used as needed by the board. Because all the calibration is conducted automatically by software commands, users don't have to adjust trimpots to calibrate the modules manually.



Timebase Architecture, for PXI-9820 Only



Specifications

Analog Input

- Number of channels: 2 simultaneous-sampled single-ended
- Resolution: 14 bits
- Maximum sampling rate
 - \cdot 65 MS/s for 2 inputs
- · 130 MS/s for Ping-Pong mode using external timebase
- Onboard sample memory

· 512 MB

- Bandwidth (-3 dB): 30 MHz minimum
- Input signal ranges: (software programmable) ±5 V, ±1 V
- Input Coupling: DC
- Overvoltage protection

e tel tellage pi etection	
Range	Overvoltage Protection
± 5 V	± 14 V
± I V	± 5 V

- Input Impedance (soldering selectable): 50 Ω, 1.5 MΩ
- Crosstalk: < -80 dB, DC to 1 MHz
- Total harmonic distortion (THD): -75 dB
- Signal-to-Noise ratio (SNR)

-	
Range	SNR
± 5 V	66 dB
±IV	62 dB

- Spurious-free dynamic range (SFDR): 75 dB
- Data transfer: bus-mastering DMA with scatter-gather

Auto Calibration

- Onboard reference: +5 V
- Onboard reference temperature drift: 2 ppm/°C
- Stability: 6 ppm/1000 Hrs

External Timebase Input

- PCI-9820: direct external timebase input
- PXI-9820: 10 MHz input for PLL or direct external timebase input
- Connector: SMB
- Impedance: 50 Ω
- Coupling: AC
- Input amplitude: I Vpp to 2 Vpp
- Overvoltage protection: 2.5 Vpp
- Frequency range: 500 kHz 65 MHz

Triggering

Analog Triggering

- Modes: pre-trigger, post-trigger, middle-trigger, delay-trigger
- Sources: CH0 and CH1
- Slope: rising/falling
- Coupling: DC
- Trigger sensitivity: 256 steps in full-scale voltage range

Digital triggering

- Modes: pre-trigger, post-trigger, middle-trigger, delay-trigger
- Source: external digital trigger from SMB
- Slope: rising/falling
- Compatibility: 5 V/TTL
- Minimum pulse width: 10 ns
- Repeated trigger rearming interval: 2 cycles of timebase
- Pre-trigger depth: 128 MB or 512 MB, depending on memory option
- Post-trigger depth: 128 MB or 512 MB, depending on memory option



Synchronous Digital Input (For PXI-9820 Only)

- Number of channels: 2
- Compatibility: 5 V/TTL
- Data transer: bus-mastering DMA with scatter/gather

General Specifications

I/O connector

- \cdot BNC x 2 for analog inputs
- \cdot SMB x 4 for external digital trigger, external time base, and synchronous digital inputs
- Operating temperature: 0°C to 50°C
- Storage temperature: -20°C to 80°C
- Relative humidity: 5% to 95%, non-condensing
- Power requirements

Power Rail	Current		
	PXI-9820	PCI-9820	
5 V	900 mA typical	895 mA	
12 V	305 mA typical	295 mA	
3.3 V	360 mA typical (with 128 MB SDRAM)	310 mA (with 128 MB SDRAM)	
3.3 V	500 mA typical (with 512 MB SDRAM)	430 mA (with 512 MB SDRAM)	

- Dimensions (not including connectors) PCI-9820: 175 mm x 107 mm
- PXI-9820: 160 mm x 100 mm

Certifications

EMC/EMI: CE, FCC Class A

Cable Accessories

Cable	Description	PXI-9820	PCI-9820
SMB-SMB-1M	I-meter SMB to SMB cable	\checkmark	
SMB-BNC-1M	I-meter SMB to BNC cable	\checkmark	
ACL-SSI-2	SSI Bus cable for 2 devices	-	
ACL-SSI-3	SSI Bus cable for 3 devices	-	
ACL-SSI-4	SSI Bus cable for 4 devices	-	





Ordering Information

- PCI-9820D/128-0
- 2-CH 14-Bit 65 MS/s Digitizer with 128 MB Memory
- PCI-9820D/512-0
- 2-CH 14-Bit 65 MS/s Digitizer with 512 MB Memory **PXI-9820D/128**
- 2-CH 14-Bit 65 MS/s Digitizer with 128 MB Memory
- PXI-9820D/512
 - 2-CH 14-Bit 65 MS/s Digitizer with 512 MB Memory