



**MODEL:  
HYPER-BT**

**PICO-ITX SBC supports 22nm Intel® Atom™/Celeron® on-board SoC,  
DDR3L, VGA/iDP, GbE, USB 3.0, SATA 3Gb/s,  
HD Audio and RoHS**

# User Manual

Rev. 1.02 - August 27, 2015



# Revision

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Date	Version	Changes
August 27, 2015	1.02	Updated Figure 1-3: Dimensions (mm) Added Section 4.4: Chassis Installation
July 4, 2014	1.01	Updated supported memory specifications in Chapter 1.
June 25, 2014	1.00	Initial release

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# Manual Conventions

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## **WARNING**

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.



## **CAUTION**

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.



## **NOTE**

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.



## **HOT SURFACE**

This symbol indicates a hot surface that should not be touched without taking care.

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Chapter

1

# Introduction

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## 1.1 Introduction



**Figure 1-1: HYPER-BT**

The HYPER-BT PICO-ITX motherboard is an Intel® Atom™/Celeron® processor platform. It supports one 204-pin 1066/1333 MHz single-channel DDR3L SO-DIMM supports up to 8GB (J1900, N2930, E3845, E3827, E3826) or 4GB (N2807, E3825, E3815).

The HYPER-BT includes a VGA connector and an iDP connector. Expansion and I/O include one USB 2.0 connector and one USB 3.0 connector on the rear panel, two USB 2.0 connectors by pin header and one SATA 3Gb/s connector. Serial device connectivity is provided by one internal RS-232 connector. One RJ-45 Ethernet connector provides the system with smooth connections to an external LAN.

## 1.2 Model Variations

The model variations of the HYPER-BT Series are listed below.

Model No.	SoC
HYPER-BT-J19001-R10	Intel® Celeron® quad-core J1900 (10W)
HYPER-BT-N29301-R10	Intel® Celeron® quad-core N2930 (7.5W)
HYPER-BT-N28071-R10	Intel® Celeron® dual-core N2807 (4.3W)
HYPER-BT-E38XX1-R10	Intel® Atom™ E38XX

**Table 1-1: HYPER-BT Model Variations**

## HYPER-BT

### 1.3 Features

Some of the HYPER-BT motherboard features are listed below:

- PICO-ITX SBC supports 22nm Intel® Atom™ or Celeron® on-board SoC
- 12V only single voltage design for AT/ATX power by DC power jack
- VGA and iDP support for dual display
- IEI One Key Recovery solution allows you to create rapid OS backup and recovery

### 1.4 Connectors

The connectors on the HYPER-BT are shown in the figure below.

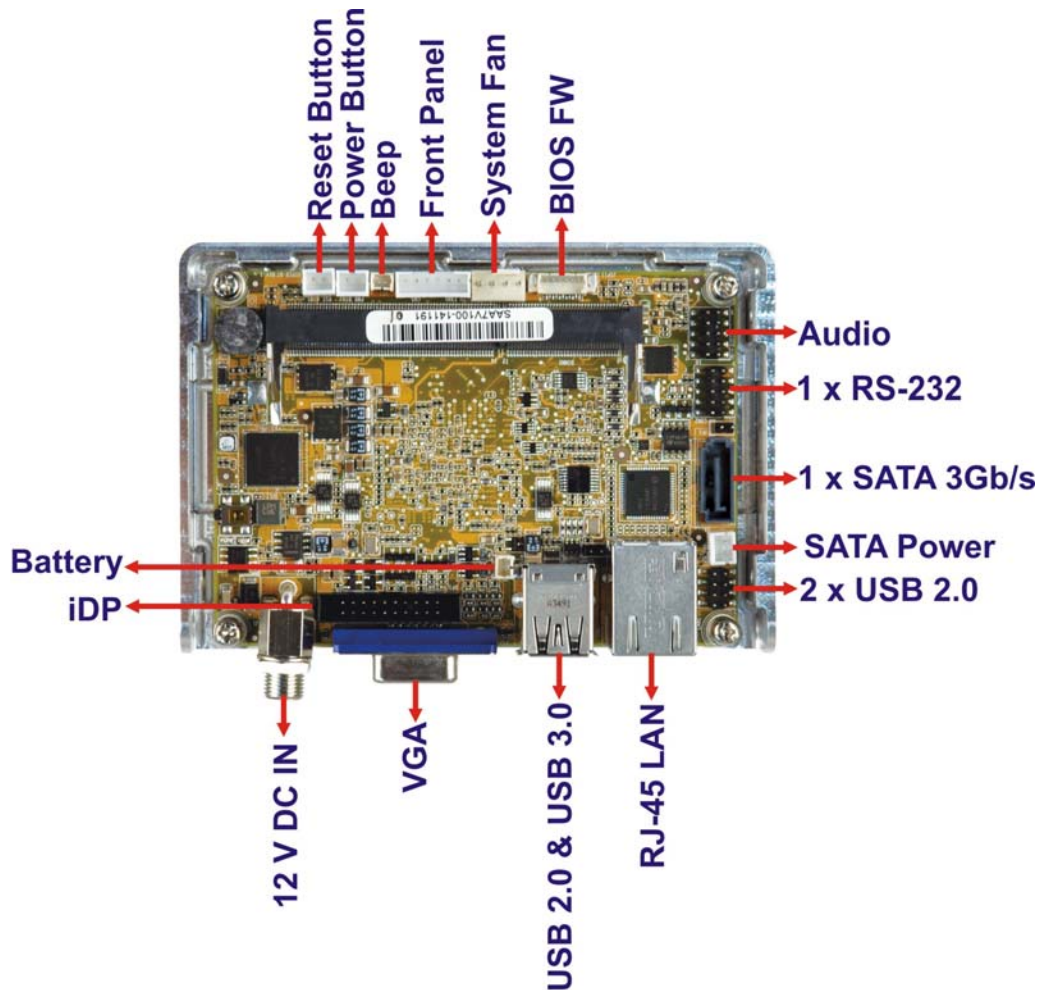


Figure 1-2: Connectors

### 1.5 Dimensions

The dimensions of the board are listed below:

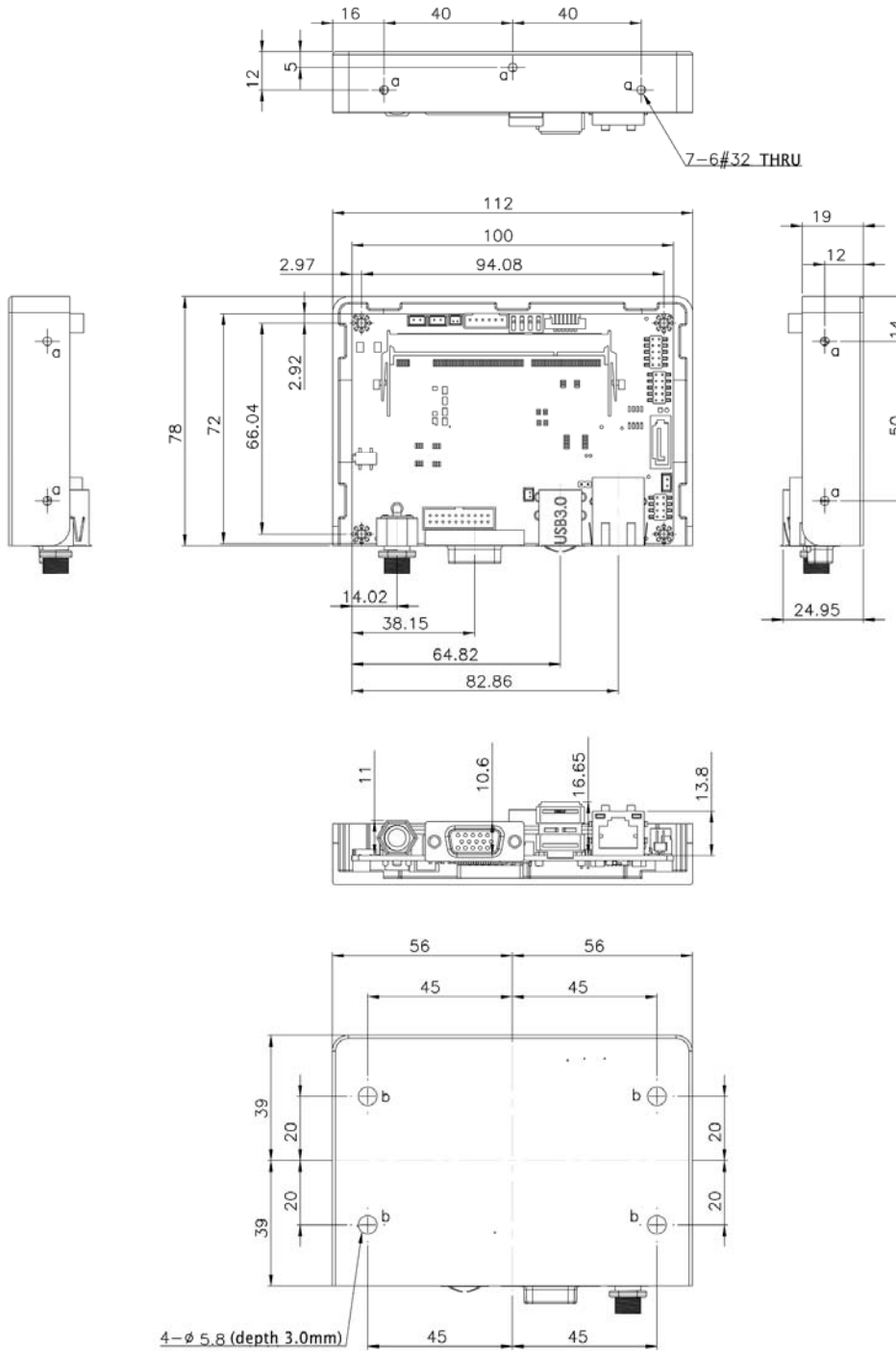


Figure 1-3: Dimensions (mm)



HYPER-BT

1.6 Data Flow

Figure 1-4 shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

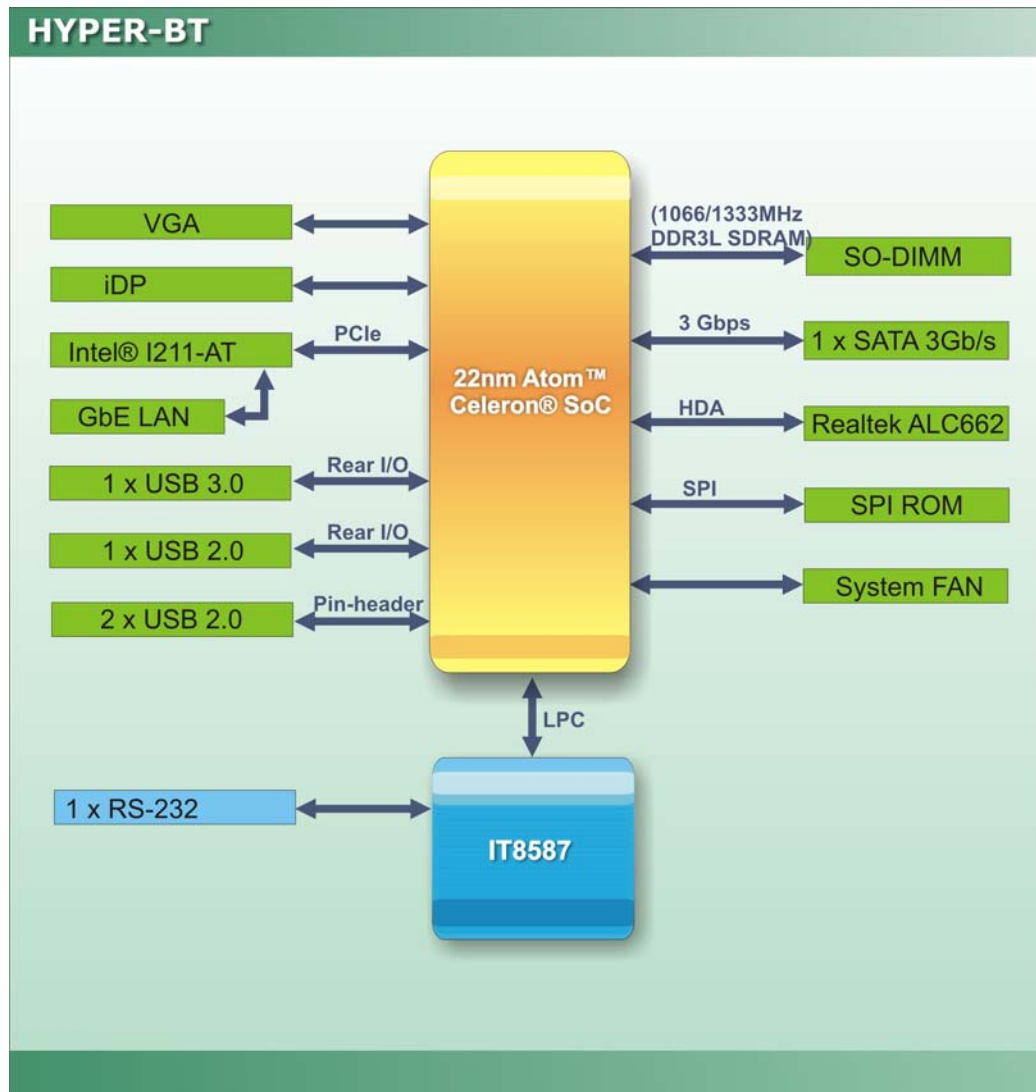


Figure 1-4: Data Flow Diagram

## 1.7 Technical Specifications

HYPER-BT technical specifications are listed below.

Specification	HYPER-BT
<b>SoC</b>	<p>Intel® Atom™ E3845 on-board SoC (1.91GHz, quad-core, 2MB cache, TDP=10W)</p> <p>Intel® Atom™ E3827 on-board SoC (1.75GHz, dual-core, 1MB cache, TDP=8W)</p> <p>Intel® Atom™ E3826 on-board SoC (1.46GHz, dual-core, 1MB cache, TDP=7W)</p> <p>Intel® Atom™ E3825 on-board SoC (1.33GHz, dual-core, 1MB cache, TDP=6W)</p> <p>Intel® Atom™ E3815 on-board SoC (1.46GHz, dual-core, 1MB cache, TDP=5W)</p> <p>Intel® Celeron® J1900 on-board SoC (2GHz, quad-core, 2MB cache, TDP=10W)</p> <p>Intel® Celeron® N2930 on-board SoC (1.83GHz, quad-core, 2MB cache, TDP=7.5W)</p> <p>Intel® Celeron® N2807 on-board SoC (1.58GHz, dual-core, 2MB cache, TDP=4.3W)</p>
<b>BIOS</b>	AMI UEFI BIOS
<b>Memory</b>	One 204-pin 1066/1333 MHz single-channel DDR3L SO-DIMM supports up to 8GB (J1900, N2930, E3845, E3827, E3826) or 4GB (N2807, E3825, E3815)
<b>Graphics</b>	Intel® HD Graphics Gen 7 Engines with 4 execution units, supporting DX11.1 OpenGL 4.2 and OpenCL 1.2
<b>Display Output</b>	<p>Dual independent display</p> <p>1 x VGA (up to 2560x1600@60Hz)</p> <p>1 x iDP interface for HDMI, LVDS, VGA, DVI, DP (up to 3840x2160@60Hz)</p>
<b>Ethernet</b>	LAN: Intel® I211-AT PCIe controller

## HYPER-BT

Specification	HYPER-BT
<b>EC</b>	IT8587
<b>Audio</b>	Realtek ALC662 HD codec supports 5.1 channel
<b>Watchdog Timer</b>	Software programmable support 1~255 sec. system reset
<b>I/O Interface</b>	
<b>Audio Connector</b>	1 x Analog audio by 10-pin (2x5) header
<b>Ethernet</b>	One RJ-45 port
<b>Serial Ports</b>	1 x RS-232 (by pin header)
<b>USB Ports</b>	1 x USB 3.0 (on rear I/O) 3 x USB 2.0 (one on rear I/O, two by pin headers)
<b>Front Panel</b>	1 x 6-pin (1x6) wafer for power LED & HDD LED 1 x 2-pin (1x2) wafer for power button 1 x 2-pin (1x2) wafer for power reset button
<b>LAN LED</b>	1 x 2-pin (1x2) header
<b>Fan</b>	1 x 4-pin (1x4) system fan connector
<b>Storage</b>	
<b>Serial ATA</b>	1 x SATA 3Gb/s with 5V SATA power connector
<b>Environmental and Power Specifications</b>	
<b>Power Supply</b>	12V DC power input only, AT/ATX supported 1 x External DC power jack
<b>Power Consumption</b>	+12V@1.35A (Intel® Celeron® J1900 CPU, 1 x 8GB 1333 MHz DDR3 memory)
<b>Operating Temperature</b>	-20°C ~ 60°C
<b>Storage Temperature</b>	-30°C ~ 70°C
<b>Humidity</b>	5% ~ 95%, non-condensing
<b>Dimensions</b>	100 mm x 72 mm
<b>Weight GW/NW</b>	600 g / 250 g

**Table 1-2: Technical Specifications**

Chapter

**2**

# Unpacking

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## HYPER-BT

### 2.1 Anti-static Precautions

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#### WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

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Make sure to adhere to the following guidelines:

- **Wear an anti-static wristband:** Wearing an anti-static wristband can prevent electrostatic discharge.
- **Self-grounding:** Touch a grounded conductor every few minutes to discharge any excess static buildup.
- **Use an anti-static pad:** When configuring any circuit board, place it on an anti-static mat.
- **Only handle the edges of the PCB:** Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

### 2.2 Unpacking Precautions

When the HYPER-BT is unpacked, please do the following:

- Follow the antistatic guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.







## 2.3 Packing List




**NOTE:**

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the HYPER-BT was purchased from or contact an IEI sales representative directly by sending an email to [sales@ieiworld.com](mailto:sales@ieiworld.com).

The HYPER-BT is shipped with the following components:








Quantity	Item and Part Number	Image
1	1 x HYPER-BT single board computer with heat sink	
1	Audio cable (P/N: 32000-072100-RS)	
1	SATA with 5V output cable kit (P/N: 32801-000201-100-RS)	
1	RS-232 cable (P/N: 32200-000049-RS)	
1	Utility CD	
1	One Key Recovery CD	

## HYPER-BT

1	Quick Installation Guide	
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## 2.4 Optional Items

The following are optional components which may be separately purchased:

Item and Part Number	Image
Dual-port USB cable without bracket (P/N: 32000-070301-RS)	
Serial port cable (P/N: 32200-000049-RS)	
DisplayPort to HDMI converter board for iEi IDP connector (P/N: DP-HDMI-R10)	
DisplayPort to 24-bit dual-channel LVDS converter board for iEi IDP connector (P/N: DP-LVDS-R10)	
DisplayPort to VGA converter board for iEi IDP connector (P/N: DP-VGA-R10)	
DisplayPort to DVI-D converter board for iEi IDP connector (P/N: DP-DVI-R10)	
DisplayPort to DisplayPort converter board for iEi IDP connector (P/N: DP-DP-R10)	

Chapter

**3**

# Connectors

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## HYPER-BT

### 3.1 Peripheral Interface Connectors

This chapter details all the jumpers and connectors.

#### 3.1.1 HYPER-BT Layout

The figures below show all the connectors and jumpers.

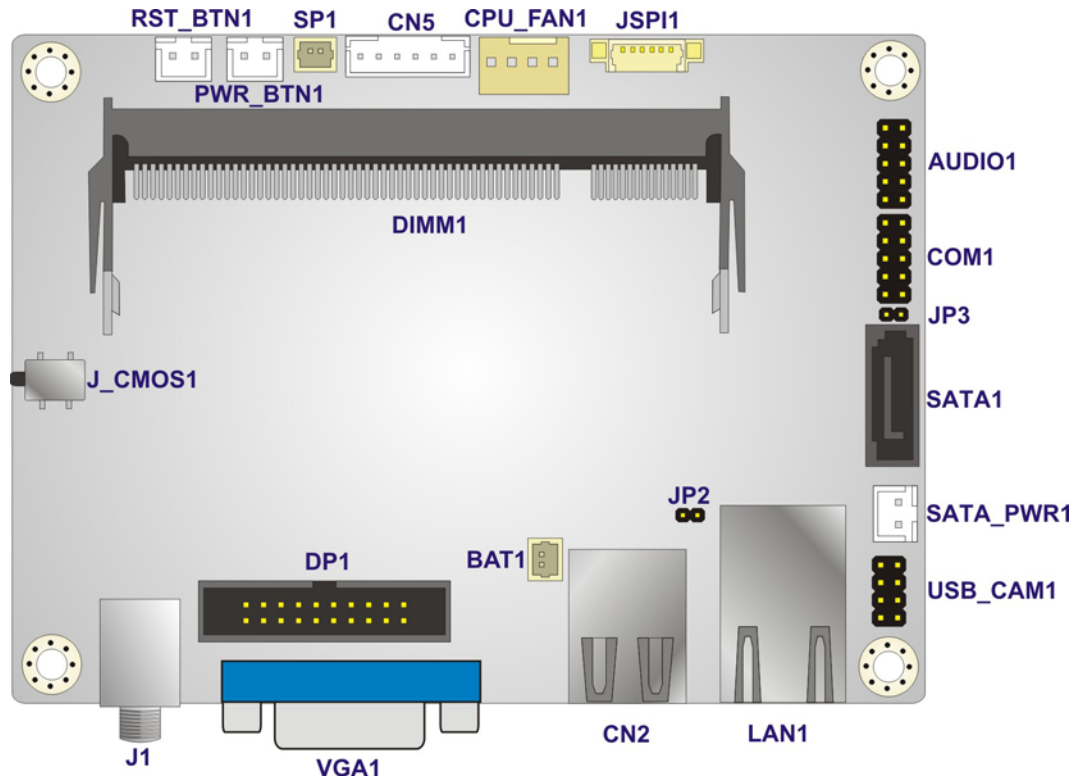


Figure 3-1: Connector and Jumper Locations (Front)

#### 3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
AT/ATX mode select switch	switch	J_ATX_AT1
Audio connector	10-pin header	AUDIO1
Battery connector	2-pin wafer	BAT1
BIOS FW connector	6-pin wafer	JSPI1

Buzzer connector	2-pin wafer	SP1
Clear CMOS button	button	J_CMOS1
CPU fan connector	4-pin wafer	CPU_FAN1
DDR3L SO-DIMM slot	DDR3L SO-DIMM slot	DIMM1
Display port connector	20-pin header	DP1
EC FW connector	2-pin wafer	JP3
Front panel connector	6-pin wafer	CN5
LAN LED connector	2-pin header	JP2
Power button connector	2-pin wafer	PWR_BTN1
Reset button connector	2-pin wafer	RST_BTN1
RS-232 serial port connector	10-pin header	COM1
SATA 3Gb/s drive connector	7-pin SATA connector	SATA1
SATA power connector	2-pin wafer	SATA_PWR1
USB 2.0 connector	8-pin header	USB_CAM1

**Table 3-1: Peripheral Interface Connectors**

### 3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
12V DC IN Connector	DC power jack	J1
LAN connector	RJ-45	LAN1
USB 2.0 & USB 3.0 connector	USB 2.0 & USB 3.0	CN2
VGA Connector	15-pin female	VGA1

**Table 3-2: Rear Panel Connectors**

## HYPER-BT

### 3.2 Internal Peripheral Connectors

The section describes all of the connectors on the HYPER-BT.

#### 3.2.1 AT/ATX Mode Select Switch

<b>CN Label:</b>	<b>J_ATX_AT1</b>
<b>CN Type:</b>	Switch
<b>CN Location:</b>	See <b>Figure 3-2</b>
<b>CN Settings:</b>	See <b>Table 3-3</b>

The AT/ATX mode select switch specifies the systems power mode as AT or ATX. AT/ATX mode select switch settings are shown in **Table 3-3**.

Setting	Description
Short A-B	AT Mode
Short B-C	ATX Mode

**Table 3-3: AT/ATX Mode Select Switch Settings**

The location of the AT/ATX mode select switch is shown in **Figure 3-2** below.

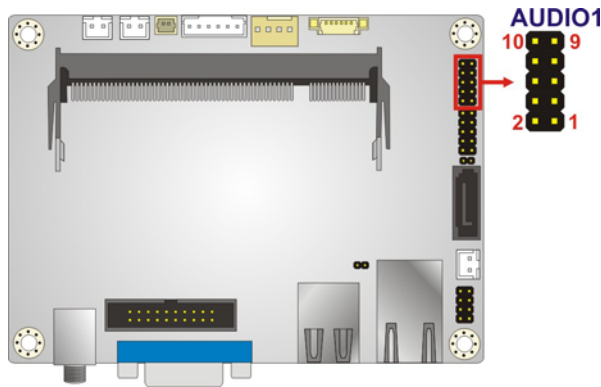


**Figure 3-2: AT/ATX Mode Select Switch Location**

### 3.2.2 Audio Connector

- CN Label:** AUDIO1
- CN Type:** 10-pin header, p=2.0 mm
- CN Location:** See **Figure 3-3**
- CN Pinouts:** See **Table 3-4**

The audio connector is connected to external audio devices including speakers and microphones for the input and output of audio signals to and from the system.



**Figure 3-3: Audio Connector Location**

Pin	Description	Pin	Description
1	LINE_OUTR	2	LINEIN_R
3	Analog_GND	4	Analog_GND
5	LINE_OUTL	6	LINEIN_L
7	Analog_GND	8	Analog_GND
9	LMIC1-R	10	LMIC1-L

**Table 3-4: Audio Connector Pinouts**

## HYPER-BT

### 3.2.3 Battery Connector



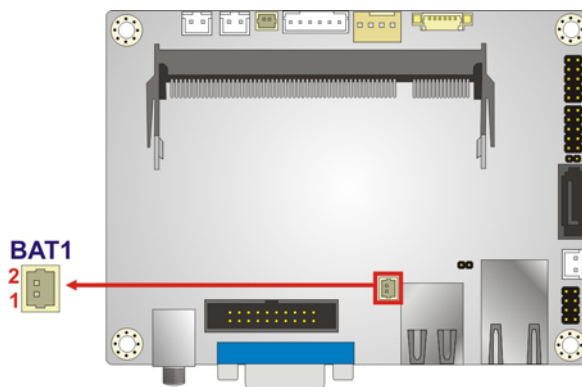
**CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- CN Label:**            **BAT1**
- CN Type:**            2-pin wafer, p=1.25 mm
- CN Location:**      See **Figure 3-4**
- CN Pinouts:**        See **Table 3-5**

The battery connector is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.



**Figure 3-4: Battery Connector Location**

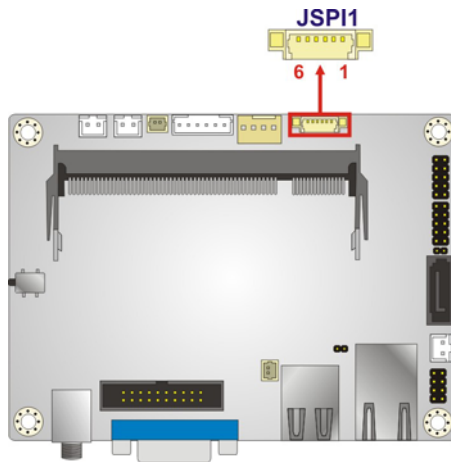
Pin	Description	Pin	Description
1	VBATT	2	GND

**Table 3-5: Battery Connector Pinouts**

### 3.2.4 BIOS FW Connector

- CN Label:** JSPI1
- CN Type:** 6-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-5**
- CN Pinouts:** See **Table 3-6**

The BIOS FW connector is used for programming the BIOS.



**Figure 3-5: BIOS FW Connector Location**

Pin	Description	Pin	Description
1	+V1.8M_SPI_CON	2	SPI_CS
3	SPI_SO_SW	4	SPI_CLK_SW
5	SPI_SI_SW	6	GND

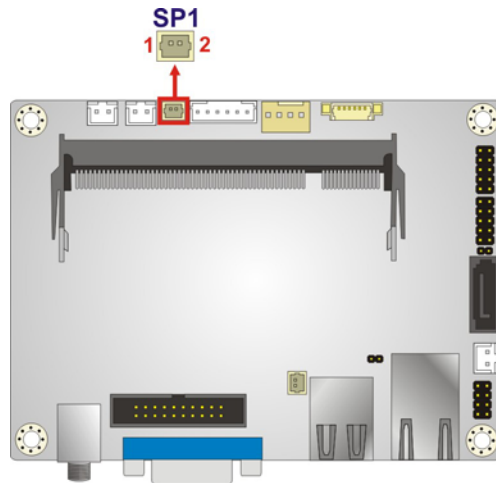
**Table 3-6: BIOS FW Connector Pinouts**

### 3.2.5 Buzzer Connector

- CN Label:** SP1
- CN Type:** 2-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-6**
- CN Pinouts:** See **Table 3-7**

## HYPER-BT

The buzzer connector is connected to the buzzer.



**Figure 3-6: Buzzer Connector Location**

Pin	Description	Pin	Description
1	Buzzer +	2	Buzzer -

**Table 3-7: Buzzer Connector Pinouts**

### 3.2.6 Clear CMOS Button

<b>CN Label:</b>	<b>J_CMOS1</b>
<b>CN Type:</b>	Push button
<b>CN Location:</b>	See <b>Figure 3-7</b>
<b>CN Settings:</b>	See <b>Table 3-8</b>

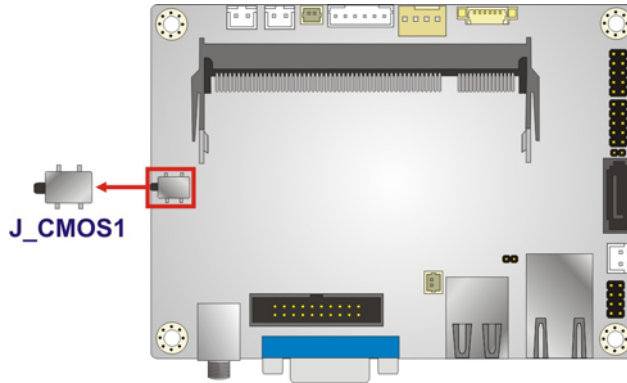
If the HYPER-BT fails to boot due to improper BIOS settings, use the button to clear the CMOS data and reset the system BIOS information.

The clear CMOS button settings are shown in **Table 3-8**.

Setting	Description	
Open	Normal Operation	Default
Push	Clear CMOS Setup	

**Table 3-8: Clear CMOS Button Settings**

The location of the clear CMOS button is shown in **Figure 3-7**.

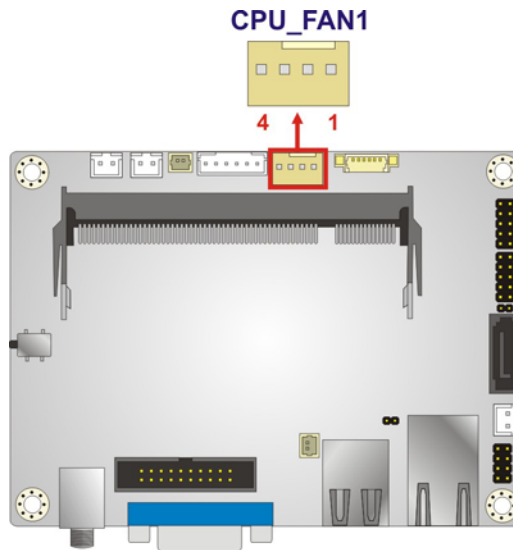


**Figure 3-7: Clear CMOS Button Location**

### 3.2.7 CPU Fan Connector

- CN Label:** CPU\_FAN1
- CN Type:** 4-pin wafer, p=2.54 mm
- CN Location:** See **Figure 3-8**
- CN Pinouts:** See **Table 3-9**

The fan connector attaches to a cooling fan.



**Figure 3-8: CPU Fan Connector Location**



## HYPER-BT

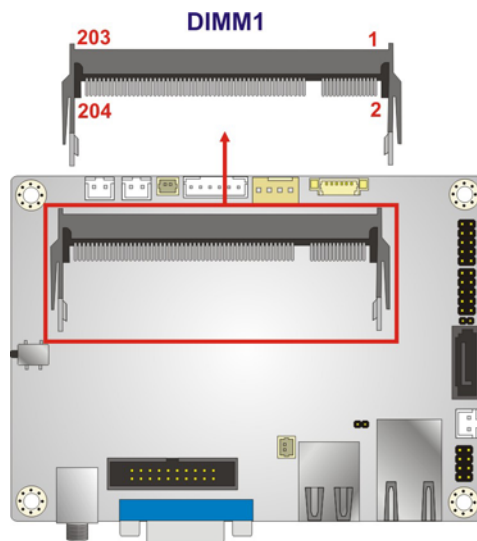
Pin	Description	Pin	Description
1	GND	2	+V12_FAN
3	FANIO1_EC	4	FANOUT1_EC

**Table 3-9: CPU Fan Connector Pinouts**

### 3.2.8 DDR3L SO-DIMM Slot

- CN Label:** DIMM1
- CN Type:** DDR3L SO-DIMM slot
- CN Location:** See **Figure 3-9**

The DDR3L SO-DIMM slot is for DDR3L SO-DIMM memory module.

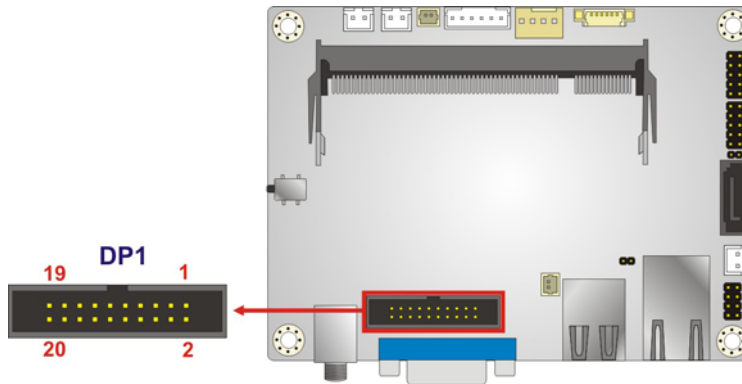


**Figure 3-9: DDR3L SO-DIMM Slot Location**

### 3.2.9 Display Port Connector

- CN Label:** DP1
- CN Type:** 20-pin box header, p=2.0 mm
- CN Location:** See **Figure 3-10**
- CN Pinouts:** See **Table 3-10**

The disport port connector provides flexible display function that supports VGA, DVI, LVDS, HDMI and DisplayPort via the disport port convert board.



**Figure 3-10: Display Port Connector Location**

Pin	Description	Pin	Description
1	DDI1_HPDP1#	2	DPD_AUX_CTRL_P2
3	GND	4	DPD_AUX_CTRL_N2
5	AUX_CTRL_DET_D	6	GND
7	GND	8	DPD_OB_LANE2_P
9	DPD_OB_LANE3_P	10	DPD_OB_LANE2_N
11	DPD_OB_LANE3_N	12	GND
13	GND	14	DPD_OB_LANE0_P
15	DPD_OB_LANE1_P	16	DPD_OB_LANE0_N
17	DPD_OB_LANE1_N	18	GND
19	VCC	20	NC

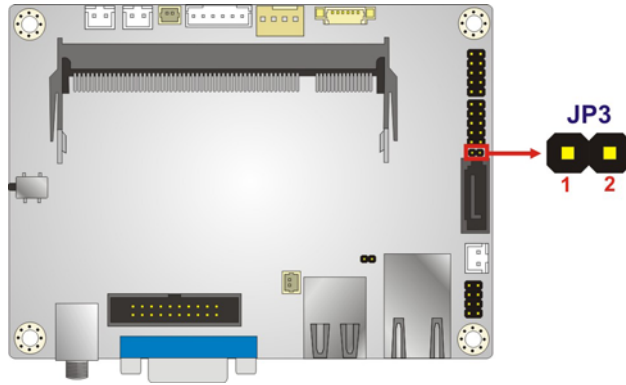
**Table 3-10: Display Port Connector Pinouts**

### 3.2.10 EC FW Connector

- CN Label:** JP3
- CN Type:** 2-pin header, p=2.0 mm
- CN Location:** See **Figure 3-11**
- CN Pinouts:** See **Table 3-11**

The EC FW connector is used for programming the EC.

**HYPER-BT**



**Figure 3-11: EC FW Connector Location**

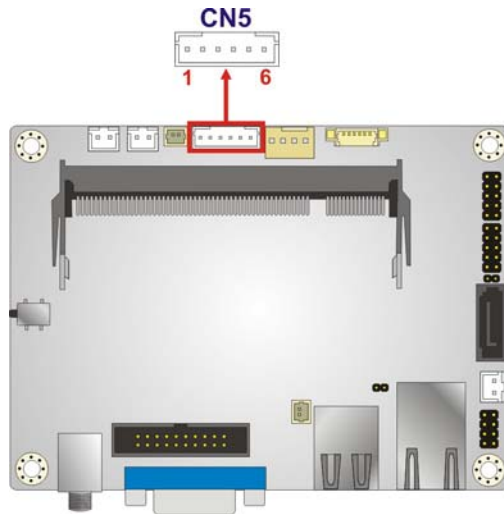
Pin	Description	Pin	Description
1	SMB_CLK_FW	2	SMB_DATA_FW

**Table 3-11: EC FW Connector Pinouts**

**3.2.11 Front Panel Connector**

- CN Label:** CN5
- CN Type:** 6-pin wafer, p=2.0 mm
- CN Location:** See **Figure 3-12**
- CN Pinouts:** See **Table 3-12**

The front panel connector connects to the indicator LEDs on the system front panel.



**Figure 3-12: Front Panel Connector Location**

Pin	Description	Pin	Description
1	+V5S	2	GND
3	PWR_LED+	4	PWR_LED-
5	HDD_LED+	6	HDD_LED-

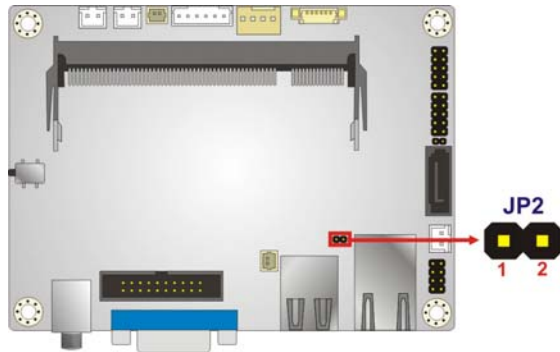
**Table 3-12: Front Panel Connector Pinouts**

### 3.2.12 LAN LED Connector

- CN Label:** JP2
- CN Type:** 2-pin header, p=2.0 mm
- CN Location:** See **Figure 3-13**
- CN Pinouts:** See **Table 3-13**

The LAN LED connectors connect to the LAN link LEDs on the system.

**HYPER-BT**



**Figure 3-13: LAN LED Connector Location**

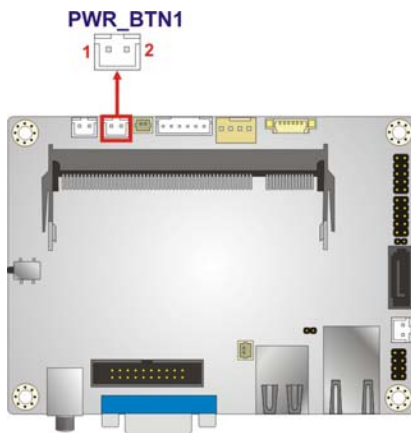
Pin	Description	Pin	Description
1	VCC	2	L1_LINK_ACT-

**Table 3-13: LAN LED Connector Pinouts**

**3.2.13 Power Button Connector**

- CN Label:** PWR\_BTN1
- CN Type:** 2-pin wafer, p=2.0 mm
- CN Location:** See **Figure 3-14**
- CN Pinouts:** See **Table 3-14**

The power button connector is connected to a power switch on the system chassis to enable users to turn the system on and off.



**Figure 3-14: Power Button Connector Location**

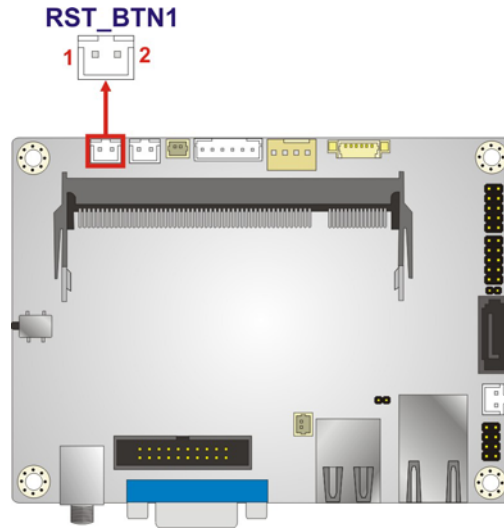
Pin	Description
1	PWRBTN_SW#
2	GND

**Table 3-14: Power Button Connector Pinouts**

### 3.2.14 Reset Button Connector

- CN Label:** RST\_BTN1
- CN Type:** 2-pin wafer, p=2.0 mm
- CN Location:** See **Figure 3-15**
- CN Pinouts:** See **Table 3-15**

The reset button connector is connected to a reset switch on the system chassis to enable users to reboot the system when the system is turned on.



**Figure 3-15: Reset Button Connector Location**

Pin	Description
1	PM_SYSRST_R#
2	GND

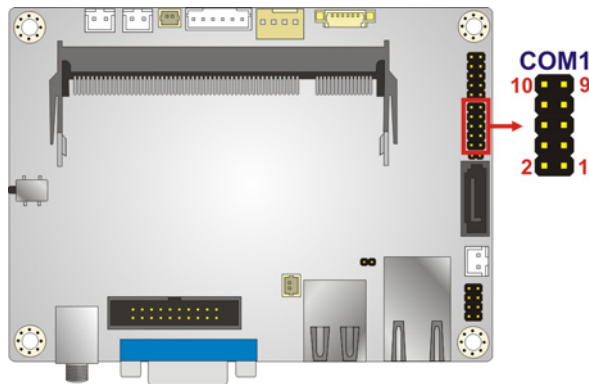
**Table 3-15: Reset Button Connector Pinouts**

**HYPER-BT**

**3.2.15 RS-232 Serial Port Connector**

- CN Label:** COM1
- CN Type:** 10-pin header, p=2.0 mm
- CN Location:** See **Figure 3-16**
- CN Pinouts:** See **Table 3-16**

The serial connector provides RS-232 connection.



**Figure 3-16: RS-232 Serial Port Connector Location**

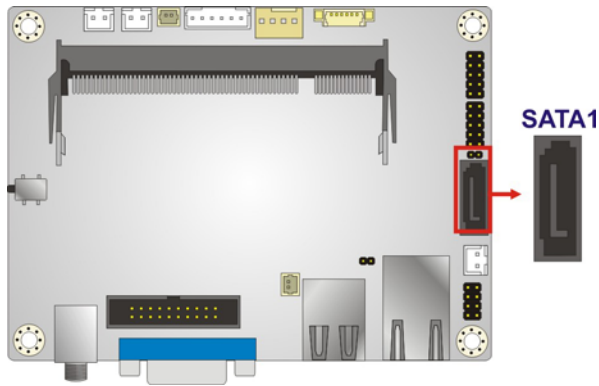
Pin	Description	Pin	Description
1	-NDCD1	2	-NDSR1
3	NSIN1	4	-NRTS1
5	NSOUT1	6	-NCTS1
7	-NDTR1	8	-XRI1
9	GND	10	GND

**Table 3-16: RS-232 Serial Port Connector Pinouts**

**3.2.16 SATA 3Gb/s Drive Connector**

- CN Label:** SATA1
- CN Type:** 7-pin SATA connector
- CN Location:** See **Figure 3-17**

The SATA 3Gb/s drive connector is connected to a SATA 3Gb/s drive. The SATA 3Gb/s drive transfers data at speeds as high as 3Gb/s.

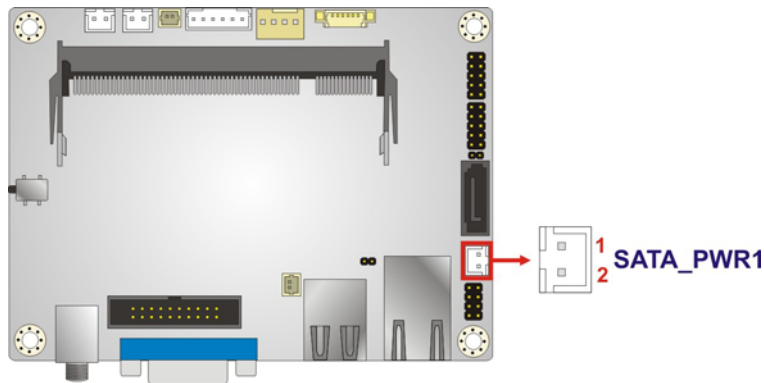


**Figure 3-17: SATA 3Gb/s Drive Connector Location**

### 3.2.17 SATA Power Connector

- CN Label:** SATA\_PWR1
- CN Type:** 2-pin wafer, p=2.0 mm
- CN Location:** See **Figure 3-18**
- CN Pinouts:** See **Table 3-17**

The SATA power connector provides +5V power output to the SATA connector.



**Figure 3-18: SATA Power Connector Location**



## HYPER-BT

Pin	Description
1	+5V
2	GND

Table 3-17: SATA Power Connector Pinouts

### 3.2.18 USB Connector

- CN Label:** USB\_CAM1
- CN Type:** 8-pin header, p=2.0 mm
- CN Location:** See Figure 3-19
- CN Pinouts:** See Table 3-18

The USB connector provides two USB 2.0 ports by dual-port USB cable.

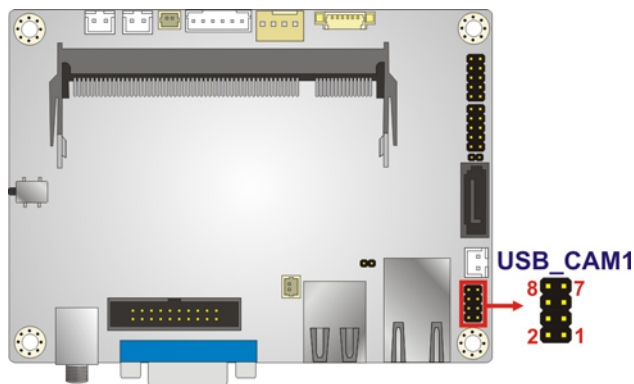


Figure 3-19: USB Connector Location

Pin	Description	Pin	Description
1	VCC	2	GND
3	DATA2_N	4	DATA3_P
5	DATA2_P	6	DATA3_N
7	GND	8	VCC

Table 3-18: USB Connector Pinouts

### 3.3 External Peripheral Interface Connector Panel

Figure 3-20 shows the HYPER-BT external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

- 1 x LAN connector
- 1 x Power connector
- 1 x USB 2.0 & USB 3.0 connector
- 1 x VGA connector

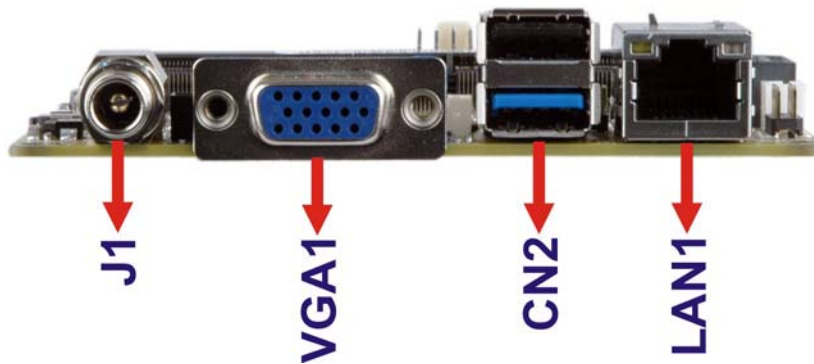


Figure 3-20: External Peripheral Interface Connector

#### 3.3.1 LAN Connector

- CN Label:** LAN1
- CN Type:** RJ-45
- CN Location:** See Figure 3-20
- CN Pinouts:** See Figure 3-21 and Table 3-19

The LAN connector connects to a local network.

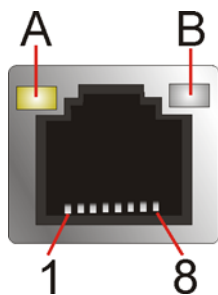


Figure 3-21: LAN Connector

## HYPER-BT

Pin	Description	Pin	Description
1	MDIA3-	5	MDIA2+
2	MDIA3+	6	MDIA1+
3	MDIA1-	7	MDIA0-
4	MDIA2-	8	MDIA0+

**Table 3-19: LAN Pinouts**

LED	Description	LED	Description
A	on: linked blinking: data is being sent/received	B	off: 10 Mb/s green: 100 Mb/s orange: 1000 Mb/s

**Table 3-20: Connector LEDs**

### 3.3.2 Power Connector

- CN Label:** J1
- CN Type:** 12V DC IN
- CN Location:** See **Figure 3-20**
- CN Pinouts:** See **Table 3-21**

The power connector supports 12V DC power input.

Pin	Description	Pin	Description
1	VCC	2	GND
3	GND		

**Table 3-21: Power Connector Pinouts**

### 3.3.3 USB Connectors

- CN Label:** CN2
- CN Type:** USB 2.0 & USB 3.0 ports
- CN Location:** See **Figure 3-20**
- CN Pinouts:** See **Table 3-21**

The HYPER-BT has one external USB 2.0 port and one external USB 3.0 port. The USB connector can be connected to a USB device. The pinouts of USB 2.0 port & USB 3.0 connectors are shown below.

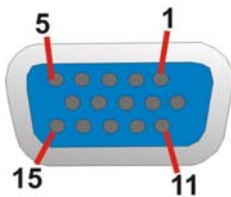
Pin	Description	Pin	Description
1	VCC_USB3_01	8	USB3P0_TXDN1
2	USB2P0_DM1_L	9	USB3P0_TXDP1
3	USB2P0_DP1_L	10	VCC_USB3_01
4	GND	11	DATA1_N
5	USB3P0_RXDN1	12	DATA1_P
6	USB3P0_RXDP1	13	GND
7	GND		

**Table 3-22: USB 2.0 & USB 3.0 Port Pinouts**

### 3.3.1 VGA Connector

- CN Label:** VGA1
- CN Type:** 15-pin female (VGA)
- CN Location:** See **Figure 3-20**
- CN Pinouts:** See **Figure 3-22** and **Table 3-23**

The VGA port connects to a monitor that accepts a standard VGA input.



**Figure 3-22: VGA Connector**

Pin	Description	Pin	Description
1	Red	2	Green
3	Blue	4	NC
5	GND	6	GND
7	GND	8	GND

## HYPER-BT

Pin	Description	Pin	Description
9	VGAVCC	10	HOTPLUG
11	NC	12	DDCDAT
13	HSYNC	14	VSYNC
15	DDCCLK		

**Table 3-23: VGA Connector Pinouts**

Chapter

**4**

# Installation

---

## HYPER-BT

### 4.1 Anti-static Precautions

---



#### WARNING:

Failure to take ESD precautions during the installation of the HYPER-BT may result in permanent damage to the HYPER-BT and severe injury to the user.

---

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the HYPER-BT. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the HYPER-BT or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband:*** Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding:*** Before handling the board, touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad:*** When configuring the HYPER-BT, place it on an anti-static pad. This reduces the possibility of ESD damaging the HYPER-BT.
- ***Only handle the edges of the PCB:*** When handling the PCB, hold the PCB by the edges.

### 4.2 Installation Considerations

---



#### NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

---

**WARNING:**

The installation instructions described in this manual should be carefully followed in order to prevent damage to the HYPER-BT, HYPER-BT components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  - The user manual provides a complete description of the HYPER-BT installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the HYPER-BT on an antistatic pad:
  - When installing or configuring the motherboard, place it on an antistatic pad. This helps to prevent potential ESD damage.
- Turn all power to the HYPER-BT off:
  - When working with the HYPER-BT, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the HYPER-BT **DO NOT**:

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

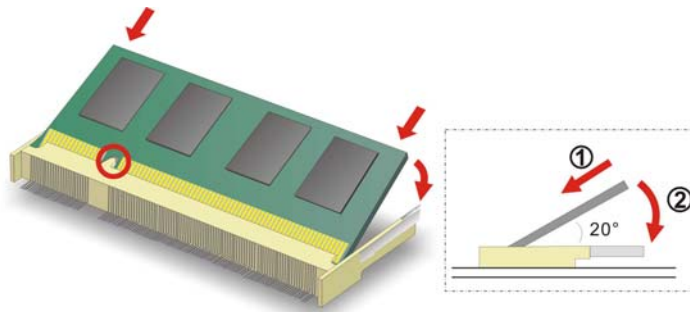


### 4.3 SO-DIMM Installation

**WARNING:**

Using incorrectly specified SO-DIMM may cause permanent damage to the HYPER-BT. Please make sure the purchased SO-DIMM complies with the memory specifications of the HYPER-BT. SO-DIMM specifications compliant with the HYPER-BT are listed in the specification table of Chapter 1.

To install an SO-DIMM, please follow the steps below and refer to Figure 4-1.



**Figure 4-1: SO-DIMM Installation**

- Step 1:** **Locate the SO-DIMM socket.** Place the board on an anti-static mat.
- Step 2:** **Align the SO-DIMM with the socket.** Align the notch on the memory with the notch on the memory socket.
- Step 3:** **Insert the SO-DIMM.** Push the memory in at a 20° angle. (See Figure 4-1)
- Step 4:** **Seat the SO-DIMM.** Gently push downwards and the arms clip into place. (See Figure 4-1)

## 4.4 Chassis Installation

### 4.4.1 Heat Sink Enclosure



**WARNING:**

Never run the HYPER-BT without the heat sink secured to the board. The heat sink ensures the system remains cool and does not need addition heat sinks to cool the system.

---



**WARNING:**

When running the HYPER-BT, do not put the HYPER-BT directly on a surface that can not dissipate system heat, especially the wooden or plastic surface. It is highly recommended to run the HYPER-BT

→ on a heat dissipation surface or

→ using copper pillars to hold the board up from the chassis

---

When the HYPER-BT is shipped, it is secured to a heat sink with four retention screws. If the HYPER-BT must be removed from the heat sink, the four retention screws must be removed.

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### 4.4.2 Motherboard Installation

Each side of the heat sink enclosure has several screw holes allowing the HYPER-BT to be mounted into a chassis (please refer to Figure 1-3 for the detailed dimensions). The user can design or select a chassis that has screw holes matching up with the holes on the heat sink enclosure for installing the HYPER-BT. The following diagram shows an example of motherboard installation.

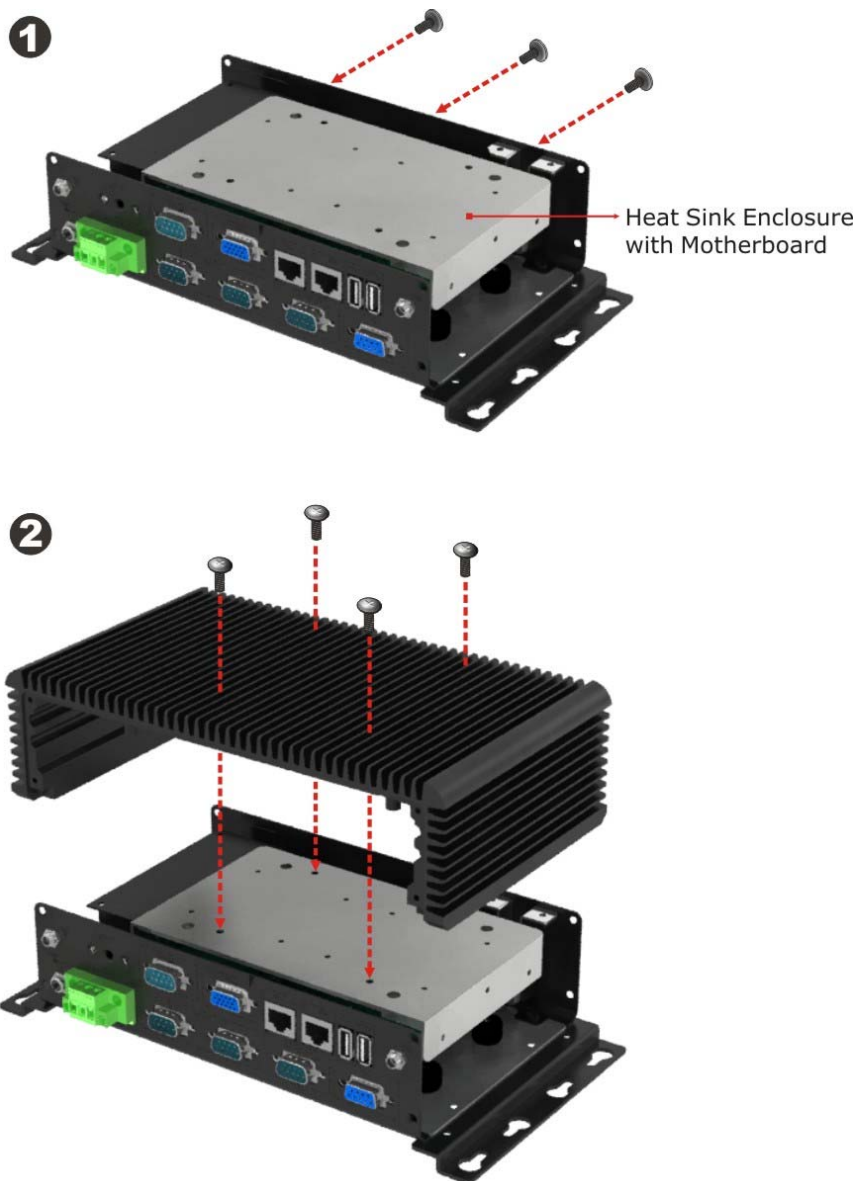


Figure 4-2: Motherboard Installation Example

## 4.5 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the on-board connectors

### 4.5.1 Audio Kit Installation

The Audio Kit that came with the HYPER-BT connects to the audio connector on the HYPER-BT. The audio kit consists of three audio jacks. Mic-in connects to a microphone. Line-in provides a stereo line-level input to connect to the output of an audio device. Line-out, a stereo line-level output, connects to two amplified speakers. To install the audio kit, please refer to the steps below:

**Step 1:** **Locate the audio connector.** The location of the 10-pin audio connector is shown in **Chapter 3**.

**Step 2:** **Align pin 1.** Align pin 1 on the on-board connector with pin 1 on the audio kit connector. Pin 1 on the audio kit connector is indicated with a white dot. See Figure 4-3.

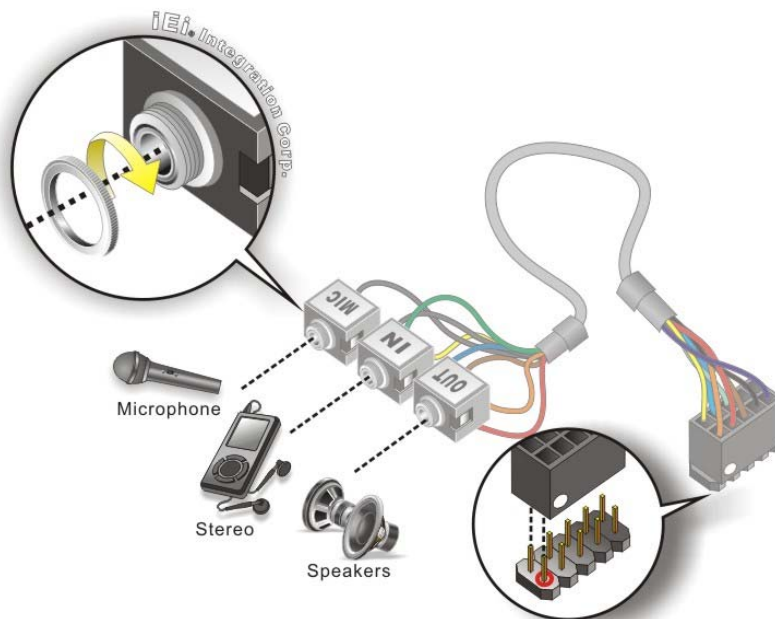


Figure 4-3: Audio Kit Cable Connection

## HYPER-BT

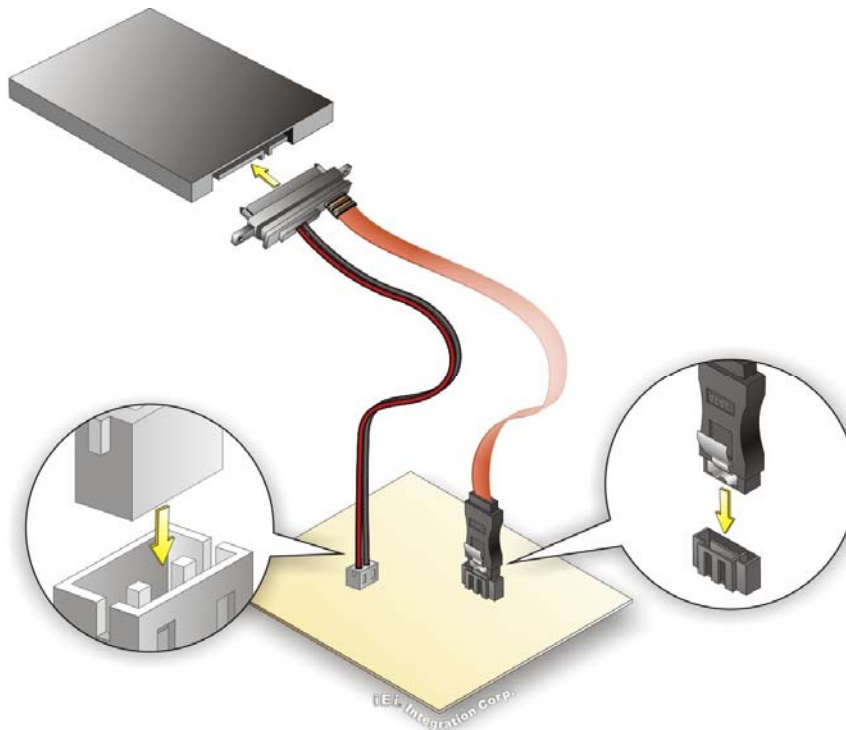
**Step 3:** **Connect the audio devices.** Connect speakers to the line-out audio jack. Connect the output of an audio device to the line-in audio jack. Connect a microphone to the mic-in audio jack.

### 4.5.2 SATA Drive Connection

The HYPER-BT is shipped with a SATA drive cable. To connect the SATA drive to the connector, please follow the steps below.

**Step 1:** **Locate the SATA connector and the SATA power connector.** The locations of the connectors are shown in **Chapter 3**.

**Step 2:** **Insert the cable connector.** Insert the cable connector into the on-board SATA drive connector and the SATA power connector. See **Figure 4-4**.



**Figure 4-4: SATA Drive Cable Connection**

**Step 3:** **Connect the cable to the SATA disk.** Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 4-4**.

**Step 4:** To remove the SATA cable from the SATA connector, press the clip on the connector at the end of the cable.

### 4.5.3 Single RS-232 Cable

The single RS-232 cable consists of one serial port connector attached to a serial communications cable that is then attached to a D-sub 9 male connector. To install the single RS-232 cable, please follow the steps below.

**Step 1:** **Locate the connector.** The location of the RS-232 connector is shown in Chapter 3.

**Step 2:** **Insert the cable connector.** Insert the connector into the serial port box header. See Figure 4-5. A key on the front of the cable connectors ensures the connector can only be installed in one direction.

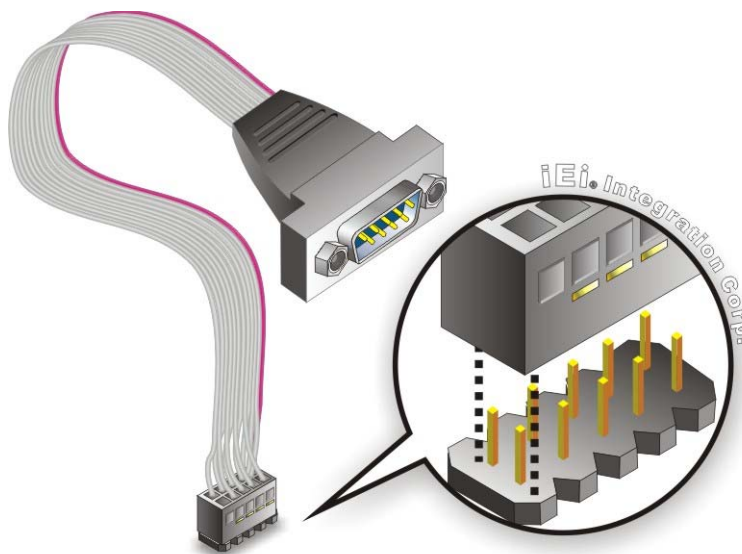


Figure 4-5: Single RS-232 Cable Installation

**Step 3:** **Secure the bracket.** The single RS-232 connector has two retention screws that must be secured to a chassis or bracket.

**Step 4:** **Connect the serial device.** Once the single RS-232 connector is connected to a chassis or bracket, a serial communications device can be connected to the system.

Chapter

**5**

# BIOS

---

## 5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.



### NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

---

### 5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. Press the **DELETE** or **F2** key as soon as the system is turned on or
2. Press the **DELETE** or **F2** key when the “**Press Del to enter SETUP**” message appears on the screen.

If the message disappears before the **DELETE** or **F2** key is pressed, restart the computer and try again.

### 5.1.2 Using Setup

Use the arrow keys to highlight items, press **ENTER** to select, use the PageUp and PageDown keys to change entries, press **F1** for help and press **ESC** to quit. Navigation keys are shown in.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes



## HYPER-BT

Key	Function
-	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2 key	Load previous values.
F3 key	Load optimized defaults
F4 key	Save changes and Exit BIOS
Esc key	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu

Table 5-1: BIOS Navigation Keys

### 5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window press **Esc** or the **F1** key again.

### 5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the jumper described in **Chapter 3**.

### 5.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Boot – Changes the system boot configuration.
- Security – Sets User and Supervisor Passwords.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

## 5.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered. The **Main** menu gives an overview of the basic system information.

Aptio Setup Utility - Copyright (C) 2013 American Megatrends, Inc.		
Main	Advanced	Chipset   Security   Boot   Save & Exit
BIOS Information		Set the Date. Use Tab to switch between Data elements.
BIOS Vendor	American Megatrends	
Core Version	5.009	
Compliancy	UEFI 2.3; PI 1.2	
Project Version	SAA7AR10.rom	
Build Date and Time	05/27/2014 11:46:33	
iWDD Vendor	iEi	
iWDD Version	SAA7ER10.bin	
CPU Configuration		
Microcode Patch	809	
BayTrail SoC	Unknown	
Memory Information		
Total Memory	4096 MB(LPDDR3)	-----
TXE Information		←→: Select Screen
Sec RC Version	00.05.00.00	↑ ↓: Select Item
TXE FW Version	01.00.02.1060	EnterSelect
System Date	[Fri 06/20/2014]	+/-: Change Opt.
System Time	[19:43:27]	F1: General Help
Access Level	Administrator	F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
Version 2.16.1242. Copyright (C) 2013 American Megatrends, Inc.		

### BIOS Menu 1: Main

The Main menu lists the following system details:

- BIOS Information
- iWDD Information
- CPU Configuration
- Memory Information
- TXE Information

## HYPER-BT

The System Overview field also has two user configurable fields:

→ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

→ **System Time [xx:xx:xx]**

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

## 5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 2**) to configure the CPU and peripheral devices through the following sub-menus:



### WARNING!

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.

```

Aptio Setup Utility - Copyright (C) 2013 American Megatrends, Inc.
Main  Advanced  Chipset  Security  Boot  Save & Exit
-----
> ACPI Settings
> IT8528 Super IO Configuration
> Hardware Monitor
> RTC Wake Settings
> Serial Port Console Redirection
> CPU Configuration
> IDE Configuration
> USB Configuration

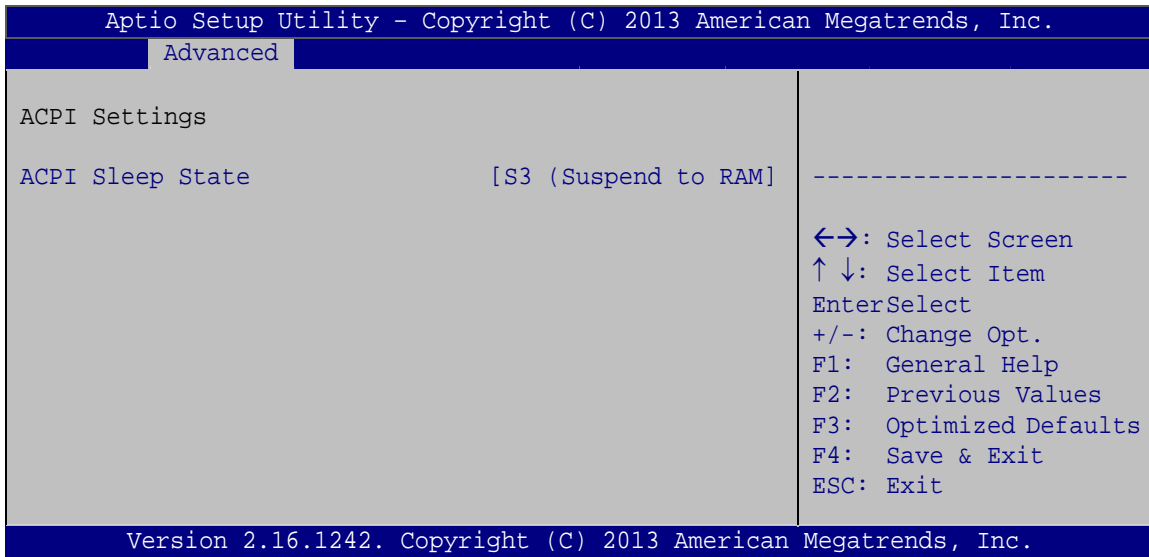
System ACPI Parameters.
-----
<=>: Select Screen
↑ ↓: Select Item
Enter>Select
F1  General Help
F2  Previous Values
F3  Optimized Defaults
F4  Save
ESC Exit

Version 2.16.1242. Copyright (C) 2013 American Megatrends, Inc.
  
```

**BIOS Menu 2: Advanced**

### 5.3.1 ACPI Settings

The **ACPI Settings** menu (**BIOS Menu 3**) configures the Advanced Configuration and Power Interface (ACPI) options.



#### BIOS Menu 3: ACPI Configuration

##### → ACPI Sleep State [S3 (Suspend to RAM)]

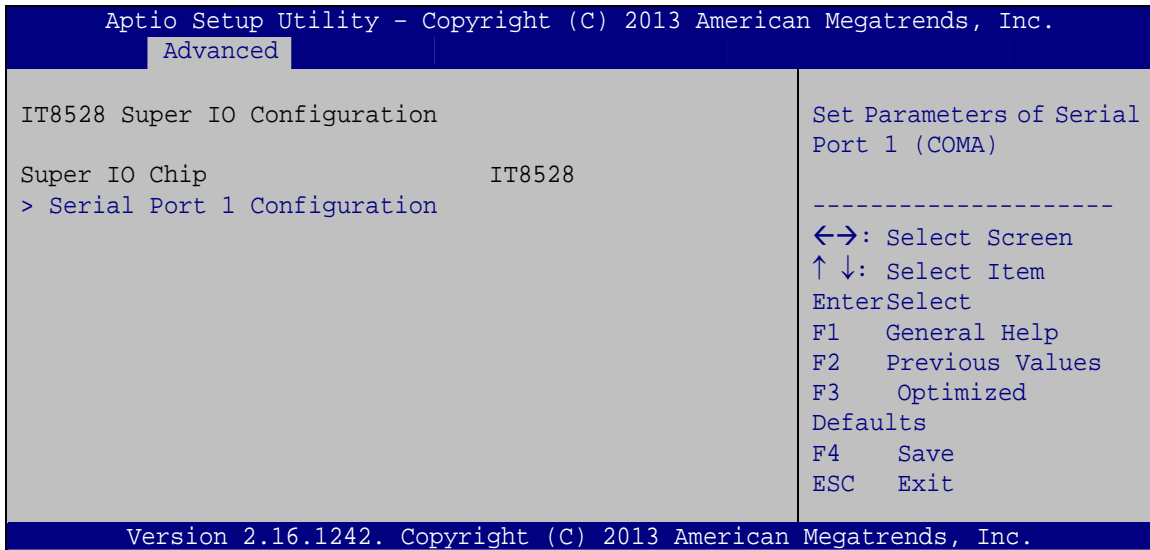
The fields in **ACPI Sleep State** option cannot be changed.

- **Suspend Disabled** Disable the suspend function.
- **S3 (Suspend to DEFAULT RAM)** The caches are flushed and the CPU is powered off. Power to the RAM is maintained. The computer returns slower to a working state, but more power is saved.

## HYPER-BT

### 5.3.2 IT8528 Super IO Configuration

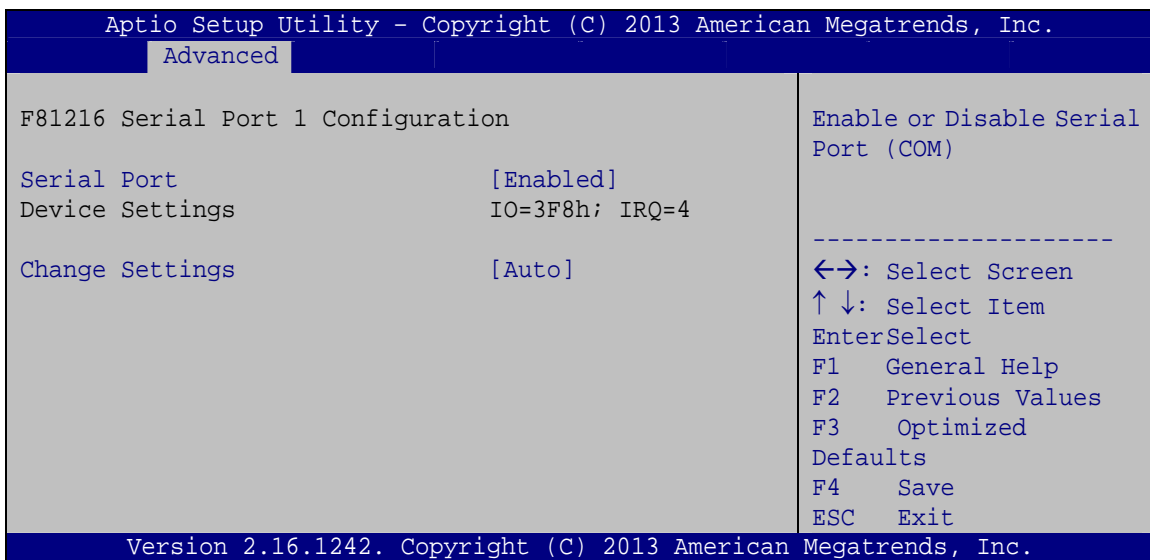
Use the **IT8528 Super IO Configuration** menu (**BIOS Menu 4**) to set or change the configurations for the serial ports.



**BIOS Menu 4: IT8528 Super IO Configuration**

#### 5.3.2.1 Serial Port 1 Configuration

Use the **Serial Port 1 Configuration** menu (**BIOS Menu 5**) to configure the serial port 1.



**BIOS Menu 5: Serial Port 1 Configuration Menu**

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled**                      Disable the serial port
- ➔ **Enabled**      **DEFAULT**      Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

- ➔ **Auto**                      **DEFAULT**              The serial port IO port address and interrupt address are automatically detected.
- ➔ **IO=3F8h; IRQ=4**                      Serial Port I/O port address is 3F8h and the interrupt address is IRQ4
- ➔ **IO=3F8h; IRQ=3, 4,5,6,7,9,10,11,12**                      Serial Port I/O port address is 3F8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12
- ➔ **IO=2F8h; IRQ=3, 4,5,6,7,9,10,11,12**                      Serial Port I/O port address is 2F8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12
- ➔ **IO=3E8h; IRQ=3, 4,5,6,7,9,10,11,12**                      Serial Port I/O port address is 3E8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12
- ➔ **IO=2E8h; IRQ=3, 4,5,6,7,9,10,11,12**                      Serial Port I/O port address is 2E8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12

**5.3.3 Hardware Monitor**

The Hardware Monitor menu (**BIOS Menu 6**) contains the fan configuration submenus and displays operating temperature, fan speeds and system voltages.

## HYPER-BT

```

Aptio Setup Utility - Copyright (C) 2013 American Megatrends, Inc.
  Advanced
PC Health Status
> Smart Fan Function
CPU temperature           :+42 C
CPU Fan Speed            :N/A
SOC_VCC                  :+0.774 V
V1.0S                    :+0.996 V
V1.35S                   :+1.348 V
V1.35_DDR3               :+1.324 V
-----
<->: Select Screen
↑ ↓: Select Item
EnterSelect
+ -  Change Opt.
F1   General Help
F2   Previous Values
F3   Optimized Defaults
F4   Save & Exit
ESC  Exit
Version 2.16.1242. Copyright (C) 2013 American Megatrends, Inc.

```

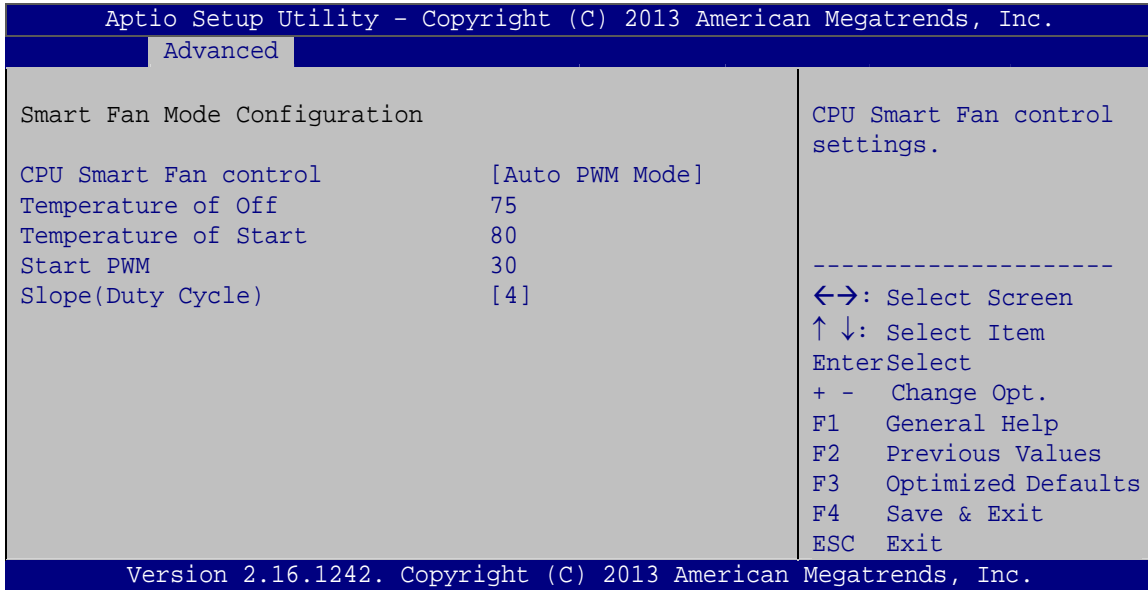
**BIOS Menu 6: Hardware Monitor****→ PC Health Status**

The following system parameters and values are shown. The system parameters that are monitored are:

- System Temperatures:
  - CPU Temperature
- Fan Speed:
  - CPU Fan Speed
- Voltages:
  - SOC\_VCC
  - V1.0S
  - V1.35S
  - V1.35\_DDR3

**5.3.3.1 Smart Fan Mode Configuration**

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 7**) to configure fan temperature and speed settings.



**BIOS Menu 7: Smart Fan Mode Configuration**

➔ **CPU Smart Fan control [Auto PWM Mode]**

Use the **CPU Smart Fan control** BIOS option to configure the CPU Smart Fan.

- ➔ **Full Mode** Fan is on all the time
- ➔ **Manual PWM Mode** The fan spins at the speed set in the manual PWM setting
- ➔ **Auto PWM Mode** **DEFAULT** The fan adjusts its speed using these settings:
  - Temperature of Off
  - Temperature of Start
  - Start PWM
  - Slope (Duty Cycle)



## HYPER-BT

### → Temperature of Off [75]

---



#### **WARNING:**

Setting this value too high may cause the fan to speed up only when the CPU is at a very high temperature and therefore cause the system to be damaged.

---

The **Temperature of Off** option can only be set if the **CPU Smart Fan control** option is set to **Auto Mode**. If the CPU temperature is lower than **Temperature of Off**, the fan speed change to be lowest. To set a value, select the **Temperature of Off** option and enter a decimal number between 0 and 127. The temperature range is specified below.

- Minimum Value: 0°C
- Maximum Value: 127°C

### → Temperature of Start [80]

---



#### **WARNING:**

Setting this value too high may cause the fan to rotate at full speed only when the CPU is at a very high temperature and therefore cause the system to be damaged.

---

The **Temperature of Start** option can only be set if the **CPU Smart Fan control** option is set to **Auto Mode**. If the CPU temperature is between **Temperature of Off** and **Temperature of Start**, the fan speed change to be **Start PWM**. To set a value, select the **Temperature of Start** option and enter a decimal number between 0 and 127. The temperature range is specified below.

- Minimum Value: 0°C
- Maximum Value: 127°C

→ **Start PWM [30]**

The **Start PWM** option can only be set if the **CPU Smart Fan control** option is set to **Auto Mode**. Use the **Start PWM** option to set the PWM start value. To set a value, select the **Start PWM** option and enter a decimal number between 0 and 100. The temperature range is specified below.

- Minimum Value: 0
- Maximum Value: 100

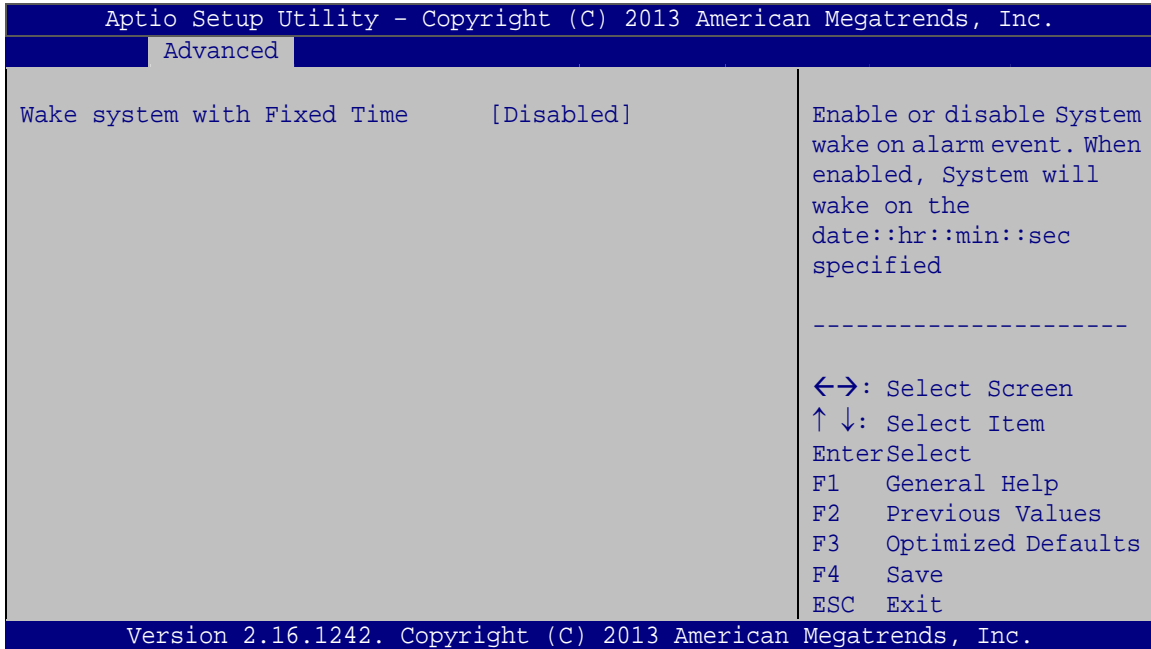
→ **Slope (Duty Cycle) [4]**

The **Slope (Duty Cycle)** option can only be set if the **CPU Smart Fan control** option is set to **Auto Mode**. Use the **Slope (Duty Cycle)** option to select the linear rate at which the PWM mode increases with respect to an increase in temperature. A list of available options is shown below:

- 0
- 1
- 2
- 4
- 8
- 16

### 5.3.4 RTC Wake Settings

The **RTC Wake Settings** menu (**BIOS Menu 8**) configures RTC wake event.



#### BIOS Menu 8: RTC Wake Settings

➔ **Wake system with Fixed Time [Disabled]**

Use the **Wake system with Fixed Time** option to enable or disable the system wake on alarm event.

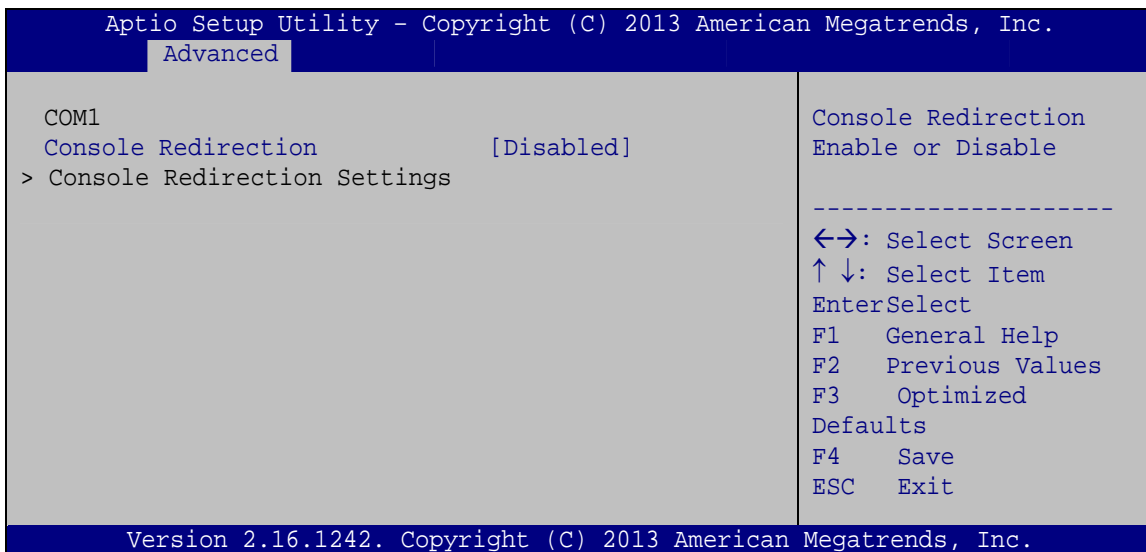
- ➔ **Disabled**      **DEFAULT**      The real time clock (RTC) cannot generate a wake event
  
- ➔ **Enabled**      If selected, the **Wake up every day** option appears allowing you to enable to disable the system to wake every day at the specified time. Besides, the following options appear with values that can be selected:
  - Wake up date
  - Wake up hour
  - Wake up minute

Wake up second

After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

### 5.3.5 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 9**) allows the console redirection options to be configured. Console redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



#### BIOS Menu 9: Serial Port Console Redirection

##### ➔ Console Redirection [Disabled]

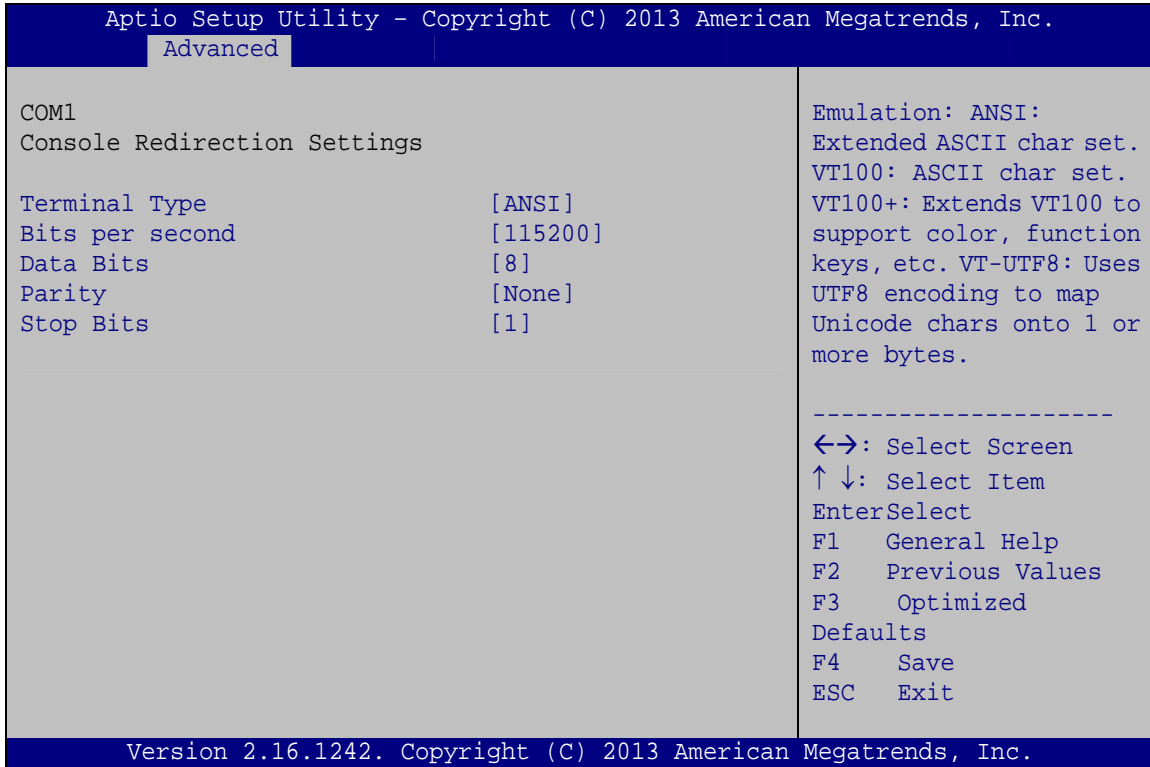
Use **Console Redirection** option to enable or disable the console redirection function.

- ➔ **Disabled**      **DEFAULT**      Disabled the console redirection function
- ➔ **Enabled**                      Enabled the console redirection function

#### 5.3.5.1 Console Redirection Settings

The **Console Redirection Settings** menu (**BIOS Menu 10**) allows the console redirection options to be configured. The option is active when Console Redirection option is enabled.

## HYPER-BT



### BIOS Menu 10: Console Redirection Settings

#### → Terminal Type [ANSI]

Use the **Terminal Type** option to specify the remote terminal type.

- **VT100**                      The target terminal type is VT100
- **VT100+**                    The target terminal type is VT100+
- **VT-UTF8**                    The target terminal type is VT-UTF8
- **ANSI**                      **DEFAULT**                    The target terminal type is ANSI

#### → Bits per second [115200]

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match the other side. Long or noisy lines may require lower speeds.

- **9600**                      Sets the serial port transmission speed at 9600.
- **19200**                      Sets the serial port transmission speed at 19200.

- **38400** Sets the serial port transmission speed at 38400.
- **57600** Sets the serial port transmission speed at 57600.
- **115200**      **DEFAULT** Sets the serial port transmission speed at 115200.

#### → Data Bits [8]

Use the **Data Bits** option to specify the number of data bits.

- **7** Sets the data bits at 7.
- **8**      **DEFAULT** Sets the data bits at 8.

#### → Parity [None]

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

- **None**      **DEFAULT** No parity bit is sent with the data bits.
- **Even** The parity bit is 0 if the number of ones in the data bits is even.
- **Odd** The parity bit is 0 if the number of ones in the data bits is odd.
- **Mark** The parity bit is always 1. This option does not provide error detection.
- **Space** The parity bit is always 0. This option does not provide error detection.

#### → Stop Bits [1]

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

- **1**      **DEFAULT** Sets the number of stop bits at 1.
- **2** Sets the number of stop bits at 2.

## HYPER-BT

### 5.3.6 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 11**) to view detailed CPU specifications and configure the CPU.

```

Aprio Setup Utility - Copyright (C) 2013 American Megatrends, Inc.
  Advanced
CPU Configuration
Intel(R) Celeron(R) CPU N2807 @ 1.58GHz
CPU Signature                30678
Microcode Patch              809
Max CPU Speed                 1580 MHz
Min CPU Speed                 500 MHz
Processor Cores               2
Intel HT Technology           Not Supported
Intel VT-x Technology         Supported

L1 Data Cache                 24 KB x 2
L1 Code Cache                 32 KB x 2
L2 Cache                      1024 KB x 1
L3 Cache                      Not Present
CPU Speed                     1584 MHz
64-bit                        Supported

Intel Virtualization Technology [Disabled]
EIST                           [Enabled]

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

-----
<->: Select Screen
^ v: Select Item
Enter>Select
F1   General Help
F2   Previous Values
F3   Optimized
Defaults
F4   Save
ESC  Exit

Version 2.16.1242. Copyright (C) 2013 American Megatrends, Inc.
  
```

#### BIOS Menu 11: CPU Configuration

##### ➔ Intel® Virtualization Technology [Disabled]

Use the **Intel® Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel Virtualization technology allows several OSs to run on the same system at the same time.

- ➔ **Disabled**      **DEFAULT**      Disables Intel Virtualization Technology.
- ➔ **Enabled**                      Enables Intel Virtualization Technology.

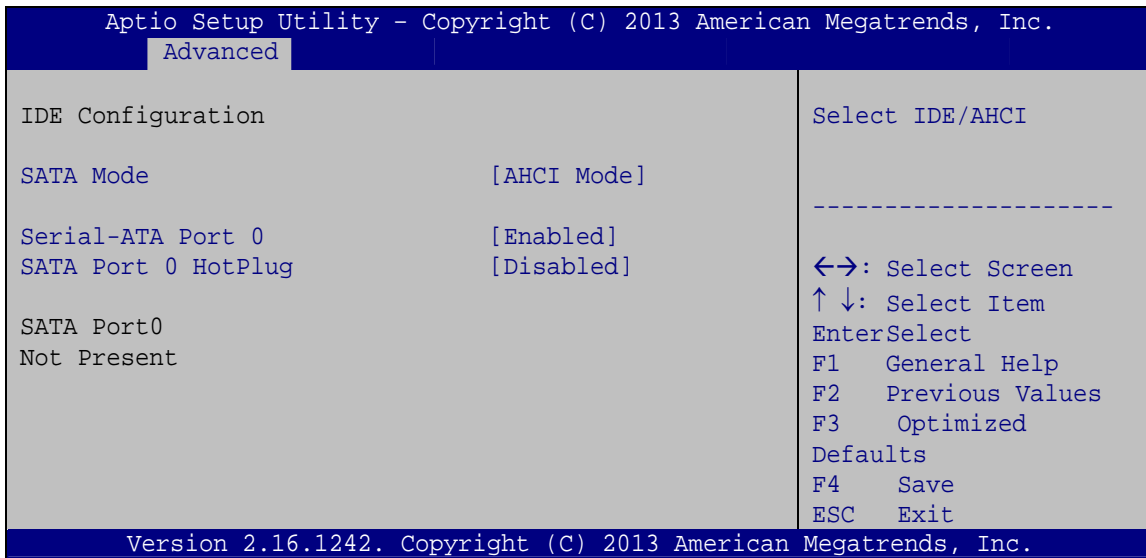
##### ➔ EIST [Enabled]

Use the **EIST** option to enable or disable the Intel Speed Step Technology.

- ➔ **Disabled**                      Disables the Intel Speed Step Technology.
- ➔ **Enabled**      **DEFAULT**      Enables the Intel Speed Step Technology.

### 5.3.7 IDE Configuration

Use the **IDE Configuration** menu (**BIOS Menu 12**) to change and/or set the configuration of the SATA devices installed in the system.



#### BIOS Menu 12: IDE Configuration

##### ➔ **SATA Mode [AHCI Mode]**

Use the **SATA Mode** option to configure SATA devices as normal IDE devices.

- ➔ **IDE Mode**                      Configures SATA devices as normal IDE device.
- ➔ **AHCI Mode**      **DEFAULT**      Configures SATA devices as AHCI device.

##### ➔ **Serial-ATA Port 0 [Enabled]**

Use the **Serial-ATA Port 0** option to enable or disable the SATA device.

- ➔ **Disabled**                      Disables the SATA device.
- ➔ **Enabled**                      **DEFAULT**      Enables the SATA device.



## HYPER-BT

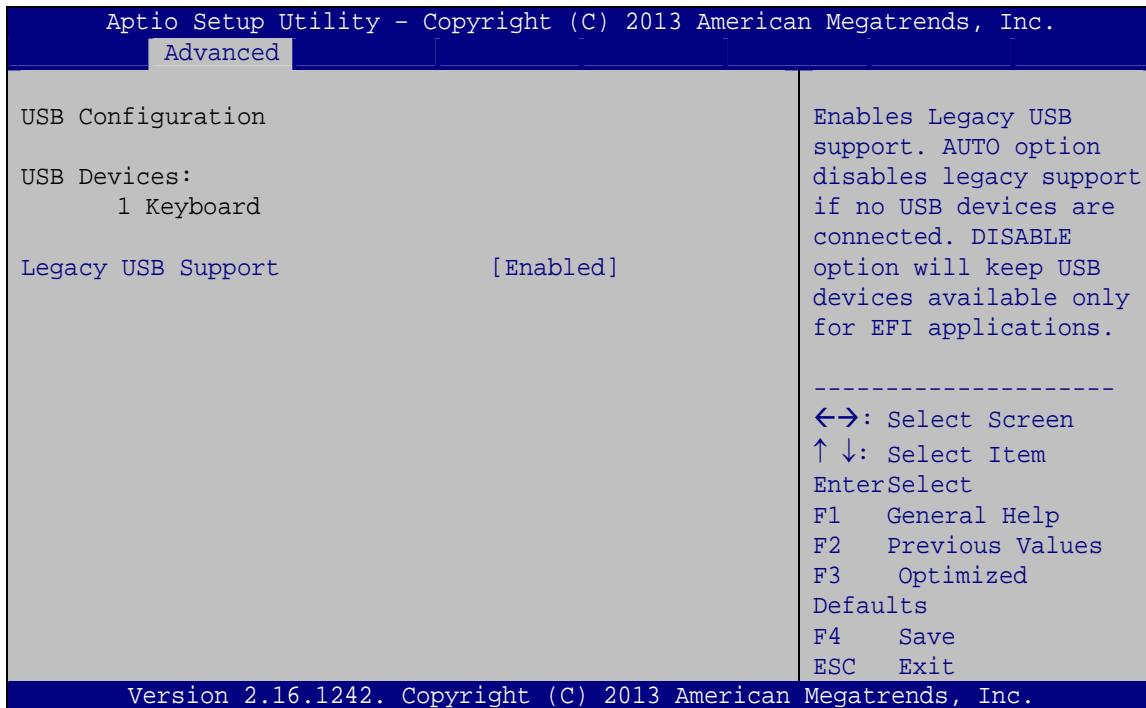
### → SATA Port 0 HotPlug [Disabled]

Use the **Serial-ATA Port 0 HotPlug** option to enable or disable the SATA device hot plug.

- **Disabled**      **DEFAULT**      Disables the SATA device hot plug.
- **Enabled**                      Enables the SATA device hot plug

## 5.3.8 USB Configuration

Use the **USB Configuration** menu (**BIOS Menu 13**) to read USB configuration information and configure the USB settings.



### BIOS Menu 13: USB Configuration

#### → USB Devices

The **USB Devices Enabled** field lists the USB devices that are enabled on the system

#### → Legacy USB Support [Enabled]

Use the **Legacy USB Support** BIOS option to enable USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard

does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.

- ➔ **Enabled**      **DEFAULT**      Legacy USB support enabled
- ➔ **Disabled**                      Legacy USB support disabled
- ➔ **Auto**                              Legacy USB support disabled if no USB devices are connected

## 5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 14**) to access the North Bridge and South Bridge configuration menus



### **WARNING!**

Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.

```

Aptio Setup Utility - Copyright (C) 2013 American Megatrends, Inc.
Main   Advanced  Chipset   Security  Boot   Save & Exit

> North Bridge
> South Bridge

North Bridge Parameters

-----
<=>: Select Screen
↑↓: Select Item
Enter>Select
+/-: Change Opt.
F1   General Help
F2   Previous Values
F3   Optimized Defaults
F4   Save & Exit
ESC  Exit

Version 2.16.1242. Copyright (C) 2013 American Megatrends, Inc.
    
```

**BIOS Menu 14: Chipset**

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### 5.4.1 North Bridge Configuration

Use the **North Bridge Configuration** menu (**BIOS Menu 15**) to configure the Intel IGD settings.

```

Aptio Setup Utility - Copyright (C) 2013 American Megatrends, Inc.
Chipset
> Intel IGD Configuration
Memory Information
Total Memory          4096 MB(LPDDR3)
Memory Slot0         4096 MB(LPDDR3)
Configure Intel IGD
Settings.

-----
<=>: Select Screen
↑ ↓: Select Item
EnterSelect
+/-: Change Opt.
F1:  General Help
F2:  Previous Values
F3:  Optimized Defaults
F4:  Save & Exit
ESC: Exit

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```

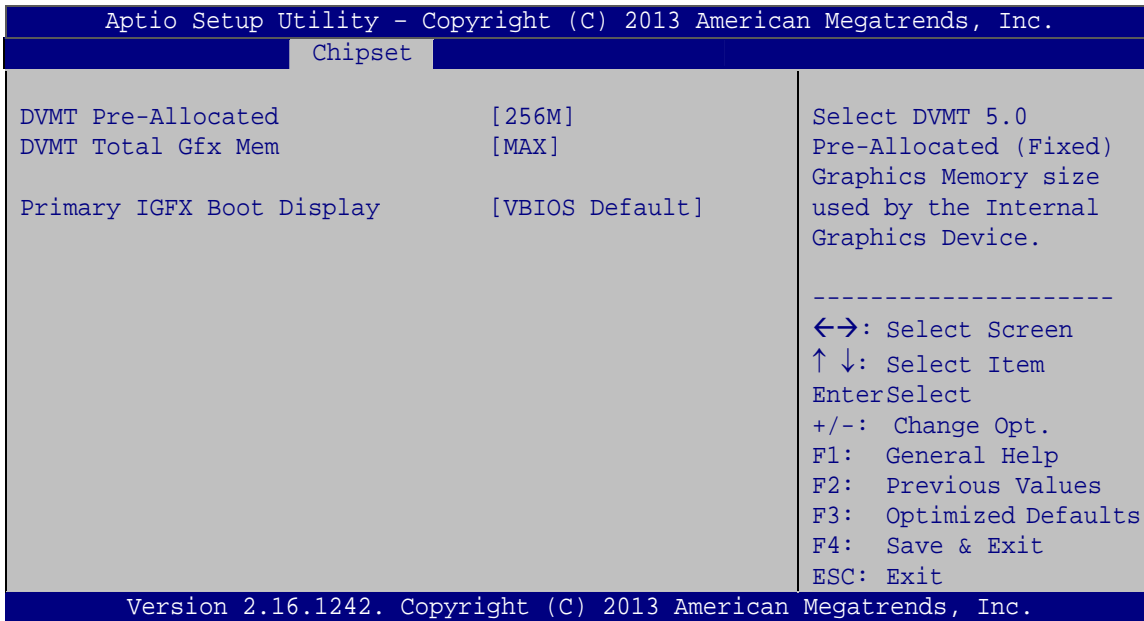
#### BIOS Menu 15: North Bridge Configuration

##### → Memory Information

The **Memory Information** lists a brief summary of the on-board memory. The fields in **Memory Information** cannot be changed.

#### 5.4.1.1 Intel IGD Configuration

Use the **Intel IGD Configuration** menu (**BIOS Menu 16**) to configure the video device connected to the system.



**BIOS Menu 16: Intel IGD Configuration**

➔ **DVMT Pre-Allocated [256MB]**

Use the **DVMT Pre-Allocated** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

- 64M
- 128M
- 256M                      **Default**
- 512M

➔ **DVMT Total Gfx Mem [MAX]**

Use the **DVMT Total Gfx Mem** option to select DVMT5.0 total graphic memory size used by the internal graphic device. The following options are available:

- 128M
- 256M
- MAX                         **Default**

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### → Primary IGFX Boot Display [VBIOS Default]

Use the **Primary IGFX Boot Display** option to select the display device used by the system when it boots. For dual display support, select “VBIOS Default.” Configuration options are listed below.

- VBIOS Default **DEFAULT**
- CRT
- DP Port

### 5.4.2 South Bridge Configuration

Use the **South Bridge Configuration** menu (**BIOS Menu 17**) to configure the south bridge chipset.

```

Aptio Setup Utility - Copyright (C) 2013 American Megatrends, Inc.
Chipset
Auto Power Button Status      [Enabled(AT)]      EUP Disable/Enable.
Power Saving(EUP)             [Disabled]
Audio Configuration
Audio Controller              [Enabled]
-----
<->: Select Screen
↑ ↓: Select Item
EnterSelect
+/-: Change Opt.
F1:  General Help
F2:  Previous Values
F3:  Optimized Defaults
F4:  Save & Exit
ESC: Exit
Version 2.16.1242. Copyright (C) 2013 American Megatrends, Inc.
  
```

#### BIOS Menu 17: South Bridge Configuration

### → Power Saving (EUP) [Disabled]

Use the **Power Saving (EUP)** option to enable or disable the power saving function.

- **Disabled**      **DEFAULT**      Power saving function is disabled.
- **Enabled**        Power saving function is enabled. It will reduce power consumption when the system is off.

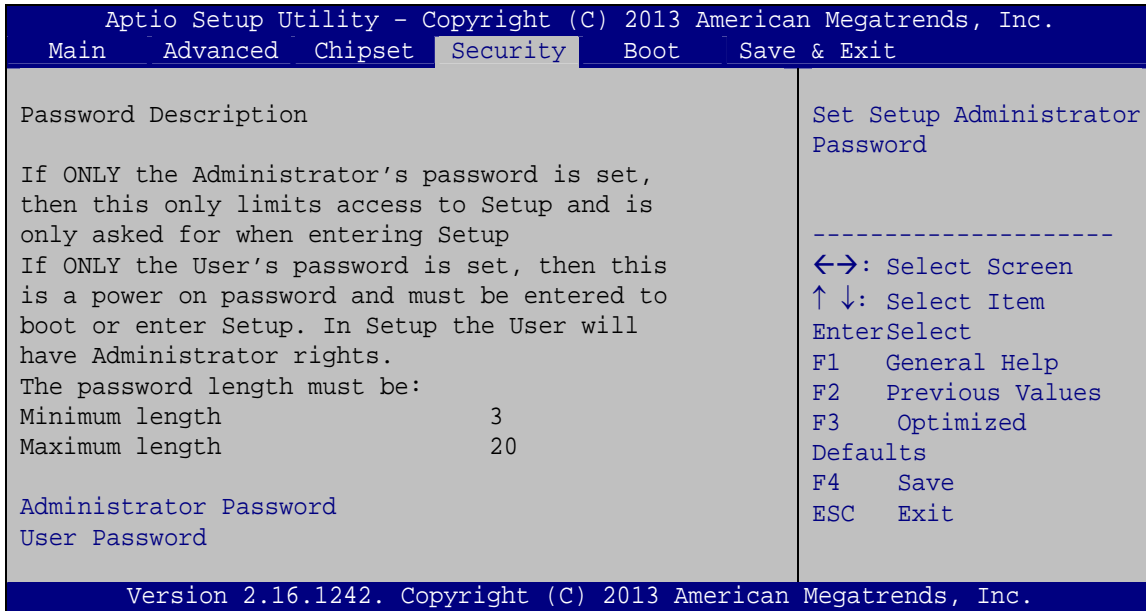
➔ **Audio Controller [Enabled]**

Use the **Audio Controller** option to enable or disable the High Definition Audio controller.

- ➔ **Disabled**                      The onboard High Definition Audio controller is disabled
- ➔ **Enabled    DEFAULT**        The onboard High Definition Audio controller is detected automatically and enabled

## 5.5 Security

Use the **Security** menu (**BIOS Menu 18**) to set system and user passwords.



**BIOS Menu 18: Security**

➔ **Administrator Password**

Use the **Administrator Password** to set or change a administrator password.

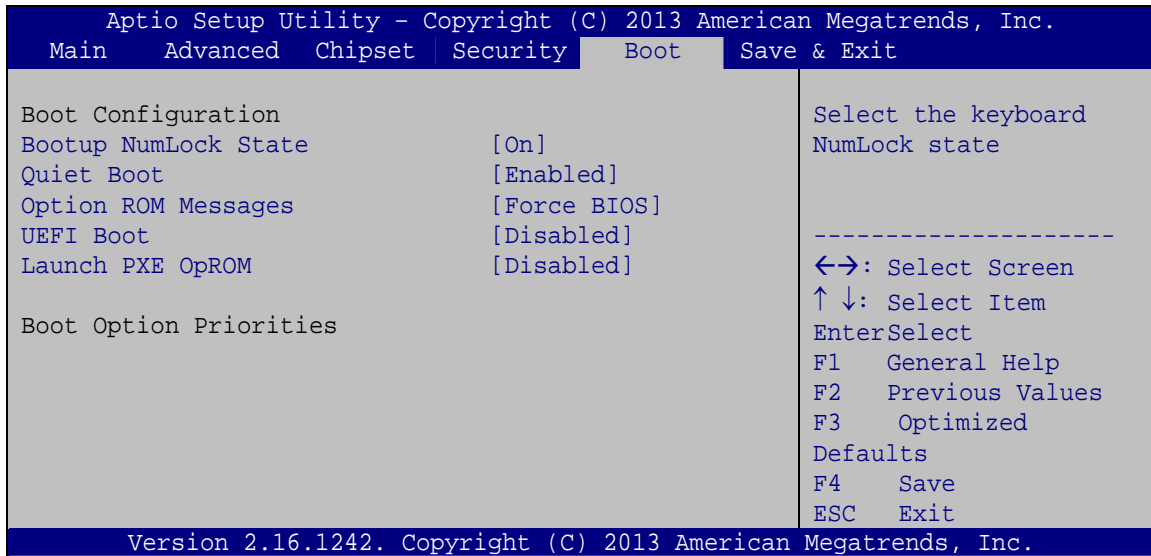
➔ **User Password**

Use the **User Password** to set or change a user password.

## HYPER-BT

### 5.6 Boot

Use the **Boot** menu (**BIOS Menu 19**) to configure system boot options.



#### BIOS Menu 19: Boot

##### → Bootup NumLock State [On]

Use the **Bootup NumLock State** BIOS option to specify if the number lock setting must be modified during boot up.

- **On**                      **DEFAULT**                      Allows the Number Lock on the keyboard to be enabled automatically when the computer system boots up. This allows the immediate use of the 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard is lit.
- **Off**                                      Does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard lights up when the Number Lock is engaged.

**→ Quiet Boot [Enabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

- **Disabled** Normal POST messages displayed
- **Enabled** **DEFAULT** OEM Logo displayed instead of POST messages

**→ Option ROM Messages [Force BIOS]**

Use the **Option ROM Messages** option to set the Option ROM display mode.

- **Force BIOS** **DEFAULT** Sets display mode to force BIOS.
- **Keep Current** Sets display mode to current.

**→ UEFI Boot [Disabled]**

Use the **UEFI Boot** option to enable or disable to boot from the UEFI devices.

- **Auto** If the first boot HDD is GPT then enable UEFI boot options, otherwise disable,
- **Enabled** Boot from UEFI devices is enabled.
- **Disabled** **DEFAULT** Boot from UEFI devices is disabled.

**→ Launch PXE OpROM [Disabled]**

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

- **Disabled** **DEFAULT** Ignore all PXE Option ROMs
- **Enabled** Load PXE Option ROMs.



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### → Boot Option Priority

Use the **Boot Option Priority** function to set the system boot sequence from the available devices. The drive sequence also depends on the boot sequence in the individual device section.

## 5.7 Exit

Use the **Exit** menu (**BIOS Menu 20**) to load default BIOS values, optimal failsafe values and to save configuration changes.

```

Aptio Setup Utility - Copyright (C) 2013 American Megatrends, Inc.
Main   Advanced   Chipset   Security   Boot   Save & Exit
-----
Save Changes and Reset
Discard Changes and Reset

Restore Defaults
Save as User Defaults
Restore User Defaults

-----
<=>: Select Screen
↑ ↓: Select Item
Enter>Select
F1   General Help
F2   Previous Values
F3   Optimized
Defaults
F4   Save
ESC  Exit

Version 2.16.1242. Copyright (C) 2013 American Megatrends, Inc.

```

### BIOS Menu 20: Exit

#### → Save Changes and Reset

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and to exit the BIOS configuration setup program.

#### → Discard Changes and Reset

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

**→ Restore Defaults**

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

**→ Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

**→ Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Appendix

**A**

# Regulatory Compliance

---

**DECLARATION OF CONFORMITY**

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

**FCC WARNING**

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

**B**

# BIOS Menu Options

---

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Appendix

**C**

# Terminology

---



**HYPER-BT**

AC '97	Audio Codec 97 (AC'97) refers to a codec standard developed by Intel® in 1997.
ACPI	Advanced Configuration and Power Interface (ACPI) is an OS-directed configuration, power management, and thermal management interface.
AHCI	Advanced Host Controller Interface (AHCI) is a SATA Host controller register-level interface.
ATA	The Advanced Technology Attachment (ATA) interface connects storage devices including hard disks and CD-ROM drives to a computer.
APM	The Advanced Power Management (APM) application program interface (API) enables the inclusion of power management in the BIOS.
ARMD	An ATAPI Removable Media Device (ARMD) is any ATAPI device that supports removable media, besides CD and DVD drives.
ASKIR	Amplitude Shift Keyed Infrared (ASKIR) is a form of modulation that represents a digital signal by varying the amplitude (“volume”) of the signal. A low amplitude signal represents a binary 0, while a high amplitude signal represents a binary 1.
BIOS	The Basic Input/Output System (BIOS) is firmware that is first run when the computer is turned on and can be configured by the end user
CODEC	The Compressor-Decompressor (CODEC) encodes and decodes digital audio data on the system.
CMOS	Complimentary metal-oxide-conductor is a type of integrated circuit used in chips like static RAM and microprocessors.
COM	COM is used to refer to serial ports. Serial ports offer serial communication to expansion devices. The serial port on a personal computer is usually a male DE-9 connector.
DAC	The Digital-to-Analog Converter (DAC) converts digital signals to analog

	signals.
DDR	Double Data Rate refers to a data bus transferring data on both the rising and falling edges of the clock signal.
DMA	Direct Memory Access (DMA) enables some peripheral devices to bypass the system processor and communicate directly with the system memory.
DIMM	Dual Inline Memory Modules are a type of RAM that offer a 64-bit data bus and have separate electrical contacts on each side of the module.
EHCI	The Enhanced Host Controller Interface (EHCI) specification is a register-level interface description for USB 2.0 Host Controllers.
GbE	Gigabit Ethernet (GbE) is an Ethernet version that transfers data at 1.0 Gbps and complies with the IEEE 802.3-2005 standard.
GPIO	General purpose input
IrDA	Infrared Data Association (IrDA) specify infrared data transmission protocols used to enable electronic devices to wirelessly communicate with each other.
L1 Cache	The Level 1 Cache (L1 Cache) is a small memory cache built into the system processor.
L2 Cache	The Level 2 Cache (L2 Cache) is an external processor memory cache.
LVDS	Low-voltage differential signaling (LVDS) is a dual-wire, high-speed differential electrical signaling system commonly used to connect LCD displays to a computer.
MAC	The Media Access Control (MAC) protocol enables several terminals or network nodes to communicate in a LAN, or other multipoint networks.
PCIe	PCI Express (PCIe) is a communications bus that uses dual data lines for full-duplex (two-way) serial (point-to-point) communications between the

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	<p>SBC components and/or expansion cards and the SBC chipsets. Each line has a 2.5 Gbps data transmission rate and a 250 MBps sustained data transfer rate.</p>
POST	<p>The Power-on Self Test (POST) is the pre-boot actions the system performs when the system is turned-on.</p>
QVGA	<p>Quarter Video Graphics Array (QVGA) refers to a display with a resolution of 320 x 240 pixels.</p>
RAM	<p>Random Access Memory (RAM) is a form of storage used in computer. RAM is volatile memory, so it loses its data when power is lost. RAM has very fast data transfer rates compared to other storage like hard drives.</p>
SATA	<p>Serial ATA (SATA) is a serial communications bus designed for data transfers between storage devices and the computer chipsets. The SATA bus has transfer speeds up to 1.5 Gbps and the SATA 3Gb/s bus has data transfer speeds of up to 3.0 Gbps.</p>
S.M.A.R.T	<p>Self Monitoring Analysis and Reporting Technology (S.M.A.R.T) refers to automatic status checking technology implemented on hard disk drives.</p>
UART	<p>Universal Asynchronous Receiver-transmitter (UART) is responsible for asynchronous communications on the system and manages the system's serial communication (COM) ports.</p>
UHCI	<p>The Universal Host Controller Interface (UHCI) specification is a register-level interface description for USB 1.1 Host Controllers.</p>
USB	<p>The Universal Serial Bus (USB) is an external bus standard for interfacing devices. USB 1.1 supports 12Mbps data transfer rates, while USB 2.0 supports 480Mbps data transfer rates.</p>
VGA	<p>The Video Graphics Array (VGA) is a graphics display system developed by IBM.</p>

Appendix

**D**

# Watchdog Timer

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**NOTE:**

The following discussion applies to DOS. Contact IEI support or visit the IEI website for drivers for other operating systems.

The Watchdog Timer is a hardware-based timer that attempts to restart the system when it stops working. The system may stop working because of external EMI or software bugs. The Watchdog Timer ensures that standalone systems like ATMs will automatically attempt to restart in the case of system problems.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

<b>AH – 6FH Sub-function:</b>	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

**Table D-1: AH-6FH Sub-function**

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

**NOTE:**

The Watchdog Timer is activated through software. The software application that activates the Watchdog Timer must also deactivate it when closed. If the Watchdog Timer is not deactivated, the system will automatically restart after the Timer has finished its countdown.

**EXAMPLE PROGRAM:**

```
; INITIAL TIMER PERIOD COUNTER
```

```
;
```

```
W_LOOP:
```

```
;
```

```
MOV      AX, 6F02H      ;setting the time-out value  
MOV      BL, 30         ;time-out value is 48 seconds  
INT      15H
```

```
;
```

```
; ADD THE APPLICATION PROGRAM HERE
```

```
;
```

```
CMP      EXIT_AP, 1     ;is the application over?  
JNE      W_LOOP        ;No, restart the application
```

```
MOV      AX, 6F02H      ;disable Watchdog Timer  
MOV      BL, 0         ;  
INT      15H
```

```
;
```

```
; EXIT ;
```

Appendix

**E**

# Hazardous Materials Disclosure

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## **E.1 Hazardous Material Disclosure Table for IPB Products Certified as RoHS Compliant Under 2002/95/EC Without Mercury**

The details provided in this appendix are to ensure that the product is compliant with the Peoples Republic of China (China) RoHS standards. The table below acknowledges the presences of small quantities of certain materials in the product, and is applicable to China RoHS only.

A label will be placed on each product to indicate the estimated “Environmentally Friendly Use Period” (EFUP). This is an estimate of the number of years that these substances would “not leak out or undergo abrupt change.” This product may contain replaceable sub-assemblies/components which have a shorter EFUP such as batteries and lamps. These components will be separately marked.

Please refer to the table on the next page.



## HYPER-BT

Part Name	Toxic or Hazardous Substances and Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
Housing	O	O	O	O	O	O
Display	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O
Battery	O	O	O	O	O	O
<p>O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in SJ/T11363-2006</p> <p>X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in SJ/T11363-2006</p>						

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有“环境友好使用期限”的标签，此期限是估算这些物质“不会有泄漏或突变”的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	○	○	○	○	○	○
显示	○	○	○	○	○	○
印刷电路板	○	○	○	○	○	○
金属螺帽	○	○	○	○	○	○
电缆组装	○	○	○	○	○	○
风扇组装	○	○	○	○	○	○
电力供应组装	○	○	○	○	○	○
电池	○	○	○	○	○	○

○: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11363-2006 标准规定的限量要求以下。  
 X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11363-2006 标准规定的限量要求。