

conga-PA3 Pico-ITX SBC

Detailed Description Of The congatec Pico-ITX Based On 3rd Generation Intel Atom

User's Guide

Revision 1.1

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes	
0.1	2015.10.30	AEM	Preliminary release	
1.0	2016.07.13	AEM	 Updated conga-PA3 product image Updated section 1.2.2 "Optional Accessories" and section 1.2.3 "Optional Cables" Corrected SPI flash size in section 2.1 "Feature List" Added sections 2.4 "Supply Voltage Power", 2.5 "Power Consumption" and 2.6 "Supply Voltage Battery Power" Updated section 4 "Cooling Solution" Added sections 8 "BIOS Setup Description" and 9 "Additional BIOS Features" Official release 	
1.1	2016.09.27	AEM	 Updated sections 1.2.3 "Optional Cables", 2.5 "Power Consumption" and 2.6.1 "CMOS Battery Power Consumption" Updated the note in section 5.1.1 "DC Power Jack (Rear I/O)" Updated the note in section 5.7.2 "LVDS" Deleted all references of USB client because this feature is no longer supported Added the changes in hardware revision B.x. 	

This user's guide provides information about the components, features and connectors available on the conga-PA3 Pico-ITX Single Board Computer.

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Describes the connector used on the Single Board Computer.

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Terminology

Term	Description
PCle	Peripheral Component Interface Express
cBC	congatec Board Controller
SDIO	Secure Digital Input Output
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial interface standard for hard disks
HDA	High Definition Audio
S/PDIF	Sony/Philips Digital Interconnect Format
HDMI	High Definition Multimedia Interface
TMDS	Transition Minimized Differential Signaling
DVI	Digital Visual Interface
LPC	Low Pin Count
I ² C Bus	Inter-Integrated Circuit Bus
SM Bus	System Management Bus
CAN	Controller Area Network
SPI	Serial Peripheral Interface
GbE	Gigabit Ethernet
LVDS	Low-Voltage Differential Signaling
DDC	Display Data Channel is an I ² C bus interface between a display and a graphics adapter.
PN	Part Number – the part number for placing orders.
N.C	Not connected
N.A	Not available
T.B.D	To be determined

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1 Introduction

1.1 Pico-ITX Concept

The Pico-ITX form factor provides system designers and manufacturers with a standardized ultra compact platform for development. With a footprint of 100mm x72mm, this scalable platform promotes the design of highly integrated, energy efficient systems. Due to its small size, the Pico-ITX form factor enables PC appliance designers not only to design attractive low cost devices but also allows them to explore a huge variety of product development options – from compact space-saving designs to fully functional Information Station and Value PC systems. This helps to reduce product design cycle and encourages rapid innovation in system design, to meet the ever-changing needs of the market.

Additionally, the boards can be passively cooled, presenting opportunities for fanless designs. The Pico-ITX boards are equipped with various interfaces such as PCI Express, SATA, USB 2.0/3.0, Ethernet, Displays and Audio.

1.2 conga-PA3

The conga-PA3 is a Single Board Computer designed based on the Pico-ITX specification. The conga-PA3 SBC features the Intel 3rd generation Atom processors. With maximum 10W TDP processors, the SBC offers Ultra Low Power boards with high computing performance and outstanding graphics. Additionally, the SBC supports onboard single channel DDR3L up to 1333 MT/s, maximum system memory capacity of 4 GB, multiple I/O interfaces, up to two independent displays and various congatec embedded features.

With smaller board size and lower height keep-out zones, the conga-PA3 SBC provides manufacturers and system designers with the opportunity to design compact systems for space restricted areas.

The various features and capabilities offered by the conga-PA3 makes it ideal for the design of compact, energy efficient, performanceoriented embedded systems.

1.2.1 Options Information

The conga-PA3 is currently available in four variants (two commercial and two industrial). The tables below show the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Part No.	047700	047701
Processor	Intel® Atom™ E3845 1.91 GHz Quad Core™	Intel® Atom™ E3826 1.46 GHz Dual Core™
L2 Cache	2 MByte	1 MByte
Burst Frequency	N.A	N.A
Onboard Memory	4GB DDRL-1333 MT/s single channel	2GB DDRL-1066 MT/s single channel
Processor Graphics	Intel [®] HD Graphics (GT1)	Intel [®] HD Graphics (GT1)
Graphics Base/Burst Freq.	542 / 792 MHz	533 / 667 MHz
LVDS	Single/Dual 18/24bit	Single/Dual 18/24bit
DDI	DisplayPort++	DisplayPort++
Processor TDP (Max)	10 W	7 W

Table 1 conga-PA3 Commercial Variants

Table 2conga-PA3 Industrial Variants

Part No.	047720	047721
Processor	Intel® Atom™ E3845 1.91 GHz Quad Core™	Intel® Atom™ E3826 1.46 GHz Dual Core™
L2 Cache	2 MByte	1 MByte
Burst Frequency	N.A	N.A
Onboard Memory	4GB DDRL-1333 MT/s single channel	2GB DDRL-1066 MT/s single channel
Processor Graphics	Intel [®] HD Graphics (GT1)	Intel [®] HD Graphics (GT1)
Graphics Base/Burst Freq.	542 / 792 MHz	533 / 667 MHz
LVDS	Single/Dual 18/24bit	Single/Dual 18/24bit
DDI	DisplayPort++	DisplayPort++
Processor TDP (Max)	10 W	7 W

1.2.2 Optional Accessories

Table 3 Accessories

Article	Part No.	Description
conga-PA3/HSP-B	047750	Standard conga-PA3 heatspreader with 3.2 mm bore hole stand-offs.
conga-PA3/CSP-B	047753	Passive cooling solution for conga-PA3. Includes standard conga-PA3 passive cooling solution with
		cooling fins and standard conga-PA3 heatspreader with 3.2 mm bore hore stand-offs.

1.2.3 Optional Cables

Table 4 Cables

Article	Part No.	Description
cab-Pico-ITX-Backlight	14000130	Backlight power cable to connect LCD panel AUO G170EG01 V.1 (Item# 10000132; Item name 17'' LVDS Panel G170EG01 V.1)
cab-Pico-ITX-Buttons-LED, 100cm	14000148	100cm buttons and LED cable.
cab-Pico-ITX-RS422	14000153	15cm RS422 cable adapter, DSUB9 Male.
cab-Pico-ITX-RS485	14000154	15cm RS485 cable adapter, DSUB9 Male.
cab-Pico-ITX-LVDS	14000167	LVDS data cable to connect LCD panel AUO G170EG01 V.1 (Item# 10000132; Item name 17'' LVDS Panel G170EG01 V.1)
cab-Pico-ITX-Power	14000172	15cm internal power cable for industrial versions.
Cable Kit	14000162	For the contents of the cable kit, see table 5 "Cable Kit" below.

Table 5 Cable Kit

Article	Part No.	Description
cab-Pico-ITX-USB20-Twin	14000123	20cm dual Type A USB 2.0 shielded high speed cable.
cab-Pico-ITX-Audio Cable Adapter	14000146	15cm audio Cable Adapter.
cab-Pico-ITX-Buttons-LED	14000147	30cm buttons and LED cable.
cab-Pico-ITX-GPIO	14000151	15cm GPIO cable with open end.
cab-Pico-ITX-RS232	14000152	15cm RS232 cable adapter, DSUB9 Male.
cab-Pico-ITX-External-Power	14000157	100cm external power cable with 4mm banana plugs (optimized to supply Pico-ITX from laboratory power source).
cab-Pico-ITX-Feature	14000161	15cm feature cable with open end.
cab-Pico-ITX-SATA-Power	14000190	SATA power cable.

2 Specification

2.1 Feature List

Table 6Feature Summary

Form Factor	Based on Pico-ITX form factor (100 x 72 mm)		
Processor	Intel [®] 3 rd Generation Atom SoC		
Memory	Single channel non-ECC DDR3L onboard memory with up to 4GB capacity a	nd up to 1333 MT/s	
cBC	Multi-stage watchdog, manufacturing and board information, board statistic	s, I2C bus, power loss control	
Chipset	Integrated in the SoC		
Audio	Realtek ALC888S-VD High Definition Audio codec		
Ethernet	1x Gigabit Ethernet support via the onboard Intel® I211 (industrial variants h	ave Intel [®] I210 controller)	
Graphics	Intel® HD Graphics with support for DirectX11, OpenGL 3.0, OpenCL 1.2, OpenGLES 2.0, full HW acceleration for decode/encode of MPEG2, H.264, MVC and dual simultaneous displays		
Graphic Interfaces	1x DD1 (DisplayPort++) and 1x LVDS		
Back Panel I/O Connectors	 1x DisplayPort ++ (DP++). Supports DP/DVI/HDMI (HDMI 1.4 or DVI possible via an external passive cable adapter) 	1x Gigabit Ethernet (without AMT) 2x USB 3.0 1x DC-IN (+12V)	
Onboard I/O Connectors	 1x LVDS 1x Backlight 1x Serial Port connector (bottom side). NOTE: The serial port on rev. B.x and later supports multi-protocol. 1 x MicroSD slot (bottom side) 2x SATA interfaces 1x Standard SATA II (3.0 Gb/s). 1x mini SATA II (shared with mini PCIe Slot) PCI Express interfaces 1x Half size mini PCIe Slot 1x Half size mini PCIe Slot (shared with mSATA) 	 1x MIPI-CSI 2.0 connector (revision A.x and later) 1x LINE OUT/SPDIF OUT/MIC connector (analog and digital audio) 1x Internal Power-IN (+12V) 1x RTC battery connector 1x Fan connector 2x USB 2.0 (internal connectors) 3x Feature connectors 1x GPIO connector (offers 4 GPIs and 4 GPOs via cBC) 1x I2C/Watchdog connector (via cBC) 1x Connector for power, reset, sleep and LID buttons, as well as power and SATA LEDs. 	
Other Features	Thermal and voltage monitoring RTC Battery congatec standard BIOS		
BIOS	AMI Aptio® UEFI 5.x firmware, 8 MB SPI flash with congatec embedded BIOS features		
Power Management	ACPI 4.0 compliant with battery support. Also supports Suspend to RAM (S3) Ultra low standby power consumption		

Note

Some of the features mentioned above are optional. Check the part number of your module and compare it to the options information list on page 11 to determine what options are available on your particular module.

2.2 Supported Operating Systems

The conga-PA3 supports the following operating systems.

- Microsoft[®] Windows[®] 10
- Microsoft[®] Windows[®] 7/8
- Microsoft® Windows® 7/8 Embedded Standard
- Windows Embedded Compact 7/2013 (WEC7/WEC2013)
- Linux

2.3 Mechanical Dimensions

- 100mm x 72mm
- 17mm height

2.4 Supply Voltage Power

• 12V DC ± 10%

2.5 Power Consumption

The power consumption values were measured using the following test setup:

- conga-PA3 SBC
- LCD monitor
- conga-PA3 cooling solution
- Windows 7 (64-bit)

Note

All peripherals were powered externally and therefore did not influence the measured values.

Table 7 Power States

System State	Description
S0: Minimum value	Sets the SBC to lowest frequency mode (LFM) with minimum core voltage during desktop idle. In this state, the CPU is stressed to its maximum frequency.
S0: Maximum value	Sets the SBC to highest frequency mode (HFM/Turbo Boost). In this state, the CPU is stressed to its maximum frequency.
S0: Peak value	Highest power spike during the measurement of "S0: Maximum value". This state shows the peak value over a short period of time (worst case power consumption value). Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.
\$3	SBC is powered by 12V.

Processor Information

The tables below provide additional information about the power consumption data for each of the conga-PA3 variants offered. The values are recorded at various operating mode.

Table 8conga-PA3 Intel® Atom™ E3845

Part No. 047700	Hardware Rev. B.1	Hardware Rev. B.1 / BIOS Rev. PAC1R009		
Max. Burst Frequency	N.A	N.A		
Memory Size	4GB onboard mer	4GB onboard memory		
Operating System	Windows 7 (64 bit	Windows 7 (64 bit)		
Power State	S0: Min	S0: Max	S0: Peak	\$3
Power consumption	0.33 A/ 3.97 W	0.70 A/ 8.39 W	1.04 A/ 12.48 W	0.08 A/ 0.95 W

Note

Same power consumption values for industrial variant with PN: 047720.

Table 9 conga-PA3 Intel[®] Atom[™] E3826

Part No. 047701	Hardware Rev. B.1	Hardware Rev. B.1 / BIOS Rev. PAC1R009		
Max. Burst Frequency	N.A	N.A		
Memory Size	4GB onboard men	4GB onboard memory		
Operating System	Windows 7 (64 bit)	Windows 7 (64 bit)		
Power State	S0: Min	S0: Max	S0: Peak	53
Power consumption	0.28 A/ 3.38 W	0.39 A/ 4.73 W	0.71 A/ 8.46 W	0.04 A/ 0.52 W

Note

Same power consumption values for industrial variant with PN: 047721.

2.6 Supply Voltage Battery Power

• Typical 3V DC

2.6.1 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	1.62 µA
20°C	3V DC	1.67 µA
70°C	3V DC	1.93 µA

Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage). The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec AG website at www.congatec.com.

⇒Note

Industrial variants with hardware revision A.x and earlier do not have the CMOS battery.

2.7 Environmental Specifications

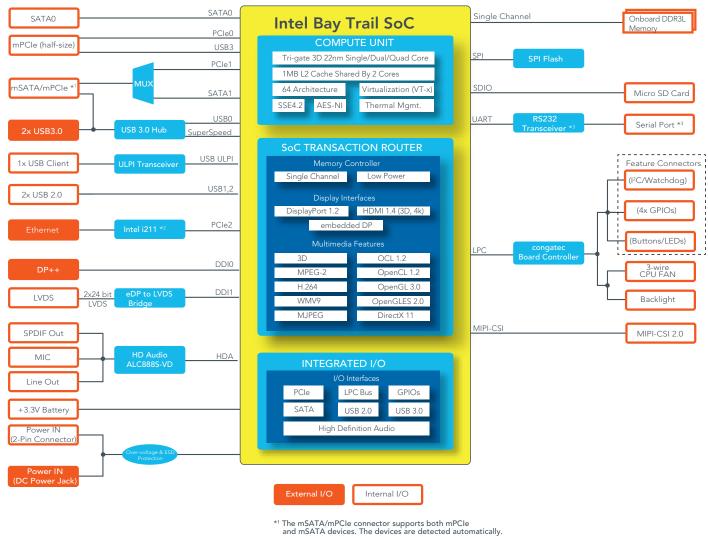
Temperature	Operation: 0° to 60°C (commercial variants)	Storage: -20° to +80°C
	Operation: -40° to 85°C (industrial variants)	Storage: -40° to +85°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%



The above operating temperatures must be strictly adhered to at all times.

The operating temperature range for industrial variants with LVDS interface is -25° to 85°C

3 Block Diagram



- *² Industrial variants are equipped with Intel i210 controller.
- *³ Revision B.x and later are equipped with a multiprotocol transceiver.

4 Cooling Solution

The conga-PA3 SBC offers Ultra Low Power boards with high computing performance and outstanding graphics. Due to its low power consumption, the SBC generates less heat and therefore requires less active cooling, allowing the use of quieter, lower profile coolers that are better suited to small form factor systems.

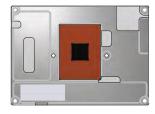
Nonetheless, all electronics contain semiconductor devices which have operating temperature ranges that should be adhered to. This means that for reliable operation, the thermal design of the conga-PA3 must be carefully considered. For this reason, it is imperative to provide sufficient air flow to each of the components, to ensure the specified operating temperature of the conga-PA3 is maintained.

congatec AG offers two cooling solutions for the conga-PA3:

- A congatec passive cooling solution (CSP).
- A congatec heatspreader. The heatspreader features a Gap Pad, heatstack and a Hi-Flow 225UT pressure sensitive, phase change thermal interface.



Passive Cooling Solution



Heatspreader

The dimensions of the cooling solutions are shown below. All measurements are in millimeters. To mount the system, follow the valid DIN/ISO specification.

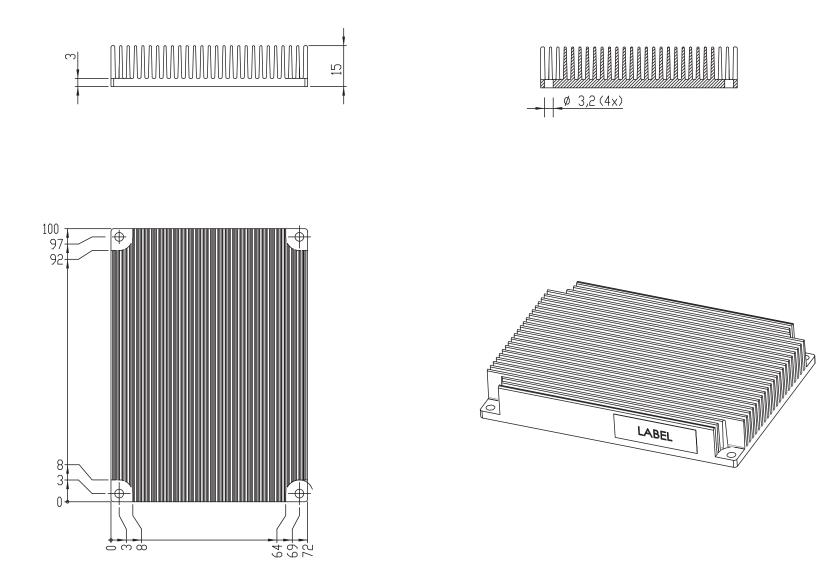
The maximum torque specification for all screws is 0.3 Nm. Higher torque may damage the SBC.

Note

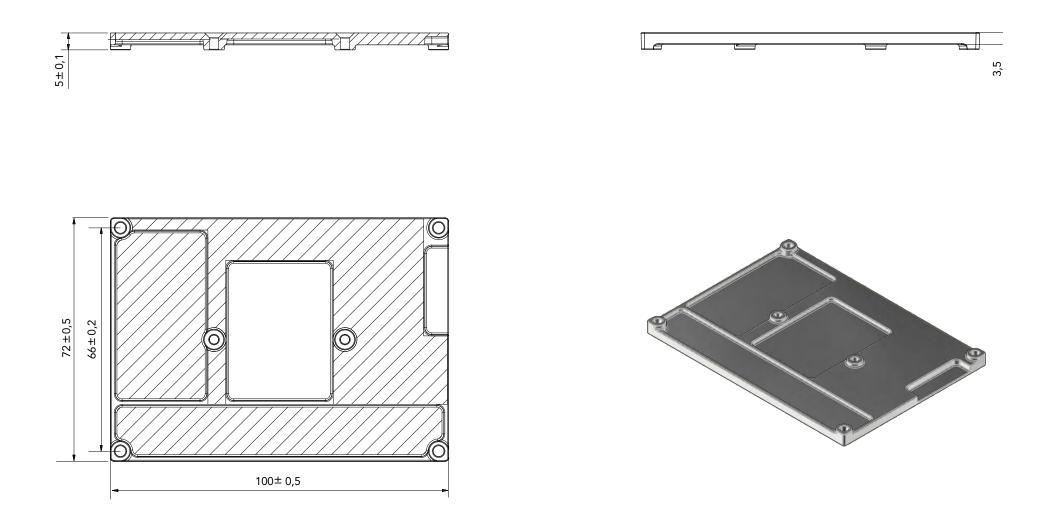
You can also use a custom cooling solution for the conga-PA3. When a passive cooling is used, the end user must ensure that adequate air flow is maintained.

See section 1.2.2 "Optional Accessories" for the part numbers of the cooling accessories. For the dimensions of the CSP and heatspreader, see sections 4.1 and 4.2.

4.1 CSP Dimension



4.2 Heatspreader Dimension





The gap pad material used on all congatec heatspreaders contains silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.



The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.

For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.

For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.

Also, do not exceed the maximum torque specified for the screws. Doing so may damage the module or/and the carrier board.

5 Connector Description

5.1 Power Supply

You can power the conga-PA3 SBC with a 12 V, 5.5 x 2.5 mm laptop type DC power supply (on connector X42) or with a 2-pin power supply (on connector X41).

Note

The supplied voltages must be within a tolerance of ± 10%. The conga-PA3 may not function if you exceed this tolerance limit.

5.1.1 DC Power Jack (Rear I/O)

The conga-PA3 SBC can be powered from a laptop type power supply connected to the DC power jack on the rear I/O. This power input offers over-voltage and ESD protection.

Table 10 Connector X42 Pinout Description

Pin	Function	
Center Pin	+12 V	
Sleeve/Barrel	GND	

Connector Type

X42 : DC power jack, 5.5 x 2.5 mm diameter

Note Note

Revision A.x and earlier conga-PA3 industrial variants do not have DC power jack (connector X42). They are equipped with internal power connector (X41) only.



The absolute maximum rating of the input voltage is 13.2 volts. Do not exceed this rating or expose the conga-PA3 to the absolute maximum voltage for a prolonged time. The system may not function, may be damaged or may have reliability issues if you do not observe this warning information.

PA3Cm11

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DC Power Jack - Connector X42



5.1.2 Power Supply (Internal Connector)

The conga-PA3 offers an internal 2-pin power connector. This connector makes it possible to use customized power supply cables/connector and also protects the input voltage from over-voltage.

Table 11 Connector X41 Pinout Description

Pin	Signal	Description
1	+12V	Power Supply +12 V
2	GND	Ground

Connector Type

X41: 2-pin, 3 mm pitch micro-fit internal power connector

Possible Mating Connector: Molex 43645-0200

Note

For conga-PA3 commercial variants, you can use connector X41 as a +12 V power output if the system is powered via the DC jack. The industrial variants have only connector X41 for power input.



The absolute maximum rating of the input voltage is 13.2 volts. Do not exceed this rating or expose the conga-PA3 to the absolute maximum voltage for a prolonged time. The system may not function, may be damaged or may have reliability issues if you do not observe this warning information.

5.1.3 Power Status LED

The conga-PA3 provides an LED signal (PWR_LED) on pin 9 of the feature connector X13. The signal indicates the different power states of the conga-PA3. Possible states of the LEDs are shown below:

PA3Cm11

Table 12Single-Color Power LED

LED State	Description	ACPI State
Off	Sleeping or power-off (not running)	S3, S5
LED on	Running	SO



Internal Power Connector X41



Note

For the feature connector pinout description, see section 6.1 "Feature Connectors".

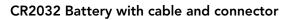
5.2 RTC Battery

The conga-PA3 provides an RTC battery on connector X10. The battery monitors and maintains the system clock. The specified battery type is CR2032.

Table 13	Battery Connector X10
----------	-----------------------

Pin	Description
1	+3 V
2	GND







Note

The CR2032 battery has an adhesive tape on its shrinking tube. This tape enables the system integrator to adequately position the battery in the system case. The industrial variants do not have this battery. Therefore, use suitable RTC battery solution for conga-PA3 industrial variants.



Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Connector Type

X10: 2 x 1, 1.25 mm PicoBlade header

Possible Mating Connector: Molex 51021-0200

5.3 Audio Interface

The conga-PA3 has a high definition audio codec (Realtek ALC888S-VD2) mounted on it. The audio codec's S/PDIF output, analog line (left and right) and microphone input channels (left and right) are routed to connector X5. This connector offers +5 V power supply pins for external speaker amplifier and optical S/PDIF transmitter.

The audio fuse limits the power budget of this pin by 750 mA hold current (maximum wattage recommended is 3 W).

Pin	Signal	Description
1	MIC_L	Analog Microphone Input – Left Channel
2	GND_HDA	Audio Ground
3	MIC_R	Analog Microphone Input – Right Channel
4	+5V AMP	+5V Power Supply (for external speaker amplifier)
5	MIC_JD	Microphone Jack Detection
6	LINE_R	Analog Line Out – Right Channel
7	GND_HDA	Audio Ground
8	LINE_L	Analog Line Out – Left Channel
9	LINE_JD	Line Out Jack Detection
10	+5V	+5V Power Supply (for S/PDIF optical transmitter)
11	GND	Digital Ground for S/PDIF
12	S/PDIF	S/PDIF Output (3.3V)

Table 14 Audio Interface (Connector X5) Pinout Description





Note

The audio codec is available on only commercial variants. The drivers for the codec can be found on the congatec website at www.congatec.com.

Connector Type

X5: 2 x 6 pin, 2.0 mm header

Possible Mating Connector: Molex 51110-1250

Universal Serial Bus (USB) 5.4

The conga-PA3 provides 4 USB ports – 2 USB 3.0 ports on the rear side and 2 USB 2.0 ports internally.

5.4.1 **Rear USB Connectors**

The conga-PA3 offers two USB 3.0 ports (connector X52) on the rear side. The USB 3.0 signals (Superspeed and USB 2.0 signals) are routed from the SoC to connector X52, via a USB 3.0 hub.

Table 15 USB 3.0 (Connectors X52) Pinout Description
--

Lov	ver Port		Up	per Port	
Pin	Signal	Description	Pin	Signal	Description
1	+5V	+5V supply	10	+5V	+5V supply
2	Data1-	Hi-speed differential transceiver (negative)	11	Data2-	Hi-speed differential transceiver (negative)
3	Data1+	Hi-speed differential transceiver (positive)	12	Data2+	Hi-speed differential transceiver (positive)
4	GND	Ground	13	GND	Ground
5	SS1_RX-	SuperSpeed receiver differential pair (negative)	14	SS2_RX-	SuperSpeed receiver differential pair (negative)
6	SS1_RX+	SuperSpeed receiver differential pair (positive)	15	SS2_RX+	SuperSpeed receiver differential pair (positive)
7	GND	Ground	16	GND	Ground
8	SS1_TX-	SuperSpeed transmitter differential pair negative)	17	SS2_TX-	SuperSpeed transmitter differential pair (negative)
9	SS1_TX+	SuperSpeed transmitter differential pair (positive)	18	SS2_TX+	SuperSpeed transmitter differential pair (positive)

Connector X52



Connector Type

X52: Dual-stacked USB 3.0 Type A connector

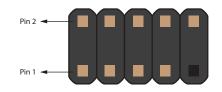
5.4.2 Internal USB Connectors

The conga-PA3 offers 2 internal USB 2.0 ports on connector X53. The USB signals are routed directly from the SoC.

Table 16	USB 2.0 Header (Connector X53) Pinout Description
----------	---

Port	t 1		Port	2	
Pin	Signal	Description	Pin	Signal	Description
1	+5V	+5V supply	2	+5V	+5V supply
3	Data1-	Hi-speed differential signal (negative)	4	Data2-	Hi-speed differential signal (negative)
5	Data1+	Hi-speed differential signal (positive)	6	Data2+	Hi-speed differential signal (positive)
7	GND	Ground	8	GND	Ground
9	No Pin	Кеу	10	NC	Not Connected

Internal USB 2.0 - Connector X53



Connector Type

X53: 2.54 mm, 2x5 pin header

Possible Mating Connector: Molex 51021-0400

5.5 Ethernet 10/100/1000

The conga-PA3 provides one Gigabit Ethernet port (connector X40) on the rear side. The Gigabit Ethernet interface is supported via the Intel Gigabit Ethernet controller i211. The controller does not support the Intel AMT feature.

Table 17 Connectors X40 Pinout Description

Pin	Description	10base-T	100Base-T	1000Base-T
1	Transmit Data+ or Bidirectional	TX+	TX+	BI_DA+
2	Transmit Data- or Bidirectional	TX-	TX-	BI_DA-
3	Receive Data+ or Bidirectional	RX+	RX+	BI_DB+
4	Not connected or Bidirectional	nc	nc	BI_DC+
5	Not connected or Bidirectional	nc	nc	BI_DC-
6	Receive Data- or Bidirectional	RX-	RX-	BI_DB+
7	Not connected or Bidirectional	nc	nc	BI_DD+
8	Not connected or Bidirectional	nc	nc	BI_DD-

Gigabit Ethernet - Connector X40



Table 18 LED Descriptions

LED Left Side	Description	LED Right Side	Description
Off	10 Mbps link speed	Off	No link
Green	100 Mbps link speed	Steady On	Link established, no activity detected
Orange	1000 Mbps link speed	Blinking	Link established, activity detected

Connector Type

X40: 8 pin RJ45 connector with Gigabit magnetic and LEDs

5.6 SATA Interfaces

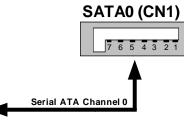
The conga-PA3 provides two SATA ports – a standard SATA port and a mini SATA port (shared with mini PCIe slot).

5.6.1 Standard SATA Port

The conga-PA3 provides one standard SATA port on connector CN1. This interface is routed directly from the SoC and supports data rates up to 3 GB/s. The SATA LED signal on the feature connector X13 indicates activity on the SATA interface.

Table 19Connector CN1 Pinout Description.

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND



Connector Type

CN1: Standard SATA connector

5.6.2 Mini SATA (shared with mini PCIe)

The mini SATA connector X9 on the conga-PA3 is used to connect mSATA devices or mini PCIe devices. When an mSATA or mPCIe device is connected to X9, the conga-PA3 automatically detects the type of device attached.

For pinout description, see section 5.10.2 "Mini PCIe (shared with mini SATA)".

Connector Type

X9: 0.8 mm pitch, 52 pin mini PCI socket



For card type recognition, pin 43 of the mSATA card must not be connected.

5.7 Display Interfaces

The conga-PA3 supports dual simultaneous displays – one Digital Display Interface and one LVDS interface.

5.7.1 Display Port Interface DP++

The conga-PA3 SBC has one DP++ connector (X3) located at the rear I/O panel. The display port supports DP, HDMI and DVI displays.

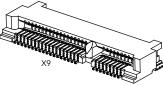
Table 20Connectors X3 Pinout Description.

Pin	Signal	Pin	Signal
1	DDI_TX0+	11	GND
2	GND	12	DDI_TX3-
3	DDI_TX0-	13	CONFIG1
4	DDI_TX1+	14	CONFIG2
5	GND	15	DDI_AUX+
6	DDI_TX1-	16	GND
7	DDI_TX2+	17	DDI_AUX-
8	GND	18	DDI_HPD
9	DDI_TX2-	19	GND
10	DDI_TX3+	20	3.3V

DP++ Connector X3







Connector Type

X3: 20 pin DisplayPort connector

5.7.2 LVDS

The conga-PA3 offers LVDS interface on connector X48 – a 40 pin LVDS connector. The LVDS signals are sourced from the SoC's eDP stream via an eDP to LVDS bridge IC. The eDP to LVDS bridge processes incoming DisplayPort stream and converts the DP protocol to LVDS, before transmitting the processed stream in LVDS format.

The LVDS interface is found on the top side of the SBC and supports 18 or 24 bit single/dual channel, selectable backlight voltage, VESA color mappings, automatic panel detection and resolution up to 1920 x 1200 at 60 Hz in dual LVDS mode.

Pin	Signal	Pin	Signal
1	GND	2	GND
3	LVDS_ODD_TX3P	4	LVDS_EVEN_TX3P
5	LVDS_ODD_TX3N	6	LVDS_EVEN_TX3N
7	GND	8	GND
9	LVDS_ODD_TX2P	10	LVDS_EVEN_TX2P
11	LVDS_ODD_TX2N	12	LVDS_EVEN_TX2N
13	GND	14	GND
15	LVDS_ODD_TX1P	16	LVDS_EVEN_TX1P
17	LVDS_ODD_TX1N	18	LVDS_EVEN_TX1N
19	GND	20	GND
21	LVDS_ODD_TX0P	22	LVDS_EVEN_TX0P
23	LVDS_ODD_TX0N	24	LVDS_EVEN_TX0N
25	GND	26	GND
27	LVDS_ODD_CLKP	28	LVDS_EVEN_CLKP
29	LVDS_ODD_CLKN	30	LVDS_EVEN_CLKN
31	GND	32	GND
33	DDC_CLK (3.3V)	34	DDC_DAT (3.3V)
35	+VCC_LVDS	36	+VCC_LVDS
37	+VCC_LVDS	38	GND
39	GND	40	LVDS_VDD_EN (3.3V)

Table 21 Connector X48 Pinout Description





Connector Type

X48: 1.25 mm, 40 pin Hirose connector (DF13 Series)

Possible Mating Connector: Hirose DF13-40DS-1.25C

• Note

congatec offers LVDS cable for only 17" AUO Optronics G170EG01 V.1 panel (see section 1.2.3 "Optional Cables"). For more information, contact congatec technical solution department.

• Note

- 1. Revision A.x and earlier support LVDS on only commercial variants.
- 2. Revision B.x and later support LVDS on both commercial and industrial variants.
- 3. Industrial variants that feature LVDS must operate within the temperature range of -25°C and 85°C.

5.7.2.1 Backlight Power Connector

The conga-PA3 provides backlight power on connector X2. The connector supports 5 V or 12 V backlight power. The backlight fuse limits the power budget of pins 1 and 5 by 1.5 A hold current.

Table 22 Connector X2 Pinout Description

Pin	Signal Name	Description
1	+12V BKLT_PWR	12V Backlight inverter power
2	GND	Ground
3	BKLT_EN (3.3V)	Backlight enable
4	BKLT_CTRL (3.3V)	Backlight control
5	+5V BKLT_PWR	5V Backlight inverter power

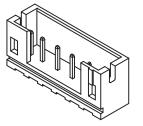
Connector Type

X2: 2 mm, 5 pin, JST connector (PH Series)

Possible Mating Connector: JST PHR-5



Backlight Power - Connector X2



⇒Note

Connector X2 is intended for LCD backlight power. If you use connector X2 for a different device, then the total output current should not exceed 2 A.

congatec offers backlight cable for 17" AUO Optronics G170EG01 V.1 panel only (see section 1.2.3 "Optional Cables"). For more information, contact congatec technical solution department.

5.7.2.2 Panel Power Selection

The conga-PA3 supports 3.3 V or 5 V LVDS panels. With jumper X54, you can set the panel voltage (pins 35 & 37 of connector X48) to 3.3 V or 5 V.

Table 23 Connector X54 Pinout Desc	cription
------------------------------------	----------

Pin	Signal Name
1	3.3V
2	Selected LCD Power
3	5V



Connector Type

X54: 2 mm, 3 pin header

5.8 Serial Ports (COM)

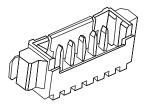
The conga-PA3 provides an RS-232 compliant UART interface on connector X16. The COM port is located at the bottom side of the SBC and can drive up to 250 kbit/s.

The conga-PA3 revision B.x and later support multi-protocol serial ports (RS232/RS422/RS485).

Pin	Signal	Description
1	COM1_GND	Ground
2	COM1_TXD	Transmit Data
3	COM1_RTS#	Request to Send
4	COM1_CTS#	Clear to Send
5	COM1_RXD	Received Data

Table 24 Serial Port – RS232 (Connector X16) Pinout Description

UART - Connector X16



Connector Type

X16: 1.25 mm pitch, 1 x 5 Molex PicoBlade pin header

Possible Mating Connector: Molex 51021-0500

Note

congatec offers an adapter cable for the COM port (see section 1.2.3 "Optional Cables). For more information, contact congatec technical solution department.

5.9 MIPI-CSI 2.0 (Camera)

The conga-PA3 provides a camera interface on connector X55. The interface supports up to two independent cameras – four data lanes for the first camera and one data lane for the second camera. Each lane operates at up to 1 GT/s depending on the camera resolution. The interfaces follow the MIPI Alliance CSI-2 specification and support up to 24 MP image capture @ 15 fps, full HD 1080p60, YUV420, YUV422, RGB444, RGB555, RGB565, RGB888, JPEG and RAW 8/10/12/14.

The table below shows the conga-PA3 MIPI-CSI 2.0 pinout description. The pinout and voltage levels comply with the SGET Camera Feature Specification.

Pin	Signal	Description	
1	CAM_PWR	3.3V +/- 5% supply voltage to power the camera device	
2	CAM_PWR	3.3V +/- 5% supply voltage to power the camera device	
3	CAM0_CSI_D0+	CSI2 Camera 0 Data Lane 0+	— MIPI-CSI 2.0
4	CAM0_CSI_D0-	CSI2 Camera 0 Data Lane 0-	(Connector X55)
5	GND		
6	CAM0_CSI_D1+	CSI2 Camera 0 Data Lane 1+	
7	CAM0_CSI_D1-	CSI2 Camera 0 Data Lane 1-	
8	GND		
9	CAM0_CSI_D2+	CSI2 Camera 0 Data Lane 2+	
10	CAM0_CSI_D2-	CSI2 Camera 0 Data Lane 2-	
11	CAM0_RST#	Camera 0 Reset (low active)	
12	CAM0_CSI_D3+	CSI2 Camera 0 Data Lane 3+	
13	CAM0_CSI_D3-	CSI2 Camera 0 Data Lane 3-	

Table 25 MIPI-CSI 2.0 (Connector X55) Pinout Description

14	GND	
15	CAM0_CSI_CLK+	CSI2 Camera 0 Differential Clock+ (Strobe)
16	CAM0_CSI_CLK-	CSI2 Camera 0 Differential Clock- (Strobe)
17	GND	
18	CAM0_I2C_CLK	Camera 0 Control Interface, CLK
19	CAM0_I2C_DAT	Camera 0 Control Interface, DATA
20	CAM0_ENA#	Camera 0 Enable (low active)
21	MCLK	Master Clock. May be used to drive camera's internal PLL (19.2MHz or 25MHz)
22	CAM1_ENA#	Camera 1 Enable (low active)
23	CAM1_I2C_CLK	Camera 1 Control Interface, CLK
24	CAM1_I2C_DAT	Camera 1 Control Interface, DATA
25	GND	
26	CAM1_CSI_CLK+	CSI2 Camera 1 Differential Clock+ (Strobe)
27	CAM1_CSI_CLK-	CSI2 Camera 1 Differential Clock- (Strobe)
28	GND	
29	CAM1_CSI_D0+	CSI2 Camera 1 Data Lane 0+
30	CAM1_CSI_D0-	CSI2 Camera 1 Data Lane 0-
31	CAM1_RST#	Camera 1 Reset (low active)
32	CAM1_CSI_D1+	N.C.
33	CAM1_CSI_D1-	N.C.
34	GND	
35	CAM0_GPIO	GPIO for Camera 0
36	CAM1_GPIO	GPIO for Camera 1

• Note

The MIPI interface fuse limits the power budget by 750 mA hold current.

5.10 PCI Express

The conga-PA3 provides two PCIe interfaces – a half-size mini PCIe (mPCIe) slot on connector X8 and a half-size mini PCIe/mini SATA slot on connector X9.

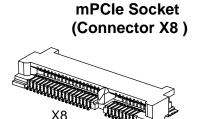
5.10.1 Mini PCIe (Half Size)

The conga-PA3 is equipped with a PCI Express Mini Card socket. The PCIe signals are routed directly from the SoC's PCIe lane 0 to connector X8. The connector supports only mini PCIe devices.

The table below lists the default pinout of the PCI Express Mini Card.

Table 26	mPCle (Connector X8) Pinout Description
----------	---

Pin	Signal	Pin	Signal
1	WAKE#	2	+3.3Vaux
3	N.C.	4	GND
5	N.C.	6	+1.5V
7	CLKREQ#	8	N.C.
9	GND	10	N.C.
11	REFCLK-	12	N.C.
13	REFCLK+	14	N.C.
15	GND	16	N.C.
17	N.C.	18	GND
19	N.C.	20	W_DISABLE#
21	GND	22	PERST#
23	PERn0	24	+3.3Vaux
25	PERp0	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	РЕТр0	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3Vaux	40	GND



Pin	Signal	Pin	Signal
41	+3.3Vaux	42	N.C
43	mSATA_mPCIe_detect	44	LED_WLAN#
45	N.C.	46	N.C
47	N.C.	48	+1.5V
49	N.C.	50	GND
51	N.C.	52	+3.3Vaux

Note

Pin 43 of the mPCIe card must be terminated to ground for card type recognition.

Connector Type

X8: PCIe mini card socket

5.10.2 Mini PCIe (shared with mini SATA)

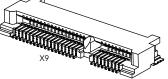
The conga-PA3 offers a mini PCIe slot on connector X9. This connector supports both mPCIe and mSATA devices. The PCIe and SATA signals are routed from the SoC to connector X9 (mPCIe/mSATA slot), via a multiplexer. The multiplexer switches the incoming signals based on the type of card inserted.

When an mPCIe or mSATA device is attached to the mPCIe/mSATA slot (connector X9), the multiplexer detects the connected device via the signal detect pin (pin 43) and sends the corresponding signals to connector X9.

Table 27 mPCle (Connector X9) Pinout Description

Pin	Signal	Pin	Signal
1	WAKE#	2	+3.3Vaux
3	N.C.	4	GND
5	N.C.	6	+1.5V
7	CLKREQ#	8	N.C.
9	GND	10	N.C.
11	REFCLK-	12	N.C.
13	REFCLK+	14	N.C.
15	GND	16	N.C.
17	N.C.	18	GND





Pin	Signal	Pin	Signal
19	N.C.	20	W_DISABLE#
21	GND	22	PERST#
23	PERn0/SATA_RX1-	24	+3.3Vaux
25	PERp0/SATA_RX1+	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0/SATA_TX1-	32	SMB_DATA
33	PETp0/SATA_TX1+	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3Vaux	40	GND
41	+3.3Vaux	42	N.C
43	mSATA_mPCIe_detect	44	N.C
45	CL_CLK	46	N.C
47	CL_DATA	48	+1.5V
49	CL_RST#	50	GND
51	N.C.	52	+3.3Vaux
53	GND	54	GND



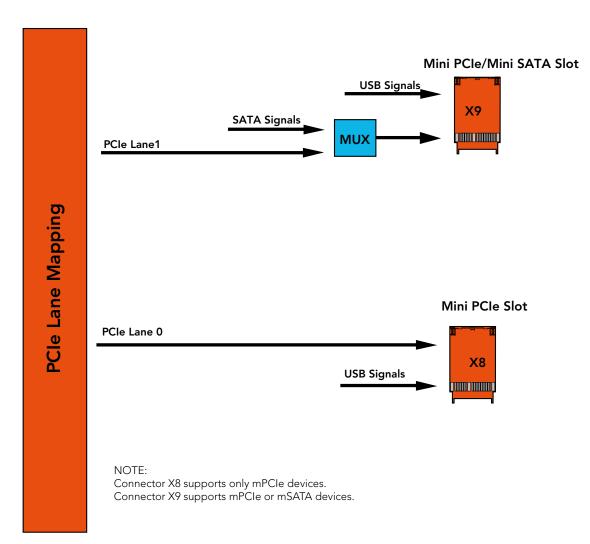
X9: PCIe mini card socket



For the conga-PA3 to detect the type of card inserted as described in the mPCIe/mSATA specification, pin 43 of the mPCIe card must be connected to ground. On mSATA card, this pin must not be connected.

5.10.3 PCI Express Routing

The diagram below shows how the PCIe lanes are routed to the PCIe connectors.



6 Additional Features

6.1 Feature Connectors

The conga-PA3 has three feature connectors (X13, X15 and X33) onboard. The SBC supports front panel features such as power button, status LEDs, I2C, watchdog, GPIOs via these connectors.

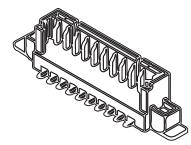
6.1.1 Buttons & LEDs

The conga-PA3 offers Lid, sleep, reset, power buttons as well as LED signals via the feature connector X13. The pinout is described below:

Table 28	Feature Connector X13 Pinout Description
----------	--

Signal Name	
LID_BTN#	
GND	
SLP_BTN#	
GND	
RST_BTN#	
GND	
PWR_BTN#	
GND	
PWR_LED (anode)	
GND (cathode)	
SATA_LED (anode)	
SATA_ACT# (cathode)	

Feature Connector X13



Connector Type

X13: 1.25 mm pitch, 12 x 1 pin PicoBlade header

Possible Mating Connector: Molex 51021-1200

• Note

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The LEDs on the conga-PA3 have series resistors. Therefore, you can connect X13 pins directly to the LED terminals.

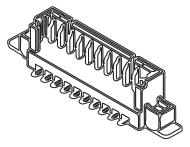
6.1.2 GPIOs

The conga-PA3 offers GPIOs via the feature connector X15. The pinout is described below:

Table 29	Feature Connector X15 Pinout Description
----------	--

Pin	Signal Name
1	GPIO
2	GPI1
3	GPI2
4	GPI3
5	GND
6	GPO0
7	GPO1
8	GPO2
9	GPO3
10	+3.3V

Feature Connector X15



Connector Type

X15: 1.25 mm pitch, 10 x 1 pin PicoBlade header

Possible Mating Connector: Molex 51021-1000



The signals are 3.3 V compatible.

The fuse limits the power budget of connectors X15 and X33 by 350 mA hold current.

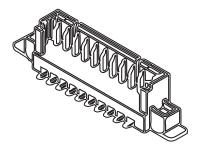
6.1.3 I2C and Watchdog

The conga-PA3 offers I2C and watchdog signals via the feature connector X33. The pinout is described below:

Table 30	Feature Connector X33 Pinout Description
----------	--

Pin	Signal Name
1	BATLOW#
2	+3.3V
3	N.C. *
4	I2C_CLK
5	I2C_DAT
6	GN D
7	WDTRIG#
8	WDOUT

Feature Connector X33



Connector Type

X33: 1.25 mm Pitch, 8 x1 pin PicoBlade header

Possible Mating Connector: Molex 51021-0800

Note

The signals are 3.3 V compatible.

The fuse limits the power budget of connector X15 and X33 by 350 mA hold current.

* On revision B.x and later, pin 3 is connected to LED_WLAN# (cathode).

6.2 congatec Board Controller (cBC)

The conga-PA3 is equipped with a Texas Instruments microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. The cBC fully isolates some of the embedded features such as system monitoring, I²C bus from the x86 core architecture. This improves performance and reliability, even during low power mode.

6.2.1 Fan Control

The congatec Board Controller on the conga-PA3 controls the power supplied to the fan with the PWM signal. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan is recommended.

6.2.2 Power Loss Control

The cBC controls the power-up of the SBC and can be used to specify how the system behaves after an AC power loss occurs. Supported modes are "Turn On", "Remain Off" and "Last State".

6.2.3 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.2.4 CPU Fan Connector

The conga-PA3 supports the connection of 12V cooling fans. The signals of the CPU fan are routed to connector X49. The pinout is described below:

Table 31	CPU Fan	Connector	(X49)	Pinout Description
----------	---------	-----------	-------	---------------------------

Pin	Signal
1	GND
2	+12VDC
3	FAN_TACHOIN

Connector Type

X49: 2.54 mm, 3 pin fan connector

Note

The recommended maximum power of the system fan is approximately 3 W.



6.3 OEM BIOS Customization

The conga-PA3 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide, which is called CGUTLm1x.pdf and can be found on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

6.3.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.3.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.3.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.3.4 OEM BIOS Code/Data

With the congatec embedded BIOS, system designers can add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the operating system loader.

Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table (OA2.0), Windows 8 OEM activation (OA3.0), verb tables for HDA codecs, PCI/PCIe opROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

6.3.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.4 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec AG defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addition to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-PA3 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery-only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about this subject, visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM³ User's Guide

6.5 API Support (CGOS)

congatec provides an API that allows application software developers to easily integrate all the features described above into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. For more information, see section 1.1 of the CGOS API software developers guide, available on the congatec website.

6.6 GPIOs

The conga-PA3 SBC provides four GPIs and four GPOs via the congatec board controller. The GPI/GPO signals are routed to the feature connector X15.

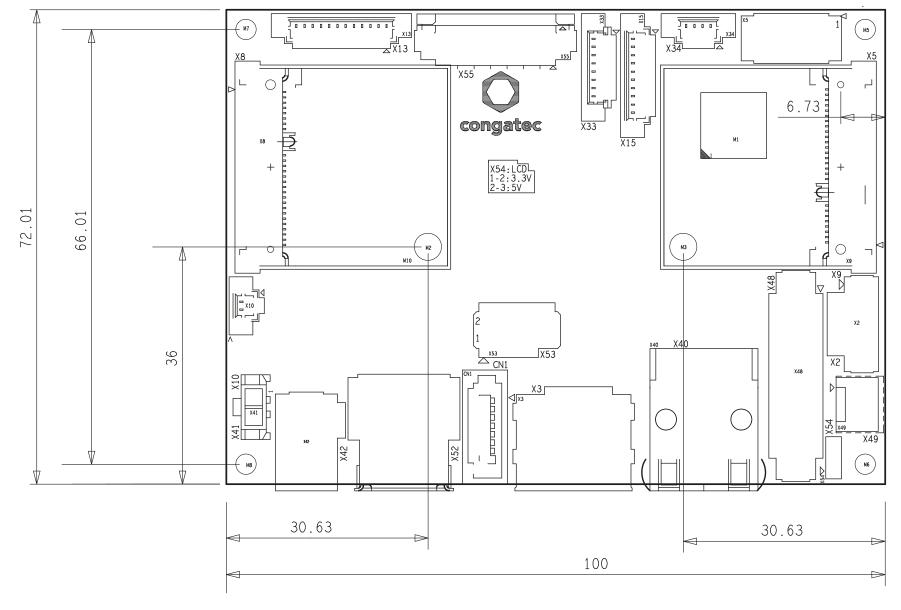
6.7 Thermal/Voltage Monitoring

The CPU onboard the conga-PA3 monitors the system temperature while the congatec Board Controller monitors the +12V input voltage and input current..

6.8 External System Wake Event

The conga-PA3 supports LAN, power/sleep/LID buttons and PCIe driven wake up events.

7 Mechanical Drawing



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8 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

8.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the or <F2> key during POST.

8.1.1 Boot Selection Popup

Press the <F11> key during POST to access the Boot Selection Popup menu. A selection menu displays immediately after POST, allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

8.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar, left frame and right frame. The menu bar is shown below:

Main	Advanced	Chipset	Boot	Security	Save & Exit
------	----------	---------	------	----------	-------------

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Кеу	Description	
←→ Left/Right	Select a setup menu (e.g. Main, Boot, Exit).	
↑ ↓ Up/Down	Select a setup item or sub menu.	
+ - Plus/Minus	Change the field value of a particular setup item.	
Tab	Select setup fields (e.g. in date and time).	
F1	Display General Help screen.	
F2	Load previous settings.	
F9	Load optimal default settings.	
F10	Save changes and exit setup.	
ESC	Discard changes and exit setup.	
ENTER	Display options of a particular setup item or enter submenu.	

8.3 Main Setup Screen

When you first enter the BIOS setup, you will see the main setup screen. The main setup screen reports BIOS, processor, memory and board information and is for configuring the system date and time. You can always return to the main setup screen by selecting the 'Main' tab.

Feature	Options	Description
Main BIOS Version	No option	Displays the main BIOS version.
OEM BIOS Version	No option	Displays the additional OEM BIOS version.
Build Date	No option	Displays the date the BIOS was built.
Product Revision	No option	Displays the hardware revision of the board.
Serial Number	No option	Displays the serial number of the board.
BC Firmware Revision	No option	Displays the firmware revision of the congatec board controller.
MAC Address	No option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	No option	Displays the number of boot-ups. (maximum 16777215).
Microcode Patch	No option	Displays the microcode patch loaded for the onboard CPU.
Baytrail SoC	No option	Displays B3 Stepping.
Total Memory	No option	Total amount of low voltage DDR3 present on the system.
System Date	Day of week, month/day/year	Specifies the current system date. Note: The date is in month/day/year format.
System Time	Hour:Minute:Second	Specifies the current system time. Note: The time is in 24 hour format.

8.4 Advanced Setup

Select the advanced tab from the setup menu to enter the advanced BIOS setup screen. The menu is used for setting advanced features and only features described within this user's guide are listed.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Watchdog				
	Graphics				
	Hardware Health Monitoring				
	Trusted Computing				
	RTC Wake				
	Module Serial Ports				
	Reserve Legacy Interrupt				
	ACPI				
	Super IO				
	Intel [®] Smart Connect Technology				
	Serial Port Console Redirection				
	CPU Configuration				
	PPM Configuration				
	Thermal Configuration				
	IDE Configuration				
	Miscellaneous Configuration				
	SCC Configuration				
	PCI Subsystem Settings				
	Network Stack				
	CSM Configuration				
	SDIO				
	USB				
	Platform Trust Technology				
	Security Configuration				
	Intel [®] I210 Gigabit Network				
	Driver Health				

8.4.1 Watchdog Submenu

Feature Options Desc		scription	
POST Watchdog	Disabled 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the system POST and provides a facility to prevent errors during boot up by performing a reset.	
Stop Watchdog for User Interaction	No Yes	Select whether the POST watchdog should be stopped during the popup of the boot selection menu or while waiting for setup password insertion.	
Runtime Watchdog	Disabled One-time Trigger Single Event Repeated Event	Select the operating mode of the runtime watchdog: 'One-time Trigger' – Disables watchdog after first trigger. 'Single Event' – Executes every stage only once before the watchdog is disabled. 'Repeated Event' – Executes last stage repeatedly until reset. Note: This watchdog will be initialized just before the operating system starts booting.	
Delay	Disabled 10sec 30sec 1min 2min 5min 10min 30min	Select delay time before runtime watchdog is activated. This ensures that the operating system has enough time to load.	
Event 1	ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 1 is reached.	
Event 2	Disabled ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 2 is reached.	
Event 3	Disabled ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 3 is reached.	

Feature	Options	Description	
Timeout 1	1sec	Select the timeout value for the first stage watchdog event.	
	2sec		
	5sec		
	10sec		
	30sec		
	1min		
	2min		
	5min		
	10min		
	30min		
Timeout 2	See above	Select the timeout value for the second stage watchdog event.	
Timeout 3	See above	Select the timeout value for the third stage watchdog event.	
Watchdog ACPI Event	Shutdown Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.	

Note Note

In ACPI mode, the 'Watchdog ACPI Event' handler cannot directly restart or shutdown the OS. For this reason, the congatec BIOS

For Shutdown: Executes an over-temperature notification. With this notification, the operating system shuts down in properly.

For Restart: Reports an ACPI fatal error to the operating system.

Additionally, the conga-PA3 module does not support the watchdog NMI mode because COM Express type 6 modules do not have the PCI_SERR# signal. Without this signal, there is no way to drive an NMI to the processor.

8.4.2 Graphics Submenu

Feature	Options	Description
Boot Display Device	VBIOS Default	· ·
CRT	Enabled Disabled	Enable or disable the CRT video interface.
Active LFP	No LVDS LVDS	Set 'Active LFP' configuration.
Always Try Auto Panel Detect	No Yes	If set to 'Yes', BIOS uses the EDID™ data set in an external EEPROM to configure the LFP. In case it cannot be found, the data set selected under 'Local Flat Panel Type' is used.
Local Flat Panel Type	AutoVGA 640x480 1x18 (002h)VGA 640x480 1x18 (013h)WVGA 800x480 1x24 (01Bh)SVGA 800x600 1x18 (01Ah)XGA 1024x768 1x18 (006h)XGA 1024x768 1x24 (008h)XGA 1024x768 2x24 (012h)WXGA 1280x768 1x24 (01Ch)SXGA 1280x1024 2x24 (00Ah)SXGA 1600x1200 2x24 (00Ch)HD 1920x1080 2x24 (01Ch)WUXGA 1920x1200 2x18 (015h)WUXGA 1920x1200 2x24 (00Ch)HD 1920x1080 2x24 (00Ch)HD 1920x1080 2x24 (00Ch)UXGA 1920x1200 2x24 (00Ch)Customized EDID™ 1Customized EDID™ 3	Select a predefined LFP type or choose 'Auto' to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID™ data set via the video I ² C bus. The number in brackets specifies the congatec internal number of the respective panel data set. Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.
Backlight Inverter Type	None PWM I2C	Select the type of backlight inverter: 'PWM' – IGD PWM signal. 'I2C' – I2C backlight inverter device connected to the video I²C bus.
Digital Display Interface 1 (DDI1)	Disabled DisplayPort HDMI/DVI Auto	Select the output type of the DDI.
PWM Inverter Frequency (Hz)	200 – 40000	Set the PWM inverter frequency in Hz. Note: This feature is only visible if the 'Backlight Inverter Type' is set to 'PWM'.
PWM Inverter Polarity	Normal Inverted	Select the PWM inverter polarity. Note: This feature is only visible if the 'Backlight Inverter Type' is set to 'PWM'.

Feature	Options	Description
Backlight Setting	0% 10% 25% 40%, 50% 60% 75% 90% 100%	Select the backlight value in percentage of the maximum setting.
Force LVDS Backlight	No Yes	If set to 'Yes', the board controller activates the backlight enable signal independently from the SoC- backlight signal.
Inhibit Backlight	No Permanent Until End Of POST	Select whether the backlight enable signal should be activated when the panel is activated, remain inhibited until the end of BIOS POST, or remain inhibited permanently.
Backlight Delay	No Delay 100ms Delay 250ms Delay 500ms Delay 1s Delay	Set a delay to adjust the LVDS panel timings. The congatec board controller will add the delay to the backlight signal coming from the SoC according this setup node. Note: Please try this feature if the panel is flickering.
LVDS SSC	Disabled 0.5% 1.0% 1.5% 2.0% 2.5%	Select the LVDS spread-spectrum clock modulation depth. Note: This feature performs center spreading with a fixed modulation frequency of 32.9kHz.

8.4.3 Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	No option	Displays the CPU temperature in °C.
Board Temperature	No option	Displays the board temperature in °C.
12V Standard	No option	Displays the actual 12V standard voltage.
5Volts Standby	No option	Displays the actual 5V standby voltage.
Input Current (12V Standard)	No option	Displays the actual input current of 12V standard power plane.
CPU Fan Speed	No option	Displays the CPU fan speed in RPM.

Feature	Options	Description
Fan PWM Frequency Mode	Low Frequency High Frequency	Select the fan PWM base frequency mode: 'Low Frequency' – 11.0 to 88.2Hz. 'High Frequency' – 1k to 63kHz.
Fan PWM Frequency (kHz)	1 – 63	Select the fan PWM base frequency. Default: 31

8.4.4 Hardware Health Monitoring Submenu

Feature	Options	Description
Security Device Support	Disabled Enabled	Enable or disable TPM support. Note: A system reset is required after changing the option.
User Confirmation	Disabled Enabled	Enable or disable user confirmation requests for certain transactions.
TPM State	Disabled Enabled	Enable or disable TPM chip. Note: The system may restart several times during POST to acquire the target state.
Pending operation	None Enable Take Ownership Disable Take Ownership TPM Clear	Select the TPM chip operation. Note: System may restart several times during POST to perform the selected operation.

8.4.5 RTC Wake Submenu

Feature	Options	Description
Wake System At Fixed Time	Disabled Enabled	Enable this feature to wake system from S5 using the RTC alarm.
Wake up hour		Specify the wake up hour. For example: Enter "3" for 3am and "15" for 3pm.
Wake up minute		Specify the wake up minute.
Wake up second		Specify the wake up second.

8.4.6 Module Serial Ports Submenu

Feature	Options	Description
Serial Port 0	Disabled Enabled	Enable or disable module's serial port 0.

8.4.7 Reserve Legacy Interrupt Submenu

Feature	Options	Description
Reserve Legacy Interrupt 1/2/3	None IRQ3, IRQ4, IRQ5, IRQ6, IRQ10, IRQ11, IRQ14, IRQ15	Use this feature to reserve the interrupt for a legacy bus device. Note: The reserved interrupt will not be assigned to a PCI/PCIe device.

8.4.8 ACPI Submenu

Feature	Options	Description
Enable ACPI Auto Configuration	Disabled Enabled	Enable or disable 'BIOS ACPI Auto Configuration'.
Enable Hibernation	Disabled Enabled	Enable or disable the system's ability to hibernate (OS S4 sleep state). Note: Ensure your operating system supports this feature if you want to use it.
ACPI Sleep State	Suspend Disabled S3 (Suspend to RAM)	Select the state used for ACPI system sleep/suspend.
Lock Legacy Resources	Disabled Enabled	Enable or disable locking of legacy resources.
LID Support	Disabled Enabled	Configure COM Express LID# signal to act as ACPI lid.
Sleep Button Support	Disabled Enabled	Configure COM Express SLEEP# signal to act as ACPI sleep button.

8.4.9 SIO Submenu

Feature	Options	Description
AMI SIO Driver Version	No option	
SIO Clock	24 MHz 48 MHz	Select Super IO base clock.
► Serial Port 1	No option	Opens 'Serial Port 1' submenu.
► Serial Port 2	No option	Opens 'Serial Port 2' submenu.
► Parallel Port	No option	Opens 'Parallel Port' submenu.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the board.

8.4.10 Serial Port 1 Submenu

Feature	Options	Description
Serial Port	Enable Disable	Enable or disable Serial Port (COM).
Change Settings	Auto IO=3F8; IRQ=3,4,5,7,9,10,11,12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11,12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11,12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11,12; DMA;	Select optimal settings for Super IO device.

8.4.11 Serial Port 2 Submenu

Feature	Options	Description
Serial Port	Enable Disable	Enable or disable Serial Port (COM).
Change Settings	Use Automatic Settings IO=3F8; IRQ=3,4,5,7,9,10,11,12; DMA IO=2F8; IRQ=3,4,5,7,9,10,11,12; DMA IO=3F8; IRQ=3,4,5,7,9,10,11,12; DMA IO=3E8; IRQ=3,4,5,7,9,10,11,12; DMA	Serial Port 2 configuration options.
Device Mode	Standard Serial Port Mode IrDA Active pulse 1.6 uS IrDA Active pulse 3/16 bit time ASKIR Mode	Change the Serial Port mode.

8.4.12 Parallel Port Submenu

Feature	Options	Description
Parallel Port	Enabled	Enable or disable Parallel Port (LPT/LPTE).
	Disabled	

8.4.13 Intel[®] Smart Connect Technology Submenu

Feature	Options	Description
ISCT Support	Disabled Enabled	Enable or disable Intel® Smart Connection Support (ISCT). When this setup node is set to disabled, all the other nodes will be invisible.
ISCT Notification Control	Disabled Enabled	Enable or disable ISCT notification control.
ISCT WLAN Power Control	Disabled Enabled	Enable or disable ISCT WLAN power control.
ISCT WWAN Power Control	Disabled Enabled	Enable or disable ISCT WWAN power control
ISCT Sleep Duration Value Format	Duration in Seconds	Enter ISCT sleep duration in seconds.
ISCT RF Kill Switch Type	Software Hardware	Select ISCT RF kill switch type.
ISCT RTC Timer Support	Disabled Enabled	Enable or disable ISCT RTC timer.

8.4.14 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	Disabled Enabled	Enable or disable serial port 0 console redirection.
► Console Redirection Settings (COM0)	Submenu	Opens console redirection configuration submenu.
COM1 Console Redirection	Disabled Enabled	Enable or disable serial port 0 console redirection.
► Console Redirection Settings (COM1)	Submenu	Opens console redirection configuration submenu.
Serial Port for Out-of-Band Management / EMS Console Redirection	Disabled Enabled	Enable or disable serial port for out-of-band management / Windows Emergency Management Services (EMS).
► Console Redirection Settings	Submenu	Opens console redirection configuration submenu.

• Note

The Serial Port Console Redirection can be enabled only if an external Super I/O offering UARTs has been implemented on the board.

8.4.14.1 Console Redirection Settings COM0 Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 ANSI	Select terminal type.
Baudrate	9600 19200 38400 57600 115200	Select baud rate.
Data Bits	7 8	Set number of data bits.
Parity	None Even Odd Mark Space	Select parity.
Stop Bits	1 2	Set number of stop bits.
Flow Control	None Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled Enabled	Enable or disable VT-UTF8 combination key support for ANSI/VT100 terminals.
Recorder Mode	Disabled Enabled	If recorder mode is enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	Disabled Enabled	Enable or disable extended terminal resolution.
Legacy OS Redirection Resolution	80x24 80x25	Select number of rows and columns supported for legacy operating system redirection.
Putty KeyPad	VT100 LINUX XTERMR6 SCO ESCN VT400	Select function key and keypad on Putty.

8.4.14.2 Console Redirection Settings COM1 Submenu

Feature	Options	Description	
Terminal Type	VT100 VT100+ VT-UTF8 ANSI	Select terminal type.	
Baudrate	9600 19200 38400 57600 115200	Select baud rate.	
Data Bits	7 8	Set number of data bits.	
Parity	None Even Odd Mark Space	Select parity.	
Stop Bits	1 2	Set number of stop bits.	
Flow Control	None Hardware RTS/CTS	Select flow control.	
VT-UTF8 Combo Key Support	Disabled Enabled	Enable or disable VT-UTF8 combination key support for ANSI/VT100 terminals.	
Recorder Mode	Disabled Enabled	If recorder mode is enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.	
Resolution 100x31	Disabled Enabled	Enable or disable extended terminal resolution.	
Legacy OS Redirection Resolution	80x24 80x25	Select number of rows and columns supported for legacy operating system redirection.	
Putty KeyPad	VT100 LINUX XTERMR6 SCO ESCN VT400	Select function key and keypad on Putty.	

8.4.14.3 Console Redirection Settings Out-of-Band Management Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 ANSI	Select terminal type.
Bits Per Second	9600, 19200, 38400, 57600, 115200	Select baud rate.
Data Bits	8	Set number of data bits.
Parity	No option	
Stop Bits	1	Set number of stop bits.

8.4.15 CPU Configuration Submenu

Feature	Options	Description	
► Socket 0 CPU Information	Submenu	Opens socket specific CPU information.	
► CPU Thermal Configuration	Submenu	Opens CPU thermal configuration options.	
CPU Speed	No option	Displays the CPU clock frequency.	
64-bit	No option	Displays whether 64-bit is supported.	
Active Processor Cores	All , 1	Enable the required number of cores.	
Limit CPUID Maximum	Disabled Enabled	If set to 'Enabled', the processor limits the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. If set to 'Disabled', the processor returns the actual maximum CPUID input value of the processor when queried. Note: Limiting the CPUID input value might be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.	
Execute Disable Bit	Disabled Enabled	Enable or disable the Execute Disable Bit (XD) of the processor. If set to 'Enabled', certain classes of malicious buffer overflow attacks can be prevented. Note: Requires operating system support.	
Hardware Prefetcher	Disabled Enabled	Enable or disable the Mid Level Cache (MLC) streamer prefetcher.	
Adjacent Cache Line Prefetch	Disabled Enabled	Enable or disable prefetching of adjacent cache lines.	
Intel Virtualization Technology	Disabled Enabled	Enable or disable support for the Intel virtualization technology.	
Power Technology	Disable Energy Efficient Custom	Configure the power technology schema for the CPU.	

8.4.15.1 Socket 0 CPU Information Submenu

Feature	Options	Description
CPU Name	No option	Displays socket specific CPU name.
CPU Signature	No option	Displays CPU signature number.
Microcode Patch	No option	Displays the CPU microcode patch number.
Max. CPU Speed	No option	Displays the maximum CPU clock frequency.
Min. CPU Speed	No option	Displays the minimum CPU clock frequency.
Processor Cores	No option	Displays the number of CPU core on socket CPU.
Intel HT Technology	No option	Displays the Intel® HT Technology support information.
Intel VT-x Technology	No option	Displays the Intel® VT-x Technology support information.
L1 Data Cache	No option	Displays the socket L1 data cache information.
L1 Code Cache	No option	Displays the socket L1 code cache information.
L2 Cache	No option	Displays the socket L2 data cache information.
L3 Cache	No option	Displays the socket L3 data cache information.

8.4.15.2 CPU Thermal Configuration Submenu

Feature	Options	Description
DTS	Enabled Disabled	Enable or disable CPU Digital Thermal Sensor (DTS). DTS is used on ACPI functions to read the CPU temperature from MSR.

8.4.16 PPM Configuration Submenu

Feature	Options	Description
CPU C state Report	Disabled Enabled	Enable or disable CPU state report to OS.
Max CPU C state	C7 C6 C1	Set maximum CPU C state supported by the CPU.
SOix	Disabled Enabled	Enable or disable CPU SOix state support.

8.4.17 Thermal Configuration

Feature	Options	Description
Critical Trip Point	110 C 105 C 100 C, 95 C 90 C 87 C 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	Set temperature for ACPI critical trip point at which the operating system will shut down.
Passive Trip Point	110 C 105 C 100 C 95 C 90 C 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	Set temperature for ACPI passive trip point at which the operating system will throttle the processor.

Feature	Options	Description
Active Trip Point High	110 C 105 C 100 C 95 C 90 C 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C	This value controls the temperature of the ACPI active Trip Point – the point in which the operating system will enable the active cooling device at maximum capacity. DTS must be enable on the CPU Submenu to make effective this Node.
Active Trip Point Low	15 C 110 C 105 C 100 C 95 C 90 C 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	This value controls the temperature of the ACPI active Trip Point – the point in which the operating system will enable the active cooling device at half capacity. DTS must be enable on the CPU Submenu to make effective this Node.

8.4.18 IDE Configuration Submenu

Feature	Options	Description
Serial-ATA (SATA)	Enabled Disabled	Enable or disable the onboard SATA controller.
SATA Test Mode	Enabled Disabled	Enable only during verification measurements.
SATA Speed Support	Gen1 Gen2	Displays the maximum SATA speed the controller supports.
SATA ODD Port	Port 0 ODD Port 1 ODD No ODD	Select which SATA port is ODD.
SATA Mode	IDE Mode AHCI Mode	Select SATA port mode.
mSATA Interface	mSATA mPCle Auto	Configures the physical interface to support mSATA or mPCIE.
Serial-ATA Port 0	Enabled Disabled	Enable or disable the SATA port 0.
SATA Port 0 Hot Plug	Disabled Enabled	Select hot plug support for SATA port 0. Note: Not possible in native IDE mode.
Serial-ATA Port 1	Enabled Disabled	Enable or disable the SATA port 1.
SATA Port 1 Hot Plug	Disabled Enabled	Select hot plug support for SATA port 1. Note: Not possible in native IDE mode.
SATA Port 0 Information	No Option	Displays Information of device detected on SATA port 0.
SATA Port 1 Information	No Option	Displays Information of device detected on SATA port 1.

8.4.19 Miscellaneous Configuration Submenu

Feature	Options	Description
High Precision Timer	Enabled Disabled	Enable or disable the high precision event timer.
Boot Timer with HPET Timer	Enabled Disabled	Allow boot timer calculation with the high precision event timer.
PCI Express Dynamic Clock Gating	Enabled Disabled	Enable or disable dynamic clock gating.

8.4.20 SCC Configuration Submenu

Feature	Options	Description
SCC Device Mode	ACPI Mode PCI Mode	Select storage control cluster working mode.
SCC eMMC Support	Enable eMMC 4.5 Support Enable eMMC 4.41 Support eMMC AUTO MODE Disable	Enable or disable SCC eMMC support and select mode.
SCC 4.5 DDR50 eMMC Support	Enabled Disabled	Enable or disable DDR50 eMMC support.
SCC 4.5 HS200 eMMC Support	Enabled Disabled	Enable or disable HS200 eMMC support.
eMMC Secure Erase	Enabled Disabled	Enable or disable eMMC secure erase support.
SCC SD Card Support	Enabled Disabled	Enable or disable storage control cluster SD card support.
SDR25 Support for SD Card	Enabled Disabled	Enable or disable SDR25 support for SD card.
DDR50 Support for SD Card	Enabled Disabled	Enable or disable DDR50 support for SD card.
MIPI Camera Support	Disabled Enabled for Windows Enabled for Linux	Enable or Disable support for ISP device, MIPI CSI interface and dedicated camera I2C bus. ISP can either be a part of IGD device (for Windows) or a separate device (for Linux).

8.4.21 PCI Subsystem Settings Submenu

Feature	Options	Description
PCI Settings		
PCI Latency Timer	32 64 96 128 160 192 224 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.

Feature	Options	Description
PCI-X Latency Timer	32	Select value to be programmed into PCI latency timer register.
2	64	
	96	
	128	
	160	
	192	
	224	
	248 PCI Bus Clocks	
VGA Palette Snoop	Disabled	Enable or disable VGA palette registers snooping.
	Enabled	
PERR# Generation	Disabled	Enable or disable PCI device to generate PERR#.
	Enabled	
SERR# Generation	Disabled	Enable or disable PCI device to generate SERR#.
	Enabled	<u> </u>
Above 4G Decoding	Disabled	Enable or disable 64-bit capable devices to be decoded in Above 4G address space.
3	Enabled	Note: The system must support 64-bit PCI decoding.
SR-IOV Support	Disabled	Enable or disable Single Root IO Virtualization (SR-IOV) support.
	Enabled	
► PCI Express Settings	Submenu	Opens the 'PCI Express Settings' submenu.
► PCI Express GEN 2 Settings	Submenu	Opens the 'PCI Express Generation 2 Settings' submenu.

8.4.22 PCI Express Settings

Feature	Options	Description	
Relaxed Ordering	Disabled Enabled	Enable or disable 'Relaxed Ordering' for the PCIe device.	
Extended Tag	Disabled Enabled	Enable to use 8-bit tag field as a requester.	
No Snoop	Disabled Enabled	Enable or disable 'No Snoop' for the PCIe device.	
Maximum Payload	Auto 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 1096 Bytes	Select maximum payload of PCIe device or set to 'Auto'.	

Feature	Options	Description
Maximum Read Request	Auto 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 1096 Bytes	Select maximum read request size of PCIe device.
ASPM Support	Disabled Auto Force L0s	Select the ASPM Level: 'Disabled' – Disables ASPM. 'Auto' – BIOS auto configure. 'Force L0s' – Force all links to L0s State.
Extended Synch	Disabled Enabled	Enable to allow generation of extended synchronization patterns.
Link Training Retry	Disabled 2 3 5	Select number of retry attempts by the software to retrain the link.
Link Training Timeout (uS)	10 – 10000	Enter duration in microseconds for the software to wait before polling 'Link Training' bit in the link status register.
Unpopulated Links	Keep Link ON Disabled	If set to 'Disabled', unpopulated PCIe links will be disabled.
Restore PCIE Registers	Enabled Disabled	On non-PCIe aware operating systems, some devices might not be properly reinitialized after S3. Enable this option to restore PCIe device configurations on S3 resume. Note: If enabled, can cause issues with other hardware after S3 resume.

8.4.23 PCI Express GEN 2 Settings

Feature	Options	Description	
Completion Timeout	Default Shorter Longer Disabled	Select the completion timeout value: 'Default' – 50us to 50ms. 'Shorter' – Software will use shorter timeout ranges. 'Longer' – Software will use longer timeout ranges.	
ARI Forwarding	Disabled Enabled	If set to 'Enabled', the downstream port disables it's traditional device number field when turning a type 1 configuration request into a type 0 configuration request, permitting access to extended functions in an ARI device immediately below the port.	
AtomicOp Requester Enable	Disabled Enabled	If set to 'Enabled', this feature initiates AtomicOp requests only if bus master enable bit is in the command register set.	
AtomicOp Egress Blocking	Disabled Enabled	If set to 'Enabled', outbound AtomicOp requests via egress ports will be blocked.	
IDO Request Enable	Disabled Enabled	If set to 'Enabled', this feature permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated.	
IDO Completion Enable	Disabled Enabled	If set to 'Enabled', this feature permits setting the number of ID-Based Ordering (IDO (Attribute[2]) requests to be initiated.	
LTR Mechanism Enable	Disabled Enabled	Enable or disable the Latency Tolerance Reporting (LTR) mechanism.	
End-End TLP Prefix Blocking	Disabled Enabled	If set to 'Enabled', this function will block forwarding of TLPs containing End-End TLP prefixes.	
Target Link Speed	Auto Force to 2.5 GT/s Force to 5.0 GT/s	Select the target link speed: 'Auto' – Uses HW initialized data. 'Force to X.X GT/s' – Sets an upper limit on link operational speed by restricting the values advertised by the upstream component in its training sequences.	
Clock Power Management	Disabled Enabled	If set to 'Enabled', the device is permitted to use CLKREQ# signal for power management of link clock in accordance to protocol as defined in appropriate form factor specification.	
Compliance SOS	Disabled Enabled	If set to 'Enabled', this feature forces LTSSM to send SKP ordered sets between sequences when sending a compliance pattern or a modified compliance pattern.	
Hardware Autonomous Width	Enabled Disabled	If set to 'Disabled', this feature disables the hardware's ability to change link width, excep for the purpose of correcting unstable link operation.	
Hardware Autonomous Speed	Enabled Disabled	If set to 'Disabled', this feature disables the hardware's ability to change link speed, except speed rate reduction for the purpose of correcting unstable link operation.	

• Note

You cannot use any of the features above if your hardware does not support it.

8.4.24 Network Stack

Feature	Options	Description
Network Stack	Enabled Disabled	Enable or disable the UEFI network stack.
Ipv4 PXE Support	Enabled Disabled	If disabled, IPV6 PXE boot option will not be created.
Ipv6 PXE Support	Enabled Disabled	If disabled, IPV6 PXE boot option will not be created.
PXE boot wait time	0 –5	Select wait time to press ESC and abort PXE Boot.

8.4.25 Info Report Configuration

Feature	Options	Description
POST Report	Disabled Enabled	POST Report Support Enabled/Disabled.
Delay Time	0–10 Until Press ESC	POST Report wait time from 0 to 10 seconds or until press ESC key.
Error Message Report	Disabled Enabled	Enable or disable Error Message support.
Summary Screen	Disabled Enabled	Enable or disable Summary Screen support
Delay Time	0–10 Until Press ESC	Summary Screen wat time from 0 to 10 seconds or until Press ESC Key.

8.4.26 CSM Submenu

Feature	Options	Description
Launch CSM	Enabled Disabled	Enable or disable the compatibility support module.
CSM16 Module Version	No option	Display CSM module version number.
Gate A20 Active	Upon Request Always	Select legacy Gate A behavior.
Option ROM Messages	Force BIOS Keep Current	Enable or disable option ROM message.

Feature	Options	Description
Boot Option Filter	UEFI and Legacy Legacy Only UEFI Only	Control which devices and boot loaders the system should boot to.
Network	Do not launch UEFI only Legacy only	Control the execution of UEFI and legacy network option ROMs.
Storage	Do not launch UEFI only Legacy only	Control the execution of UEFI and legacy storage option ROMs.
Video	Do not launch UEFI only Legacy only	Control the execution of UEFI and legacy video option ROMs
Other PCI Devices	UEFI only Legacy only	Control the execution of UEFI and legacy option ROMs for PCI devices different to network, video and storage.

8.4.27 SDIO Submenu

Feature	Options	Description
SDIO Access Mode	Auto DMA PIO	Control the SDIO access mode to the device.

8.4.28 USB Submenu

Feature	Options	Description	
USB Module Version	No option	Displays the version of the USB module.	
USB Devices	No option	Displays the detected USB devices.	
Legacy USB Support	Enabled Disabled Auto	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.	
xHCI Hand-off	Enabled Disabled	This feature can be used as a workaround for operating systems without xHCl hand-off support. Note: If this feature is enabled, the xHCl ownership change should be claimed by the xHCl operating system driv	
EHCI Hand-off	Disabled Enabled	This feature can be used as a workaround for operating systems without EHCI hand-off support. Note: If this feature is enabled, the EHCI ownership change should be claimed by the EHCI operating system drive	
USB Mass Storage Driver Support	Disabled Enabled	Enable or disable mass storage driver support.	

Feature	Options	Description
Device Reset Timeout	10 sec	Select USB legacy mass storage device start unit command timeout.
	20 sec	
	30 sec 40 sec	
USB Transfer Timeout	1 sec	Select the timeout value for control, bulk, and interrupt transfers.
	5 sec	
	10 sec	
	20 sec	
Device Power-Up	Auto	Select maximum time a USB device might need before it properly reports itself to the host controller.
Delay Selection	Manual	'Auto' – Selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.
Device Power-Up Delay Value	0–40	Set power-up delay value in seconds. Default: 5

8.4.29 Platform Trust Technology

Feature	Options	Description
fTPM	Disable Enable	Enable or disable trusted platform module support.

8.4.30 Security Configuration

Feature	Options	Description
TXE	Enabled Disabled	Enable or disable trusted execution engine.
TXE HMRFPO	Enable Disable	Enable or disable Host ME Region Flash Protection Overwrite (HMRFPO).
TXE Firmware Update	Enabled Disabled	Enable or disable firmware update.
TXE EOP Message	Enabled Disabled	Enable or disable TXE End of Post (EOP) message.
TXE Unconfiguration Perform	No option	Execute a TXE unconfiguration command
Intel [®] Anti-Theft Technology Configuration	No option	
Intel [®] AT	Enable Disable	Enable or disable Anti-Theft (AT) technology.

Feature	Options	Description	
Intel [®] AT Platform PBA	Enable Disable	Enable or disable AT platform Pre-Boot Authentication (PBA).	
Intel® AT Suspend Mode	Enable Disable	Enable AT suspend mode.	

8.4.31 Intel[®] Ethernet Connection I210 Submenu

Feature	Options	Description	
 NIC Configuration 	Submenu	Opens the NIC Configuration submenu.	
Blink LEDs	0 –15	Enter the number of seconds for the Ethernet LEDs to blink.	
UEFI Driver	No option	Displays the UEFI driver version.	
Adapter PBA	No option	Displays the adapter PBA.	
Chip Туре	No option	Displays the type of the chip in which the Ethernet controller is integrated.	
PCI Device ID	No option	Displays the PCI device ID of the Ethernet controller.	
Bus:Device:Function	No option	Displays the PCI Bus:Device:Function number of the Ethernet controller.	
Link Status	No option	Displays the link status.	
MAC Address	No option	Displays the MAC address.	

8.4.31.1 NIC Configuration Submenu

Feature	Options	Description
Link Speed	Auto Negotiated 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Select the port speed for the selected boot protocol.
Wake on LAN	Disabled Enabled	Enable or disable Wake on LAN (WOL) feature

8.4.32 Driver Health Submenu

Feature	Options	Description
►Intel [®] PRO/1000	Submenu	Opens health status submenu for the drivers/controllers connected to the system.

8.5 Chipset Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

8.5.1 North Bridge Submenu

Feature	Options	Description
Memory Information		
Total Memory	No option	Displays total amount of memory detected by the system
Memory Slot 0	No option	Displays memory detected by the system on slot 0.
Memory Slot 1	No option	Displays memory detected by the system on slot 1
Max TOLUD	Dynamic 2 GB, 2.25 GB, 2.5 GB, 2.75 GB, 3 GB	Set the maximum Top of Low Usable DRAM (TOLUD).
Aperture Size	128MB, 256MB , 512MB	Select aperture size.
PAVC	Enable Disable	Enable or disable Protected Audio Video Control (PAVC).

8.5.2 South Bridge Submenu

Feature	Options	Description
► Azalia HD Audio	Submenu	Opens the Azalia HD Audio submenu.
► USB	Submenu	Opens the USB submenu.
 PCI Express Configuration 	Submenu	Opens the PCIe configuration submenu.
High Precision Timer	Enabled Disabled	Enable high precision event timer.
Serial IRQ	Quiet Continuous	Configure IRQ serial mode.
Global SMI Lock	Enabled Disabled	Enable or disable SMI lock.
BIOS Read/Write Protection	Enable Disable	Enable BIOS SPI region read/write protection.
Isolate SMBus Segments	Never During POST Always	Allows to isolate the off-module/external SMBus segment from the on-module SMBus segment. This can be a workaround for non-spec conform external SMBus devices.

8.5.2.1 Azalia HD Audio

Feature	Options	Description
LPE Audio Support	Disable LPE Audio PCI Mode LPE Audio ACPI Mode	Enable or disable LPE audio support.
Audio Controller	Enabled Disabled	Enable or disable audio controller.
Azalia Vci Enable	Enabled Disabled	Enable or disable Azalia Vci.
Azalia Docking Support Enable	Enable Disable	Enable or disable Azalia docking support.
Azalia PME Enable	Enabled Disabled	Enable or disable Azalia PME support.
Azalia HDMI Codec	Enabled Disabled	Enable or disable Azalia HDMI codec.
HDMI Port B	Enabled Disabled	Enable or disable HDMI port B audio.
HDMI Port C	Enable Disable	Enable or disable HDMI port C audio.

8.5.2.2 USB Submenu

Feature	Options	Description
USB OTG Support	Disabled Enabled	Enable USB OTG support.
USB VBUS	On Off	Select 'On' for host mode and 'Off' for OTG device mode.
xHCI Mode	Enable Disable Auto Smart Auto	Select mode for all USB ports (0–3): 'Enabled' – USB ports will function in USB 3.0 mode but require driver on the operating system. USB ports will not function in pre-operating time time if USB 3.0 support in BIOS is disabled (see the USB 3.0 support in BIOS item). 'Disabled' – USB ports will function in USB 2.0 mode only and routed to the EHCI1 controller. 'Auto' – USB ports will initially function in USB 2.0 mode but the operating system driver can switch to USB 3.0. 'Smart Auto' – Identical to 'Auto', except the BIOS will take over the operating system driver setting after each restart.
USB2 Link Power Management	Disabled Enabled	Enable or disable USB2 Link Power Management (LPM).
USB 2.0 (EHCI) Support	Disabled Enabled	Enable or disable USB 2.0 EHCI functions.

Feature	Options	Description	
USB Per Port Control	Disabled Enabled	Select whether each USB Port (0–3) can be enabled and disabled individually.	
USB Port 0	Disabled Enabled	Enable or disable USB port 0.	
USB Port 1	Disabled Enabled	Enable or disable USB port 1.	
USB Port 2	Disabled Enabled	Enable or disable USB port 2.	
USB Port 3	Disabled Enabled	Enable or disable USB port 3.	

8.5.2.3 PCI Express Configuration Submenu

Feature	Options	Description
PCIe noncompliance Card	Not Supported Supported	Select whether to support PCIe 1.0 cards. Note: If set to 'Supported', the speed of all PCIe ports defaults to Gen 1.
PCI Express Port 0	Disabled Enabled	Enable or disable PCIe port 0.
Speed	Auto Gen 2 Gen 1	Select PCIe speed on port 0. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
PCI Express Port 1	Disabled Enabled	Enable or disable PCIe port 1.
Speed	Auto Gen 2 Gen 1	Select PCIe speed on port 1. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
PCI Express Port 2	Disabled Enabled	Enable or disable PCIe port 2.
Speed	Auto Gen 2 Gen 1	Select PCIe speed on port 2. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
PCI Express Port 3	Disabled Enabled	Enable or disable PCIe port 3.
Speed	Auto Gen 2 Gen 1	Select PCIe speed on port 3.

8.6 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

8.6.1 Boot Settings Configuration

Feature	Options	Description
Setup Prompt Timeout	0 – 65535	Enter number of seconds to wait for setup activation key. Default: 1 Note: 0 is not recommended. 65535 means infinite wait.
Bootup NumLock State	On Off	Select the keyboard numlock state.
Quiet Boot	Disabled Enabled	'Disabled' – Displays normal POST diagnostic messages. 'Enabled' – Displays OEM logo instead of POST messages. The default OEM logo is a dark screen.
Enter Setup If No Boot Device	No Yes	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No Yes	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based Type Based	Select between device and type based boot priority lists: 'Device Based' – Select boot priority from a list of currently detected devices. 'Type Based' – Select boot priority from a list of device types even if they are not connected yet.
Power Loss Control	Remain Off Turn On Last State	Select the mode of operation if an AC power loss occurs: 'Remain Off' – Keeps the power off until the power button is pressed. 'Turn On' – Restores power to the computer. 'Last State' – Restores the previous power state before power loss occurred. Note: Only works with an ATX type power supply.
AT Shutdown Mode	System Reboot Hot S5	Select the behavior of an AT-powered system after a shutdown.
Battery Support	Auto (Battery Manager) Battery-Only On I2C Bus Battery-Only On I2C Bus	Select the battery system support bus.
System Off Mode	G3/Mech Off S5/Soft Off	Select system state after shutdown if a battery system is present.
Fast Boot	Disabled Enabled	Enable to boot with a minimum set of devices. No effect for BBS / legacy boot options.

Note

The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. The standby voltage is continuously monitored after the system is turned off. If the standby voltage is not detected within 30 seconds, this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, it is assumed that the system was switched off properly.

Inexpensive ATX power supplies often have problems with short AC power sags. The system turns off but might not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually, an AC power off/on cycle is necessary to recover from this situation.

8.7 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

8.7.1 Security Settings

Feature	Options	Description
Administrator Password	Enter password	Enter the setup administrator password.
HDD Security Configuration		
List of all detected hard disks supporting the security feature set		Select device to open device security configuration submenu.

8.7.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently; however, the drive will only lock if a user password is installed.

8.8 Save & Exit Menu

Select the Save & Exit tab from the setup menu with the <Arrow> keys to enter the Save & Exit setup screen.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset, if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.

Feature	Description
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.
Boot Override	
List of all boot devices currently detected	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to "Device Based".

9 Additional BIOS Features

The conga-PA3 uses a congatec/AMI AptioEFI stored in an onboard flash ROM chip and can be updated using the congatec system utility. The system utility is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen, identifying the BIOS project name and a revision code. The initial production BIOS is identified as PAC1R1xx where:

- PAC1 BIOS for modules with Baytrail Single Channel Memory SoC
- R Identifier for BIOS ROM file
- 1 Feature number
- xx Major and minor revision number

9.1 Supported Flash Devices

The conga-PA3 supports the following flash devices:

• Winbond W25Q64FWSSIG (8MB)

The flash device listed above is tested and can be used on the board for external BIOS support. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.

9.2 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

10 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG products.

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
Serial ATA Specification, Revision 3.0	http://www.serialata.org
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications