STK-MBa6x
User's Manual

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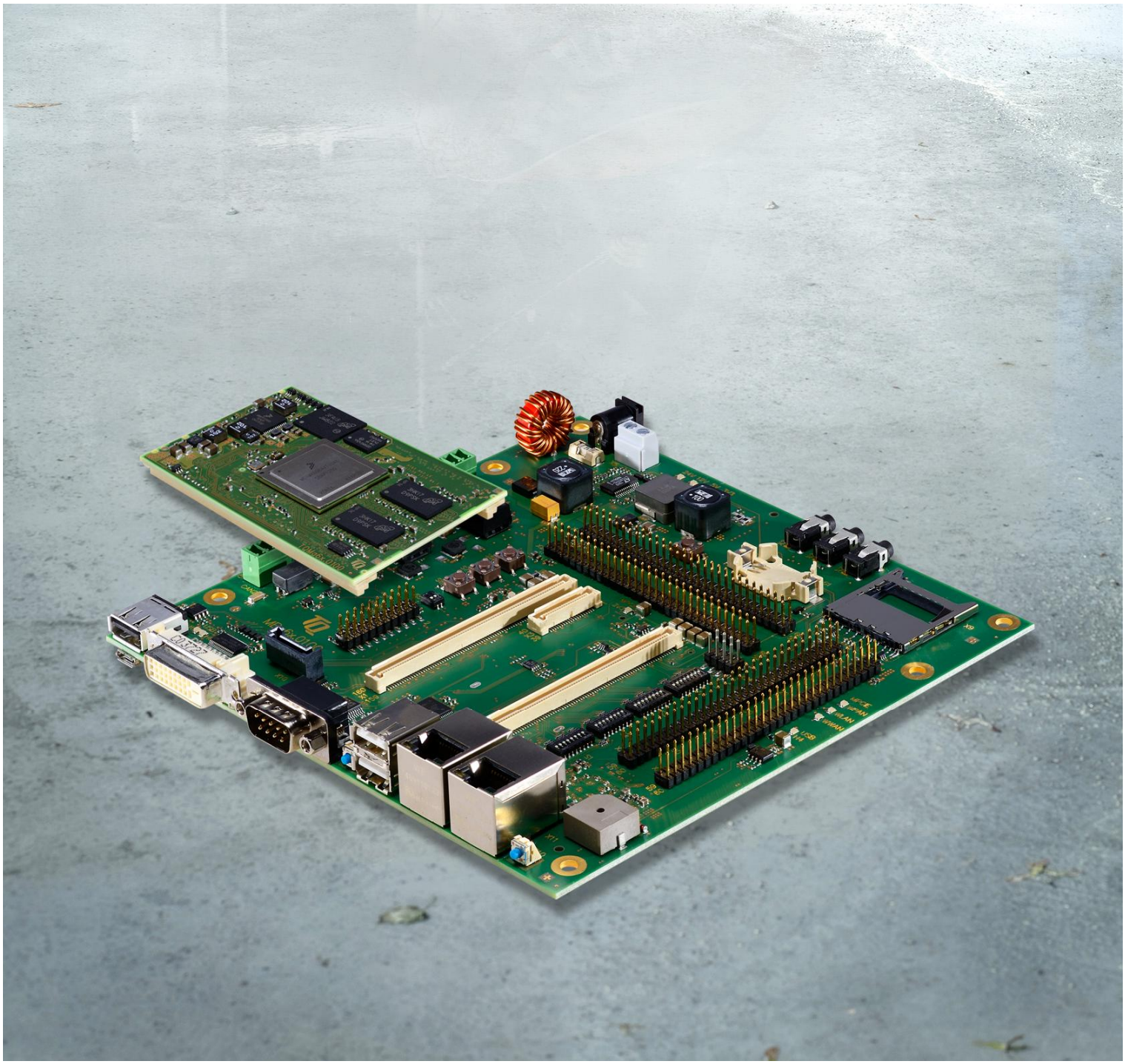

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the STK-MBa6x and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- Circuit diagram STK-MBa6x
- CPU Reference Manual IMX6DQRM
- User's Manual TQMa6x
- Documentation of boot loader U-Boot (http://www.denx.de/wiki/U-Boot/Documentation)
- Documentation of PTXdist (http://www.ptxdist.de)

2. BRIEF DESCRIPTION

The STK-MBa6x is designed as a carrier board for the TQMa6x.

All of the TQMa6x interfaces are available on the STK-MBa6x. The characteristics of the i.MX6 CPU can be evaluated, and therefore the software development for a TQMa6x project can be started immediately.

The STK-MBa6x supports all TQMa6x modules with a Solo, Dual or Quad i.MX6 CPU.

3. TECHNICAL DATA

3.1 System architecture and functionality

3.1.1 Block diagram

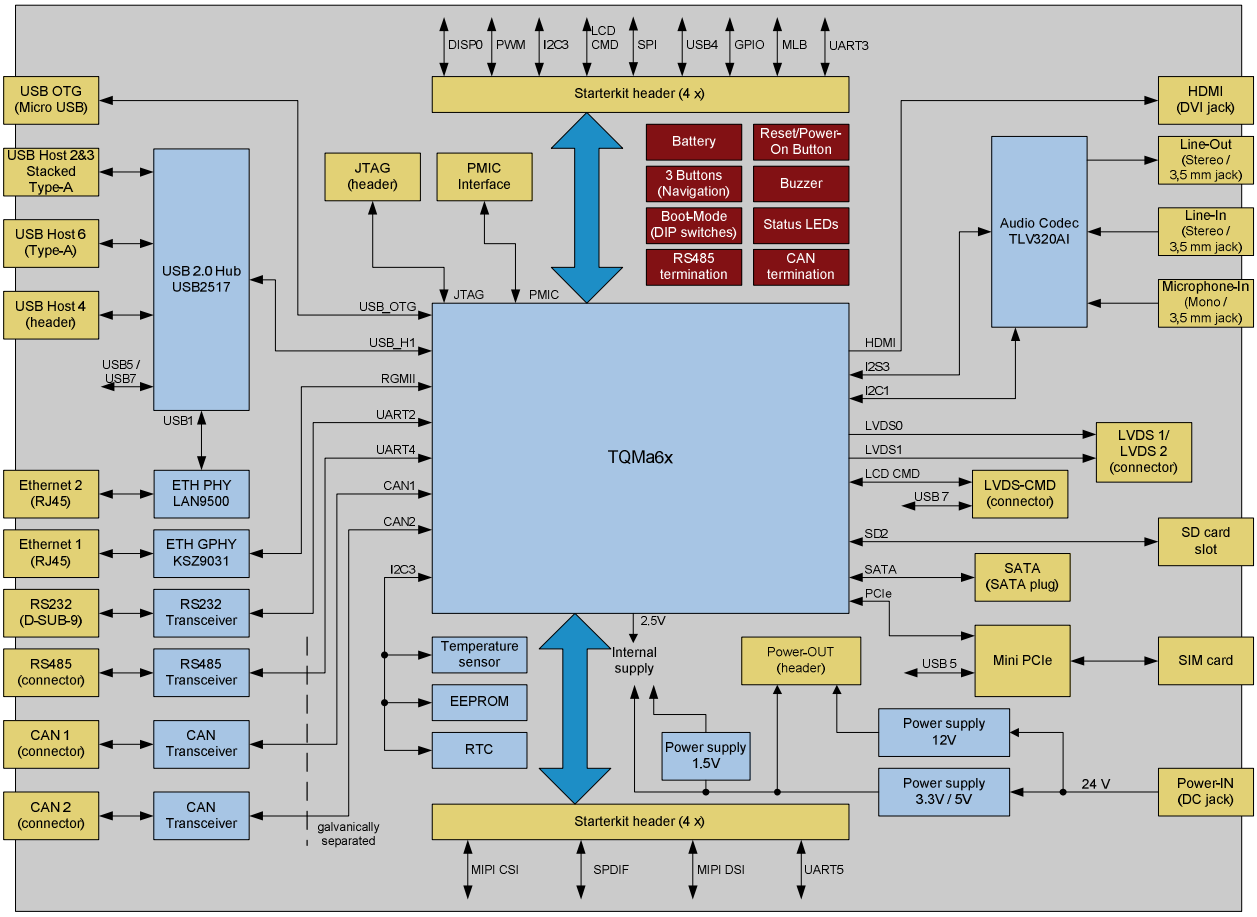


Illustration 1: Block diagram STK-MBa6x

3.1.2 Functionality

The core of the system is the TQMa6x processor module with a Freescale i.MX6 CPU.
The TQMa6x connects all peripheral components to each other.

In addition to the standard communication interfaces like USB, Ethernet, RS232, RS485, LVDS etc. all other available signals of the TQMa6x are routed to 2.54 mm standard headers.

The following interfaces / functions and user's interfaces are provided on the STK-MBa6x:

Table 2: Overview interfaces

Interface	Qty.	Type of connector	Remark
USB 2.0 Hi-Speed host	2	USB receptacle type A	Dual port receptacle, right angle
USB 2.0 Hi-Speed host	1	USB receptacle type A	Single port receptacle, right angle
USB 2.0 Hi-Speed host	1	Header	
USB 2.0 Hi-Speed OTG	1	USB receptacle type Micro-AB	
Ethernet 100BASE-T	1	RJ45 receptacle	Receptacle with integrated magnetics
Ethernet 1000BASE-T	1	RJ45 receptacle	Receptacle with integrated magnetics
CAN	2	Phoenix basic housing	Straight version, gal. separated
RS485	1	Phoenix basic housing	Straight version, gal. separated
RS232	1	D-Sub 9-pin connector	Right angle, Debug-UART
HDMI	1	DVI receptacle	
LVDS	1	DF19 receptacle	LVDS data
LVDS-CMD	1	DF19 receptacle	LVDS control lines
Audio Out	3	Jack 3.5 mm	1 × Line-out (stereo) 1 × Line-in (stereo) 1 × Microphone (mono)
SD card	1	Push-Pull-Type	
SATA	1	SATA socket	Straight version
PCIe	1	Mini PCIe	
	1	SIM-Card holder	
Headers	4	Header, 2.54 mm pitch	• DISP0 • PWM • I2C3, I2C1 • LCD-CMD • SPI1, SPI5 • USB4 • GPIOs • MLB • UART3, UART5 • SPDIF • MIPI DSI, MIPI CSI • 3.3 V @ 2 A • 5 V @ 2 A • 12 V @ 3 A
Power In	1	DC jack (2.5 mm / 5.5 mm)	
(V_{IN} = 24 V ±5 % DC)	1	DC jack 2-pin (screw terminals)	
Battery holder	1	CR2032 holder	Backup battery RTC

Table 3: Overview diagnose and user's interfaces

Interface	Qty.	Component	Remark
Status-LEDs	16	Chip LEDs	Among others Power-LEDs, LEDs at GPIOs, …
Temperature sensor	1	LM75	
Power / reset button	3	Push button	
Navigation buttons	3	Push button	
Boot-Mode configuration	32 + 2	DIP switch	
CAN - and RS485 termination	4	DIP switch	
Signal generator	1	Buzzer	
PMIC Diagnosis interface	1	Header	
JTAG	1	20-pin header, 2.54 mm pitch	

4. ELECTRONICS

4.1 System components

4.1.1 TQMa6x

4.1.1.1 Overview TQMa6x

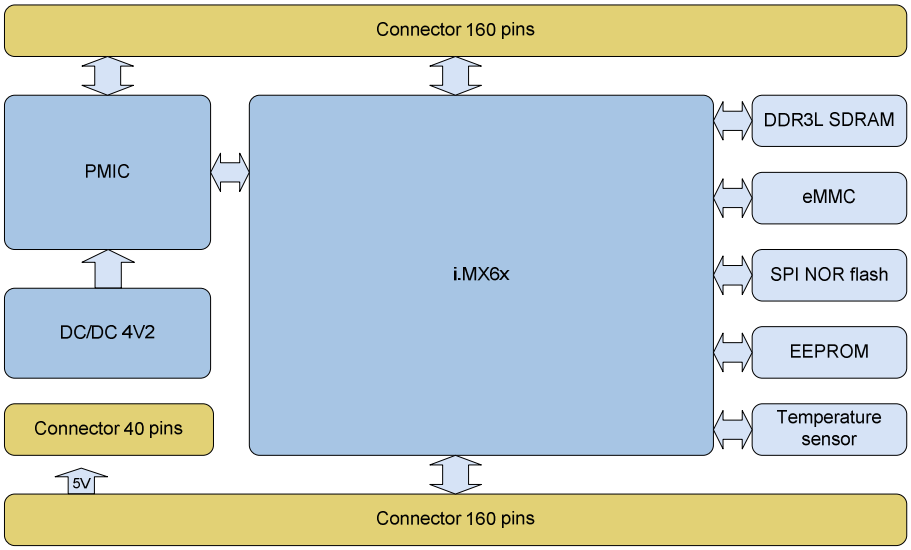


Illustration 2: Block diagram TQMa6x

The TQMa6x with the i.MX6 CPU is the central system component. It provides DDR3-SDRAM, eMMC, NOR flash and EEPROM memory. All voltages required by the TQMa6x are derived from the supply voltage of 5 V. More detailed information is to be taken from the accompanying User's Manual of the TQMa6x.

The boot behaviour of the TQMa6x can be customised. The required boot-mode configuration can be set with DIP switches, see section 4.3.5.

4.1.1.2 Pinout X!, X2, X3

The available signals are routed via three connectors onto the STK-MBa6x.
The pins assignment listed in Table 4, Table 5 and Table 6 refer to the corresponding standard BSP of TQ-Systems GmbH.

Table 4: Pinout connector X1

Ball	I/O	Level	Group	Signal	Pin		Pin	Signal	Group	Level	I/O	Ball
–	P	5 V	POWER	VCC5V	1		2	VCC5V	POWER	5 V	P	–
–	P	5 V	POWER	VCC5V	3		4	VCC5V	POWER	5 V	P	–
–	P	5 V	POWER	VCC5V	5		6	VCC5V	POWER	5 V	P	–
–	P	0 V	POWER	DGND	7		8	DGND	POWER	0 V	P	–
–	P	0 V	POWER	DGND	9		10	DGND	POWER	0 V	P	–
–	P	0 V	POWER	DGND	11		12	DGND	POWER	0 V	P	–
A18	I/O	3.3 V	GPIO	GPIO2_IO00	13		14	PCIE_TXM	PCIE	–[1]	O	A03
C17	I/O	3.3 V	GPIO	GPIO2_IO01	15		16	PCIE_TXP	PCIE	–[1]	O	B03
F16	I/O	3.3 V	GPIO	GPIO2_IO02	17		18	DGND	POWER	0 V	P	–
D17	I/O	3.3 V	GPIO	GPIO2_IO03	19		20	PCIE_RXM	PCIE	–[1]	I	B01
D18	I/O	3.3 V	GPIO	GPIO2_IO08	21		22	PCIE_RXP	PCIE	–[1]	I	B02
A20	I/O	3.3 V	GPIO	GPIO2_IO11	23		24	DGND	POWER	0 V	P	–
C15	I/O	3.3 V	GPIO	GPIO6_IO07	25		26	CLK1_N	XTAL	2.5 V	O	C07
A16	I/O	3.3 V	GPIO	GPIO6_IO08	27		28	CLK1_P	XTAL	2.5 V	O	D07
F15	I/O	3.3 V	GPIO	GPIO6_IO11	29		30	DGND	POWER	0 V	P	–
C16	I/O	3.3 V	GPIO	GPIO6_IO14	31		32	USB_H1_DP	USB	–[2]	I/O	E10
B19	O	3.3 V	PWM	PWM3	33		34	USB_H1_DN	USB	–[2]	I/O	F10
–	P	0 V	POWER	DGND	35		36	DGND	POWER	0 V	P	–
D10	P	5 V	POWER	USB_H1_VBUS	37		38	HDMI_CLKM	HDMI	3.3 V	O	J05
T05	O	3.3 V	USB	USB_H1_PWR	39		40	HDMI_CLKP	HDMI	3.3 V	O	J06
R07	I	3.3 V	USB	USB_H1_OC	41		42	DGND	POWER	0 V	P	–
E09	P	5 V	POWER	USB_OTG_VBUS	43		44	HDMI_D0M	HDMI	3.3 V	O	K05
T04	I	3.3 V	USB	USB_OTG_ID	45		46	HDMI_D0P	HDMI	3.3 V	O	K06
–	P	0 V	POWER	DGND	47		48	DGND	POWER	0 V	P	–
A06	I/O	–[2]	USB	USB_OTG_DP	49		50	HDMI_D1M	HDMI	3.3 V	O	J03
B06	I/O	–[2]	USB	USB_OTG_DN	51		52	HDMI_D1P	HDMI	3.3 V	O	J04
–	P	0 V	POWER	DGND	53		54	DGND	POWER	0 V	P	–
A14	I	0.5 V	SATA	SATA_RXM	55		56	HDMI_D2M	HDMI	3.3 V	O	K03
B14	I	0.5 V	SATA	SATA_RXP	57		58	HDMI_D2P	HDMI	3.3 V	O	K04
–	P	0 V	POWER	DGND	59		60	DGND	POWER	0 V	P	–
B12	O	0.5 V	SATA	SATA_TXM	61		62	HDMI_DDC_SCL	HDMI	3.3 V	O	U05
A12	O	0.5 V	SATA	SATA_TXP	63		64	HDMI_DDC_SDA	HDMI	3.3 V	I/O	T07
–	P	0 V	POWER	DGND	65		66	HDMI_HPD	HDMI	3.3 V	I	K01
C02	I	3.3 V	JTAG	JTAG_TRST#	67		68	BOOT_MODE0	CONFIG	3.0 V[3]	I	C12
C03	I	3.3 V	JTAG	JTAG_TMS	69		70	BOOT_MODE1	CONFIG	3.0 V[3]	I	F12
G05	I	3.3 V	JTAG	JTAG_TDI	71		72	GPIO7_IO12	GPIO	3.3 V	I/O	R01
G06	O	3.3 V	JTAG	JTAG_TDO	73		74	GPIO4_IO06	GPIO	3.3 V	I/O	W05
H06	I_{PD}	3.3 V	JTAG	JTAG_MOD	75		76	VSNVS_REF_OUT	POWER	3.0 V	P	–
H05	O	3.3 V	JTAG	JTAG_TCK	77		78	CCM_CLKO1	CLKO	3.3 V	O	P04
–	P	0 V	POWER	DGND	79		80	DGND	POWER	0 V	P	–

1: See PCIe 1.1/2.0 Specification.
2: See USB 2.0 Specification.
3: Use VSNVS_REF_OUT only as reference voltage.

Table 4: Pinout connector X1 (continued)

Ball	I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O	Ball
L01	I	3.3 V	UART	UART4_RX	81	82	GPIO5_IO18	GPIO	3.3 V	I/O	P01
M02	O	3.3 V	UART	UART4_TX	83	84	GPIO5_IO21	GPIO	3.3 V	I/O	N02
L04	I	3.3 V	UART	UART4_RTS#	85	86	I2C3_SCL	I2C	3.3 V	O_{PU}	R04
L03	O	3.3 V	UART	UART4_CTS#	87	88	I2C3_SDA	I2C	3.3 V	I/O_{PU}	T03
M05	I	3.3 V	UART	UART5_RX	89	90	CAN2_RX	CAN	3.3 V	I	V05
M04	O	3.3 V	UART	UART5_TX	91	92	CAN2_TX	CAN	3.3 V	O	T06
M06	I	3.3 V	UART	UART5_RTS#	93	94	CAN1_RX	CAN	3.3 V	I	W04
L06	O	3.3 V	UART	UART5_CTS#	95	96	CAN1_TX	CAN	3.3 V	O	W06
–	P	0 V	POWER	DGND	97	98	DGND	POWER	0 V	P	–
M01	I	3.3 V	AUDIO	AUD3_RXC	99	100	AUD3_TXC	AUDIO	3.3 V	O	N01
M03	I	3.3 V	AUDIO	AUD3_RXFS	101	102	AUD3_TXFS	AUDIO	3.3 V	O	N04
N03	I	3.3 V	AUDIO	AUD3_RXD	103	104	AUD3_TXD	AUDIO	3.3 V	O	P02
F17	O	3.3 V	PWM	PWM4	105	106	GPIO1_IO21	GPIO	3.3 V	I/O	F18
N05	O	3.3 V	I2C	I2C1_SCL	107	108	SPI5_MISO	SPI	3.3 V	I	A21
N06	I/O	3.3 V	I2C	I2C1_SDA	109	110	SPI5_MOSI	SPI	3.3 V	O	B21
P03	I/O	3.3 V	GPIO	GPIO5_IO20	111	112	SPI5_SS0#	SPI	3.3 V	O	C20
P05	I/O	3.3 V	GPIO	GPIO4_IO05	113	114	SPI5_SCK	SPI	3.3 V	O	D20
–	P	0 V	POWER	DGND	115	116	DGND	POWER	0 V	P	–
Y01	O	1.2 V	LVDS	LVDS1_TX0_N	117	118	LVDS0_TX0_N	LVDS	1.2 V	O	U02
Y02	O	1.2 V	LVDS	LVDS1_TX0_P	119	120	LVDS0_TX0_P	LVDS	1.2 V	O	U01
–	P	0 V	POWER	DGND	121	122	DGND	POWER	0 V	P	–
AA02	O	1.2 V	LVDS	LVDS1_TX1_N	123	124	LVDS0_TX1_N	LVDS	1.2 V	O	U04
AA01	O	1.2 V	LVDS	LVDS1_TX1_P	125	126	LVDS0_TX1_P	LVDS	1.2 V	O	U03
–	P	0 V	POWER	DGND	127	128	DGND	POWER	0 V	P	–
AB01	O	1.2 V	LVDS	LVDS1_TX2_N	129	130	LVDS0_TX2_N	LVDS	1.2 V	O	V02
AB02	O	1.2 V	LVDS	LVDS1_TX2_P	131	132	LVDS0_TX2_P	LVDS	1.2 V	O	V01
–	P	0 V	POWER	DGND	133	134	DGND	POWER	0 V	P	–
Y03	O	1.2 V	LVDS	LVDS1_CLK_N	135	136	LVDS0_CLK_N	LVDS	1.2 V	O	V04
Y04	O	1.2 V	LVDS	LVDS1_CLK_P	137	138	LVDS0_CLK_P	LVDS	1.2 V	O	V03
–	P	0 V	POWER	DGND	139	140	DGND	POWER	0 V	P	–
AA03	O	1.2 V	LVDS	LVDS1_TX3_N	141	142	LVDS0_TX3_N	LVDS	1.2 V	O	W02
AA04	O	1.2 V	LVDS	LVDS1_TX3_P	143	144	LVDS0_TX3_P	LVDS	1.2 V	O	W01
–	P	0 V	POWER	DGND	145	146	DGND	POWER	0 V	P	–
T02	O	3.3 V	PWM	PWM1	147	148	GPIO7_IO13	GPIO	3.3 V	I/O	P06
U20	I/O	ENET[4]	GPIO	GPIO1_IO30	149	150	GPIO7_IO11	GPIO	3.3 V	I/O	R02
W20	I/O	ENET[4]	GPIO	GPIO1_IO29	151	152	GPIO1_IO07	GPIO	3.3 V	I/O	R03
V21	I/O	ENET[4]	GPIO	GPIO1_IO28	153	154	GPIO1_IO26	GPIO	ENET[4]	I/O	W22
U21	I/O	ENET[4]	GPIO	GPIO1_IO25	155	156	SPDIF_OUT	AUDIO	ENET[4]	O	W21
R05	I/O	3.3 V	GPIO	GPIO1_IO08	157	158	SPDIF_IN	AUDIO	ENET[4]	I	W23
–	P	0 V	POWER	DGND	159	160	DGND	POWER	0 V	P	–

4: 2.5 V if NVCC_ENET_IN is connected to VCC2V5_RGMII_OUT. 3.3 V if NVCC_ENET_IN is connected to VCC3V3_REF_OUT.

Table 5: Pinout connector X2

Ball	I/O	Level	Group	Signal	Pin		Pin	Signal	Group	Level	I/O	Ball
–	P	0 V	POWER	DGND	1		2	DGND	POWER	0 V	P	–
A22	I/O	3.3 V	SD	SD2_DAT0	3		4	SD2_DAT1	SD	3.3 V	I/O	E20
A23	I/O	3.3 V	SD	SD2_DAT2	5		6	SD2_DAT3	SD	3.3 V	I/O	B22
A19	I/O	3.3 V	SD	SD2_DAT4	7		8	SD2_DAT5	SD	3.3 V	I/O	B18
E17	I/O	3.3 V	SD	SD2_DAT6	9		10	SD2_DAT7	SD	3.3 V	I/O	C18
T1	I	3.3 V	SD	SD2_WP	11		12	SD2_CMD	SD	3.3 V	I	F19
C21	O	3.3 V	SD	SD2_CLK	13		14	SD2_CD#	SD	3.3 V	I	R6
–	P	0 V	POWER	DGND	15		16	DGND	POWER	0 V	P	–
–	P	3.3 V	POWER	LICELL	17		18	VCC8V25_OTP	CONFIG	8.25 V	P	–
–	I_{PU}	3.3 V	CONFIG	PMIC_PWRON	19		20	VCC3V3_OTP	CONFIG	3.3 V	P	–
D12	I_{PU}	3.3 V	CONFIG	MX6_ONOFF	21		22	OTP_SCL	CONFIG	3.3 V	I	–
C11	I_{PU}	3.3 V	CONFIG	MX6_POR#	23		24	OTP_SDA	CONFIG	3.3 V	I/O	–
–	O_{OD}	3.3 V	CONFIG	RESET_OUT#	25		26	RFU	RFU	–	I	–
E18	I	3.3 V	UART	UART2_RX	27		28	UART2_RTS#	UART	3.3 V	I	C19
D19	O	3.3 V	UART	UART2_TX	29		30	UART2_CTS#	UART	3.3 V	O	B20
–	P	0 V	POWER	DGND	31		32	DGND	POWER	0 V	P	–
B25	I	2.5 V	RGMII	RGMII_RXC	33		34	RGMII_TXC	RGMII	2.5 V	O	D21
–	P	0 V	POWER	DGND	35		36	DGND	POWER	0 V	P	–
C24	I	2.5 V	RGMII	RGMII_RD0	37		38	RGMII_TD0	RGMII	2.5 V	O	C22
B23	I	2.5 V	RGMII	RGMII_RD1	39		40	RGMII_TD1	RGMII	2.5 V	O	F20
B24	I	2.5 V	RGMII	RGMII_RD2	41		42	RGMII_TD2	RGMII	2.5 V	O	E21
D23	I	2.5 V	RGMII	RGMII_RD3	43		44	RGMII_TD3	RGMII	2.5 V	O	A24
D22	I	2.5 V	RGMII	RGMII_RX_CTL	45		46	RGMII_TX_CTL	RGMII	2.5 V	O	C23
–	P	0 V	POWER	DGND	47		48	DGND	POWER	0 V	P	–
V20	O	ENET[5]	MII	ENET_MDC	49		50	ENET_REFCLK	RGMII	ENET[5]	I	V22
V23	I/O	ENET[5]	MII	ENET_MDIO	51		52	DGND	POWER	0 V	P	–
R19	P	ENET[5]	POWER	NVCC_ENET_IN	53		54	VCC2V5_RGMII_OUT	POWER	2.5 V	P	–
V06	I/O	3.3 V	GPIO	GPIO4_IO07	55		56	VCC3V3_REF_OUT	POWER	3.3 V	P	–
U07	I/O	3.3 V	GPIO	GPIO4_IO08	57		58	GPIO4_IO09	GPIO	3.3 V	I/O	U06
E16	I	3.3 V	UART	UART3_RX	59		60	WDOG1#	WDOG	3.3 V	O	E19
B17	O	3.3 V	UART	UART3_TX	61		62	DGND	POWER	0 V	P	–
F21	I	3.3 V	SPI	SPI1_MISO	63		64	SPI1_SCK	SPI	3.3 V	O	C25
G21	O	3.3 V	SPI	(SPI1_SS1#)/DNC	65		66	SPI1_MOSI	SPI	3.3 V	O	D24
H20	I	3.3 V	USB	USB_OTG_OC	67		68	GPIO3_IO20	GPIO	3.3 V	I/O	G20
D25	I/O	3.3 V	GPIO	GPIO3_IO23	69		70	USB_OTG_PWR	USB	3.3 V	O	E23
G22	O	3.3 V	SPI	SPI1_SS3#	71		72	SPI1_SS2#	SPI	3.3 V	O	F22
–	P	0 V	POWER	DGND	73		74	DGND	POWER	0 V	P	–
E25	I/O	3.3 V	GPIO	GPIO3_IO27	75		76	GPIO3_IO26	GPIO	3.3 V	I/O	E24
J19	I/O	3.3 V	GPIO	GPIO3_IO29	77		78	GPIO3_IO28	GPIO	3.3 V	I/O	G23
H21	I	3.3 V	UART	UART3_RTS#	79		80	UART3_CTS#	UART	3.3 V	O	J20

5: 2.5 V, if NVCC_ENET_IN is connected to VCC2V5_RGMII_OUT. 3.3 V, if NVCC_ENET_IN is connected to VCC3V3_REF_OUT.

Table 5: Pinout connector X2 (continued)

Ball	I/O	Level	Group	Signal	Pin		Pin	Signal	Group	Level	I/O	Ball
J24	I/O	3.3 V	GPIO	GPIO2_IO25	81		82	CCM_CLKO2	CCM	3.3 V	O	A17
J23	I/O	3.3 V	GPIO	GPIO2_IO24	83		84	GPIO2_IO23	GPIO	3.3 V	I/O	H24
F23	I	3.3 V	BOOT	BOOT_CFG4_7	85		86	BOOT_CFG4_6	BOOT	3.3 V	I	E22
–	P	0 V	POWER	DGND	87		88	DGND	POWER	0 V	P	–
K20	I	3.3 V	BOOT	BOOT_CFG4_5	89		90	BOOT_CFG4_4	BOOT	3.3 V	I	K23
K21	I	3.3 V	BOOT	BOOT_CFG4_3	91		92	BOOT_CFG4_2	BOOT	3.3 V	I	K22
M25	I	3.3 V	BOOT	BOOT_CFG4_1	93		94	GPIO6_IO16	GPIO	3.3 V	I/O	D16
H19	I/O	3.3 V	HDMI	HDMI_CEC_LINE	95		96	BOOT_CFG4_0	BOOT	3.3 V	I	F25
J21	I	3.3 V	BOOT	BOOT_CFG3_7	97		98	BOOT_CFG3_6	BOOT	3.3 V	I	F24
H23	I	3.3 V	BOOT	BOOT_CFG3_5	99		100	BOOT_CFG3_4	BOOT	3.3 V	I	H22
G25	I	3.3 V	BOOT	BOOT_CFG3_3	101		102	BOOT_CFG3_2	BOOT	3.3 V	I	J22
G24	I	3.3 V	BOOT	BOOT_CFG3_1	103		104	BOOT_CFG3_0	BOOT	3.3 V	I	H25
–	P	0 V	POWER	DGND	105		106	DGND	POWER	0 V	P	–
N24	I	3.3 V	BOOT	BOOT_CFG2_7	107		108	BOOT_CFG2_6	BOOT	3.3 V	I	N23
M23	I	3.3 V	BOOT	BOOT_CFG2_5	109		110	BOOT_CFG2_4	BOOT	3.3 V	I	M24
M20	I	3.3 V	BOOT	BOOT_CFG2_3	111		112	BOOT_CFG2_2	BOOT	3.3 V	I	M22
M21	I	3.3 V	BOOT	BOOT_CFG2_1	113		114	BOOT_CFG2_0	BOOT	3.3 V	I	L24
L25	I	3.3 V	BOOT	BOOT_CFG1_7	115		116	BOOT_CFG1_6	BOOT	3.3 V	I	K25
L23	I	3.3 V	BOOT	BOOT_CFG1_5	117		118	BOOT_CFG1_4	BOOT	3.3 V	I	L22
K24	I	3.3 V	BOOT	BOOT_CFG1_3	119		120	BOOT_CFG1_2	BOOT	3.3 V	I	L21
J25	I	3.3 V	BOOT	BOOT_CFG1_1	121		122	BOOT_CFG1_0	BOOT	3.3 V	I	L20
–	P	0 V	POWER	DGND	123		124	DGND	POWER	0 V	P	–
N19	O	3.3 V	DISP	DISP0_CLK	125		126	GPIO6_IO31	GPIO	3.3 V	I/O	N22
N21	O	3.3 V	DISP	DISP0_DRDY	127		128	DISP0_HSYNC	DISP	3.3 V	O	N25
P25	O	3.3 V	DISP	DISP0_CONTRAST	129		130	DISP0_VSYNC	DISP	3.3 V	O	N20
–	P	0 V	POWER	DGND	131		132	DGND	POWER	0 V	P	–
P24	O	3.3 V	DISP	DISP0_DAT0	133		134	DISP0_DAT1	DISP	3.3 V	O	P22
P23	O	3.3 V	DISP	DISP0_DAT2	135		136	DISP0_DAT3	DISP	3.3 V	O	P21
P20	O	3.3 V	DISP	DISP0_DAT4	137		138	DISP0_DAT5	DISP	3.3 V	O	R25
R23	O	3.3 V	DISP	DISP0_DAT6	139		140	DISP0_DAT7	DISP	3.3 V	O	R24
R22	O	3.3 V	DISP	DISP0_DAT8	141		142	DISP0_DAT9	DISP	3.3 V	O	T25
R21	O	3.3 V	DISP	DISP0_DAT10	143		144	DISP0_DAT11	DISP	3.3 V	O	T23
–	P	0 V	POWER	DGND	145		146	DGND	POWER	0 V	P	–
T24	O	3.3 V	DISP	DISP0_DAT12	147		148	DISP0_DAT13	DISP	3.3 V	O	R20
U25	O	3.3 V	DISP	DISP0_DAT14	149		150	DISP0_DAT15	DISP	3.3 V	O	T22
T21	O	3.3 V	DISP	DISP0_DAT16	151		152	DISP0_DAT17	DISP	3.3 V	O	U24
V25	O	3.3 V	DISP	DISP0_DAT18	153		154	DISP0_DAT19	DISP	3.3 V	O	U23
U22	O	3.3 V	DISP	DISP0_DAT20	155		156	DISP0_DAT21	DISP	3.3 V	O	T20
V24	O	3.3 V	DISP	DISP0_DAT22	157		158	DISP0_DAT23	DISP	3.3 V	O	W24
–	P	0 V	POWER	DGND	159		160	DGND	POWER	0 V	P	–

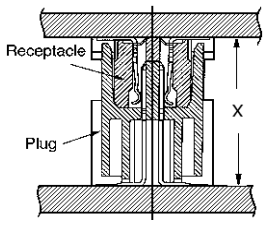
Table 6: Pinout connector X3

Ball	I/O	Level	Group	Signal	Pin		Pin	Signal	Group	Level	I/O	Ball
–	P	0 V	POWER	DGND	1		2	DGND	POWER	0 V	P	–
F04	I	–[6]	MIPI-CSI	CSI_CLK0M	3		4	MLB_CN	MLB	–[6]	O	A11
F03	I	–[6]	MIPI-CSI	CSI_CLK0P	5		6	MLB_CP	MLB	–[6]	O	B11
–	P	0 V	POWER	DGND	7		8	DGND	POWER	0 V	P	–
E04	I	–[6]	MIPI-CSI	CSI_D0M	9		10	MLB_DN	MLB	–[6]	I/O	B10
E03	I	–[6]	MIPI-CSI	CSI_D0P	11		12	MLB_DP	MLB	–[6]	I/O	A10
–	P	0 V	POWER	DGND	13		14	DGND	POWER	0 V	P	–
D01	I	–[6]	MIPI-CSI	CSI_D1M	15		16	MLB_SN	MLB	–[6]	I/O	A09
D02	I	–[6]	MIPI-CSI	CSI_D1P	17		18	MLB_SP	MLB	–[6]	I/O	B09
–	P	0 V	POWER	DGND	19		20	DGND	POWER	0 V	P	–
E01	I	–[6]	MIPI-CSI	CSI_D2M	21		22	DSI_CLK0M	MIPI-DSI	–[6]	O	H03
E02	I	–[6]	MIPI-CSI	CSI_D2P	23		24	DSI_CLK0P	MIPI-DSI	–[6]	O	H04
–	P	0 V	POWER	DGND	25		26	DGND	POWER	0 V	P	–
F02	I	–[6]	MIPI-CSI	CSI_D3M	27		28	DSI_D0M	MIPI-DSI	–[6]	O	G02
F01	I	–[6]	MIPI-CSI	CSI_D3P	29		30	DSI_D0P	MIPI-DSI	–[6]	O	G01
–	P	0 V	POWER	DGND	31		32	DGND	POWER	0 V	P	–
C5	O	2.5 V	XTAL	CLK2_N	33		34	DSI_D1M	MIPI-DSI	–[6]	I	H02
D5	O	2.5 V	XTAL	CLK2_P	35		36	DSI_D1P	MIPI-DSI	–[6]	I	H01
–	P	0 V	POWER	DGND	37		38	DGND	POWER	0 V	P	–
E11	I	3.0 V[7]	CONFIG	TAMPER	39		40	SPI-NOR_WP#	CONFIG	3.3 V	I	–

4.1.1.3 Connectors on STK-MBa6x

The connectors used on the STK-MBa6x are listed in Table 7.
If a different board-to-board distance is required, higher connectors can be used. Suitable types are to be taken from Table 7.

Table 7: Suitable carrier board mating connectors

Manufacturer	Pin count / Part number	Remark	Stack height (X)	
TE connectivity	40-pin: 5177986-1 160-pin: 5177986-8	Used on STK-MBa6x	5 mm	
TE connectivity	40-pin: 1-5177986-1 160-pin: 2-5179230-8	Alternative	6 mm	
TE connectivity	40-pin: 2-5177986-1 160-pin: 5179030-8	Alternative	7 mm	
TE connectivity	40-pin: 3-5177986-1 160-pin: 3-5177986-8	Alternative	8 mm	

Attention:	
	Depending on the selected TQMa6x, not all interfaces are available. Available interfaces are to be taken from the User's Manual and the pinout table of the TQMa6x.

6: See datasheets of i.MX6, (1), (2).
7: Use VSNVS_REF_OUT only as reference voltage.

4.1.2 I²C address mapping

4.1.2.1 Overview I²C bus

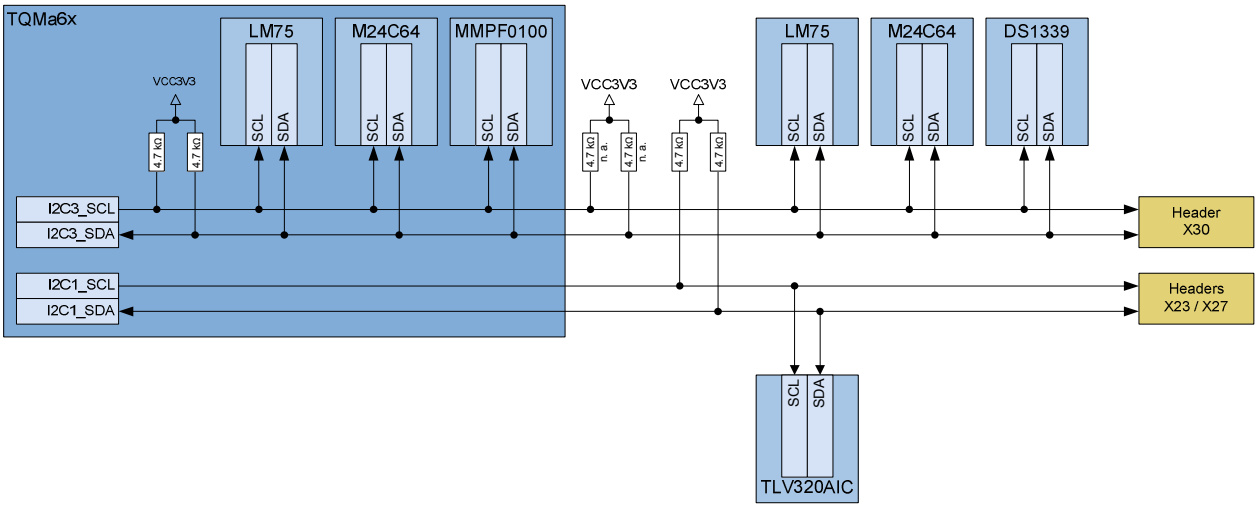


Illustration 3: Block diagram I2C bus

I2C1 and I2C3 are used on the Starterkit.
A temperature sensor, an EEPROM and an RTC can be addressed via I2C3.
The audio-codec is connected to I2C1. Table 8, Table 9 and Table 10 show the device addresses used.
Both interfaces are also available on headers.

Table 8: I2C1 address mapping – STK-MBa6x

			Address						
Device	Ref.	Hex	MSB			Binary			LSB
Audio Codec (TLV320AIC)	N1800	0x18	0	0	1	1	0	0	0

Table 9: I2C3 address mapping – TQMa6x

			Address						
Device	Ref.	Hex	MSB			Binary			LSB
Temperature sensor (LM75A)	–	0x48	1	0	0	1	0	0	0
EEPROM (M24C64)	–	0x50	1	0	1	0	0	0	0
PMIC (MMPF0100)	–	0x08	0	0	0	1	0	0	0

Table 10: I2C3 address mapping – STK-MBa6x

			Address						
Device	Ref.	Hex	MSB			Binary			LSB
Temperature sensor (LM75A)	D2000	0x49	1	0	0	1	0	0	1
EEPROM (M24C64)	D2002	0x4F	1	0	0	1	1	1	1
RTC (DS1339)	D2003	0x68	1	1	0	1	0	0	0

Attention:	
	Attention when using I2C3. Since the PMIC can be addressed via this interface, errors on the bus can lead to instabilities of the TQMa6x!

4.1.3 Temperature sensor

4.1.3.1 Overview temperature sensor

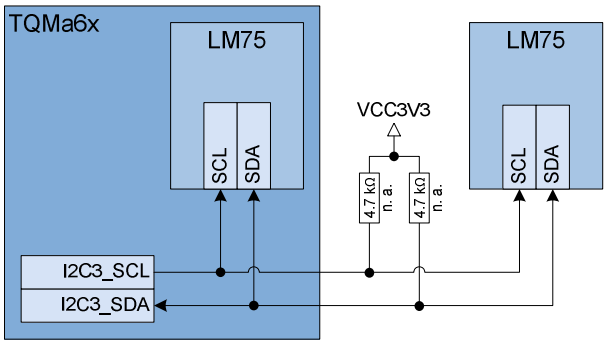


Illustration 4: Block diagram temperature sensor

An LM75A sensor is available on the TQMa6x and on the STK-MBa6x, to monitor the temperature.
Both sensors are connected via I2C3 and have an individual device address.

The address of the sensor on the STK-MBa6x can be changed by reassembling some resistors.
If the address is changed, attention has to be paid that no address conflicts with already existing I2C device occur.

Table 11: Electrical characteristics LM75A

Parameter	Value	Range	Unit
Accuracy	−2 … +2 −3 … +3	−25 … +100 −55 … +125	°C °C
Resolution	0.125	11 Bit	–

4.1.3.2 Position of LM75A

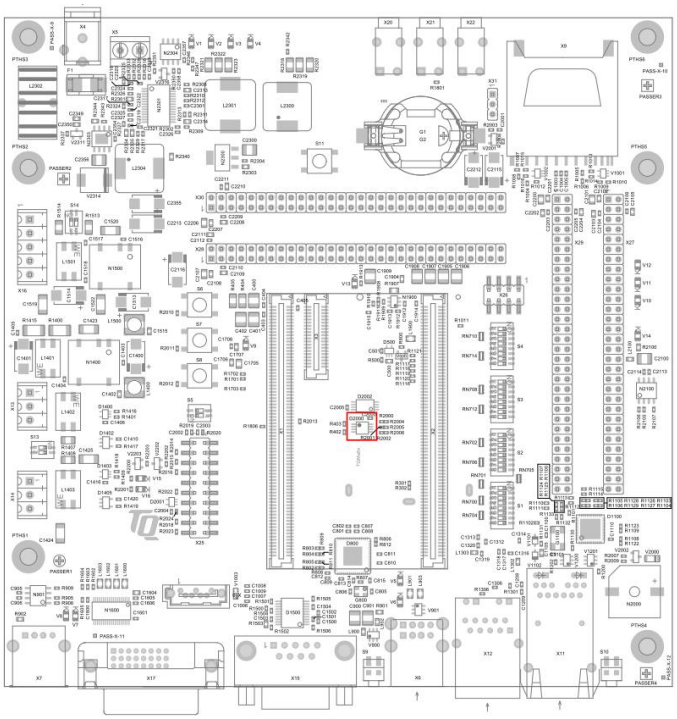


Illustration 5: Position of LM75A (D2000) – STK-MBa6x

The LM75A is on the top side of the STK-MBa6x, in the middle of the plug-in position for the TQMa6x.

4.1.4 EEPROM

4.1.4.1 Overview EEPROM

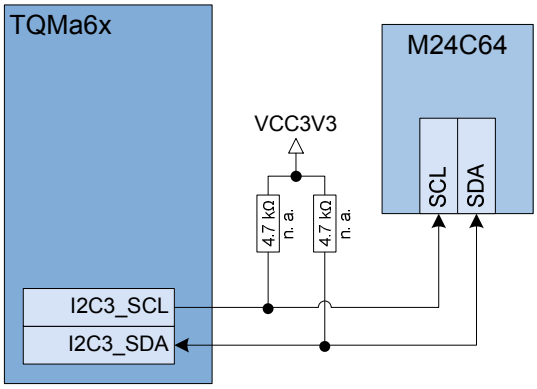


Illustration 6: Block diagram EEPROM

The STK-MBa6x provides a 64 Kbit EEPROM to save data (e.g., the MAC addresses of the Ethernet PHYs).

4.1.4.2 Position of EEPROM

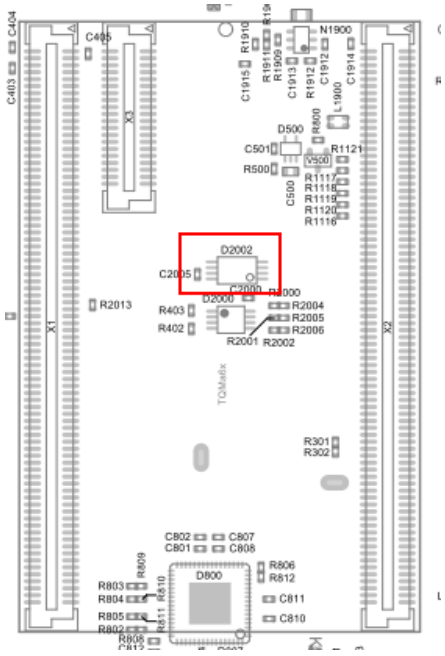


Illustration 7: Position of EEPROM (D2002)

The EEPROM is on the top side, in the middle of the plug-in position for the TQMa6x.

4.1.5 RTC

4.1.5.1 Overview RTC

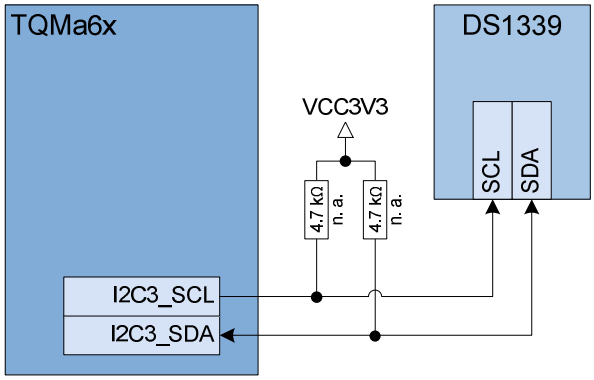


Illustration 8: Block diagram RTC

The STK-MBa6x provides an RTC. Another RTC is provided by the i.MX6 of the TQMa6x.
A lithium battery with very low self-discharge is available as a backup supply for both RTCs.
A jumper connects the battery with the desired RTC.

Table 12: RTC supply – jumper settings

Component	Jumper X31	Remark
CPU RTC	1 – 2	PMIC connects the RTC of the CPU with the battery.
STK-MBa6x RTC	2 – 3	RTC on STK-MBa6x is connected with the battery.

The increased current consumption must be considered, if the RTC in the i.MX6 is used. This leads to a fast discharge of the battery. More detailed information can be found in the User's Manual of the TQMa6x.
For the RTCs installed on the STK-MBa6x the following applies:

Table 13: Electrical parameters DS1339 RTC

Parameter	Min.	Typ.	Max.	Unit
Backup voltage at DS1339-VBACKUP (V_{RTC})	1.3	–	3.7	V
Current consumption DS1339	–	0.4	0.7	µA

4.1.5.2 Component and position of RTC

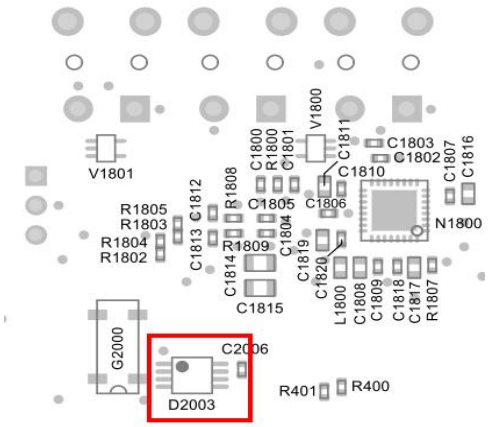


Illustration 9: Position of RTC (D2003)

The RTC on the STK-MBa6x is on the bottom side, near the audio codec.

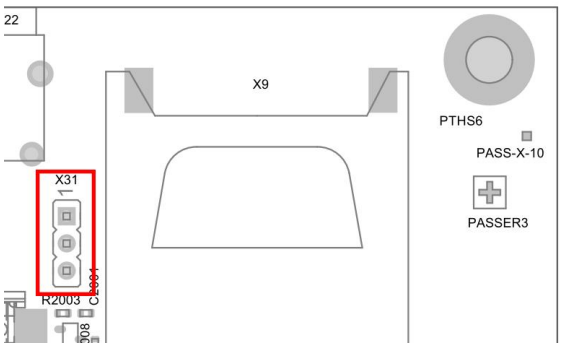


Illustration 10: Header for selection of battery supply (X31)

The header for the battery supply is on the top side, next to the SD card holder.

Table 14: Pinout X31

Pin	Pin name	Signal	Dir.
1	1	LICELL	P
2	2	VBATT	P
3	3	VRTC	P

Table 15: Components for RTC backup supply

Manufacturer / Number	Description	Package
Sony / CR2032	Lithium battery 3.0 V, 220 mAh	MECH
RENATA / SMTU2032	CR2032 battery holder	SMD2
FISCHER ELEKTRONIK / SL-11-124-3-G	3-pin header, straight, 2.54 mm pitch	THT3

4.1.6 Power and Reset

4.1.6.1 Overview Power and Reset

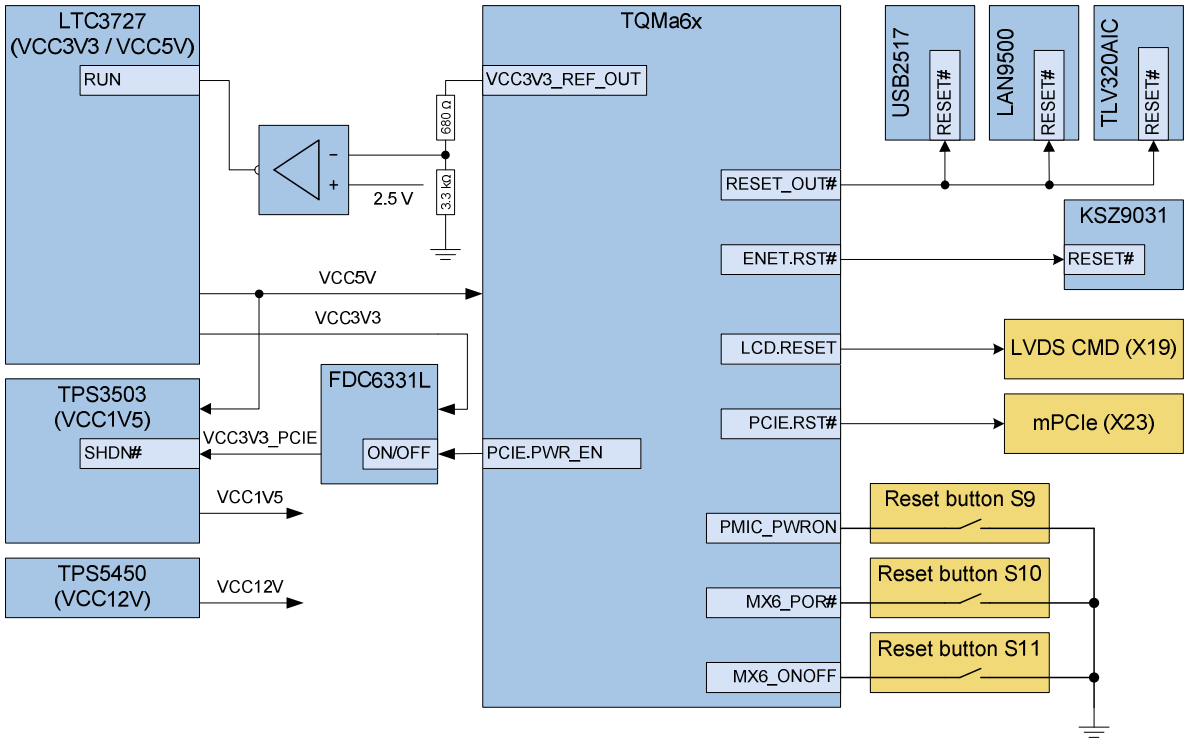


Illustration 11: Block diagram Power and Reset

The STK-MBa6x provides several options to trigger a complete or partial reset of the assembly.
The STK-MBa6x provides four signals to reset sections of the circuit.

Table 16: STK-MBa6x Reset signals

STK-MBa6x Reset-Signal	Description
RESET_OUT	Signal resets USB hub (USB2517), USB Ethernet PHY (LAN9500) and audio-codec (TLV320AIC)
ENET.RST#	Signal resets the Gbit Ethernet PHYs (KSZ9031)
LCD.RESET	Signal resets a connected display
PCIE.RST#	Signal resets the PCIe device

Two signals are provided for selective reset of the TQMa6x. [8]

Table 17: TQMa6x Reset signals

TQMa6x Reset-Signal	Description
PMIC_PWRON	Signal triggers a restart of the PMIC Restarting the PMIC automatically triggers a reset of the CPU
MX6_POR#	Signal restarts the i.MX6, the PMIC is not affected

Two signals are provided to control the switching regulators.

8: The exact functions and characteristics of the signals is to be taken from the manual of the TQMa6x (7), the PMIC (5), and the CPU (1), (2).

Table 18: Switching regulator control

Signal	Description
PCIE.PWR_EN	This signal activates the power-switch in the supply of the PCIe interface. As soon as it is activated, N2302 begins to generate the 1.5 V.
VCC3V3_REF_OUT	This signal indicates, whether the TQMa6x is in the Power-Down mode. In the Power-Down mode the 3.3 V generated by the TQMa6x are switched off. As soon as this voltage drops below 3 V, the 3.3 V generated by the STK-MBa6x are also switched off, to prevent a cross supply.

4.1.6.2 Components and position Reset-Button / Power-Button

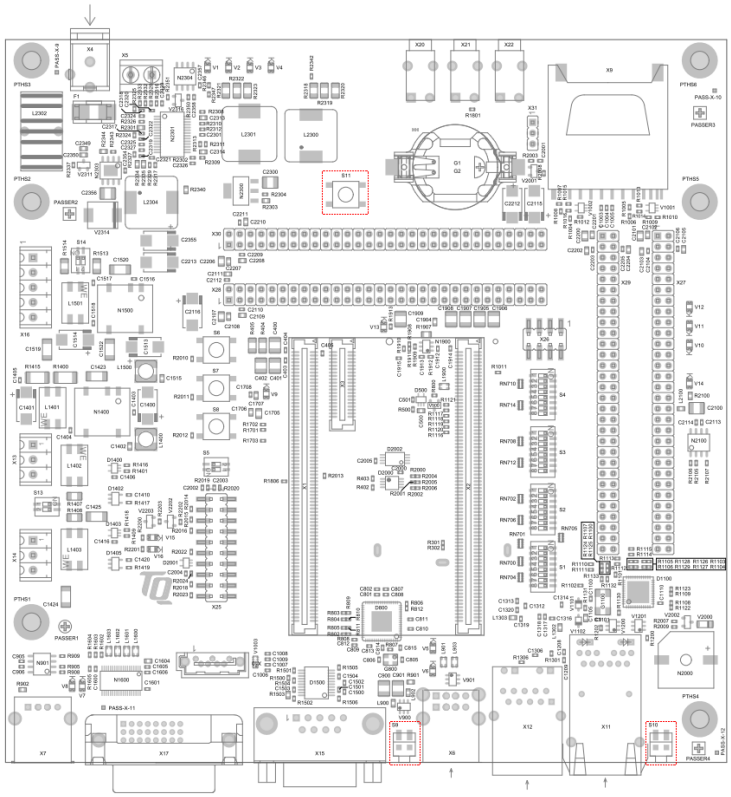


Illustration 12: Position of Reset-Button / Power-Button (S9, S10, S11)

Table 19: Components Reset button / Power button

Switch	Manufacturer / Number	Description	Package
S9, S10	Knitter switch / TMSE 10J-RA	Push button	SMT4
S11	Knitter switch / TSS 61N	Push button	SMT4

4.1.7 Power supply

4.1.7.1 Overview power supply

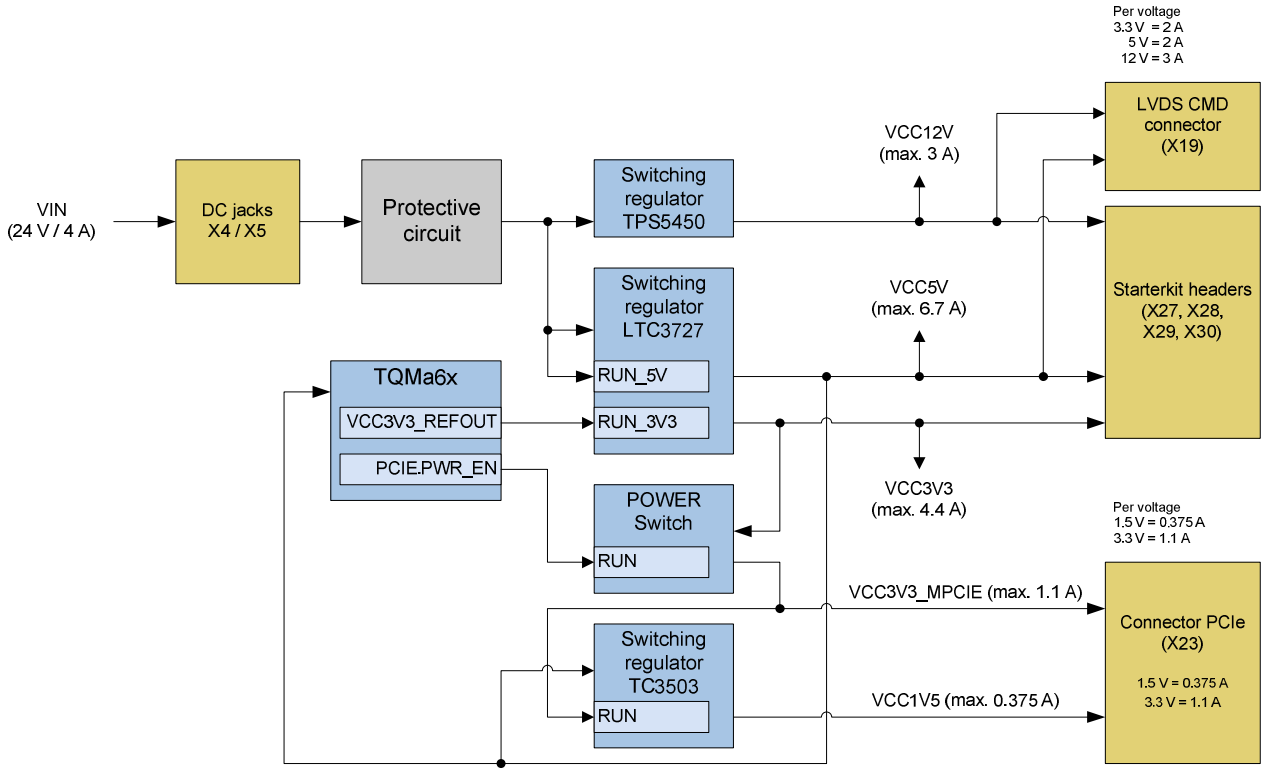


Illustration 13: Block diagram power supply

The STK-MBa6x is supplied with 24 V via X4 or X5. From this voltage 1.5 V, 3.3 V, 5 V and 12 V are generated on the STK-MBa6x. These voltages are used to supply the components on the STK-MBa6x.

Additionally, 3.3 V, 5 V and 12 V are available at each of the four headers (X27, X28, X29 and X30). 5 V and 12 V are available at the LVDS-CMD connector (X19). All five connectors share the available power (2 A 3.3 V, 2 A 5 V, 3 A 12 V).

The PCIe connector is supplied with 1.5 V and 3.3 V. 1.5 V is generated from 3.3 V and is only available at the PCIe connector. The 1.5 V rail can supply 0.375 A, the 3.3 V rail can supply 1.1 A.

Attention:	
	In the own design, the switching regulator for VCC3V3 should be switched on or off with the signal VCC3V3_REFOUT from the TQMa6x, to avoid cross supply and errors in the power-up/down sequence. [9]

9: Attention: When the PMIC is switched off, the voltage VCC3V3_REFOUT (from the TQMa6x) drops to approx. 2.7 V due to cross-supply effects of the still activated 3.3 V (on the STK-MBa6x). It must be ensured that the circuitry can respond to this level.

4.1.7.2 Protective circuit and power consumption

The 3.3 V / 5 V and the 12 V switching regulators are supplied with V_{IN}.
The protective circuit (Illustration 14) has the following characteristics:

- Fuse
- Excess voltage protection diode
- PI filter
- Inverse-polarity protection
- Capacitors to voltage smoothing

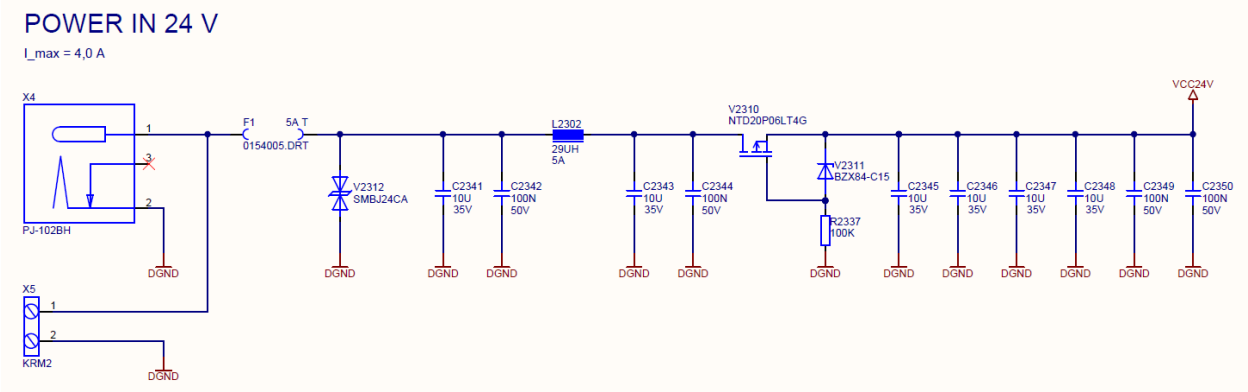


Illustration 14: Protective circuit for VIN

Table 20: Parameter of protective circuit

Parameter	Min.	Typ.	Max.	Unit
Overcurrent limitation by fuse (inertly)	–	5	–	A
Excess voltage limitation by SMBJ24CA	26.7	–	26.9	V

Under full load the assembly takes 94 W (all supply voltages are loaded with maximum current). The power supply used has to be selected accordingly. In most applications the power consumption will be, however, significantly lower.

4.1.7.3 Electrical parameters switching regulator

The parameters in the following tables apply for the switching regulators LTC3727, LT3503 and TPS5450.

Table 21: Parameter LTC3727

Parameter	Min.	Typ.	Max.	Unit	Remark
VCC3V3					
Output voltage	3.25	–	3.35	V	1 % feedback resistors
Output current	–	–	3	A	
Ripple	– –	52 53	– –	mV_{pp} mV_{pp}	(I_{OUT} = 2 A) (I_{OUT} = 4.5 A)
Load step change – add load Drop Control time	 – –	 64 125	 – –	 mV µs	I_{OUT} = 0 A ⇨ 2 A
Load step change – remove load overshot Control time	 – –	 63 100	 – –	 mV µs	I_{OUT} = 2 A ⇨ 0 A
VCC5V					
Output voltage	4.93	–	5.08	V	
Output current	–	–	6.7	A	
Ripple	– –	61 64	– –	mV_{pp} mV_{pp}	(I_{OUT} = 2 A) (I_{OUT} = 7 A)
Load step change – add load drop Control time	 – –	 54 150	 – –	 mV µs	I_{OUT} = 0 A ⇨ 2 A
Load step change – remove load overshot Control time	 – –	 54 125	 – –	 mV µs	I_{OUT} = 2 A ⇨ 0 A

Table 22: Parameter TPS5450

Parameter	Min.	Typ.	Max.	Unit	Remark
Output voltage	11.4	–	12.6	V	1 % feedback resistors
Output current	–	–	3	A	
Ripple	– –	36 46	– –	mV_{pp} mV_{pp}	(I_{OUT} = 1 A) (I_{OUT} = 3 A)
Load step change – add load drop Control time	 – –	 552 500	 – –	 mV µs	I_{OUT} = 0.1 A ⇨ 1 A
Load step change – remove load overshot Control time	 – –	 210 12.5	 – –	 mV ms	I_{OUT} = 1 A ⇨ 0.1 A

Table 23: Parameter LT3503

Parameter	Min.	Typ.	Max.	Unit	Remark
Output voltage	1.425	–	1.575	V	1 % feedback resistors
Output current	–	–	0.375	A	
Ripple	– –	8 27	– –	mV_{pp} mV_{pp}	(I_{OUT} = 0 A) (I_{OUT} = 0.75 A)
Load step change – add load drop Control time	 – –	 142 15	 – –	 mV µs	I_{OUT} = 0 A ⇨ 0.75 A
Load step change – remove load overshot Control time	 – –	 66.4 25	 – –	 mV µs	I_{OUT} = 0.75 A ⇨ 0 A

4.1.7.4 Connectors X4, X5

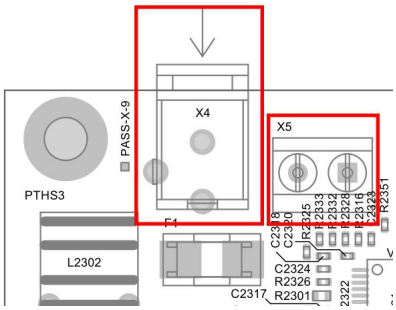


Illustration 15: Position of connectors (X4, X5)

Table 24: Devices power supply

Manufacturer / Number	Description	Package
Cui Stack / PJ-102BH	DC jack 2.5 mm / 5.5 mm, nominal: 5 A / 24 V	THT3
Lumberg / KRM2	2-pin screw terminal, 250 V / 15 A	THT2

4.2 Communication interfaces

4.2.1 USB 2.0 Hi-Speed Host

4.2.1.1 Overview USB-Hub

A USB hub provides five USB 2.0 Hi-Speed host interfaces.
The hub provides an upstream port and seven downstream ports.

The USB connectors are supplied with 5 V by power distribution switches. The components used provide current monitoring and can switch off the bus voltage with overload and/or overheating. USB host 2 and 3 are routed to a stacked USB Type-A connector (X6). USB host 6 is routed to a single Type-A connector (X7). USB host 4 is available at Starterkit header X27 and USB host 7 at the LVDS-CMD connector (X19).

On the STK-MBa6x, USB host 1 is connected to the USB-Ethernet-PHY (LAN9500) and USB host 5 to the Mini PCIe interface (X23).

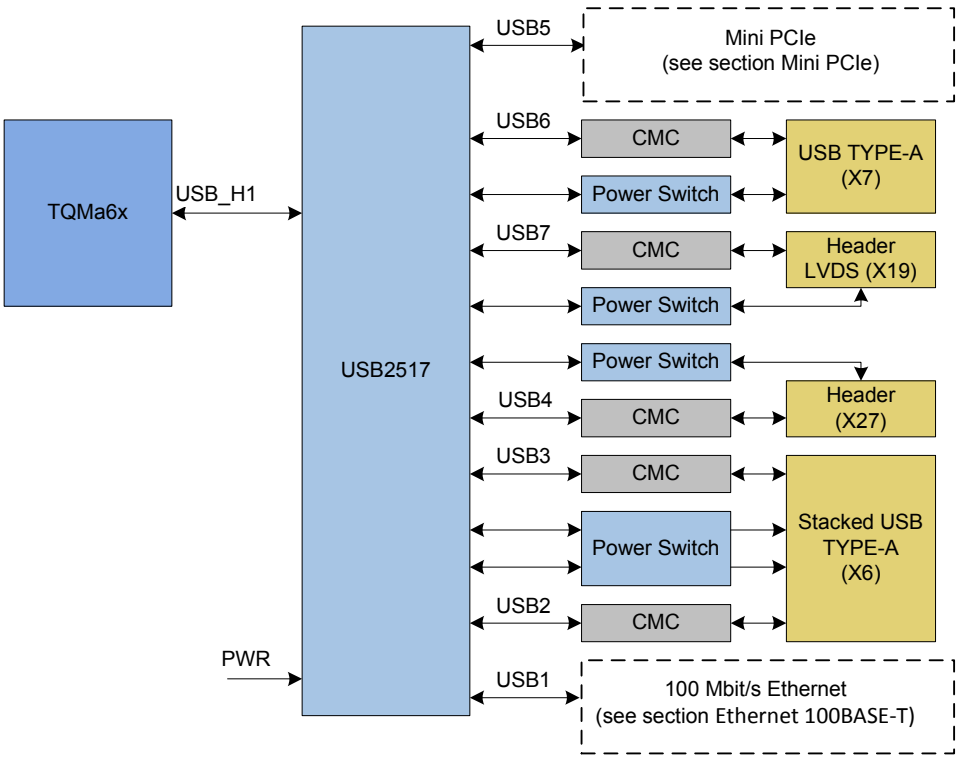


Illustration 16: Block diagram USB-Hub

4.2.1.2 Characteristics of USB-Hub

The USB host port of the TQMa6x provides a theoretical data rate of 480 Mbit/s. The data rate is shared amongst the connected ports. The data rates of the ports can significantly deviate depending on the hardware and software used.

Table 25: Characteristics USB

Parameter	Min.	Typ.	Max.	Unit	Remark
Voltage	4.75	5.00	5.25	V	
Current	–	500	900	mA	
Load step change	–	–90	–	mV	Host 2 – when adding a load of 500 mA
Read rate	–	23.7	–	MByte/s	Host 2 - USB-HDD an Port 3: 1.2 GByte file, 16 MByte block size
Write rate	–	18.3	–	MByte/s	Host 2 - USB-HDD an Port 3: 1.2 GByte file, 16 MByte block size

4.2.1.3 Connectors and pinout of USB

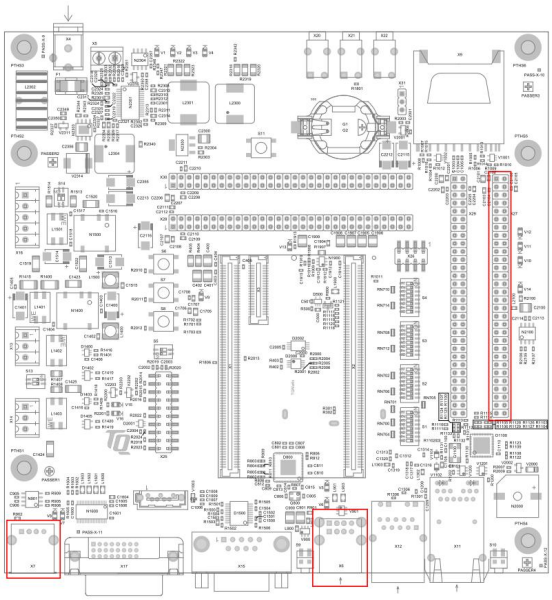


Illustration 17: Position of USB (X6, X7, X27)

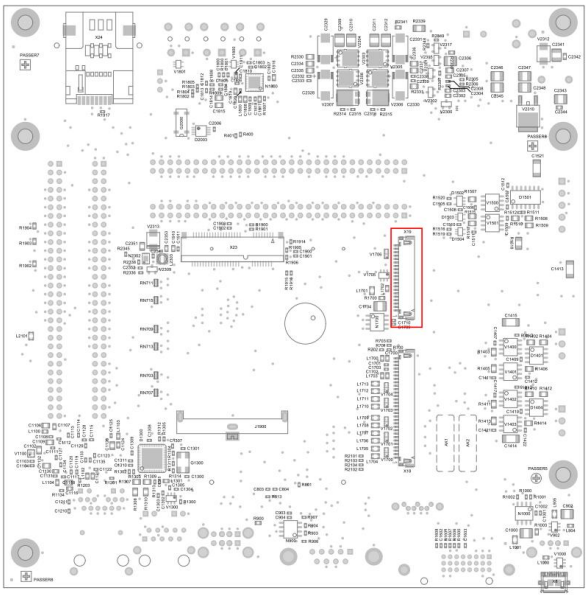


Illustration 18: Position of LVDS-CMD (X19)

Table 26: Devices USB Hub

Manufacturer / Number	Description	Package
Yamaichi / USB-A-002A	Dual port USB receptacle, type USB-A, U_N=30 V AC_{RMS} / I_N=1 A	THT8
Molex / 67643-2910	Single port USB receptacle type USB-A, U_N=30 V / I_N=1.5 A	THT4
Hirose / DF19G-20P-1H	Board-to-Cable connector 20-pin, 1 mm pitch	SMT20
Fischer Elektronik / SL 22 124 60 G	Header, 2.54 mm pitch, 2 × 30 pins	THT30

Table 27: Pinout USB-Host 2/3 (X6)

Pin	Pin name	Signal	Dir.	Remark
1A	VBUS	USB_H2_VBUS	P	100 µF to DGND; EMI filter
2A	D–	USB_H2_D_N	I/O	Common mode choke in series
3A	D+	USB_H2_D_P	I/O	Common mode choke in series
4A	DGND	DGND	P	
1B	VBUS	USB_H3_VBUS	P	100 µF to DGND; EMI filter
2B	D–	USB_H3_D_N	I/O	Common mode choke in series
3B	D+	USB_H3_D_P	I/O	Common mode choke in series
4B	DGND	DGND	P	
M1-4	DGND	DGND	P	

Table 28: Pinout USB-Host 6 (X7)

Pin	Pin name	Signal	Dir.	Remark
1A	VBUS	USB_H6_VBUS	P	100 µF to DGND; EMI filter
2A	D–	USB_H6_D_N	I/O	Common mode choke in series
3A	D+	USB_H6_D_P	I/O	Common mode choke in series
4A	DGND	DGND	P	
M1-2	DGND	DGND	P	

Table 29: Pinout USB-Host 7 (X19)

Pin	Pin name	Signal	Dir.	Remark
11	VBUS	USB_H7_VBUS	P	100 µF to DGND; EMI filter
13	D–	USB_H7_D_N	I/O	Common mode choke in series
14	D+	USB_H7_D_P	I/O	Common mode choke in series

Table 30: Pinout USB-Host 4 (X27)

Pin	Pin name	Signal	Dir.	Remark
34	VBUS	USB_H4_VBUS	P	100 µF to DGND; EMI filter
36	D–	USB_H4_D_N	I/O	Common mode choke in series
38	D+	USB_H4_D_P	I/O	Common mode choke in series

4.2.2 USB 2.0 Hi-Speed OTG

4.2.2.1 Overview USB 2.0 Hi-Speed OTG

The USB OTG interface of the TQMa6x is provided on the STK-MBa6x. The OTG compatibility is maintained by a 5-pin Micro-AB connector. The ID signal is directly routed to the CPU.

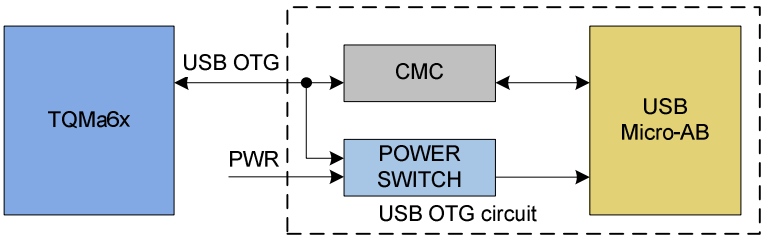


Illustration 19: Block diagram USB 2.0 Hi-Speed OTG

The interface can be a client or a host. To use this feature the appropriate software support is however necessary.

4.2.2.2 Characteristics of USB 2.0 Hi-Speed OTG

The OTG port provides a theoretical data rate of 480 Mbit/s. The data rate can significantly deviate depending on the hardware and software used.

Table 31: Characteristics USB 2.0 Hi-Speed OTG

Parameter	Min.	Typ.	Max.	Unit	Remark
Voltage	4.75	5.00	5.25	V	
Current	–	500	900	mA	
Load step change	–	–85	–	mV	When adding a load of 500 mA
Read rate	–	23.7	–	MByte/s	USB-HDD at USB OTG: 1.2 GByte file, 16 MByte block size
Write rate	–	18.3	–	MByte/s	USB-HDD at USB OTG: 1.2 GByte file, 16 MByte block size

4.2.2.3 Connector and pinout USB 2.0 Hi-Speed OTG

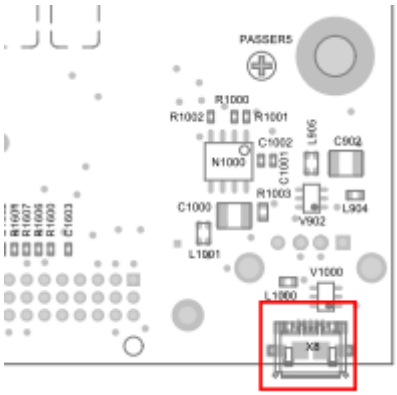


Illustration 20: Position of USB 2.0 Hi-Speed OTG (X8)

Table 32: Device USB Hub

Manufacturer / Number	Description	Package
TE Connectivity / 1981584-1	USB receptacle, type Micro-AB	SMT8

Table 33: Pinout USB-Host OTG (X8)

Pin	Pin name	Signal	Dir.	Remark
1	VBUS	USB_OTG_VBUS	P	100 µF to DGND; EMI filter, I_{max} = 100 mA
2	D–	USB_OTG_D_N	I/O	Common mode choke in series
3	D+	USB_OTG_D_P	I/O	Common mode choke in series
4	ID	USB_OTG.ID	I	
5	DGND	DGND	P	
M1-6	DGND	DGND	P	

4.2.3 Ethernet 100BASE-T

4.2.3.1 Overview Ethernet 100BASE-T

The 100 Mbit/s Ethernet interface is provided by a USB to Ethernet controller.
The LAN9500 is connected to USB host 1.
The following illustration shows the connection.

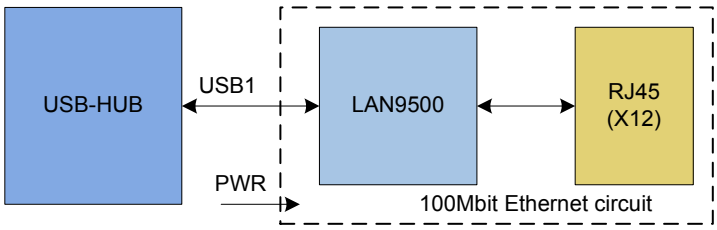


Illustration 21: Block diagram Ethernet 100 BASE-T

Jack X12 contains integrated magnetics and two status LEDs.

4.2.3.2 Characteristics Ethernet 100BASE-T

This Ethernet interface corresponds to the IEEE 802.3 standard and offers an Auto-MDI-X detection.

Table 34: Characteristics Ethernet 100BASE-T

Parameter	Min.	Typ.	Max.	Unit	Remark
Transfer rate UDP	–	85.2	–	Mbit/s	Upstream – tested with 100 m CAT6 cable
Transfer rate TCP	–	75.4	–	Mbit/s	Upstream – tested with 100 m CAT6 cable
Transfer rate UDP	–	82.0	–	Mbit/s	Downstream – tested with 100 m CAT6 cable
Transfer rate TCP	–	59.4	–	Mbit/s	Downstream – tested with 100 m CAT6 cable
Cable length	100	–	–	m	Tested with 100 m CAT6 cable

4.2.3.3 Connector and pinout Ethernet 100BASE-T

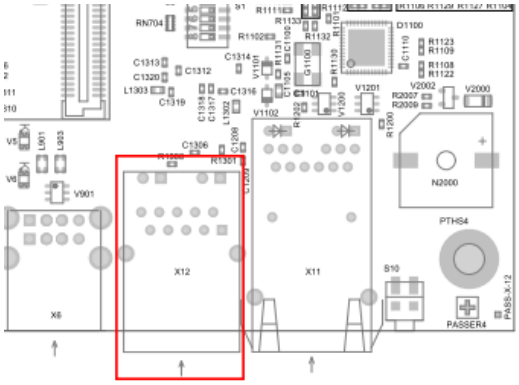


Illustration 22: Position of Ethernet 100BASE-T (X12)

Table 35: Device Ethernet 100BASE-T

Manufacturer / Number	Description	Package
Würth / 7499210124A WUE	RJ45 receptacle, 10/100BASE-T, integrated magnetics	THT 14

Table 36: Pinout Ethernet 100BASE-T

Pin	Pin name	Signal	Dir.	Remark
1	TX+	ETH100_TX_P	I/O	
2	TX–	ETH100_TX_N	I/O	
3	RX+	ETH100_RX_P	I/O	
4	–	–	–	
5	–	–	–	
6	RX–	ETH100_RX_N	I/O	
7	–	–	–	
8	–	–	–	

4.2.4 Ethernet 1000BASE-T

4.2.4.1 Overview Ethernet 1000BASE-T

The STK-MBa6x provides a Gigabit Ethernet interface.
This is implemented by the Micrel PHY KSZ9031.

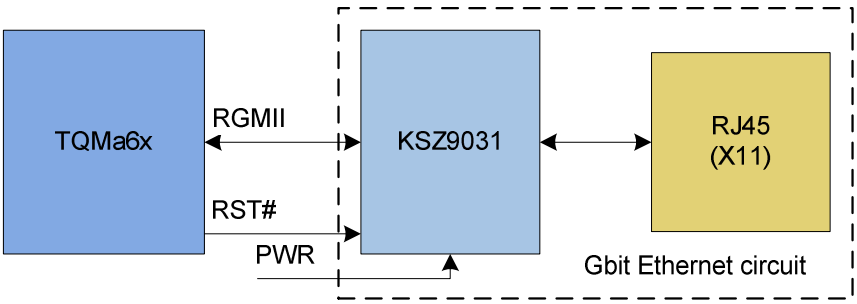


Illustration 23: Block diagram Ethernet 1000BASE-T

The RJ45 jack (X11) contains integrated magnetics and two status LEDs.

4.2.4.2 Characteristics Ethernet 1000BASE-T

The PHY has the following characteristics:

- Auto-negotiation capable
- Different speeds (10/100/1000 Mbps)
- Duplex-Modi (full/half)
- IEEE 802.3 compatible
- Wake-on-LAN
- Jumbo Frame Support

Table 37: Characteristics Ethernet 1000BASE-T

Parameter	Min.	Typ.	Max.	Unit	Remark
Transfer rate TCP	–	–	286	Mbit/s	Upstream, 5 m cable
Transfer rate TCP	–	–	510	Mbit/s	Downstream, 5 m cable
Transfer rate TCP	–	–	130 273	Mbit/s	Upstream, 5 m cable Downstream, 5 m cable

Attention:	
	The interface operates in Master-Mode on account of an erratum in the PHY (7). For this reason it is not possible to connect the STK-MBa6x to other devices whose Ethernet interface also works in Master-Mode.

4.2.4.3 Connector and pinout Ethernet 1000BASE-T

Table 38: Device Ethernet 1000BASE-T

Manufacturer / Number	Description	Package
Pulse / JK0-0145NL	RJ45 receptacle, 10/100/1000BASE-T, integrated magnetics	THT16

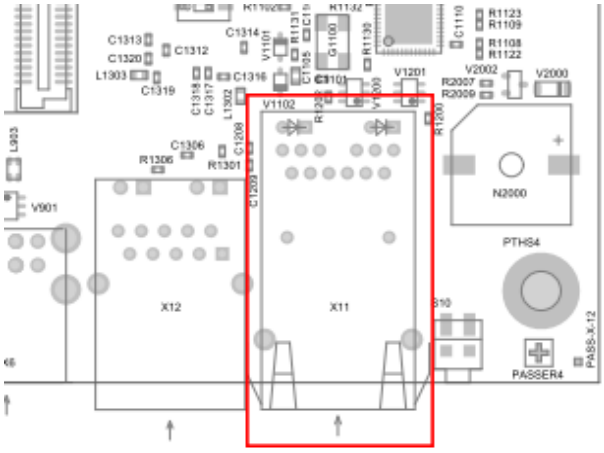


Illustration 24: Position of Ethernet 1000BASE-T (X11)

Table 39: Pinout Ethernet 1000BASE-T

Pin	Pin name	Signal	Dir.
1	D1+	ETH1G_D1_P	I/O
2	D1–	ETH1G_D1_N	I/O
3	D2+	ETH1G_D2_P	I/O
4	D3+	ETH1G_D3_P	I/O
5	D3–	ETH1G_D3_N	I/O
6	D2–	ETH1G_D2_N	I/O
7	D4+	ETH1G_D4_P	I/O
8	D4–	ETH1G_D4_N	I/O

4.2.5 CAN

4.2.5.1 Overview CAN

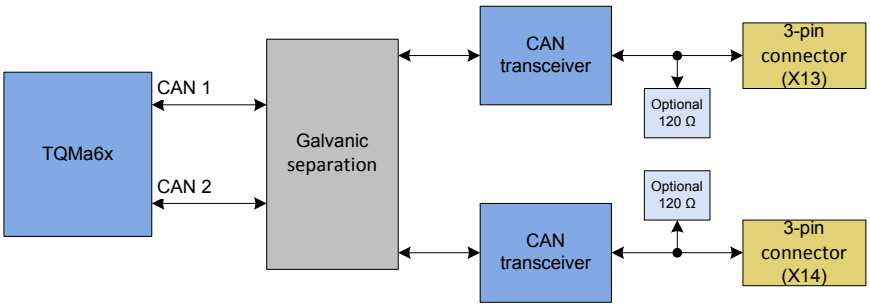


Illustration 25: Block diagram CAN

Both CAN interfaces of the STK-MBa6x are directly connected to the CAN ports of the TQMa6x and are made available at the 3-pin connectors X13 and X14. Both interfaces are galvanically separated.
The CAN interfaces are galvanically not separated among themselves.

4.2.5.2 Characteristics CAN

The high speed mode is configured by default using a configuration resistor at the input RS of the CAN transceiver MCP2551 (390 Ω to Ground è maximum slew rate).

The high speed mode supports data rates up to 1 Mbit/s or maximum cable length. When required, the resistor at the RS input can be increased (10 … 120 kΩ) to reduce the slew rate. [10]

The CAN signals can be terminated with 120 Ω using DIP switches S13-1 and S13-2.

Table 40: CAN DIP switch settings

Switch	Interface	ON	OFF
S13-1	CAN1	CAN1 terminated with 120 Ω	CAN1 not terminated
S13-2	CAN2	CAN2 terminated with 120 Ω	CAN2 not terminated

The following characteristics apply to the interfaces:

Table 41: Characteristics CAN

Parameter	Min.	Typ.	Max.	Unit	Remark
Transfer rate	–	–	2.0	Mbaud	Tested up to 2.5 Mbaud
Line length	–	–	100	m	CAT.6 cable at 0.6 Mbaud
Line length	–	–	0.1	m	CAT.5 cable at 2 Mbaud
Electric strength	–	–	1.0	kV	
Output voltage CANL	0.5	1.6	2.25	V	Dominant
Output voltage CANL	2.0	2.58	3.0	V	Recessive
Output voltage CANH	2.75	3.7	4.5	V	Dominant
Output voltage CANH	2.0	2.58	3.0	V	Recessive
Insulation clearance	1.4	–	–	mm	Inner layer
Insulation clearance	2.6	–	–	mm	Outer layer

10: See data sheet MCP2551.

4.2.5.3 Connector and pinout of CAN

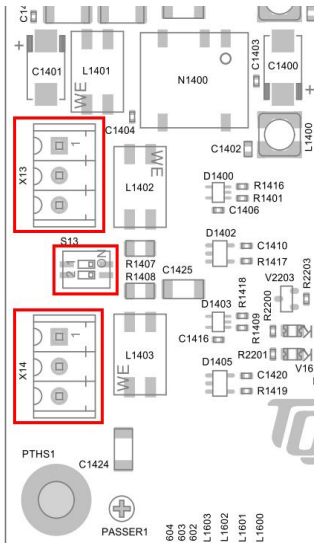


Illustration 26: Position of CAN (X13, X14, S13)

Table 42: Devices CAN

Manufacturer / Number	Description	Package
Phoenix Contact / MCV 1,5/ 3-G-3,5	3-pin housing, 160 V / 8 A, 3.5 mm pitch	THT3
NIDEC COPAL ELECTRONICS / CHS-02TA	DIP switch, I_{max} = 0.1 A	SMT4

Table 43: Pinout CAN1 (X13)

Pin	Pin name	Signal	Dir.	Remark
1	CAN_H	CAN1_H	I/O	Galvanically separated
2	CAN_L	CAN1_L	I/O	Galvanically separated
3	DGND	DGND_CAN	P	Galvanically separated

Table 44: Pinout CAN2 (X14)

Pin	Pin name	Signal	Dir.	Remark
1	CAN_H	CAN2_H	I/O	Galvanically separated
2	CAN_L	CAN2_L	I/O	Galvanically separated
3	DGND	DGND_CAN	P	Galvanically separated

4.2.6 RS485

4.2.6.1 Overview RS485

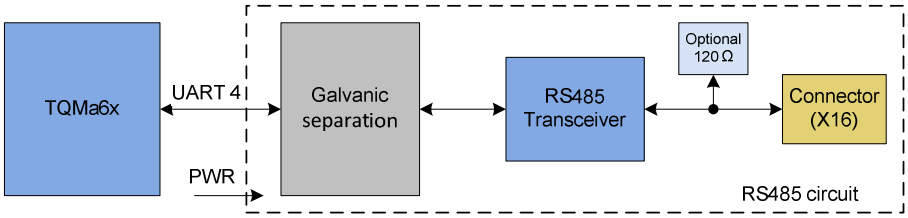


Illustration 27: Block diagram RS485

The UART4 interface of the TQMa6x is routed to an RS485 transceiver (SP491), which provides the signals at the 9-pin D-Sub connector X16. The RS485 interface is galvanically separated.

4.2.6.2 Characteristics RS485

In full-duplex mode the interface can operate with a maximum data rate of 1 Mbit/s. With an assembly option half-duplex is also possible.

Table 45: RS485 mode settings

Modus	R1511	R1512	Remark
Full-duplex	n.a.	0 Ω	Receiver always active (default)
Half-duplex	0 Ω	n.a.	Receiver controlled by CTS# (UART4.CTS#)

The RS485 signals can be terminated with 120 Ω using DIP switches S14-1 and S14-2.

Table 46: RS485 DIP switch settings

Switch	Interface	ON	OFF
S14-1	RS485	Receive path terminated with 120 Ω	Receive path not terminated
S14-2	RS485	Transmit path terminated with 120 Ω	Transmit path not terminated

The following characteristics apply to the interface:

Table 47: Characteristics RS485

Parameter	Min.	Typ.	Max.	Unit	Remark
Transfer rate	–	–	460.8	kbit/s	Tested up to 921.6 kbit/s with max. permitted error rate of 3.3 %
Error rate	–	–	0.9	%	At 115.2 kbit/s with 1.8 m cable
Error rate	–	–	3.3	%	At 460.8 kbit/s with 1.8 m cable
Electric strength	–	–	1	kV	
Output voltage RS485_TXD	2	5.32	5.5	V	High-Level
Output voltage RS485_TXD	0	0.24	0.8	V	Low-Level
Input voltage RS485_RXD	2	5.2	5.5	V	High-Level
Input voltage RS485_RXD	0	0.36	0.8	V	Low-Level
Insulation clearance	1.4	–	–	mm	Inner layer
Insulation clearance	2.6	–	–	mm	Outer layer

4.2.6.3 Connector and pinout RS485

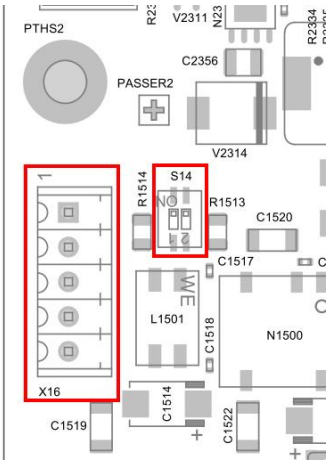


Illustration 28: Position of RS485 (X16)

Table 48: Devices RS485

Manufacturer / Number	Description	Package
Phoenix Contact / MCV1,5/5-G-3,5	5-pin housing , 160 V / 8 A, 3.5 mm pitch	THT5
NIDEC COPAL ELECTRONICS / CHS-02TA	DIP switch, I_{max} = 0.1 A	SMT4

Table 49: Pinout RS485 (X16)

Pin	Pin name	Signal	Dir.	Remark
1	A	RS485_A	I	Galvanically separated
2	B	RS485_B	I	Galvanically separated
3	Y	RS485_Y	O	Galvanically separated
4	Z	RS485_Z	O	Galvanically separated
5	DGND	DGND_ RS485	P	Galvanically separated

4.2.7 RS232

4.2.7.1 Overview RS232

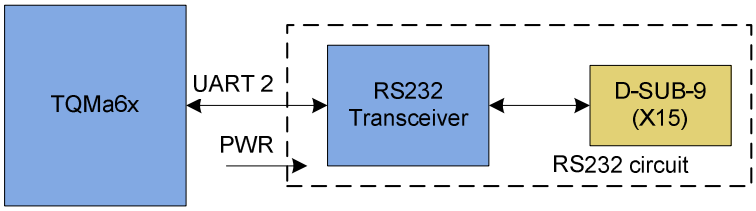


Illustration 29: Block diagram RS232

The UART2 interface of the TQMa6x is routed to transceiver SP3222E, which provides the signals at the 9-pin D-Sub connector X15. For UART2 the handshake signals RTS# and CTS# are available.

The interface is used to output debug information.

Additional information (e.g.: default baud rate) can be found in the TQMa6x Support-Wiki.

4.2.7.2 Characteristics RS232

The following characteristics apply to the RS232 interface:

Table 50: Characteristics RS232

Parameter	Min.	Typ.	Max.	Unit	Remark
Line length	–	–	120	m	Measured with 57,600 baud
Error rate	–	0.2	–	%	At 115.2 kbit/s, 8N1, with 3 m cable

4.2.7.3 Connector and pinout RS232

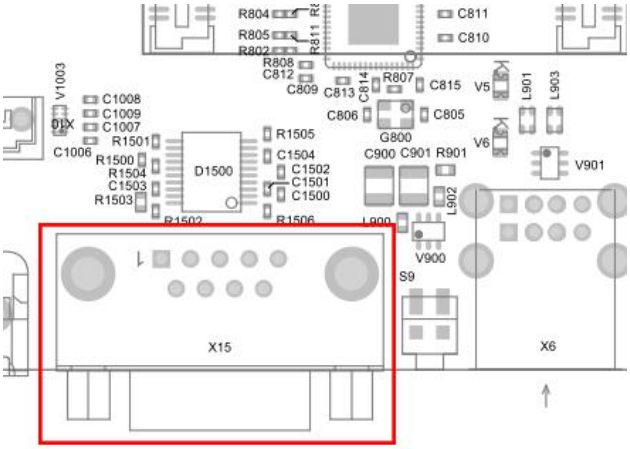


Illustration 30: Position of RS232 (X15)

Table 51: Device RS232

Manufacturer / Number	Description	Package
Yamaichi / DRA-09P11-ZN	9-pin D-Sub connector	THT9

Table 52: Pinout RS485 (X15)

Pin	Pin name	Signal	Dir.	Remark
1	DCD	n.c.	–	Not used
2	RXD	RS232_RXD	I	
3	TXD	RS232_TXD	O	
4	DTR	n.c.	–	Not used
5	DGND	DGND	P	
6	DSR	n.c.	–	Not used
7	RTS	RS232_RTS#	O	
8	CTS	RS232_CTS#	I	
9	RI	n.c.	–	Not used
M1-2	DGND	DGND	P	

4.2.8 HDMI

4.2.8.1 Overview HDMI

An external monitor can be connected at the HDMI interface.
For licence and stability reasons a DVI-D connector is used instead of an HDMI connector.

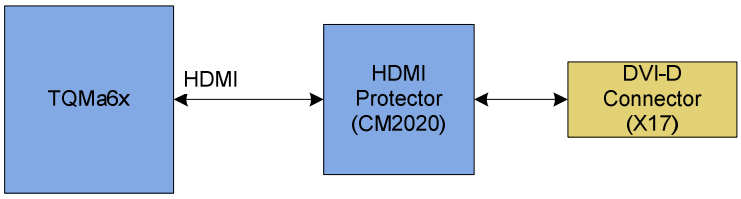


Illustration 31: Block diagram HDMI

The interface is protected against ESD by an HDMI protector (CM2020).

4.2.8.2 Characteristics HDMI

The characteristics of the interface are determined by the HDMI transmitter in the CPU.
More information can be taken from the Reference Manual of the respective CPU.
Analog signals are not supported by the interface.

4.2.8.3 Connector and pinout HDMI

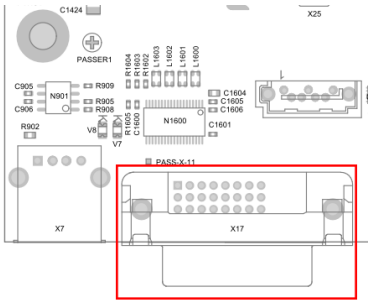


Illustration 32: Position of HDMI (X17)

Table 53: Device HDMI

Manufacturer / Number	Description	Package
Molex / 74320-4000	DVI-D receptacle	THT24

Table 54: Pinout HDMI (X17)

Pin	Pin name	Signal	Dir.	Remark
1	TMDS data 2–	HDMI_D2_N	O	Additional common mode choke in series
2	TMDS data 2+	HDMI_D2_P	O	Additional common mode choke in series
3	DGND	DGND	P	
4	–	n.c.	–	
5	–	n.c.	–	
6	DDC clock	HDMI_DDC_SCL_R	O	
7	DDC data	HDMI_DDC_SDA_R	I/O	
8	–	n.c.	–	
9	TMDS data 1–	HDMI_D1_N	O	Additional common mode choke in series
10	TMDS data 1+	HDMI_D1_P	O	Additional common mode choke in series
11	DGND	DGND	P	
12	–	n.c.	–	
13	–	n.c.	–	
14	+5 V	HDMI_5V_OUT	P	I_{max} = 75 mA
15	DGND	DGND	P	
16	Hot Plug Detect	HDMI_HPD	I	
17	TMDS data 0–	HDMI_D0_N	O	Additional common mode choke in series
18	TMDS data 0+	HDMI_D0_P	O	Additional common mode choke in series
19	DGND	DGND	P	
20	–	n.c.	–	
21	–	n.c.	–	
22	DGND	DGND	P	
23	TMDS clock +	HDMI_CLK_P	O	Additional common mode choke in series
24	TMDS clock –	HDMI_CLK_N	O	Additional common mode choke in series
M1-2	DGND	DGND	P	

4.2.9 LVDS

4.2.9.1 Overview LVDS

Both LVDS interfaces of the TQMa6x (a clock pair and four data pairs) are directly routed to the 30-pin FFC (X18).
In addition to the LVDS signals 3.3 V and 5 V are provided at the connector.

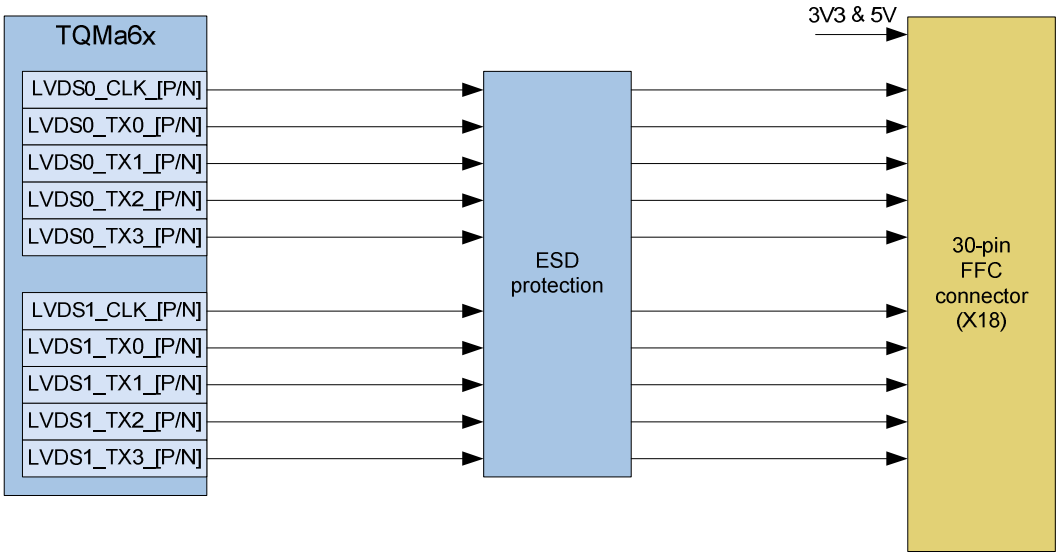


Illustration 33: Block diagram LVDS

4.2.9.2 Characteristics LVDS

The characteristics of the interface are determined by the LVDS transmitter in the CPU.
More information can be taken from the Reference Manual of the respective CPU.

4.2.9.3 Connector and pinout LVDS

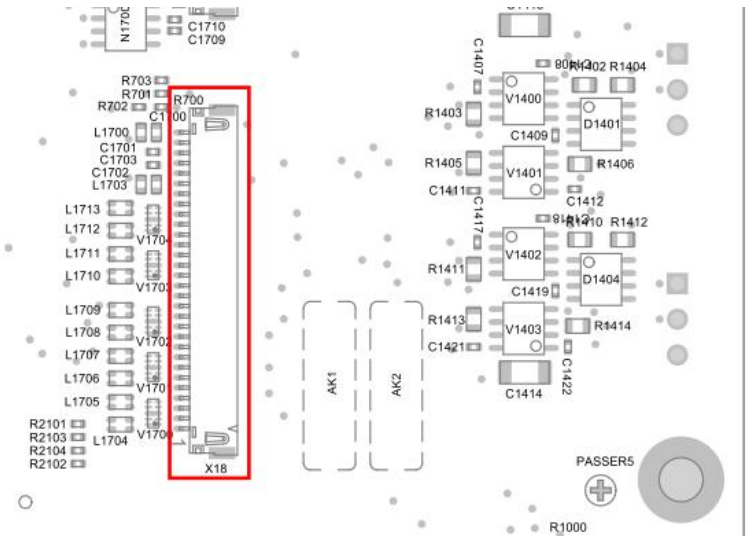


Illustration 34: Position of LVDS (X18)

Table 55: Device LVDS connector

Manufacturer / Number	Description	Package
Hirose / DF19G-30P-1H	Board-to-Cable FFC connector, 30-pin, 1 mm pitch	SMT30

Table 56: Pinout LVDS (X18)

Pin	Pin name	Signal	Dir.	Remark
1	0_TX0–	LVDS0_TX0_N	O	Additional common mode choke in series
2	0_TX0+	LVDS0_TX0_P	O	Additional common mode choke in series
3	0_TX1–	LVDS0_TX1_N	O	Additional common mode choke in series
4	0_TX1+	LVDS0_TX1_P	O	Additional common mode choke in series
5	0_TX2–	LVDS0_TX2_N	O	Additional common mode choke in series
6	0_TX2+	LVDS0_TX2_P	O	Additional common mode choke in series
7	DGND	DGND	P	
8	0_CLK–	LVDS0_CLK_N	O	Additional common mode choke in series
9	0_CLK+	LVDS0_CLK_P	O	Additional common mode choke in series
10	0_TX3–	LVDS0_TX3_N	O	Additional common mode choke in series
11	0_TX3+	LVDS0_TX3_P	O	Additional common mode choke in series
12	1_TX0–	LVDS1_TX0_N	O	Additional common mode choke in series
13	1_TX0+	LVDS1_TX0_P	O	Additional common mode choke in series
14	DGND	DGND	P	
15	1_TX1–	LVDS1_TX1_N	O	Additional common mode choke in series
16	1_TX1+	LVDS1_TX1_P	O	Additional common mode choke in series
17	DGND	DGND	P	
18	1_TX2–	LVDS1_TX2_N	O	Additional common mode choke in series
19	1_TX2+	LVDS1_TX2_P	O	Additional common mode choke in series
20	1_CLK–	LVDS1_CLK_N	O	Additional common mode choke in series
21	1_CLK+	LVDS1_CLK_P	O	Additional common mode choke in series
22	1_TX3–	LVDS1_TX3_N	O	Additional common mode choke in series
23	1_TX3+	LVDS1_TX3_P	O	Additional common mode choke in series
24	DGND	DGND	P	
25	VCC5V	VCC5V_LVDS	P	I_{max}= 1 A [11] (excluding the current drawn from the headers) 10 µF + 1 µF to Ground; ferrite in series
26	VCC5V	VCC5V_LVDS	P	
27	VCC5V	VCC5V_LVDS	P	
28	VCC3V3	VCC3V3_LVDS	P	I_{max}= 1 A [13] (excluding the current drawn from the headers) 10 µF + 1 µF to Ground; ferrite in series
29	VCC3V3	VCC3V3_LVDS	P	
30	VCC3V3	VCC3V3_LVDS	P	
M1-2	DGND	DGND	P	

11: Due to max. load of FFC contacts.

4.2.10 LVDS-CMD

4.2.10.1 Overview LVDS-CMD

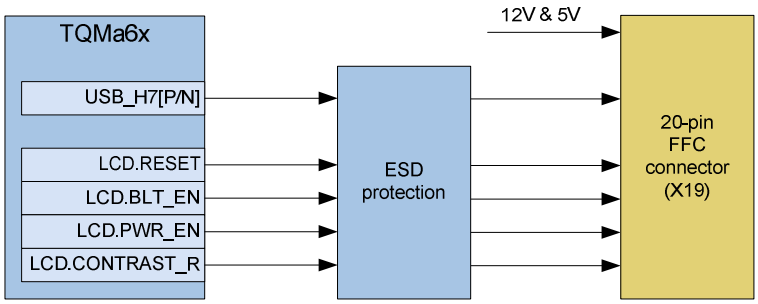


Illustration 35: Block diagram LVDS-CMD

To connect an LVDS display, the LVDS-CMD connector (X19) is placed near the LVDS connector (X18).
The FFC connector X19 provides a USB interface and control signals for display and backlight.
In addition to the data signals 5 V and 12 V are available as supply voltages.

4.2.10.2 Characteristics LVDS-CMD

Table 57: Characteristics LVDS-CMD

Parameter	Min.	Typ.	Max.	Unit	Remark
Current at 12 V	–	–	1	A	
Current at 5 V	–	–	1	A	
USB signals	–	–	–	–	Characteristics see section 4.2.1
Level for display / backlight signals	0	–	3.3	V	

4.2.10.3 Connector and pinout LVDS-CMD

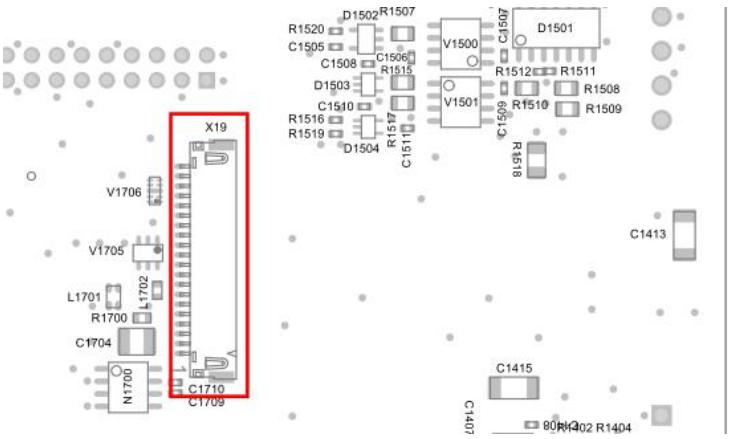


Illustration 36: Position of LVDS-CMD (X19)

Table 58: Device LVDS-CMD connector

Manufacturer / Number	Description	Package
Hirose / DF19G-20P-1H	Board-to-Cable FFC connector 20-pin, 1 mm pitch	SMT20

Table 59: Pinout LVDS CMD (X19)

Pin	Pin name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	I_{max}= 1 A [12] (excluding the current drawn from the headers) 10 µF + 1 µF to Ground
2	VCC12V	VCC12V	P	
3	VCC12V	VCC12V	P	
4	DGND	DGND	P	
5	DGND	DGND	P	
6	DGND	DGND	P	
7	VCC5V	VCC5V	P	I_{max}= 1 A (excluding the current drawn from the headers) 10 µF + 1 µF to Ground
8	VCC5V	VCC5V	P	
9	DGND	DGND	P	
10	DGND	DGND	P	
11	VBUS	USB_H7_VBUS	P	100 µF to DGND; EMI filter
12	DGND	DGND	P	
13	D+	USB_H7_D_N	I/O	Common mode choke in series
14	D–	USB_H7_D_P	I/O	Common mode choke in series
15	DGND	DGND	P	
16	LCD_RESET	LCD.RESET	O	
17	LCD_BL_EN	LCD.BLT_EN	O	
18	LCD_PWR_EN	LCD.PWR_EN	O	
19	LCD_CONTRAST	LCD.CONTRAST_R	O	
20	DGND	DGND	P	
M1-2	DGND	DGND	P	

12: Due to max. load of FFC contacts.

4.2.11 Audio

4.2.11.1 Overview Audio

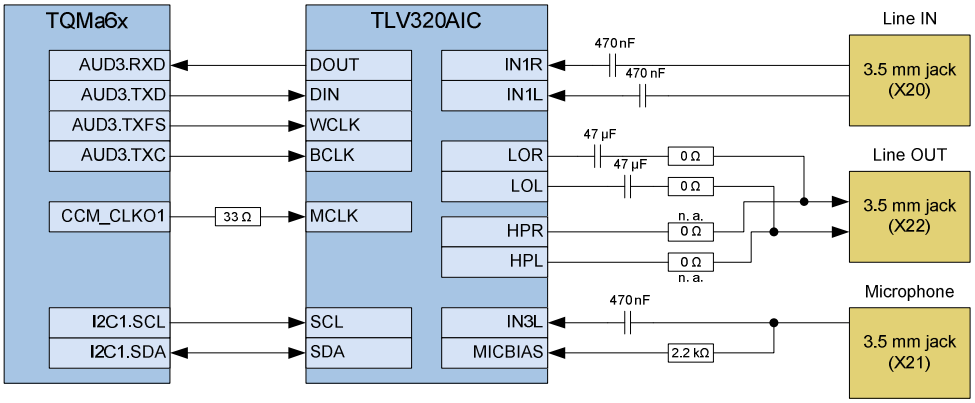


Illustration 37: Block diagram audio

Audio input and output is possible with the audio codec TLV320AIC. The codec is routed to the AUD3 interface of the i.MX6. The STK-MBa6x provides a stereo line-in, a stereo line-out and a microphone input.

4.2.11.2 Characteristics Audio

An assembly option selects between line-out and headphone. The following table shows the possible configuration.

Table 60: Configuration line-out or headphone

Modus	R1802	R1803	R1804	R1805	Remark
Headphone	n.a.	n.a.	0 Ω	0 Ω	Default
Line-out	0 Ω	0 Ω	n.a.	n.a.	

The following tables show the characteristics of the audio codec.

Table 61: Characteristics audio of headphone

Parameter	Min.	Typ.	Max.	Unit	Remark
Load resistor	14.4	16	–	Ω	Single-ended configuration
Load resistor	24.4	32	–	Ω	Differential configuration
Output power	–	64	–	mW	At 16 Ω input impedance at –40 dB THD
Output power	–	40	–	mW	At 32 Ω input impedance at –40 dB THD
Signal-noise ratio	87	100	–	dB	

Table 62: Characteristics audio line-out

Parameter	Min.	Typ.	Max.	Unit	Remark
Load resistor	0.6	106	–	kΩ	
Signal-noise ratio	87	100	–	dB	

Table 63: Characteristics audio line-in

Parameter	Min.	Typ.	Max.	Unit	Remark
Signal-noise ratio	80	93	–	dB	

Table 64: Characteristics Microphone

Parameter	Min.	Typ.	Max.	Unit	Remark
Output Noise	–	10	–	μV_{RMS}	
Current	–	3	–	mA	

4.2.11.3 Connectors and pinout Audio

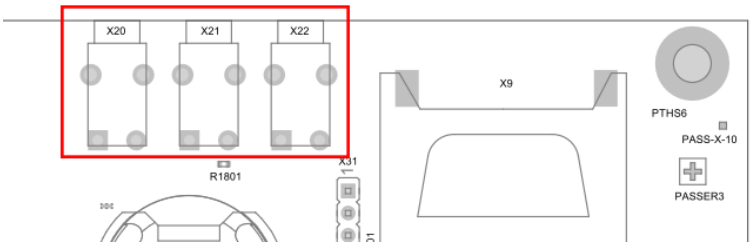


Illustration 38: Position of audio connectors (X20, X21, X22)

Table 65: Devices audio

Manufacturer / Number	Description	Package
Yamaichi / LJE3530K	Jack 3.5 mm	THT4

Table 66: Pinout line-in (X20)

Pin	Pin name	Signal	Dir.	Remark
1	Ground	AGND_AUDIO	P	
2A,2B	Left	LINE_IN_L	I	470 nF in series; ESD protection
3	Right	LINE_IN_R	I	470 nF in series; ESD protection

Table 67: Pinout Microphone (X21)

Pin	Pin name	Signal	Dir.	Remark
1	Ground	AGND_AUDIO	P	
2A,2B	Left	MIC_IN	I	2.2 kΩ in series to MIC_BIAS; ESD protection
3	Right	AGND_AUDIO	I	10 kΩ in series, right channel not used (only mono)

Table 68: Pinout line-out (X22)

Pin	Pin name	Signal	Dir.	Remark
1	Ground	AGND_AUDIO	P	
2A,2B	Left	AUDIO_OUT_L	O	1 µF and 100 Ω in series; 47 nF to AGND_AUDIO; optional connection to HP_L; ESD protection is possible
3	Right	AUDIO_OUT_R	O	1 µF and 100 Ω in series; 47 nF to AGND_AUDIO; optional connection to HP_R; ESD protection is possible

4.2.12 SD card

4.2.12.1 Overview SD card

The SD card slot is directly connected with the SDHC controller of the TQMa6x.
Serial resistors are integrated in the data lines or control lines to adjust the line attenuation.

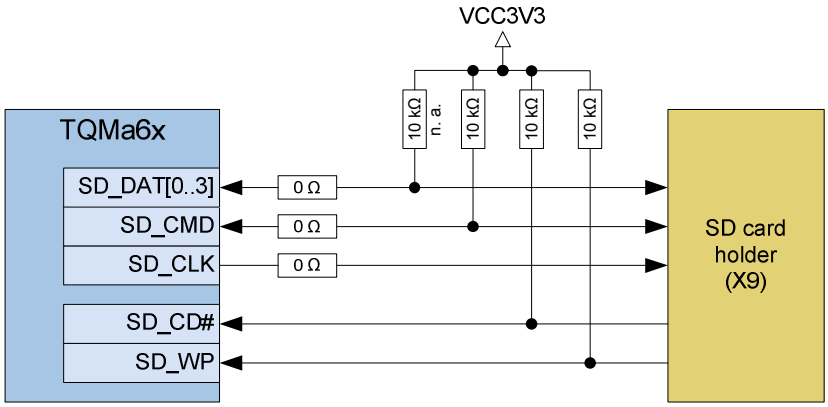


Illustration 39: Block diagram SD card

It is possible to boot from SD card (see section 4.3.5).

4.2.12.2 Characteristics SD card

The read and write speeds of the SD card interface depend on the SD card used.
The following table shows values measured with Class 4 and Class 10 SD cards.
The maximum available data rate is to be taken from the respective CPU Reference Manual.

Table 69: Characteristics SD card

Parameter	Min.	Typ.	Max.	Unit	Remark
Read	–	17.7	–	MByte/s	SanDisk Class 10 SD card, 200 MByte file with 25 MByte block size
Write	–	15.6	–	MByte/s	
Read	–	17.1	–	MByte/s	SanDisk Class 4 SD card, 200 MByte file with 25 MByte block size
Write	–	3.5	–	MByte/s	

4.2.12.3 Connector and pinout SD card

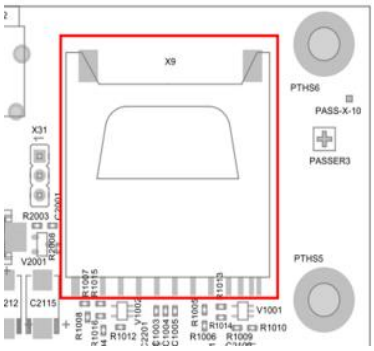


Illustration 40: Position of SD card (X9)

Table 70: Device SD card

Manufacturer / Number	Description	Package
Yamaichi / FPS009-2405-0	SD-/MMC card connector	SMD9

Table 71: Pinout SD card (X9)

Pin	Pin name	Signal	Dir.	Remark
1	CD/DAT3/CS	SD2.DAT3_R	I/O	0 Ω in series
2	CMD/DI	SD2.CMD_R	I/O	0 Ω in series; 10 kΩ to VCC3V3
3	VSS1	DGND	P	
4	VDD	VCC3V3	P	1 µF + 100 nF + 10 nF to Ground
5	CLK	SD2.CLK_R	O	0 Ω in series
6	VSS2	DGND	P	
7	DAT0/DO	SD2.DAT0_R	I/O	0 Ω in series
8	DAT1	SD2.DAT1_R	I/O	0 Ω in series
9	DAT2	SD2.DAT2_R	I/O	0 Ω in series
CDS	CARD_DETECT	SD2.CD#	I	10 kΩ to VCC3V3
COM	COMMON	DGND	P	
WP	WRITE_PROTECT	SD2.WP	I	10 kΩ to VCC3V3
M1-2	DGND	DGND	P	

4.2.13 SATA

4.2.13.1 Overview SATA

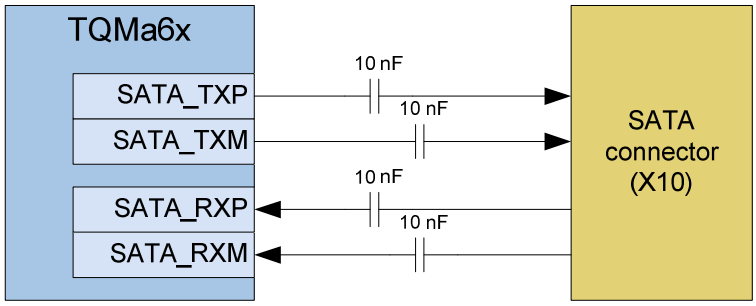


Illustration 41: Block diagram SATA interface

The SATA interface of the TQMa6x is directly connected to a 7-pin SATA connector via capacitive coupling (10 nF). A SATA device must be supplied separately, e.g., via the power OUT header. All four data lines have an ESD protection.

It is possible to boot from SATA (see section 4.3.5).

4.2.13.2 Characteristics SATA

The SATA interface has the following characteristics:

- Serial ATA 3.0
- AHCI Revision 1.3
- AMBA 2.0 from ARM
- 1.5 Gbit/s and 3.0 Gbit/s SATA data rate

Table 72: Characteristics SATA [13]

Parameter	Min.	Typ.	Max.	Unit	Remark
Read	–	57.0	–	MByte/s	1 GByte with block size 512 KByte
Write	–	9.0	–	MByte/s	1 GByte with block size 512 KByte
Read	–	56.9	–	MByte/s	1 GByte with block size 10 MByte
Write	–	24.8	–	MByte/s	1 GByte with block size 10 MByte

13: Tested with hard disk WD1200JS.

4.2.13.3 Connector and pinout SATA

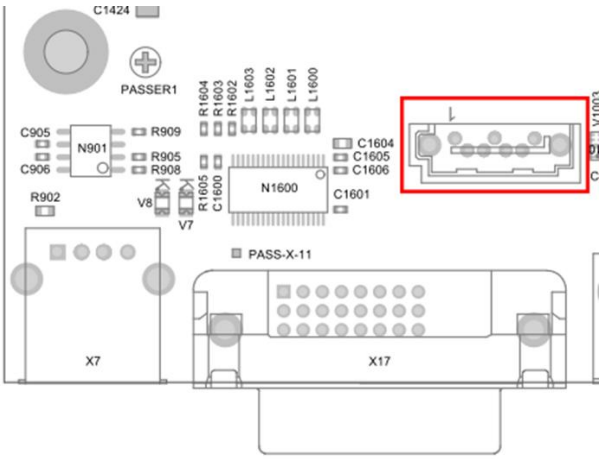


Illustration 42: Position of SATA (X10)

Table 73: Device SATA

Manufacturer / Number	Description	Package
3M / 5607-5102-SH	SATA connector, 7-pin	THT7

Table 74: Pinout SATA (X10)

Pin	Pin name	Signal	Dir.	Remark
1	DGND	DGND	P	
2	TX+	SATA_TX_P	I	10 nF in series; ESD protection
3	TX–	SATA_TX_N	I	10 nF in series; ESD protection
4	DGND	DGND	P	
5	RX–	SATA_RX_N	O	10 nF in series; ESD protection
6	RX+	SATA_RX_P	O	10 nF in series; ESD protection
7	DGND	DGND	P	
M1-2	DGND	DGND	P	

4.2.14 Mini PCIe

4.2.14.1 Overview Mini PCIe

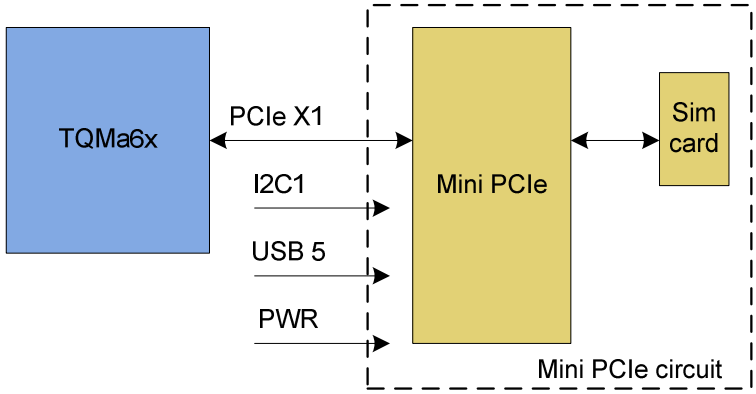


Illustration 43: Block diagram Mini PCIe

The STK-MBa6x provides a Mini PCIe interface. It is fully connected (PCIe lane, I^2C, USB) and thereby permits the use of various Mini PCIe devices.

A SIM card holder is also available to connect an UMTS / GSM modem.

4.2.14.2 Characteristics Mini PCIe

Table 75: Characteristics Mini PCIe

Parameter	Min.	Typ.	Max.	Unit	Remark
Current @ 3.3 V	–	–	1.1	A	
Current @ 1.5 V	–	–	0.375	A	
USB signals	–	–	–	–	Characteristics see section 4.2.1

4.2.14.3 Connector and pinout Mini PCIe

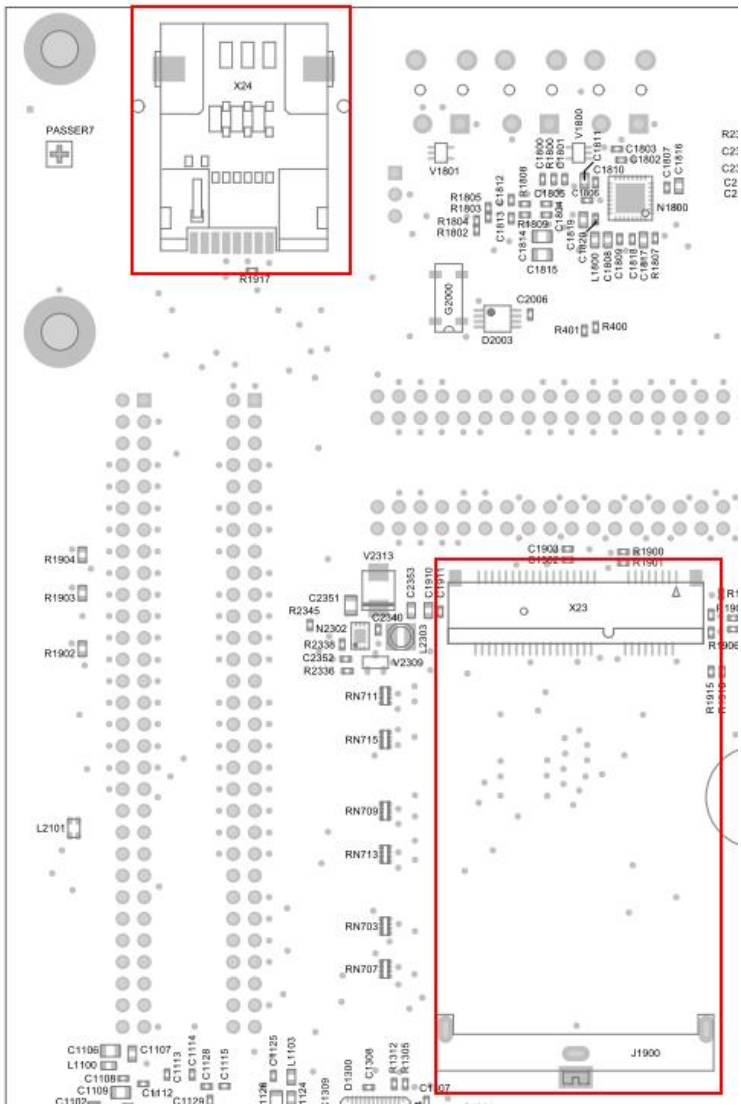


Illustration 44: Position of Mini PCIe (X23, X24, J1900)

Table 76: Devices Mini PCIe

Manufacturer / Number	Description	Package
Nexus / 5020HB56R	Mini PCIe connector	SMT54
Nexus / 5022M56R	Mini PCIe holder	THT3
YAMAICHI / FMS006Z-2101-0	SIM card holder	SMT10

Table 77: Pinout Mini PCIe (X23)

Pin	Pin name	Signal	Dir.	Remark
1	WAKE	PCIE.WAKE#	O	
2	VCC3V3	VCC3V3_MPCIE	P	Can be switched off by N1900; 5 × 100 µF + 4.7 µF to Ground
3	–	n.c.	–	
4	DGND	DGND	P	
5	–	n.c.	–	
6	VCC1V5	VCC1V5	P	Can be switched off indirectly by N1900; 3 × 100 µF + 4.7 µF to Ground
7	–	n.c.	–	
8	UIM_PWR	UIM_PWR	P	
9	DGND	DGND	P	
10	UIM_DATA	UIM_DATA	I/O	
11	CLK–	PCIE_REFCLK_N	O	100 nF in series; 49.9 Ω to Ground
12	UIM_CLK	UIM_CLK	I	
13	CLK+	PCIE_REFCLK_P	O	100 nF in series; 49.9 Ω to Ground
14	UIM_RST	UIM_RST	I	
15	DGND	DGND	P	
16	UIM_VPP	UIM_VPP	P	
17	–	n.c.	–	
18	DGND	DGND	P	
19	–	n.c.	–	
20	DIS	PCIE.DIS#	O	
21	DGND	DGND	P	
22	RST	PCIE.RST#	O	
23	RX–	PCIE_RX_N	I	0 Ω in series
24	VCC3V3	VCC3V3_MPCIE	P	Can be switched off by N1900; 5 × 100 µF + 4.7 µF to Ground
25	RX+	PCIE_RX_P	I	0 Ω in series
26	DGND	DGND	P	
27	DGND	DGND	P	
28	VCC1V5	VCC1V5	P	Can be switched off indirectly by N1900; 3 × 100 µF + 4.7 µF to Ground
29	DGND	DGND	P	
30	SCL	I2C1.SCL	O	
31	TX–	PCIE_TX_N	O	100 nF in series
32	SDA	I2C1.SDA	I/O	
33	TX+	PCIE_TX_P	O	100 nF in series
34	DGND	DGND	P	
35	DGND	DGND	P	
36	USB_D–	USB_H5_D_N	I/O	Common mode choke in series
37	DGND	DGND	P	
38	USB_D+	USB_H5_D_P	I/O	Common mode choke in series
39	VCC3V3	VCC3V3_MPCIE	P	Can be switched off by N1900; 5 × 100 µF + 4.7 µF to Ground
40	DGND	DGND	P	
41	VCC3V3	VCC3V3_MPCIE	P	Can be switched off by N1900; 5 × 100 µF + 4.7 µF to Ground
42	WWAN	LED_WWAN#	I	Connected to LED
43	DGND	DGND	P	
44	WLAN	LED_WLAN#	I	Connected to LED
45	–	n.c.	–	
46	WPAN	LED_WPAN#	I	Connected to LED
47	–	n.c.	–	
48	VCC1V5	VCC1V5	P	Can be switched off indirectly by N1900; 3 × 100 µF + 4.7 µF to Ground
49	–	n.c.	–	
50	DGND	DGND	P	
51	–	n.c.	–	
52	VCC3V3	VCC3V3_MPCIE	P	Can be switched off by N1900; 5 × 100 µF + 4.7 µF to Ground

Table 78: Pinout SIM-Card (X24)

Pin	Pin name	Signal	Dir.	Remark
C1	PWR	UIM_PWR	P	
C2	RST	UIM_RST	O	
C3	CLK	UIM_CLK	O	
C5	DGND	DGND	P	
C6	VPP	UIM_VPP	P	
C7	DATA	UIM_DATA	I/O	
SW1-2	–	–	–	

4.2.15 Headers

4.2.15.1 Overview headers

All unused signals are routed to the headers X27, X28, X29, X30 on the STK-MBa6x, to permit a comprehensive evaluation of the TQMa6x modules. All headers are 60-pin with 2.54 mm pitch.
The headers are positioned in such a way, that adaptor boards which additional electronics and connectors can be plugged in.

4.2.15.2 Connectors and pinout headers

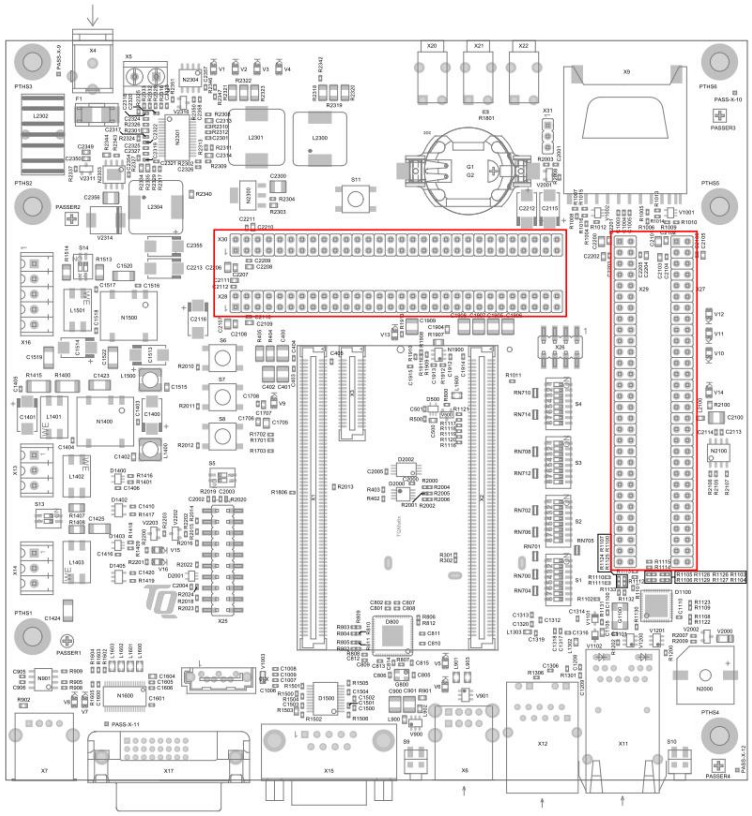


Illustration 45: Position of Starterkit headers (X27, X28, X29, X30)

Table 79: Device headers

Manufacturer / Number	Description	Package
Fischer Elektronik / SL 22 124 60 G	Header, 2.54 mm pitch, 2 × 30 pins	THT30

Table 80: Pinout header 1 (X27)

Pin	Interface	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	100 µF + 10 µF + 1 µF to DGND, I_{max} = 1 A
2	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
3	VCC5V	VCC5V	P	10 µF + 1 µF to DGND, I_{max} = 1 A
4	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
5	DGND	DGND	P	
6	DGND	DGND	P	
7	DISP0	DISP0.CLK	O	
8	DISP0	DISP0.DRDY	O	
9	DISP0	DISP0.HSYNC	O	
10	DISP0	DISP0.DAT1	O	
11	DISP0	DISP0.VSYNC	O	
12	DISP0	DISP0.DAT3	O	
13	DISP0	DISP0.DAT0	O	
14	DISP0	DISP0.DAT5	O	
15	DISP0	DISP0.DAT2	O	
16	DISP0	DISP0.DAT7	O	
17	DISP0	DISP0.DAT4	O	
18	DISP0	DISP0.DAT9	O	
19	DISP0	DISP0.DAT6	O	
20	DISP0	DISP0.DAT11	O	
21	DISP0	DISP0.DAT8	O	
22	DISP0	DISP0.DAT13	O	
23	DISP0	DISP0.DAT10	O	
24	DISP0	DISP0.DAT15	O	
25	DISP0	DISP0.DAT12	O	
26	DISP0	DISP0.DAT17	O	
27	DISP0	DISP0.DAT14	O	
28	DISP0	DISP0.DAT19	O	
29	DISP0	DISP0.DAT16	O	
30	DISP0	DISP0.DAT21	O	
31	DISP0	DISP0.DAT18	O	
32	DISP0	DISP0.DAT23	O	
33	DISP0	DISP0.DAT20	O	
34	USB	USB_H4_VBUS	P	100 µF to DGND; EMI filter
35	DISP0	DISP0.DAT22	O	
36	USB	USB_H4_D_N	I/O	Common mode choke in series
37	DGND	DGND	P	
38	USB	USB_H4_D_P	I/O	Common mode choke in series
39	I2C1	I2C1.SCL	O	
40	DGND	DGND	P	
41	I2C1	I2C1.SDA	I/O	
42	SPI1	SPI1.SS2#	O	
43	SPI1	SPI1.MOSI	O	
44	SPI1	SPI1.MISO	I	
45	SPI1	SPI1.SS3#	O	
46	SPI1	SPI1.SCLK	O	
47	–	–	–	
48	DGND	DGND	P	
49	LCD	LCD.PWR_EN	O	Pull-Down or Pull-Up can be assembled
50	LCD	LCD.BLT_EN	O	
51	LCD	LCD.RESET	O	Pull-Down or Pull-Up can be assembled
52	LCD	LCD.CONTRAST_R	O	
53	DGND	DGND	P	
54	DGND	DGND	P	
55	–	–	–	
56	–	–	–	
57	–	–	–	
58	–	–	–	
59	DGND	DGND	P	
60	DGND	DGND	P	

Table 81: Pinout header 2 (X28)

Pin	Pin name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	100 µF + 10 µF + 1 µF to DGND, I_{max} = 1 A
2	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
3	VCC5V	VCC5V	P	10 µF + 1 µF to DGND, I_{max} = 1 A
4	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
5	DGND	DGND	P	
6	DGND	DGND	P	
7	DGND	DGND	P	
8	DGND	DGND	P	
9	XTAL2	XTAL2.CLK2_P	O	
10	MIPI_DSI	MIPI_DSI.CLK0_N	O	
11	XTAL2	XTAL2.CLK2_N	O	
12	MIPI_DSI	MIPI_DSI.CLK0_P	O	
13	DGND	DGND	P	
14	DGND	DGND	P	
15	DGND	DGND	P	
16	DGND	DGND	P	
17	MIPI_CSI	MIPI_CSI.D3_P	I	
18	MIPI_DSI	MIPI_DSI.D0_N	O	
19	MIPI_CSI	MIPI_CSI.D3_N	I	
20	MIPI_DSI	MIPI_DSI.D0_P	O	
21	DGND	DGND	P	
22	DGND	DGND	P	
23	MIPI_CSI	MIPI_CSI.D2_P	I	
24	MIPI_DSI	MIPI_DSI.D1_N	O	
25	MIPI_CSI	MIPI_CSI.D2_N	I	
26	MIPI_DSI	MIPI_DSI.D1_P	O	
27	DGND	DGND	P	
28	DGND	DGND	P	
29	MIPI_CSI	MIPI_CSI.D1_P	I	
30	DGND	DGND	P	
31	MIPI_CSI	MIPI_CSI.D1_N	I	
32	MLB	MLB.C_N	O	
33	DGND	DGND	P	
34	MLB	MLB.C_P	O	
35	MIPI_CSI	MIPI_CSI.D0_P	I	
36	DGND	DGND	P	
37	MIPI_CSI	MIPI_CSI.D0_N	I	
38	MLB	MLB.D_N	I/O	
39	DGND	DGND	P	
40	MLB	MLB.D_P	I/O	
41	DGND	DGND	P	
42	DGND	DGND	P	
43	MIPI_CSI	MIPI_CSI.CLK0_P	I	
44	MLB	MLB.S_N	I/O	
45	MIPI_CSI	MIPI_CSI.CLK0_N	I	
46	MLB	MLB.S_P	I/O	
47	DGND	DGND	P	
48	DGND	DGND	P	
49	DGND	DGND	P	
50	USB_H.PWR	USB_H.PWR	O	Unused USB signal line for USB_H (used for upstream port USB-Hub)
51	ECSPI5	ECSPI5.MISO	I	
52	USB_H.OC	USB_H.OC	I	Unused USB signal line for USB_H (used for upstream port USB-Hub)
53	ECSPI5	ECSPI5.MOSI	O	
54	DGND	DGND	P	
55	ECSPI5	ECSPI5.SS0#	O	
56	DEBUG	SPI-NOR_WP#	I	
57	ECSPI5	ECSPI5.SCLK	O	
58	DEBUG	TAMPER	I	
59	DGND	DGND	P	
60	DGND	DGND	P	

Table 82: Pinout header 3 (X29)

Pin	Pin name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	100 µF + 10 µF + 1 µF to DGND, I_{max} = 1 A
2	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
3	VCC5V	VCC5V	P	10 µF + 1 µF to DGND, I_{max} = 1 A
4	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
5	DGND	DGND	P	
6	DGND	DGND	P	
7	BOOT	BOOT.CFG4_6	I	Pin is not configured in default BSP
8	BOOT	BOOT.CFG4_7	I	Pin is not configured in default BSP
9	DGND	DGND	P	
10	DGND	DGND	P	
11	BOOT	BOOT.CFG4_4	I	Pin is not configured in default BSP
12	BOOT	BOOT.CFG4_5	I	Pin is not configured in default BSP
13	BOOT	BOOT.CFG4_2	I	Pin is not configured in default BSP
14	BOOT	BOOT.CFG4_3	I	Pin is not configured in default BSP
15	DGND	DGND	P	
16	BOOT	BOOT.CFG4_1	I	Pin is not configured in default BSP
17	BOOT	BOOT.CFG4_0	I	Pin is not configured in default BSP
18	DGND	DGND	P	
19	BOOT	BOOT.CFG3_6	I	Pin is not configured in default BSP
20	BOOT	BOOT.CFG3_7	I	Pin is not configured in default BSP
21	BOOT	BOOT.CFG3_4	I	Pin is not configured in default BSP
22	BOOT	BOOT.CFG3_5	I	Pin is not configured in default BSP
23	BOOT	BOOT.CFG3_2	I	Pin is not configured in default BSP
24	BOOT	BOOT.CFG3_3	I	Pin is not configured in default BSP
25	BOOT	BOOT.CFG3_0	I	Pin is not configured in default BSP
26	BOOT	BOOT.CFG3_1	I	Pin is not configured in default BSP
27	DGND	DGND	P	
28	DGND	DGND	P	
29	BOOT	BOOT.CFG2_6	I	Pin is not configured in default BSP
30	BOOT	BOOT.CFG2_7	I	Pin is not configured in default BSP
31	BOOT	BOOT.CFG2_4	I	Pin is not configured in default BSP
32	BOOT	BOOT.CFG2_5	I	Pin is not configured in default BSP
33	BOOT	BOOT.CFG2_2	I	Pin is not configured in default BSP
34	BOOT	BOOT.CFG2_3	I	Pin is not configured in default BSP
35	BOOT	BOOT.CFG2_0	I	Pin is not configured in default BSP
36	BOOT	BOOT.CFG2_1	I	Pin is not configured in default BSP
37	BOOT	BOOT.CFG1_6	I	Pin is not configured in default BSP
38	BOOT	BOOT.CFG1_7	I	Pin is not configured in default BSP
39	BOOT	BOOT.CFG1_4	I	Pin is not configured in default BSP
40	BOOT	BOOT.CFG1_5	I	Pin is not configured in default BSP
41	BOOT	BOOT.CFG1_2	I	Pin is not configured in default BSP
42	BOOT	BOOT.CFG1_3	I	Pin is not configured in default BSP
43	BOOT	BOOT.CFG1_0	I	Pin is not configured in default BSP
44	BOOT	BOOT.CFG1_1	I	Pin is not configured in default BSP
45	DGND	DGND	P	
46	DGND	DGND	P	
47	UART3	UART3.RX	I	
48	–	–	–	
49	UART3	UATR3.TX	O	
50	PWM	PWM3	O	
51	UART3	UART3.RTS#	O	
52	PWM	PWM4	O	
53	UART3	UART3.CTS#	I	
54	DGND	DGND	P	
55	DGND	DGND	P	
56	UART4	UART4.RTS#	O	Unused UART signal line of UART4 (used for RS485)
57	CCM	CCM_CLKO2	O	
58	DEBUG	RFU	I	Reserved for future use
59	DGND	DGND	P	
60	DGND	DGND	P	

Table 83: Pinout header 4 (X30)

Pin	Pin name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	100 µF + 10 µF + 1 µF to DGND, I_{max} = 1 A
2	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
3	VCC5V	VCC5V	P	10 µF + 1 µF to DGND, I_{max} = 1 A
4	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
5	DGND	DGND	P	
6	DGND	DGND	P	
7	DGND	DGND	P	
8	DGND	DGND	P	
9	GPIO	GPIO1_IO26	I/O	
10	SPDIF	SPDIF.OUT	O	
11	GPIO	GPIO1_29	I/O	
12	SPDIF	SPDIF.IN	I	
13	GPIO	GPIO1_30	I/O	
14	DGND	DGND	P	
15	GPIO	GPIO2_IO01	I/O	
16	UART5	UART5.RX	I	
17	GPIO	GPIO2_IO02	I/O	
18	UART5	UART5.TX	O	
19	GPIO	GPIO2_IO03	I/O	
20	UART5	UART5.RTS#	O	
21	DGND	DGND	P	
22	UART5	UART5.CTS#	I	
23	GPIO	GPIO2_IO08	I/O	
24	DGND	DGND	P	
25	GPIO	GPIO2_IO23	I/O	
26	I2C3	I2C3.SCL	O	
27	GPIO	GPIO2_IO24	I/O	
28	I2C3	I2C3.SDA	I/O	
29	GPIO	GPIO2_IO25	I/O	
30	DGND	DGND	P	
31	GPIO	GPIO3_IO20	I/O	
32	GPIO	GPIO5_IO18	I/O	
33	GPIO	GPIO3_IO23	I/O	
34	GPIO	GPIO5_IO20	I/O	
35	DGND	DGND	P	
36	GPIO	GPIO5_IO21	I/O	
37	GPIO	GPIO3_IO26	I/O	
38	GPIO	GPIO6_IO08	I/O	
39	GPIO	GPIO3_IO27	I/O	
40	GPIO	GPIO6_IO14	I/O	
41	GPIO	GPIO3_IO28	I/O	
42	DGND	DGND	P	
43	GPIO	GPIO3_IO29	I/O	
44	GPIO	GPIO6_IO16	I/O	With LED
45	GPIO	GPIO4_IO06	I/O	
46	GPIO	GPIO6_IO31	I/O	With LED
47	GPIO	GPIO4_IO07	I/O	
48	GPIO	GPIO4_IO08	I/O	
49	DGND	DGND	P	
50	GPIO	GPIO4_IO09	I/O	
51	SD	SD2.DAT4	I/O	Unused SD signal line of SD2 (used for SD card)
52	DGND	DGND	P	
53	SD	SD2.DAT5	I/O	Unused SD signal line of SD2 (used for SD card)
54	AUD3	AUD3.RXC	I	Unused AUDIO signal line of AUD3 (used for Audio)
55	SD	SD2.DAT6	I/O	Unused SD signal line of SD2 (used for SD card)
56	AUD3	AUD3.RXFS	I	Unused AUDIO signal line of AUD3 (used for Audio)
57	SD	SD2.DAT7	I/O	Unused SD signal line of SD2 (used for SD card)
58	DEBUG	DNC	I	Do not connect
59	DGND	DGND	P	
60	DGND	DGND	P	

4.3 Diagnose- and user interfaces

4.3.1 Diagnose LEDs

4.3.1.1 Overview diagnose LEDs

The STK-MBa6x provides 20 diagnose LEDs to indicate the system condition.

Table 84: Meaning of diagnose LEDs

Function	Reference	Colour	Signal
Power	V1	Green	24 V Power-LED (lights up when supply 24 V is active)
	V2	Green	12 V Power-LED (lights up when supply 12 V is active)
	V3	Green	5 V Power-LED (lights up when supply 5 V is active)
	V4	Green	3.3 V Power-LED (lights up when supply 3.3 V is active)
USB	V5	Green	VBUS USB Host 2 (lights up when VBUS of USB Host 2 is active)
	V6	Green	VBUS USB Host 3 (lights up when VBUS of USB Host 3 is active)
	V7	Green	VBUS USB Host 6 (lights up when VBUS of USB Host 6 is active)
	V8	Green	VBUS USB OTG (lights up when VBUS of USB OTG is active)
	V9	Green	VBUS USB Host 7 (LVDS-CMD, lights up when VBUS of USB Host 7 is active)
	V14	Green	VBUS USB Host 4 (header 1, lights up when VBUS of USB Host 4 is active)
Mini PCIe	V10	Green	Mini PCIe WWAN
	V11	Green	Mini PCIe WLAN
	V12	Green	Mini PCIe WPAN
	V13	Green	Mini PCIe 3.3 V Power-LED (lights up when PCIe supply 3.3 V is active)
Ethernet	X11B	Yellow	Activity-LED Ethernet 1000BASE-T (blinks at transfer)
	X11C	Green	Link-LED Ethernet 1000BASE-T (lights up when connected)
	X12B	Yellow	Speed-LED Ethernet 100BASE-T (lights up at 100 Mbit/s, is not lit at 10 Mbit/s)
	X12C	Green	Link-LED Ethernet 100BASE-T (lights up at valid link, blinks at transfer)
GPIOs	V15	Green	GPIO6_IO16 (high-active)
	V16	Green	GPIO6_IO31 (high-active)

4.3.1.2 Components and position diagnose LEDs

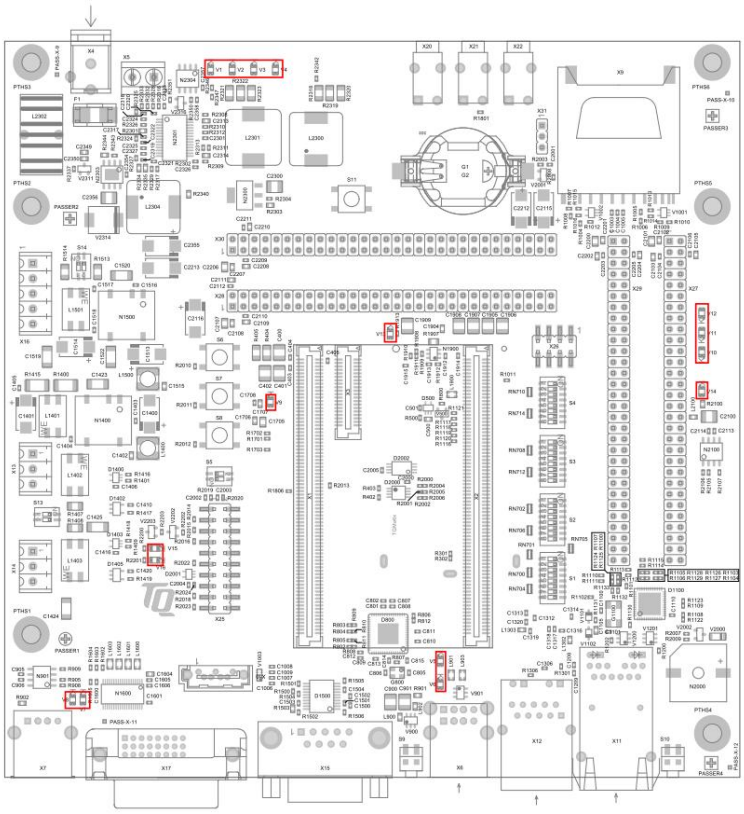


Illustration 46: Position of LEDs (V1 … V16)

Table 85: Devices status LEDs

Manufacturer / Number	Description	Package
Osram / LGR971-KN-1	SMD LED, green	SMT2

4.3.2 Navigation buttons

4.3.2.1 Overview navigation buttons

Three navigation buttons are available on the STK-MBa6x for development purposes.
The buttons are not debounced in hardware. Hence, the buttons have to be debounced in software.

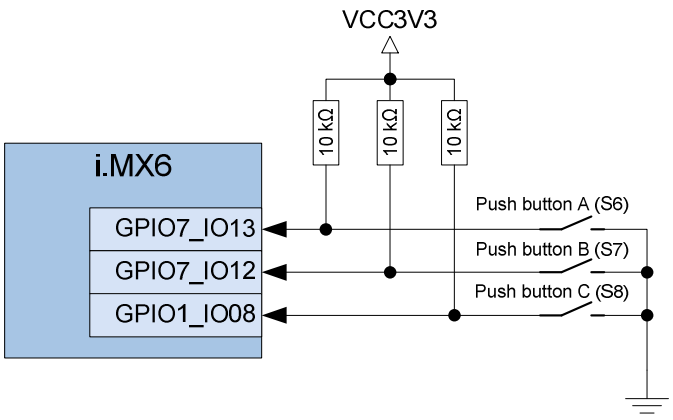


Illustration 47: Block diagram navigations buttons

4.3.2.2 Components and position navigation buttons

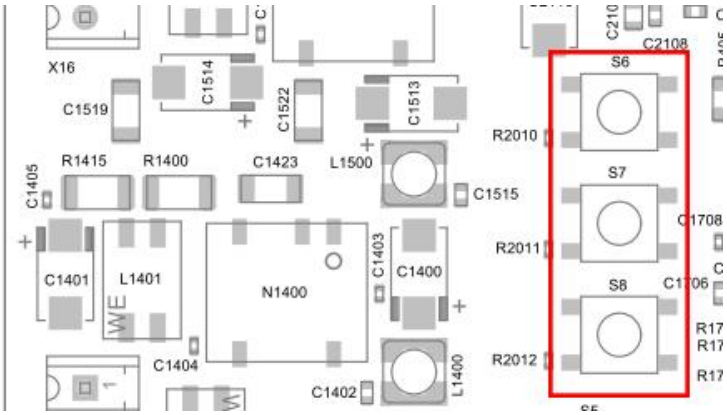


Illustration 48: Position of navigations buttons (S6, S7, S8)

Table 86: Device navigations buttons

Manufacturer / Number	Description	Package
Knitter switch / TSS 61N	Push button	SMT4

4.3.3 Power-On and Reset-button

For further information see section 4.1.6.

4.3.4 CAN and RS485 termination

For further information see section 4.2.5 and 4.2.6.

4.3.5 Boot-Mode configuration

4.3.5.1 Overview Boot-Mode configuration

The i.MX6 can boot from different media:

- eMMC
- SD-/MMC-Card
- SATA HDD [14]
- Serial ROM

The setting of switches S1 to S5 determines which device is selected to boot from. [15]
Each signal and its meaning for the boot process is to be taken from the User's Manual of the TQMa6x.

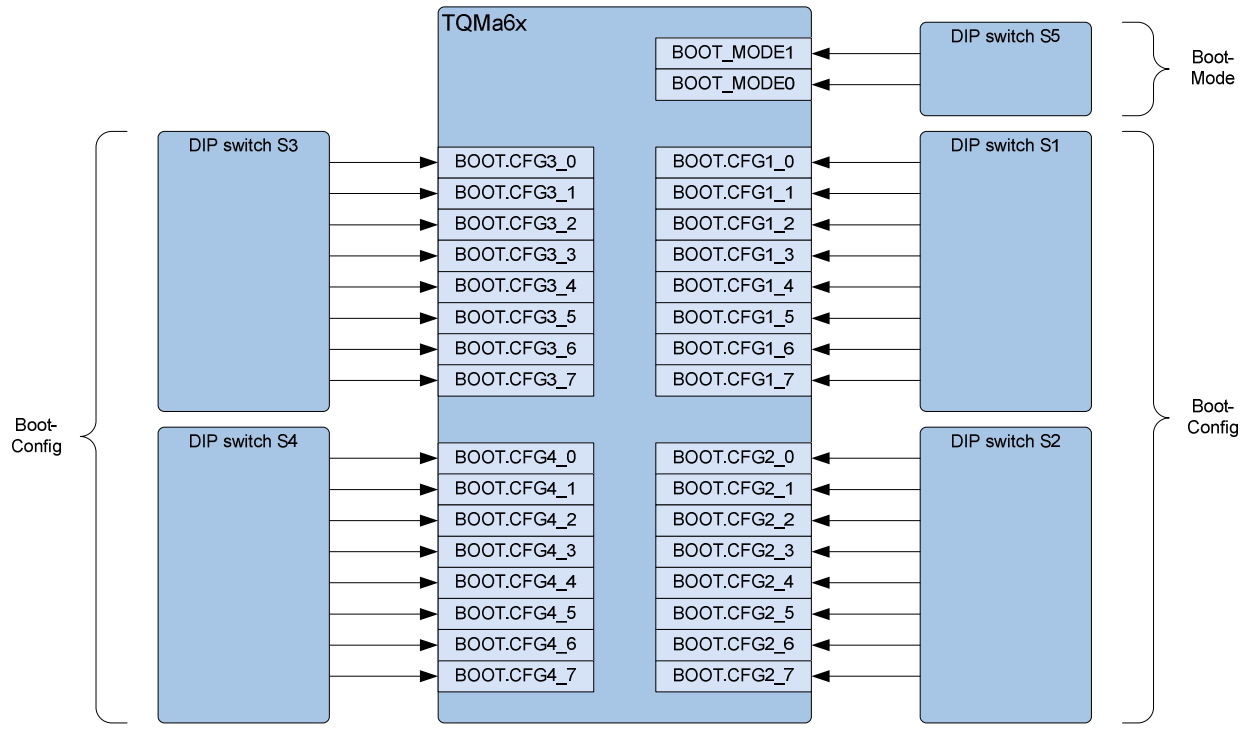


Illustration 49: Configuration of boot loader with DIP switches S1 to S5

The following settings can be used as default.

14: Only available with Dual or Quad CPUs.
15: Only applies to modules with unburnt eFuses.

Table 87: Boot-Mode configuration (S5)

Boot-Mode	S5-1 BOOT_MODE1	S5-2 MOOT_MODE0
Boot from eFuses	0	0
Serial Downloader	0	1
Internal Boot [16]	1	0
Reserved	1	1

Table 88: Standard boot-configurations (S1, S2, S4) [17]

Boot-Device			eMMC	Serial ROM	SD card	SATA
BOOT_CFG1_	7	S1-1	0	0	0	0
	6	S1-2	1	0	1	0
	5	S1-3	1	1	0	1
	4	S1-4	0	1	1	0
	3	S1-5	0	x	0	x
	2	S1-6	x	x	0	x
	1	S1-7	1	x	0	x
	0	S1-8	x	x	0	x
BOOT_CFG2_	7	S2-1	0	x	0	x
	6	S2-2	1	x	0	x
	5	S2-3	0	x	1	x
	4	S2-4	1	x	0	0
	3	S2-5	0	x	1	0
	2	S2-6	0	x	x	0
	1	S2-7	0	x	0	0
	0	S2-8	0	x	0	0
BOOT_CFG4_	7	S4-1	x	x	x	x
	6	S4-2	x	0	x	x
	5	S4-3	x	0	x	x
	4	S4-4	x	1	x	x
	3	S4-5	x	1	x	x
	2	S4-6	x	0	x	x
	1	S4-7	x	0	x	x
	0	S4-8	x	0	x	x

With S3 settings can be made, which are independent of the boot device.
More information is to be taken from the User's Manual of the TQMa6x.

16: Boot configuration is set with DIP switches S2 to S4.
17: Switch setting: 0 = OFF / 1 = ON / x = DONT CARE.

4.3.5.2 Components and position Boot-Mode configuration switches

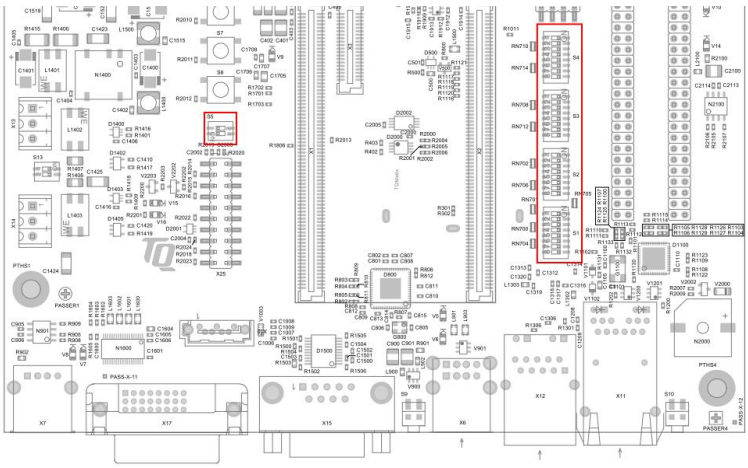


Illustration 50: Position of Boot-Mode configuration switches (S1, S2, S3, S4, S5)

Table 89: Devices Boot-Mode

Manufacturer / Number	Description	Package
Nidec Copal / CHS-08TA	8-fold DIP switch, 1.27 mm pitch	SMT16
Nidec Copal / CHS-02TA	2-fold DIP switch, 1.27 mm pitch	SMT4

4.3.6 Buzzer

4.3.6.1 Overview buzzer

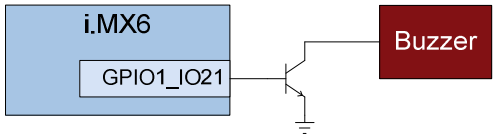


Illustration 51: Block diagram buzzer

The STK-MBa6x provides a buzzer to signal acoustic events.
The buzzer is directly controlled with a GPIO from the TQMa6x.

4.3.6.2 Component and position buzzer

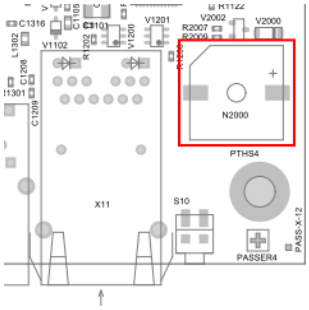


Illustration 52: Position of buzzer (N2000)

Table 90: Device buzzer

Manufacturer / Number	Description	Package
PUI Audio / SMI-1324-TW-5V-2-R	Buzzer, 5 V (typ.), 30 mA (max.)	SMD2

4.3.7 PMIC diagnosis interface

4.3.7.1 Overview PMIC diagnosis interface

The behaviour of the PMIC on the TQMa6x can be changed using the diagnosis interface (X26).
The switching frequency, the output voltages or the work mode can be changed, for example.
Further information is to be taken from the TQMa6x User's Manual (7), or the PMIC data sheet (5).

Attention:	
	The usability of the PMIC diagnosis interface depends on placement options of the TQMa6x. Update of PMIC settings may only be carried out with extreme care. Wrong settings can lead to system instabilities or irreparable damage the hardware.

4.3.7.2 Connector and position PMIC diagnosis interface

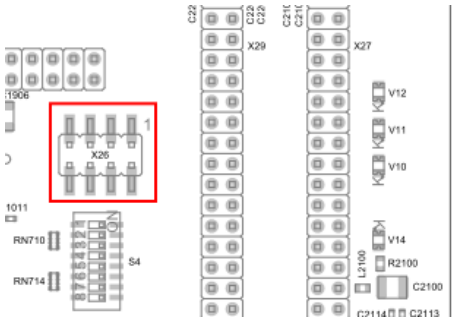


Illustration 53: Position of PMIC diagnose interface (X25)

Table 91: Connector PMIC diagnose interface

Manufacturer / Number	Description	Package
Fischer Elektronik / SL-11-SMD-052-8-Z-BTR	Header, 2.54 mm pitch, 2 × 4 pins	SMD8

Table 92: Pinout PMIC diagnose interface (X25)

Pin	Pin name	Signal	Dir.	Remark
1	VDD8V25	VDD8V25_OTP	P	Programming voltage for OTP fuses
2	VDD3V3	VDD3V3_OTP	P	Auxiliary 3.3 V supply
3	GND	GND	P	
4	SCL	SCL_OTP	I	I2C3 Master clock
5	SDA	SDA_OTP	I/O	I2C3 Master data
6	PWRON	PWRON	I	Logic output to turn-on / turn-off the PMIC
7	–	–	–	
8	–	–	–	

4.3.8 JTAG

4.3.8.1 Overview JTAG

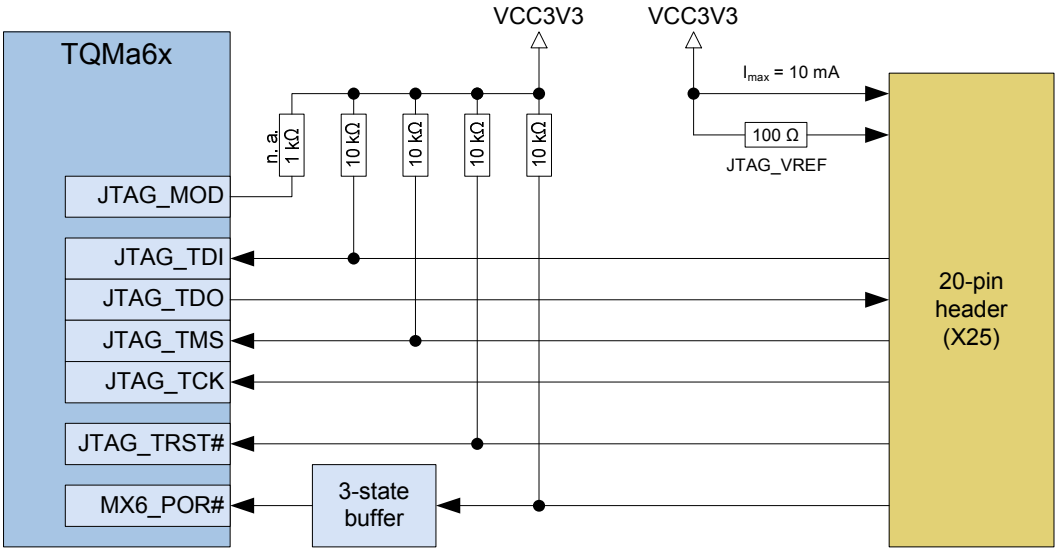


Illustration 54: Block diagram JTAG

The JTAG interface is routed to a 20-pin header (X25).
The pull-ups for the lines TDI, TMS, TRST# and SRST# are assembled on the STK-MBa6x.
All signal lines use 3.3 V as a reference.
The JTAG interface has no ESD protection.

4.3.8.2 Connector and pinout JTAG

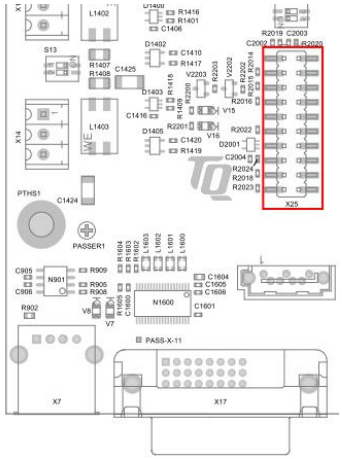


Illustration 55: Position of JTAG (X25)

Table 93: Device JTAG

Manufacturer / Number	Description	Package
Fischer Elektronik / SL-11-SMD-052-20-G-BTR	Header, 2.54 mm pitch, 2 × 10 pins	SMD20

Table 94: Pinout JTAG (X25)

Pin	Pin name	Signal	Dir.	Remark
1	VREF	JTAG.VREF	P	100 Ω in series to VCC3V3, use only as reference
2	VSUPPLY	VCC3V3	P	0 Ω in series to VCC3V3, I_{max}= 10 mA
3	TRST#	JTAG.TRST#	I	10 kΩ Pull-Up to VCC3V3
4	DGND	DGND	P	
5	TDI	JTAG.TDI	I	10 kΩ Pull-Up to VCC3V3
6	DGND	DGND	P	
7	TMS	JTAG.TMS	I	10 kΩ Pull-Up to VCC3V3
8	DGND	DGND	P	
9	TCK	JTAG.TCK	I	
10	DGND	DGND	P	
11	DGND	DGND	P	10 kΩ in series to DGND
12	DGND	DGND	P	
13	TDO	JTAG.DTO	O	
14	DGND	DGND	P	
15	SRST#	JTAG.SRST#	I	10 kΩ Pull-Up to VCC3V3; open drain buffer at MX6_POR#
16	DGND	DGND	P	
17	VCC3V3	VCC3V3	P	
18	DGND	DGND	P	
19	DBGACK	DGND	P	10 kΩ in series to DGND
20	DGND	DGND	P	

5. MECHANICS

5.1 Dimensions

The overall dimensions (length × width) of the STK-MBa6x are 170 × 170 mm².
The maximum height of the STK-MBa6x is approximately 24.1 mm.
The STK-MBa6x has six mounting holes with a diameter of 4.3 mm.
The STK-MBa6x weighs approximately 260 g.

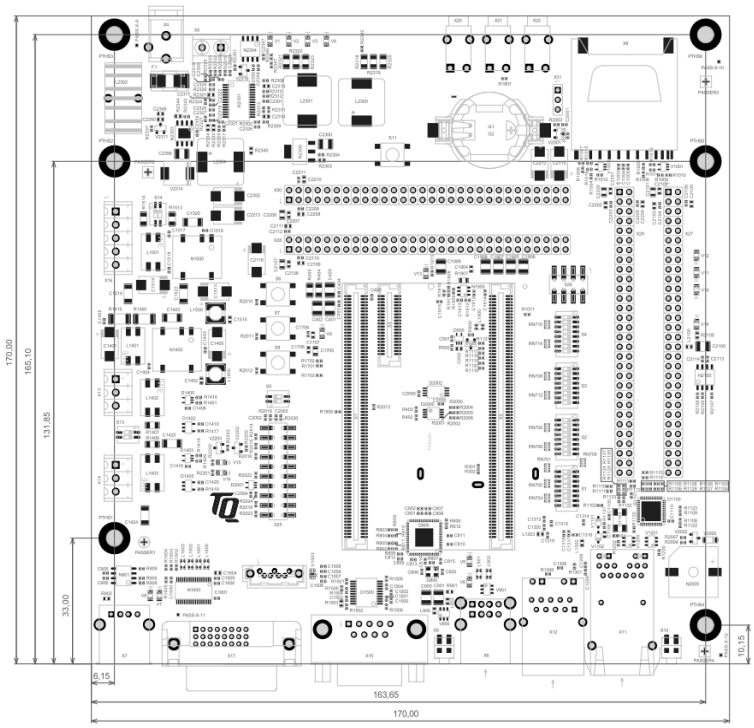


Illustration 56: STK-MBa6x dimensions

5.2 Thermal management

No special precautions were taken concerning the thermal management of the STK-MBa6x.
Cooling the TQMa6x may be necessary depending on the software or the TQMa6x used (Solo/Dual/Quad).
More information is to be taken from the User's Manual of the TQMa6x.

5.3 Assembly

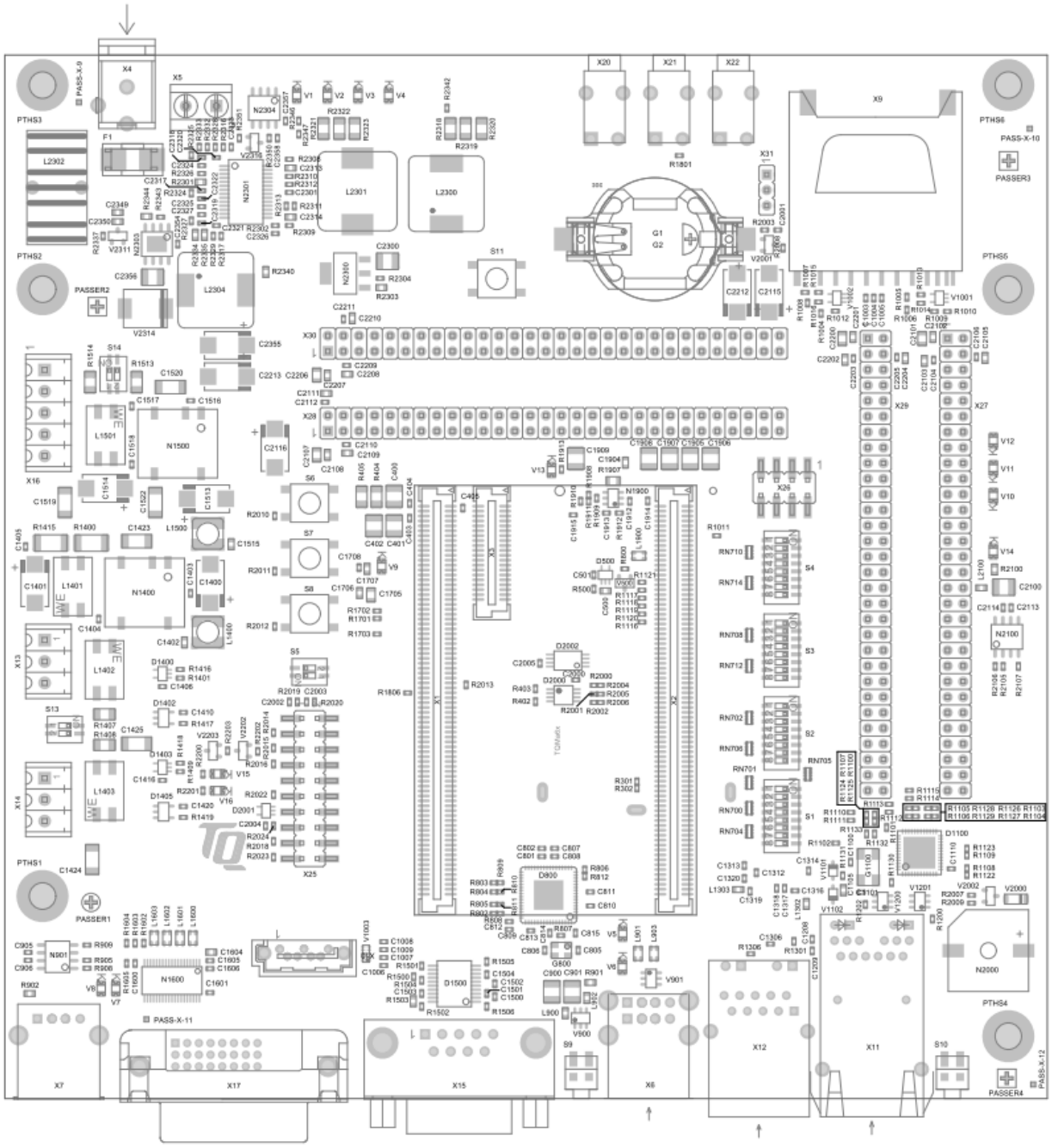


Illustration 57: Component placement top

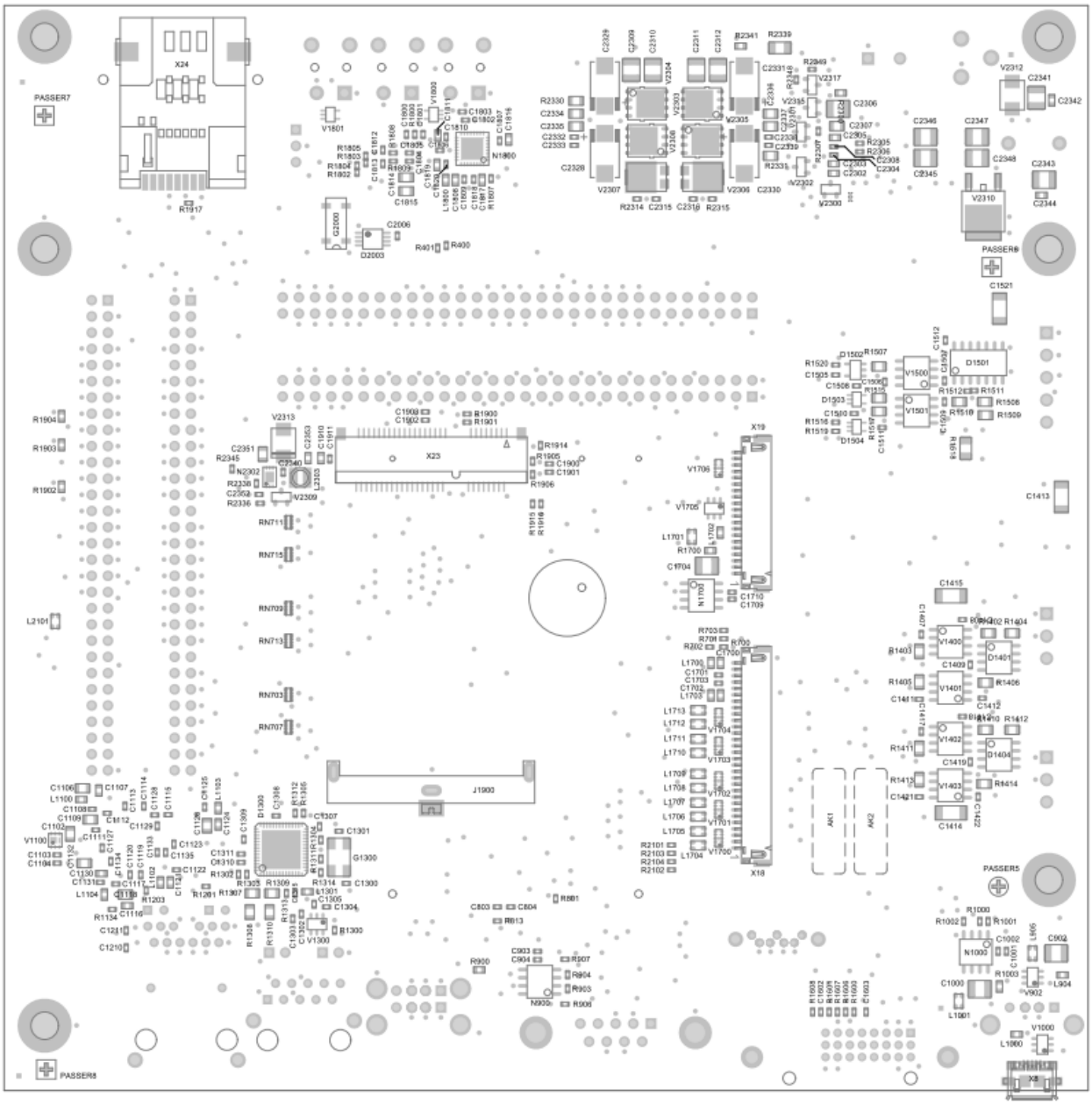


Illustration 58: Component placement bottom

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

Because the STK-MBa6x is a development platform, no EMC specific tests have been carried out.
During the development of the STK-MBa6x the following standard was taken into account:

- EMC-Interference radiation:
  Measurement of the electrically radiated emission for standard, residential, commercial and light industrial environments in the range of 30 MHz to 1 GHz according to DIN EN 55022 A1:2007.

6.2 ESD

Most of the interfaces on the STK-MBa6x are protected against electrostatic discharge. [18]
The interfaces, which provide an ESD protection is to be taken from the circuit diagram.

6.3 Operational safety and personal security

Due to the occurring voltages (≤30 V DC), tests with respect to the operational and personal safety haven't been carried out.

7. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 95: Climatic and operational conditions STK-MBa6x (without TQMa6x)

Parameter	Range	Remark
Permitted environmental temperature	0 … 70 °C	Without Lithium battery CR2032
Permitted environmental temperature	0 … 60 °C	With Lithium battery CR2032
Permitted storage temperature	–10 … 60 °C	–
Relative air humidity (operation / storing)	10 … 90 %	Not condensing

7.1 Protection against external effects

Protection class IP00 was defined for the STK-MBa6x. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the STK-MBa6x. The STK-MBa6x is designed to be insensitive to vibration and impact.

18: The JTAG and PMIC interfaces do not provide ESD protection.

8. ENVIRONMENT PROTECTION

8.1 RoHS compliance

The STK-MBa6x is manufactured RoHS compliant.

- All components and assemblies used are RoHS compliant
- RoHS compliant soldering processes are used

8.2 WEEE regulation

The company placing the product on the market is responsible for the observance of the WEEE regulation (TQ-Systems GmbH).
To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

8.3 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
To be able to reuse the STK-MBa6x, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.
The energy consumption of this subassembly is minimised by suitable measures.
The STK-MBa6x is delivered in reusable packaging.

8.4 Batteries

8.4.1 General notes

Due to technical reasons a battery is necessary for this product. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used. If this is unavoidable for technical reasons, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

8.4.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 g per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.
- During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.5 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
The energy consumption of this subassembly is minimised by suitable measures.
Printed pc-boards are delivered in reusable packaging.
Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.
Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 96: Acronyms

Acronym	Meaning
ADR	Accord européen relatif au transport international des marchandises Dangereuses par Route
AHCI	Advanced Host Controller Interface
AMBA	Advanced Microcontroller Bus Architecture
ARM®	Advanced RISC Machine
ATA	Advanced Technology Attachment
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
CSI	Camera Serial Interface
DC	Direct Current
DDC	Display Data Channel
DDR3	Double Data Rate 3
DIN	Deutsche Industrie Norm
DIP	Dual In-line Package
DNC	Do Not Connect
DSI	Display Serial Interface
DVI	Digital Visual Interface
DVI-D	Digital Visual Interface-Digital
ECSPI	Enhanced Capability Serial Peripheral Interface
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
eMMC	embedded MultiMediaCard (Flash)
EN	European Standard (Europäische Norm)
ESD	Electrostatic Discharge
eSPI	Enhanced Serial Peripheral Interface
FFC	Flat Flex Cable
FR4	Flame Retardant-4
GPIO	General Purpose Input/Output
GSM	Global System for Mobile Communications (Groupe Spécial Mobile)
HDD	Hard Disk Drive
HDMI	High Definition Multimedia Interface
I	Input
I/O	Input/Output
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
IPD	Input with Pull-Down (resistor)
IPU	Input with Pull-Up (resistor)
I^2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signalling

Table 96: Acronyms (continued)

Acronym	Meaning
MAC	Media Access Control
MII	Media-Independent Interface
MIPI	Mobile Industry Processor Interface
MMC	Multimedia Card
MSB	Most Significant Bit
MTBF	Mean operating Time Between Failures
n.a.	Not Assembled
n.c.	Not Connected
NOR	Not-Or
O	Output
OOD	Output with Open Drain
OPU	Output with Pull-Up
OTG	On-The-Go
OTP	One-Time Programmable
P	Power
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management IC
PU	Pull-Up
PWM	Pulse Width Modulation
PWR	Power
RFU	Reserved for Future Usage
RGMII	Reduced Gigabit Media Independent Interface
RJ45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
SATA	Serial ATA
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SMD	Surface-Mounted Device
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
TCP	Transmission Control Protocol
THD	Through Hole Device
THT	Through-Hole Technology
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
WDOG	Watchdog
WEEE	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WP	Write-Protection
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

9.2 References

Table 97: Further applicable documents

No.	Name	Revision / Date	Author	Company
(1)	IMX6DSDLRM	Rev. 1, 04/2013	Freescale	Freescale
(2)	IM&DQRM	Rev. 1, 04/2013	Freescale	Freescale
(3)	IMX6SDLCE	Rev. 5, 12/2014	Freescale	Freescale
(4)	IMX6DQCE	Rev. 4, 07/2014	Freescale	Freescale
(5)	MMPF0100	Rev. 7.7, 12/2013	Freescale	Freescale
(6)	TQMa6x.UM	Current Revision	TQ-Systems	TQ-Systems
(7)	KSZ9031 Errata Sheet	11/2012	Micrel	Micrel

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Technology in Quality