Qseven® conga-QAF

AMD G-Series Processor with AMD A55E Controller Hub

User's Guide

Revision 1.1

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
1.0	2012.04.26	GDA	• Official release.
1.1	2013.04.09	AEM	• Added Microsoft Windows 8 support in section 1.2 "Supported Operating System".
			• Changed maximum torque rating for heatspreader screws in section 3.1 "Heatspreader Dimensions" and added a caution statement.
			• Added additional conga-QAF variants in "Options Information" and section 1.1 "Feature List".
			• Added the inrush and maximum peak current values in section 4.15 "Power Control"
			• Updated section 9 "BIOS Setup Description".
			• Added section 10.1 "Supported Flash Devices". Updated the whole document.

Preface

This user's guide provides information about the components, features, connector and BIOS Setup menus available on the conga-QAF. It is one of three documents that should be referred to when designing a Qseven® application. The other reference documents that should be used include the following:

> Qseven® Design Guide
>
> Qseven® Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
PCI Express (PCIe)	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4, x8, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4, x8, or x16 link.
ExpressCard	A PCMCIA standard built on the latest USB 2.0 and PCI Express buses.
PCI Express Mini Card	PCI Express Mini Card add-in card is a small size unique form factor optimized for mobile computing platforms.
MMCplus	MMCplus was defined for first time in MMC System Specification v4.0. MMCplus is backward compatible with MMC. MMCplus has 13 pins.
SDIO card	SDIO (Secure Digital Input Output) is a non-volatile memory card format developed for use in portable devices.
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial-interface standard for hard disks
HDA	High Definition Audio
S/PDIF	S/PDIF (Sony/Philips Digital Interconnect Format) specifies a Data Link Layer protocol and choice of Physical Layer specifications for carrying digital audio signals between devices and stereo components.
DDI	Digital Display Interface. DDI can operate as DisplayPort or HDMI or DVI.
DP	DisplayPort is an VESA's open digital communications interface.
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
LPC	Low Pin-Count: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy device support into a single IC.
I²C Bus	Inter-Integrated Circuit Bus: is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system.
SM Bus	System Management Bus: is a popular derivative of the I²C-bus.
SPI Bus	Serial Peripheral Interface is a synchronous serial data link standard named by Motorola that operates in full duplex mode.
CAN Bus	Controller-area network is a vehicle bus standard designed to allow microcontrollers and devices to communicate with each other within a vehicle without a host computer.
GbE	Gigabit Ethernet
LVDS	Low-Voltage Differential Signaling
SDVO	Serial Digital Video Out is a proprietary technology introduced by Intel® to add additional video signaling interfaces to a system.
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

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Qseven® Concept

The Qseven® concept is an off-the-shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm and a specified pinout based on the high speed MXM system connector. The pinout remains the same regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

The Qseven® evaluation carrier board provides carrier board designers with a reference design platform and the opportunity to test all the Qseven® I/O interfaces available and then choose what are suitable for their application. Qseven® applications are scalable, which means once a carrier board has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another, no need to redesign the carrier board.

This document describes the features available on the Qseven® evaluation carrier board. Additionally, the schematics for the Qseven® evaluation carrier board can be found on the congatec website.

Certification

congatec AG is certified to DIN EN ISO 9001:2008 standard.

Technical Support

congatec AG technicians and engineers are committed to providing the best possible technical support for our customers so that our products can be easily used and implemented. We request that you first visit our website at www.congatec.com for the latest documentation, utilities and drivers, which have been made available to assist you. If you still require assistance after visiting our website then contact our technical support department by email at support@congatec.com

Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

conga-QAF Options Information

The conga-QAF is available in six base variants. This user's guide describes all of these variants. The table below shows the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

conga-QAF

Part-No.	015300	015301	015302	015303	015304	015305
Processor	AMD T40R	AMD T40E	AMD T24L	AMD T40 E	AMD T40R	AMD T16R
Clock Speed	1.0 GHz	1.0 GHz	1.0 GHz	1.0 GHz	1.0 GHz	1.0 GHz
Core	Single	Dual	Single	Dual	Single	Single
L2 Cache	512kB	512kB x2	512kB	512kB x2	512kB	512kB
TDP	5.5 W	6.4 W	5 W	6.4 W	5.5 W	5.5 W
Onboard Memory	DDR3L-1066	DDR3L-1066	DDR3L-1066	DDR3L-1066	DDR3L-1066	DDR3L-1066
Size	2GB	2GB	2GB	2GB	2GB	2GB
Graphics	Radeon™ HD 6250	Radeon™ HD 6250	N/A	Radeon™ HD 6250	Radeon™ HD 6250	Radeon™ HD 6250
LVDS	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit
DDI	DP / HDMI / DVI	DP / HDMI / DVI	DP / HDMI / DVI	DP / HDMI / DVI	DP / HDMI / DVI	DP / HDMI / DVI
SDVO	N/A	N/A	N/A	N/A	N/A	N/A
SSD	N/A	N/A	N/A	4GB	8GB	4GB

Note

The processor TDP is defined for PCIe Gen1 configuration. When PCIe Gen2 is used, the processor TDP increases up to +2.5W.

The conga-QAF variants equipped with the AMD T24L processor do not support graphics display.

Contents

List of Tables

1 Specifications

1.1 Feature List

Table 1   Feature Summary

Form Factor	Based on Qseven® form factor specification revision 1.20
Processor	AMD T40E 1.0 GHz Dual Core with 2x 512kB L2 cache AMD T40R 1.0 GHz Single Core with 512kB L2 cache AMD T24L 1.0 GHz Single Core with 512KB L2 cache AMD T16R 1.0 GHz Single Core with 512KB L2 cache
Memory	Onboard DDR3L 1066 MT/s (533 MHz) up to 4 GB
Chipset	A55E Controller Hub
Audio	HDA (High Definition Audio)/digital audio interface with support for multiple codecs
Ethernet	Gigabit Ethernet: Intel® 82574
Graphics Options	Integrated High Performance, DirectX®11 Graphics with UVD 3.0. Dual Simultaneous Display Support

	• Flat panel Interface (provided by Analogix ANX3110 to LVDS converter). Supports: Digital Display Interface (uses APU DP1 port) can operate as
	    • Single-channel LVDS interface: 1 x 18 bpp or 1 x 24 bpp • DisplayPort 1.1a, resolutions up to 1920x1200 @ 60 Hz-,
	    • Dual-channel LVDS interface: 2 x 18 bpp or 2 x 24 bpp panel • HDMI 1.3a Port, resolution up to 1920x1080 @ 60 Hz-,
	    • VESA standard or JEDIA data mapping • Single-link DVI, resolutions up to 1920x1200 @ 60 Hz
	    • Automatic Panel Detection via EDID/EPI (Embedded Panel Interface based on VESA EDID™ 1.3)
	    • Resolutions 800x600 up to 1900x1200 (WUXGA) @ 60 Hz

Peripheral Interfaces	• 2x Serial ATA® up to 3Gb/s with support RAID 0,1 • Optional onboard SSD up to 32 GB • 4x x1 PCI Express® Gen2 links up to 5.0 GT/s per lane • 1x SD/MMC • 8x USB 2.0 (EHCI) • LPC Bus • 2x ExpressCard • I²C Bus, multimaster
BIOS	AMI Aptio® UEFI 2.x firmware, 4MByte serial SPI with congatec Embedded BIOS features
Power Management	ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 8 of this user's guide to determine what options are available on your particular module.

1.2 Supported Operating Systems

The conga-QAF supports the following operating systems.

- Microsoft® Windows® 8 32/64-Bit

- Microsoft® Windows® 7 32/64-Bit

- Microsoft® Windows® 7 Embedded 32/64-Bit

- Microsoft® Windows® XP

- Microsoft® Windows® XP Embedded

- Linux

1.3 Mechanical Dimensions

- 70.0 mm x 70.0 mm @ (2 ¾" x 2 ¾")

- The Qseven™ module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12mm thick.
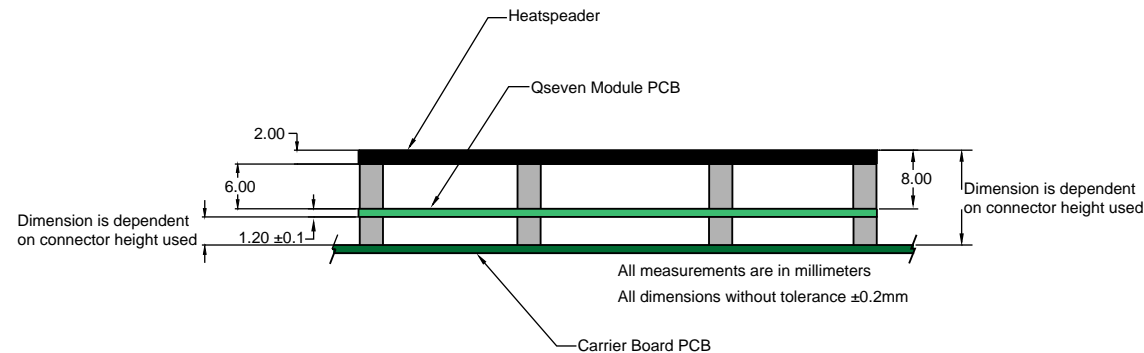
Rear View of Qseven Module

1.4 Supply Voltage Standard Power

- 5V DC ± 5%

The dynamic range shall not exceed the static range.
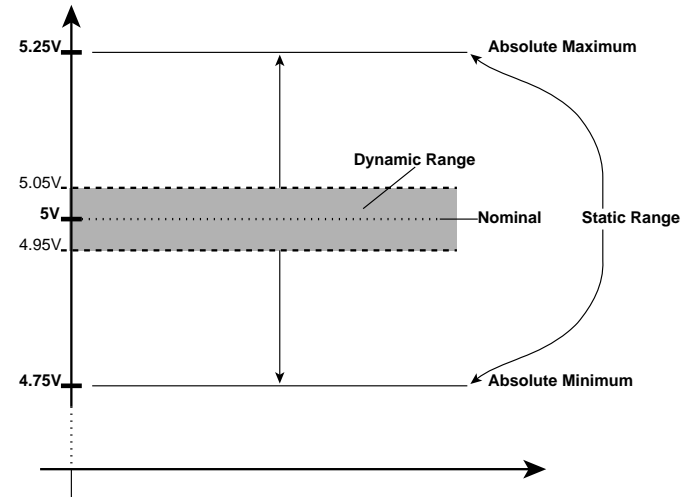
1.4.1 Electrical Characteristics

Characteristics			Min.	Typ.	Max.	Units	Comment
5V	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	± 50	mV$_{PP}$	0-20MHz
	Current						
5V_SB	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple				± 50	mV$_{PP}$	

1.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

Note

For information about the input power sequencing of the Qseven® module refer to the Qseven® specification.

1.5   Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used includes a conga-QAF module, conga-QEVAL, SATA drive, USB keyboard and USB mouse. The SATA drive, USB Keyboard, USB mouse were powered separately so that they do not influence the power consumption value that is measured for the module.

Each module was measured while running Windows XP Professional with SP3 (service pack 3) and the "Power Scheme" was set to "Portable/ Laptop". This setting ensures that the AMD G-Series processors run in (lowest frequency mode) with minimal core voltage during desktop idle. Power consumption values were recorded during the following stages:

Windows XP Professional SP3

• Desktop Idle

• 100% CPU workload (see note below)

• Suspend to RAM (requires setup node "Suspend Mode" in BIOS to be configured to S3 STR (suspend to RAM)). Supply power for S3 mode is 5V SB.

Note

A software tool was used to stress the CPU to 100% workload.

Processor Information

In the following power tables there is some additional information about the processors. AMD describes the type of manufacturing process used for each processor. The following term is used:

nm=nanometer

The manufacturing process description is included in the power tables. See example below. For information about the manufacturing process visit AMD's website.

AMD T40E 1.0 GHz Dual Core 512kB x2 Cache
40nm

1.5.1 conga-QAF AMD T40R 1.0 GHz Single Core

With 2GB onboard memory

conga-QAF Art. No. 015300	AMD T40R 1.0 GHz Single Core 512kB L2 Cache 40nm Layout Rev. QBRALA0 /BIOS Rev. QBRAR002		
Memory Size	2GB		
Operating System	Windows XP SP3		
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V SB Input
Power consumption (measured in Amperes/Watts)	1.09A / 5.43W	1.44A / 7.21W	0.06A / 0.30W

1.5.2 conga-QAF AMD T40R 1.0 GHz Single Core with 8GB SSD

With 2GB onboard memory and 8GB SSD

conga-QAF Art. No. 015304	AMD T40R 1.0 GHz Single Core 512kB L2 Cache 40nm Layout Rev. QBRALA0 /BIOS Rev. QBRAR002		
Memory Size	2GB		
Operating System	Windows XP SP3		
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V SB Input
Power consumption (measured in Amperes/Watts)	TBD A / TBD W	TBD A / TBD W	TBD A / TBD W

1.5.3 conga-QAF AMD T24L 1.0 GHz Single Core without GPU

With 2GB onboard memory

conga-QAF Art. No. 015302	AMD T24L 1.0 GHz Single Core 512kB L2 Cache 40nm Layout Rev. QBRALA0 /BIOS Rev. QBRAR002		
Memory Size	2GB		
Operating System	Windows XP SP3		
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V SB Input
Power consumption (measured in Amperes/Watts)	1.12A / 5.60W	1.38A / 6.92W	NA

1.5.4 conga-QAF AMD T16R 1.0 GHz Single Core with 4GB SSD

With 2GB onboard memory and 4GB SSD

conga-QAF Art. No. 015305	AMD T16R 1.0 GHz Single Core 512kB L2 Cache 40nm Layout Rev. QBRALA0 /BIOS Rev. QBRAR002		
Memory Size	2GB		
Operating System	Windows XP SP3		
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V SB Input
Power consumption (measured in Amperes/Watts)	TBD A / TBD W	TBD A / TBD W	TBD A / TBD W

1.5.5 conga-QAF AMD T40E 1.0 GHz Dual Core

With 2GB onboard memory

conga-QAF Art. No. 015301	AMD T40E 1.0 GHz Dual Core 512kB x2 L2 Cache 40nm Layout Rev. QBRALA0 /BIOS Rev. QBRAR002		
Memory Size	2GB		
Operating System	Windows XP SP3		
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V SB Input
Power consumption (measured in Amperes/Watts)	1.14A / 5.70W	1.64A / 8.18W	0.06A / 0.30W

1.5.6   conga-QAF AMD T40E 1.0 GHz Dual Core with 4GB SSD

With onboard 2GB memory and 4GB SSD

conga-QAF Art. No. 015303	AMD T40E 1.0 GHz Dual Core 512kB x2 Cache 40nm Layout Rev. QBRALA0 /BIOS Rev. QBRAR002		
Memory Size	2GB		
Operating System	Windows XP SP3		
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V SB Input
Power consumption (measured in Amperes/Watts)	1.20A / 6.00 W	1.73 A / 8.64 W	0.06A / 0.30W

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

The conga-QAF variants equipped with the AMD T24L processor do not support graphics.

1.6   Supply Voltage Battery Power

- 2.5V-3.6V DC

- Typical 3V DC

1.6.1   CMOS Battery Power Consumption

RTC @ 20ºC	Voltage	Current
Integrated in the AMD A55E FCH	3V DC	Typ. 2.05µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

1.7 Environmental Specifications

Temperature   Operation: 0° to 60°C   Storage: -20° to +80°C

Humidity   Operation: 10% to 90%   Storage: 5% to 95%

⚠ Caution

The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.

If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

For more information about operating a congatec module without heatspreader, contact congatec technical support.

Humidity specifications are for non-condensing conditions.

2 Block Diagram
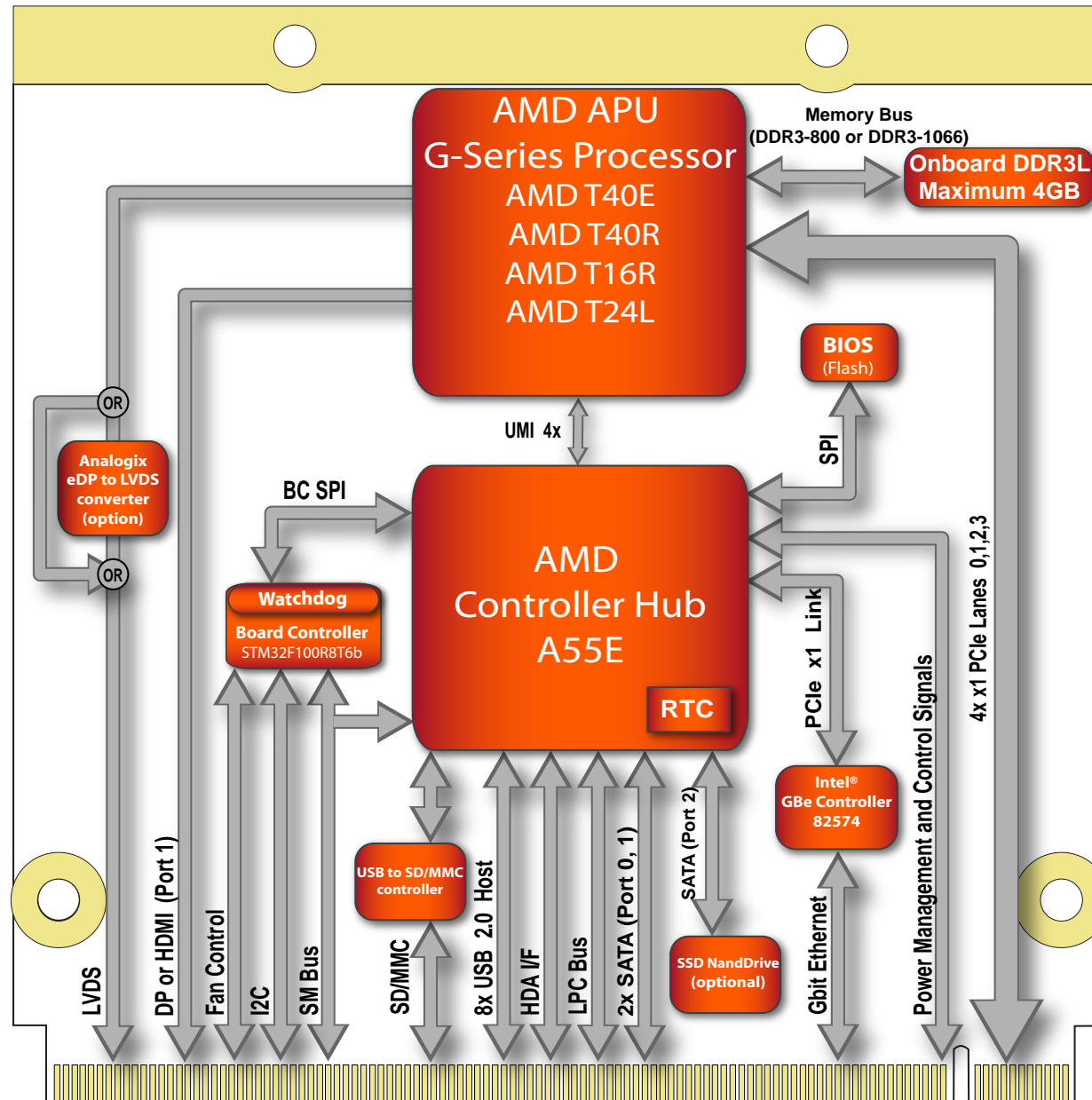
3 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module and its aluminium plate is 2mm thick.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.

⚠ Caution

Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

Only heatspreaders that feature micro pins that secure the thermal stacks should be used for applications that require the heatspreader to be mounted vertically. It cannot be guaranteed that the thermal stacks will not move if a heatspreader that does not have the micro pin feature is used in vertically mounted applications.

Additionally, the gap pad material used on all heatspreaders contains silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.

3.1 Heatspreader Dimensions

Heatspreader plate

Aluminum Standoff
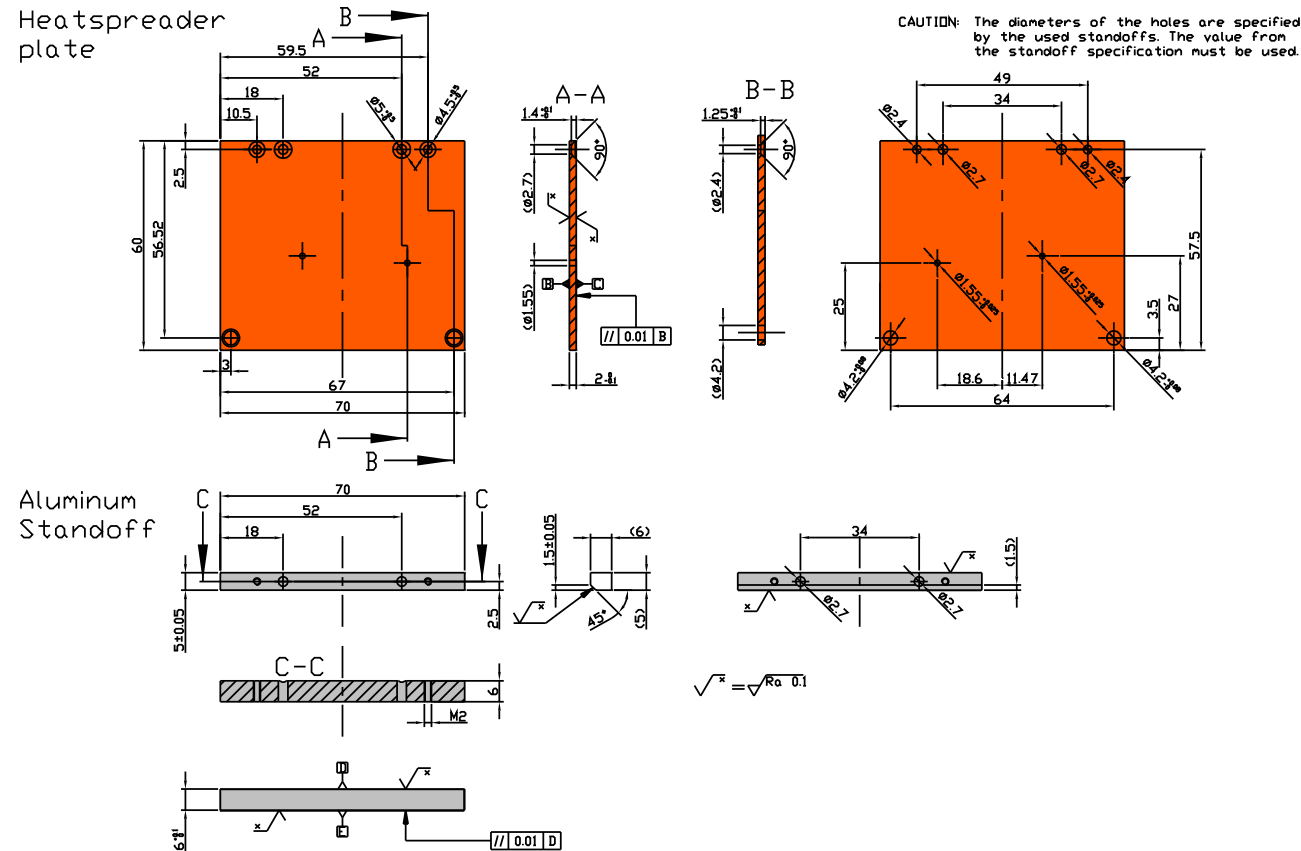
> **Note**
>
> *All measurements are in millimeters. Torque specification for heatspreader screws is 0.3 Nm. Mechanical system assembly mounting shall follow the valid DIN/IS0 specifications. The cooling strip found on the conga-QAF is connected directly to the ground plane when mounted in the conga-QEVAL evaluation carrier board. For more information about connecting the conga-QAF's PCB cooling plate to the carrier board ground plane, refer to the Qseven Design Guide.*

> **Caution**
>
> *When using the heatspreader in a high shock and/or vibration environment, congatec recommends the use of a thread-locking fluid on the heatspreader screws to ensure the above mentioned torque specification is maintained.*

4   Connector Subsystems

The conga-QAF is based on the Qseven® standard and therefore has 115 edge fingers on the top and bottom side of the module that mate with the 230-pin card-edge MXM connector located on the carrier board. This connector is able to interface the available signals of the conga-QAF with the carrier board peripherals.

4 PCI Express Lanes
2x Serial ATA
8x USB 2.0
HDA/Digital Audio I/F
Gigabit Ethernet
(Uses one PCI Express Lane)
LPC Bus
1x SDIO

I²C Bus
SPI Bus
LVDS
Watchdog
Power Control
Power Management
Fan Control
DisplayPort/HDMI
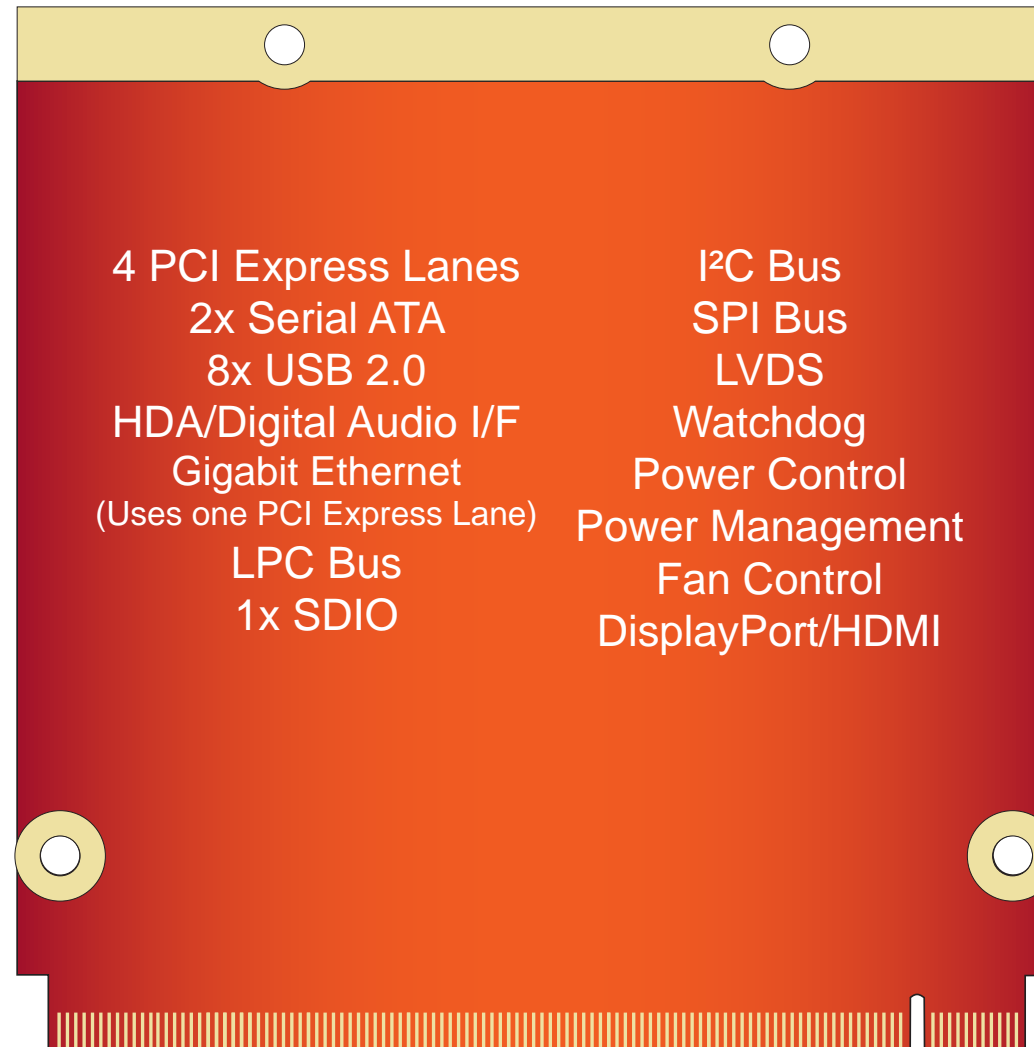
4.1　PCI Express™

The AMD G-Series processor supports 4 PCI Express Gen2 lanes as PCIe channel 0, 1, 2 and 3 on the carrier board and are made available externally via the MXM connector. The lanes can be configured to support PCI Express devices, edge cards or express cards. The PCI Express interface supports PCI Express Specification 2.0.

For more information refer to the conga-QAF pinout table in section 7 "Signal Descriptions and Pinout Tables." A 4 x1 or 1 x4 PCI Express lane configuration is possible.

4.2　ExpressCard™

The conga-QAF can support the implementation of two express cards, each requiring the dedication of one USB port and one PCI Express lane. Refer to section 7, "Signal Descriptions and Pinout Tables" for information about ExpressCard port pins.

4.3　Gigabit Ethernet

The conga-QAF is equipped with a Gigabit Ethernet Media Dependent Interface (GbE MDI), provided by the Intel® 82574 GbE controller that is connected to a AMD Controller Hub by PCI Exprees x1 lane. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

4.4　Serial ATA™ (SATA)

Two 3Gb/s Serial ATA (SATA port 0 and 1) connections are provided by a SATA controller integrated in the AMD Controller Hub A55E found on the conga-QAF. The optional SSD feature uses SATA port 2.

4.5　USB 2.0

The conga-QAF offers a USB 2.0 host controller provided by the AMD Controller Hub A55E. This controller complies with USB standard 1.1 and 2.0 and provides a total of 8 USB ports via the card-edge MXM connector. All ports are capable of supporting USB 1.1 and 2.0 compliant devices. The USB client port is not supported by conga-QAF.

4.6　SD/MMC

The SMSC USB 2.0 Flash Media Card Controller USB2244 found on the conga-QAF provides a SD/MMC expansion port for communicating with non-volatile SD or MMC card. This port is available externally and supports SD Revision 2.0 and MMC Revision 4.2 and is backward compatible with previous interface specifications.

Note

Only DOS and Linux (Ubuntu, Xandros) boot support for SDIO/MMC devices is available.

4.7　High Definition Audio (HDA)

The conga-QAF provides an interface that supports the connection of HDA audio codecs.

4.8　LVDS

The conga-QAF offers an LVDS interface via Analogix DP to LVDS converter, connected to the DP0 interface of the AMD G-Series processor. It supports 18 or 24 bit single/dual channel VESA or JEIDA data mapping with resolutions ranging from 800x600@60Hz to 1920x1200@60Hz. Automatic panel detection via EDID/EPI is supported.

4.9　SDVO

The conga-QAF does not offer an SDVO interface.

4.10　DisplayPort

DisplayPort is an open, industry standard digital display interface, that has been developed within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

The DP is provided by the DDI of the AMD G-Series processor (DP1 interface) and is shared with the HDMI. The supported resolution is up to 1920x1200@60Hz.

4.11 HDMI

High-Definition Multimedia Interface (HDMI) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video.

The HDMI is provided by the DDI of the AMD G-Series processor (DP1 interface) and is shared with DisplayPort. The supported resolution is up to 1920x1200@60Hz.

4.12 LPC

The conga-QAF offers the LPC (Low Pin Count) bus through the use of the AMD Controller Hub A55E. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals and functionality. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific carrier board using this bus. Only certain devices such as Super I/O or TPM 1.2 chips can be implemented on the carrier board.

4.13 SPI

The conga-QAF offers the SPI interface only for booting a BIOS from an SPI Flash device placed on the carrier board.

4.14 CAN Bus

The conga-QAF does not offer the CAN bus.

4.15 Power Control

The conga-QAF supports ATX-style power supplies control. In order to do this the power supply must provide a constant source of VCC_5V_SB power. The AT-style power supply (5V only) is also supported. In this case, the conga-QAF's pin PWRBTN# should be left unconnected, pin SUS_S3# should control the main power regulators on the carrier board (+3.3V...) and pins VCC_5V_SB should be connected to the 5V input power rail according to the Qseven specification.

PWGIN

PWGIN (pin 26) can be connected to an external power good circuit. This input is optional and should be left unconnected when not used. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies, the conga-QAF module is capable of

generating its own power-on good.

SUS_S3#

The SUS_S3# (pin 18) signal is an active-low output that can be used to control the main 5V rail of the power supply for module and all other main power supplies on carrier board. In order to accomplish this, the signal must be inverted with an inverter/transistor that is supplied by standby voltage (ATX-style) or system input voltage (AT-style) and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin 20) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3.3V_SB using a 10k resistor. When PWRBTN# is asserted, it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-QAF. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-QAF application:

• It has also been noticed that on some occasions, problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush-current on the conga-QAF VCC_5V_SB power rail (8ms soft-start) can go up as high as 0.4A for a maximum of 100µs. Sufficient decoupling capacitance must be implemented to ensure proper power-up sequencing.

The maximum peak-current on the conga-QAF VCC (5V) power rail can be as high as 3.0A. This requires that the power supply be properly dimensioned.

Note

For more information about power control event signals refer to the Qseven® specification.

4.16 Power Management

ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3). No support for legacy APM.

4.17 I²C Bus

The I²C bus is implemented through the use of STMicroelectronics STM32F100R8 microcontroller. It provides a multi-master I²C Bus that has maximum I²C bandwidth.

4.18 Watchdog

The conga-QAF is equipped with a multi stage watchdog solution that can be triggered by software or external hardware. For more information about the watchdog feature, see the BIOS setup description of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

4.19 Fan Control

The conga-QAF has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

A four wire fan must be used to generate the correct speed readout.

5 Additional Features

5.1 congatec Board Controller (cBC)

The conga-QAF is equipped with an STMicroelectronics STM32F100R8 microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

5.2 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

5.3 Watchdog

The conga-QAF is equipped with a multi stage watchdog solution that is triggered by software. The Qseven™ Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-QAF does not support external hardware triggering.

For more information about the Watchdog feature, see the BIOS setup description section 9.4.2 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

5.4 I²C Bus

The conga-QAF offers support for the frequently used I²C bus. Thanks to the I²C host controller in the cBC, the I²C bus is multi-master capable.

5.5 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are "Always On", "Remain Off" and "Last State".

5.6 Embedded BIOS

The conga-QAF is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. These are the most important embedded PC features:

5.6.1 CMOS Backup in Non Volatile Memory

A copy of the CMOS memory (SRAM) is stored in the BIOS flash device. This prevents the system from not booting up with the correct system configuration if the backup battery (RTC battery) fails. Additionally, it provides the ability to create systems that do not require a CMOS backup battery.

5.6.2 OEM CMOS Default Settings and OEM BIOS Logo

This feature allows system designers to create and store their own CMOS default configuration and BIOS logo (splash screen) within the BIOS flash device. Customized BIOS development by congatec for these changes is no longer necessary because customers can easily do these changes by themselves using the congatec system utility CGUTIL.

5.6.3 OEM BIOS Code

With the congatec embedded BIOS it is even possible for system designers to add their own code to the BIOS POST process. Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table, verb tables for HDA codecs, rare graphic modes and Super I/O controllers.

For more information about customizing the congatec embedded BIOS, refer to the congatec system utility user's guide (CGUTLm1x.pdf) and can be found on the congatec AG website at www.congatec.com or contact congatec technical support.

5.6.4 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a smart battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI-capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for additional modifications to the system BIOS.

The conga-QAF BIOS fully supports this interface. For more information about this subject, visit the congatec website and view the following documents:

• congatec Battery Management Interface Specification

• Battery System Design Guide

• conga-SBM[3] User's Guide

5.6.5 API Support (CGOS/EAPI)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux and QNX. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

Other COM (Computer on Modules) vendors offer similar driver solutions for these kind of embedded PC features, which are by nature proprietary. All the API solutions that can be found on the market are not compatible to each other. As a result, writing application software that can run on more than one vendor's COM is not so easy. Customers have to change their application software when switching to another COM vendor.

EAPI (Embedded Application Programming Interface) is a programming interface defined by the PICMG that addresses this problem. With this unified API it is now possible to run the same application on all vendor's COMs that offer EAPI driver support. Contact congatec technical support for more information about EAPI.

5.7 Suspend to RAM

The Suspend to RAM feature is available on the conga-QAF.

5.8   Onboard Solid State Disk

A solid-state drive (SSD) is a data storage device that uses solid-state memory to store persistent data. An SSD is a hard disk drive without the traditional moving parts, thus easily replacing traditional hard drives in most applications. The conga-QAF can be optionally equipped with an SSD up to 32 GByte in capacity.

Due to the nature of NAND Flash technology, there is a limitation of maximum write cycles related to each storage cell. According to the manufacturer datasheet, an endurance of 10 million (for commercial MLC technology) or 100 million (for industrial SLC technology) write cycles is specified. Unlimited write cycles IS NOT specified. Since an advanced NAND memory management technology firmware is implemented in the SSD drive, it will balance the wear on erased blocks with an advanced wear-leveling algorithm, which provides a maximum of 10 million (or 100 million depending of the type of SSD used) product write cycles. In most applications this will be an acceptable and secure solution but it must be mentioned that the device lifetime will be affected mainly by the following parameters:

1. Operation time and used OS: If a 24/7 application is running under a write-intensive OS (such as Windows XP etc.) without EWF (Enhanced Write Filter), the amount of guaranteed write-cycles may be reached before the defined MTBF of the complete system.

2. The ratio between used and unused SSD capacity will also affect the lifetime. Since the wear-leveling algorithm uses access statistics for balancing the wears on the blocks, the SSD endurance will increase or decrease according to the amount of used and unused SSD space.

3. Given the information in parameters 1 and 2, if the SSD application is a 24/7 continuously running OS equipped SSD drive, with frequent write accesses and there is not enough free capacity available for wear leveling, the SSD endurance will decrease accordingly. For this reason it is necessary to avoid a configuration that will result in not enough free capacity being available for wear leveling and therefore it is required that an EWF mechanism is used thereby limiting the write-cycles in order to maintain sufficient free disk space. Failure to use a EWF mechanism will void the warranty of the SSD drive.

▷ **Note**

For more information about the SSD drive's capability refer to the manufacturers datasheet.

6 conga Tech Notes

The conga-QAF has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the system resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

6.1 AHCI

The AMD A55E FCH provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

6.2 RAID

The industry-leading RAID capability provides high performance RAID 0 and 1 functionality on the 2 SATA ports of the conga-QAF. Software components include an Option ROM for pre-boot configuration and boot functionality, a Microsoft Windows compatible driver, and a user interface for configuration and management of the RAID capability of the AMD A55E FCH.

For more information about RAID support on the conga-QAF refer to application note AN15_Configure_RAID_System.pdf, which can be found on the congatec AG website at www.congatec.com.

6.3 Native vs. Legacy IDE mode

6.3.1 Legacy Mode

When operating in legacy mode, the SATA controllers need two legacy IRQs (14 and 15) and are unable to share these IRQs with other devices. This is because the SATA controllers emulate the primary and secondary legacy IDE controllers.

6.3.2 Native Mode

Native mode allows the SATA controllers to operate as true PCI devices and therefore do not need dedicated legacy resources. This means they can be configured anywhere within the system. When either SATA controller 1 or 2 runs in native mode it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system. Setting "Native IDE" mode in the BIOS setup

program will automatically enable Native mode. See section 9.4.9 for more information about this. Running in native mode frees up interrupt resources (IRQs 14 and 15) and decreases the chance that there may be a shortage of interrupts when installing devices.

Note

If your operating system supports native mode then congatec AG recommends you enable it.

6.4 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-QAF ACPI thermal solution offers three different cooling policies.

• **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

• **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the "active cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

• **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

6.5   ACPI Suspend Modes and Resume Events

conga-QAF supports S3 (STR= Suspend to RAM). For more information about S3 wake events see section 9.4.4 "ACPI Configuration Submenu".

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

• Windows 7, Windows Vista, Windows XP and Linux

This table lists the "Wake Events" that resume the system from S3 unless otherwise stated in the "Conditions/Remarks" column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, the following must be done for a USB Mouse/Keyboard Event to be used as a Wake Event. USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). Under Windows XP add following registry entries: Add this key: HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\usb Under this key add the following value: "USBBIOSx"=DWORD:00000000 *Note that Windows XP disables USB wakeup from S3, so this entry has to be added to re-enable it.* Configure USB keyboard/mouse to be able to wake up the system: In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'. *Note: When the standby state is set to S3 in the ACPI setup menu, the power management tab for USB keyboard /mouse devices only becomes available after adding the above registry entry and rebooting to allow the registry changes to take affect.*
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

▷ Note

The above list has been verified using a Windows XP SP3 ACPI enabled installation.

7   Signal Descriptions and Pinout Tables

The following section describes the signals found on Qseven® module's edge fingers.

Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

Not all the signals described in this section are available on all conga-QAF variants. Use the article number of the module and refer to the options table on page 8 to determine the options available on the module.

Table 2   Signal Tables Terminology Descriptions

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PP	Push Pull
I/O	Bi-directional Input/Output Pin
P	Power Input
NA	Not applicable
NC	Not Connected
PCIE	PCI Express differential pair signals. In compliance with the PCI Express Base Specification 2.0
GB_LAN	Gigabit Ethernet Media Dependent Interface differential pair signals. In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet Specification.
USB	Universal Serial Bus differential pair signals. In compliance with the Universal Serial Bus Specification 2.0
SATA	Serial Advanced Technology Attachment differential pair signals. In compliance with the Serial ATA High Speed Serialized AT Attachment Specification 2.6.
SPI	Serial Peripheral Interface bus is a synchronous serial data link that operates in full duplex mode.
CAN	Controller Area Network bus is a vehicle bus standard that allows microcontrollers and devices to communicate with each other within a vehicle without a host computer.
LVDS	Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0.
TMDS	Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0.
CMOS	Logic input or output.

Table 3   Edge Finger Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Power Ground	2	GND	Power Ground
3	GBE_MDI3-	Gigabit Ethernet MDI3-	4	GBE_MDI2-	Gigabit Ethernet MDI2-
5	GBE_MDI3+	Gigabit Ethernet MDI3+	6	GBE_MDI2+	Gigabit Ethernet MDI2+
7	GBE_LINK100#	100 Mbps link speed	8	GBE_LINK1000#	1000 Mbps link speed
9	GBE_MDI1-	Gigabit Ethernet MDI1-	10	GBE_MDI0-	Gigabit Ethernet MDI0-
11	GBE_MDI1+	Gigabit Ethernet MDI1+	12	GBE_MDI0+	Gigabit Ethernet MDI0+
13	GBE_LINK#	Gigabit Ethernet Link indicator	14	GBE_ACT#	Gigabit Ethernet Activity indicator
15	GBE_CTREF	Reference voltage for GBE	16	SUS_S5#	S5 (Soft OFF) – shutdown state
17	WAKE#	External system wake event	18	SUS_S3#	S3 (Suspend to RAM) – SLP
19	SUS_STAT#	Suspend status	20	PWRBTN#	Power button
21	SLP_BTN#	Sleep button	22	LID_BTN#	LID button
23	GND	Power Ground	24	GND	Power Ground
25	GND	Power Ground	26	PWGIN	Power good input
27	BATLOW#	Battery low input	28	RSTBTN#	Reset button input
29	SATA0_TX+	Serial ATA Channel 0 TX+	30	SATA1_TX+	Serial ATA Channel 1 TX+
31	SATA0_TX-	Serial ATA Channel 0 TX-	32	SATA1_TX-	Serial ATA Channel 1 TX-
33	SATA_ACT#	Serial ATA Activity	34	GND	Power Ground
35	SATA0_RX+	Serial ATA Channel 0 RX+	36	SATA1_RX+	Serial ATA Channel 1 RX+
37	SATA0_RX-	Serial ATA Channel 0 RX-	38	SATA1_RX-	Serial ATA Channel 1 RX-
39	GND	Power Ground	40	GND	Power Ground
41	BIOS_DISABLE# /BOOT_ALT#	BIOS Module disable Boot Alternative Enable	42	SDIO_CLK	SDIO Clock Output
43	SDIO_CD#	SDIO Card Detect	44	SDIO_LED	SDIO LED
45	SDIO_CMD	SDIO Command/Response	46	SDIO_WP	SDIO Write Protect
47	SDIO_PWR#	SDIO Power Enable	48	SDIO_DAT1	SDIO Data Line 1
49	SDIO_DAT0	SDIO Data Line 0	50	SDIO_DAT3	SDIO Data Line 3
51	SDIO_DAT2	SDIO Data Line 2	52	SDIO_DAT5	SDIO Data Line 5
53	SDIO_DAT4	SDIO Data Line 4	54	SDIO_DAT7	SDIO Data Line 7
55	SDIO_DAT6	SDIO Data Line 6	56	RESERVED	
57	GND	Power Ground	58	GND	Power Ground
59	HDA_SYNC	HD Audio/AC'97 Synchronization	60	SMB_CLK	SMBus Clock line
61	HDA_RST#	HD Audio/AC'97 Codec Reset	62	SMB_DAT	SMBus Data line
63	HDA_BITCLK	HD Audio/AC'97 Serial Bit Clock	64	SMB_ALERT#	SMBus Alert input
65	HDA_SDI	HD Audio/AC'97 Serial Data In	66	I2C_CLK	I2C Bus Clock
67	HDA_SDO	HD Audio/AC'97 Serial Data Out	68	I2C_DAT	I2C Bus Data
69	THRM#	Thermal Alarm active low	70	WDTRIG#	Watchdog trigger signal
71	THRMTRIP#	Thermal Trip indicates an overheating condition	72	WDOUT	Watchdog event indicator
73	GND	Power Ground	74	GND	Power Ground
75	USB_P7-	USB Port 7 Differential Pair-	76	USB_P6-	USB Port 6 Differential Pair-

Pin	Signal	Description	Pin	Signal	Description
77	USB_P7+	USB Port 7 Differential Pair+	78	USB_P6+	USB Port 6 Differential Pair+
79	USB_6_7_OC#	Over current detect input 6/7 USB	80	USB_4_5_OC#	Over current detect input 4/5 USB
81	USB_P5-	USB Port 5 Differential Pair-	82	USB_P4-	USB Port 4 Differential Pair-
83	USB_P5+	USB Port 5 Differential Pair+	84	USB_P4+	USB Port 4 Differential Pair+
85	USB_2_3_OC#	Over current detect input 2/3 USB	86	USB_0_1_OC#	Over current detect input 0/1 USB
87	USB_P3-	USB Port 3 Differential Pair-	88	USB_P2-	USB Port 2 Differential Pair-
89	USB_P3+	USB Port 3 Differential Pair+	90	USB_P2+	USB Port 2 Differential Pair+
91	USB_CC (*)	USB Client present detect pin	92	USB_ID (*)	USB ID pin
93	USB_P1-	USB Port 1 Differential Pair-	94	USB_P0-	USB Port 0 Differential Pair-
95	USB_P1+	USB Port 1 Differential Pair+	96	USB_P0+	USB Port 0 Differential Pair+
97	GND	Power Ground	98	GND	Power Ground
99	LVDS_A0+	LVDS Primary channel 0+	100	LVDS_B0+	LVDS Secondary channel 0+
101	LVDS_A0-	LVDS Primary channel 0-	102	LVDS_B0-	LVDS Secondary channel 0-
103	LVDS_A1+	LVDS Primary channel 1+	104	LVDS_B1+	LVDS Secondary channel 1+
105	LVDS_A1-	LVDS Primary channel 1-	106	LVDS_B1-	LVDS Secondary channel 1-
107	LVDS_A2+	LVDS Primary channel 2+	108	LVDS_B2+	LVDS Secondary channel 2+
109	LVDS_A2-	LVDS Primary channel 2-	110	LVDS_B2-	LVDS Secondary channel 2-
111	LVDS_PPEN	LVDS Power enable	112	LVDS_BLEN	LVDS Backlight enable
113	LVDS_A3+	LVDS Primary channel 3+	114	LVDS_B3+	LVDS Secondary channel 3+
115	LVDS_A3-	LVDS Primary channel 3-	116	LVDS_B3-	LVDS Secondary channel 3-
117	GND	Power Ground	118	GND	Power Ground
119	LVDS_A_CLK+	LVDS Primary channel CLK+	120	LVDS_B_CLK+	LVDS Secondary channel CLK+
121	LVDS_A_CLK-	LVDS Primary channel CLK-	122	LVDS_B_CLK-	LVDS Secondary channel CLK-
123	LVDS_BLT_CTRL /GP_PWM_OUT0	PWM Backlight brightness General Purpose PWM Output	124	RESERVED	
125	LVDS_DID_DAT /GP_I2C_DAT	DDC Display ID Data line General Purpose I2C Data line	126	LVDS_BLC_DAT (*)	SSC clock chip data line
127	LVDS_DID_CLK //GP_I2C_CLK	DDC Display ID Clock line General Purpose I2C Clock line	128	LVDS_BLC_CLK (*)	SSC clock chip clock line
129	CAN0_TX (*)	CAN TX Output for CAN Bus Channel 0	130	CAN0_RX (*)	CAN RX Input for CAN Bus Channel 0
131	DP_LANE3+	DisplayPort differential pair line lane 3	132	SDVO_INT+ (*)	SDVO Interrupt line+
133	DP_LANE3-	DisplayPort differential pair line lane 3	134	SDVO_INT- (*)	SDVO Interrupt line-
135	GND	Power Ground	136	GND	Power Ground
137	DP_LANE1+	DisplayPort differential pair line lane 1	138	DP_AUX+	DisplayPort auxiliary channel
139	DP_LANE1-	DisplayPort differential pair line lane 1	140	DP_AUX-	DisplayPort auxiliary channel
141	GND	Power Ground	142	GND	Power Ground
143	DP_LANE2+	DisplayPort differential pair line lane 2	144	SDVO_TVCLKIN+ (*)	SDVO TV-Out line+
145	DP_LANE2-	DisplayPort differential pair line lane 2	146	SDVO_TVCLKIN- (*)	SDVO TV-Out line-
147	GND	Power Ground	148	GND	Power Ground
149	DP_LANE0+	DisplayPort differential pair line lane 0	150	HDMI_CTRL_DAT	DDC based control signal (data) for HDMI/DVI device.
151	DP_LANE0-	DisplayPort differential pair line lane 0	152	HDMI_CTRL_CLK	DDC based control signal (clock) for HDMI/DVI device.

Pin	Signal	Description	Pin	Signal	Description
153	HDMI_HPD#	Hot plug detection for HDMI	154	DP_HPD#	Hot plug detection for Display port
155	PCIE_CLK_REF+	PCI Express Reference Clock+	156	PCIE_WAKE#	PCI Express Wake event
157	PCIE_CLK_REF-	PCI Express Reference Clock-	158	PCIE_RST#	Reset Signal for external devices
159	GND	Power Ground	160	GND	Power Ground
161	PCIE3_TX+	PCI Express Channel 3 Output+	162	PCIE3_RX+	PCI Express Channel 3 Input+
163	PCIE3_TX-	PCI Express Channel 3 Output-	164	PCIE3_RX-	PCI Express Channel 3 Input-
165	GND	Power Ground	166	GND	Power Ground
167	PCIE2_TX+	PCI Express Channel 2 Output+	168	PCIE2_RX+	PCI Express Channel 2 Input+
169	PCIE2_TX-	PCI Express Channel 2 Output-	170	PCIE2_RX-	PCI Express Channel 2 Input-
171	EXCD0_PERST#	Express Card slot#0 reset	172	EXCD1_PERST#	Express Card slot#1 reset
173	PCIE1_TX+	PCI Express Channel 1 Output+	174	PCIE1_RX+	PCI Express Channel 1 Input+
175	PCIE1_TX-	PCI Express Channel 1 Output-	176	PCIE1_RX-	PCI Express Channel 1 Input-
177	EXCD0_CPPE#	Express Card slot#0 Capable/Req	178	EXCD1_CPPE#	Express Card slot#0 Capable/Req
179	PCIE0_TX+	PCI Express Channel 0 Output+	180	PCIE0_RX+	PCI Express Channel 0 Input+
181	PCIE0_TX-	PCI Express Channel 0 Output-	182	PCIE0_RX-	PCI Express Channel 0 Input-
183	GND	Power Ground	184	GND	Power Ground
185	LPC_AD0	LPC Interface Address/Data 0	186	LPC_AD1	LPC Interface Address/Data 1
187	LPC_AD2	LPC Interface Address/Data 0	188	LPC_AD3	LPC Interface Address/Data 3
189	LPC_CLK	LPC Interface Clock	190	LPC_FRAME#	LPC frame indicator
191	SERIRQ	Serialized interrupt	192	LPC_LDRQ#	LPC DMA request
193	VCC_RTC	3V backup cell input	194	SPKR /GP_PWM_OUT2	Output for audio enunciator General Purpose PWM Output
195	FAN_TACHOIN /GP_TIMER_IN	Fan tachometer input General Purpose Timer In	196	FAN_PWMOUT /GP_PWM_OUT1	Fan speed control (PWM) General Purpose PWM Output
197	GND	Power Ground	198	GND	Power Ground
199	SPI_MOSI	SPI Master serial output/Slave serial input	200	SPI_CS0#	SPI Chip Select 0 Output
201	SPI_MISO	SPI Master serial input/Slave serial output signal	202	SPI_CS1#	SPI Chip Select 1 Output
203	SPI_SCK	SPI Clock Output	204	MFG_NC4	Do not connect on carrier board
205	VCC_5V_SB	+5VDC,Standby ±5%	206	VCC_5V_SB	+5VDC Standby ±5%
207	MFG_NC0	Do not connect on carrier board	208	MFG_NC2	Do not connect on carrier board
209	MFG_NC1	Do not connect on carrier board	210	MFG_NC3	Do not connect on carrier board
211	VCC	Power supply +5VDC ±5%	212	VCC	Power supply +5VDC ±5%
213	VCC	Power supply +5VDC ±5%	214	VCC	Power supply +5VDC ±5%
215	VCC	Power supply +5VDC ±5%	216	VCC	Power supply +5VDC ±5%
217	VCC	Power supply +5VDC ±5%	218	VCC	Power supply +5VDC ±5%
219	VCC	Power supply +5VDC ±5%	220	VCC	Power supply +5VDC ±5%
221	VCC	Power supply +5VDC ±5%	222	VCC	Power supply +5VDC ±5%
223	VCC	Power supply +5VDC ±5%	224	VCC	Power supply +5VDC ±5%
225	VCC	Power supply +5VDC ±5%	226	VCC	Power supply +5VDC ±5%
227	VCC	Power supply +5VDC ±5%	228	VCC	Power supply +5VDC ±5%
229	VCC	Power supply +5VDC ±5%	230	VCC	Power supply +5VDC ±5%

📓 **Note**

The signals in the previous table marked with an asterisk symbol (*) are not supported on the conga-QAF.

Table 4   PCI Express Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE0_RX+ PCIE0_RX-	180 182	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE0_TX+ PCIE0_TX-	179 181	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE1_RX+ PCIE1_RX-	174 176	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0.
PCIE1_TX+ PCIE1_TX-	173 175	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE2_RX+ PCIE2_RX-	168 170	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE2_TX+ PCIE2_TX-	167 169	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE3_RX+ PCIE3_RX-	162 164	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0.
PCIE3_TX+ PCIE3_TX-	161 163	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCI Express Reference Clock for Lanes 0 to 3.	O PCIE		
PCIE_WAKE#	156	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I 3.3VSB	PU 10k 3.3VSB	
PCIE_RST#	158	Reset Signal for external devices.	O 3.3V		

Table 5   ExpressCard Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE#	177	ExpressCard slot #0 capable card request.	I 3.3VSB	PU 10k 3.3VSB	
EXCD0_PERST#	171	ExpressCard slot #0 reset.	O 3.3V		
EXCD1_CPPE#	178	ExpressCard slot #1 capable card request.	I 3.3VSB	PU 10k 3.3VSB	
EXCD1_PERST#	172	ExpressCard slot #1 reset.	O 3.3V		

Table 6   Ethernet Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GBE_MDI0+ GBE_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI1+ GBE_MDI1-	11 9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI2+ GBE_MDI2-	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI3+ GBE_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_CTREF	15	Reference voltage for carrier board Ethernet magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		conga-QAF GbE uses 1.9V center tab voltage.
GBE_LINK#	13	Ethernet controller 0 link indicator, active low.	O 3.3VSB PP		see note below
GBE_LINK100#	7	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB PP		
GBE_LINK1000#	8	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB PP		
GBE_ACT#	14	Ethernet controller 0 activity indicator, active low.	O 3.3VSB		see note below, pulled to 3.3VSB

Note

The GbE Controller used on the conga-QAF supports only three LEDs outputs:

GBE_LINK100#   100Mb/s link indicator

GBE_LINK1000#   1000Mb/s link indicator

GBE_LINK#/ACT   Combined all speed link with link activity that is connected to GBE_LINK# pin on Qseven connector.

The conga-QAF can drive directly GbE LEDs with up to 10mA.

Table 7   SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA_ACT#	33	Serial ATA Led. Open collector output pin driven during SATA command activity.	O 3.3V		up to 10mA

Table 8   USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_P0+ USB_P0-	96 94	Universal Serial Bus Port 0 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P1+ USB_P1-	95 93	Universal Serial Bus Port 1 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P2+ USB_P2-	90 88	Universal Serial Bus Port 2 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P3+ USB_P3-	89 87	Universal Serial Bus Port 3 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P4+ USB_P4-	84 82	Universal Serial Bus Port 4 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P5+ USB_P5-	83 81	Universal Serial Bus Port 5 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P6+ USB_P6-	78 76	Universal Serial Bus Port 6 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P7+ USB_P7-	77 75	Universal Serial Bus Port 7 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	86	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	I 3.3VSB	PU 10k 3.3VSB	
USB_2_3_OC#	85	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	I 3.3VSB	PU 10k 3.3VSB	
USB_4_5_OC#	80	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	I 3.3VSB	PU 10k 3.3VSB	
USB_6_7_OC#	79	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	I 3.3VSB	PU 10k 3.3VSB	

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_ID	92	USB ID pin. Configures the mode of the USB Port 1. If the signal is detected as being 'high active' the BIOS will automatically configure USB Port 1 as USB Client and enable USB Client support. This signal should be driven as OC signal by external circuitry.	I 3.3VSB		Not connected
USB_CC#	91	USB Client Connect pin. If USB Port 1 is configured for client mode then an externally connected USB host should set this signal to high-active in order to properly make the connection with the module's internal USB client controller. If the external USB host is disconnected, this signal should be set to low-active in order to inform the USB client controller that the external host has been disconnected. A level shifter/protection circuitry should be implemented on the carrier board for this signal.	I 3.3V		Not connected

Table 9   SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	43	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I/O 3.3V	PU 50k 3.3V	
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	O 3.3V		
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O 3.3V OD/PP	PU 50k 3.3V	
SDIO_LED	44	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	O 3.3V		
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I/O 3.3V	PU 10k 3.3V	
SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	OD 3.3V	PU 10k 3.3V	
SDIO_DAT0 SDIO_DAT1 SDIO_DAT2 SDIO_DAT3 SDIO_DAT4 SDIO_DAT5 SDIO_DAT6 SDIO_DAT7	49 48 51 50 53 52 55 54	SDIO Data lines. These signals operate in push-pull mode.	I/O 3.3V PP	PU 50k 3.3V	

Table 10   HDA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST#	61	HD Audio Codec Reset.	O 3.3VSB		
HDA_SYNC	59	HD Audio Serial Bus Synchronization.	O 3.3VSB		
HDA_BITCLK	63	HD Audio 24 MHz Serial Bit Clock from Codec.	O 3.3VSB		
HDA_SDO	67	HD Audio Serial Data Output to Codec.	O 3.3VSB		
HDA_SDI	65	HD Audio Serial Data Input from Codec.	I 3.3VSB	PD 50k	

Table 11   LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_PPEN	111	Controls panel power enable.	O 3.3V		
LVDS_BLEN	112	Controls panel Backlight enable.	O 3.3V		
LVDS_BLT_CTRL /GP_PWM_OUT0	123	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
LVDS_A0+ LVDS_A0-	99 101	LVDS primary channel differential pair 0.	O LVDS		
LVDS_A1+ LVDS_A1-	103 105	LVDS primary channel differential pair 1.	O LVDS		
LVDS_A2+ LVDS_A2-	107 109	LVDS primary channel differential pair 2.	O LVDS		
LVDS_A3+ LVDS_A3-	113 115	LVDS primary channel differential pair 3.	O LVDS		
LVDS_A_CLK+ LVDS_A_CLK-	119 121	LVDS primary channel differential pair clock lines.	O LVDS		
LVDS_B0+ LVDS_B0-	100 102	LVDS secondary channel differential pair 0.	O LVDS		
LVDS_B1+ LVDS_B1-	104 106	LVDS secondary channel differential pair 1.	O LVDS		
LVDS_B2+ LVDS_B2-	108 110	LVDS secondary channel differential pair 2.	O LVDS		
LVDS_B3+ LVDS_B3-	114 116	LVDS secondary channel differential pair 3.	O LVDS		
LVDS_B_CLK+ LVDS_B_CLK-	120 122	LVDS secondary channel differential pair clock lines.	O LVDS		

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_DID_CLK /GP_I2C_CLK	127	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus clock line.	I/O 3.3V OD	PU 2.2k 3.3V	
LVDS_DID_DAT /GP_I2C_DAT	125	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus data line.	I/O 3.3V OD	PU 2.2k 3.3V	
LVDS_BLC_CLK	128	Control clock signal for external SSC clock chip.	I/O 3.3V OD	PU 4.7k 3.3V	Not supported
LVDS_BLC_DAT	126	Control data signal for external SSC clock chip.	I/O 3.3V OD	PU 4.7k 3.3V	Not supported

Table 12   SDVO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDVO_BCLK+ SDVO_BCLK-	131 133	SDVO differential pair clock lines.	O PCIE		Not Supported
SDVO_INT+ SDVO_INT-	132 134	SDVO differential pair interrupt input lines.	I PCIE		Not Supported
SDVO_GREEN+ SDVO_GREEN-	137 139	SDVO differential pair green data lines.	O PCIE		Not Supported
SDVO_BLUE+ SDVO_BLUE-	143 145	SDVO differential pair blue data lines.	O PCIE		Not Supported
SDVO_RED+ SDVO_RED-	149 151	SDVO differential pair red data lines.	O PCIE		Not Supported
SDVO_FLDSTALL+ SDVO_FLDSTALL-	138 140	SDVO differential pair field stall lines.	I PCIE		Not Supported
SDVO_TVCLKIN+ SDVO_TVCLKIN-	144 146	SDVO differential pair TV-Out synchronization clock lines.	I PCIE		Not Supported
SDVO_CTRL_CLK	152	I²C based control signal (clock) for SDVO device. *Note: If the control bus from the SDVO device has a different signaling voltage, then a level shifting device will be required on the carrier board to properly translate the voltage level for this signal.*	I/O 3.3V OD	PU 100k 3.3V	Not Supported
SDVO_CTRL_DAT	150	I²C based control signal (data) for SDVO device. *Note: If the control bus from the SDVO device has a different signaling voltage, then a level shifting device will be required on the carrier board to properly translate the voltage level for this signal.*	I/O 3.3V OD	PU 100k 3.3V	Not Supported

Note

The SDVO interface signals are shared with the signals for the DisplayPort interface and/or the TMDS interface. The conga-QAF does not support the SDVO interface.

Table 13   DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP_LANE3+ DP_LANE3-	131 133	DisplayPort differential pair lines lane 3.	O PCIE		Shared with SDVO_BCLK+ and SDVO_BCLK-
DP_LANE2+ DP_LANE2-	143 145	DisplayPort differential pair lines lane 2.	O PCIE		Shared with SDVO_BLUE+ and SDVO_BLUE-
DP_LANE1+ DP_LANE1-	137 139	DisplayPort differential pair lines lane 1.	O PCIE		Shared with SDVO_GREEN+ and SDVO_GREEN-
DP_LANE0+ DP_LANE0-	149 151	DisplayPort differential pair lines lane 0.	O PCIE		Shared with SDVO_RED+ and SDVO_RED-
DP_AUX+ DP_AUX-	138 140	Auxiliary channel used for link management and device control. Differential pair lines.	I/O PCIE		Shared with SDVO_FLDSTALL+ and SDVO_FLDSTALL-
DP_HPD#	154	Hot plug active low detection signal that serves as an interrupt request.	I 3.3V	PU 22k 3.3V	Should by driven by OD output. ADD2-N adapter card with 0.8V (PCIe) logic level HPD# is supported.

Note

The DisplayPort interface signals are shared with the signals for the SDVO interface and/or the TMDS interface. SDVO interface is not supported on the conga-QAF.

Table 14   HDMI/DVI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS_CLK+ TMDS_CLK-	131 133	TMDS differential pair clock lines.	O TMDS		Passive level shifter shall use PD 499R.
TMDS_LANE0+ TMDS_LANE0-	143 145	TMDS differential pair lines lane 0.	O TMDS		Passive level shifter shall use PD 499R.
TMDS_LANE1+ TMDS_LANE1-	137 139	TMDS differential pair lines lane 1.	O TMDS		Passive level shifter shall use PD 499R.
TMDS_LANE2+ TMDS_LANE2-	149 151	TMDS differential pair lines lane 2.	O TMDS		Passive level shifter shall use PD 499R.
HDMI_CTRL_CLK	152	DDC based control signal (clock) for HDMI/DVI device.	I/O 3.3V OD		Shared with SDVO_CTRL_CLK PU 10k to 3.3V shall by placed on carrier board between Qseven connector and level shifter FET, PU 2.2k to 5V shall by placed between level shifter FET and HDMI/DVI connector.
HDMI_CTRL_DAT	150	DDC based control signal (data) for HDMI device.	I/O 3.3V OD		Shared with SDVO_CTRL_DAT PU 10k to 3.3V shall by placed on carrier board between Qseven connector and level shifter FET, PU 2.2k to 5V shall by placed between level shifter FET and HDMI/DVI connector.
HDMI_HPD#	153	Hot plug active low detection signal that serves as an interrupt request.	I 3.3V		Should by driven by OD output. ADD2-N adapter card with 0.8V (PCIe) logic level HPD# is supported.

> **Note**
>
> *The TMDS interface signals are shared with the signals for the SDVO interface and/or the DisplayPort interface. SDVO interface is not supported on the conga-QAF.*

Table 15   LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	185 186 187 188	Multiplexed Command, Address and Data.	I/O 3.3V	PU 15k 3.3V	
LPC_FRAME#	190	LPC frame indicates the start of a new cycle or the termination of a broken cycle.	O 3.3V		
LPC_LDRQ#	192	LPC DMA request.	I 3.3V	PU 15k	
LPC_CLK	189	LPC clock.	O 3.3V		
SERIRQ	191	Serialized Interrupt.	I/O 3.3V	PU 8.2k 3.3V	

Table 16   SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_MOSI	199	Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device.	O 3.3VSB		
SPI_MISO	201	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module.	I 3.3VSB		
SPI_SCK	203	SPI clock output.	O 3.3VSB		
SPI_CS0#	200	SPI chip select 0 output.	O 3.3VSB		
SPI_CS1#	202	SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.	O 3.3VSB		

Table 17   CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN0_TX	129	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	O 3.3V		Not connected
CAN0_RX	130	RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	I 3.3V		Not connected

Table 18   Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	211-230	Power Supply +5VDC ±5%.	P		
VCC_5V_SB	205-206	Standby Power Supply +5VDC ±5%.	P		
VCC_RTC	193	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.5 - 3.3 V).	P		
GND	1, 2, 23-25, 34, 39-40, 57-58, 73-74, 97-98, 117-118, 135-136, 141-142, 147-148, 159-160, 165-166, 183-184, 197-198	Power Ground.	P		

Table 19   Power Control Signal Descriptions

Signal	Pin #	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	26	High active input for the Qseven® module indicates that power from the power supply is ready.	I 5V	PU 50k 3.3V	Should be driven by OD output.
PWRBTN#	20	Power Button: Low active power button input. This signal is triggered on the falling edge.	I 3.3VSB	PU 10k 3.3VSB	

Table 20   Power Management Signal Descriptions

Signal	Pin #	Description of Power Management signals	I/O	PU/PD	Comment
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module.	I 3.3V	PU 10k 3.3V	
BATLOW#	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	I 3.3VSB	PU 10k 3.3VSB	
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	I 3.3VSB	PU 10k 3.3VSB	
SUS_STAT#	19	Suspend Status: indicates that the system will be entering a low power state soon.	O 3.3VSB		
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	O 3.3VSB		
SUS_S5#	16	S5 State: This signal indicates S4 or S5 (Soft Off) state.	O 3.3VSB		
SLP_BTN#	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	I 3.3VSB	PU 10k 3.3VSB	
LID_BTN#	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again.	I 3.3VSB	PU 10k 3.3VSB	

Table 21   Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse.	I 3.3V	PU 10k 3.3V	
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	O 3.3V		
I2C_CLK	66	Clock line of I²C bus.	I/O 3.3V OD	PU 2.2k 3.3V	
I2C_DAT	68	Data line of I²C bus.	I/O 3.3V OD	PU 2.2k 3.3V	
SMB_CLK	60	Clock line of System Management Bus.	I/O 3.3VSB OD	PU 2.2k 3.3VSB	
SMB_DAT	62	Data line of System Management Bus.	I/O 3.3VSB OD	PU 2.2k 3.3VSB	
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	I/O 3.3VSB OD	PU 10k 3.3V	
SPKR /GP_PWM_OUT2	194	Primary functionality is output for audio enunciator, the "speaker" in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
BIOS_DISABLE# /BOOT_ALT#	41	Module BIOS disable input signal. Pull low to disable module's onboard BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a bootloader.	I 3.3VSB	PU 10k 3.3VSB	

Table 22   Manufacturing Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
MFG_NC0	207	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TCK signal for boundary scan purposes during production or as a vendor specific control signal. When used as a vendor specific control signal the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC1	209	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDO signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_TX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC2	208	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDI signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_RX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC3	210	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TMS signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific BOOT signal for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC4	204	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TRST# signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 (JTAG / UART). When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes.	NA	NA	
RSVD	124	Do not connect.	NA	NA	

Note

The MFG_NC0..4 pins are reserved for manufacturing and debugging purposes. It's recommended to route the signals to a connector on the carrier board.

The carrier board must not drive the MFG_NC-pins or have pull-up or pull-down resistors implemented for these signals. MFG_NC0...4 are defined to have a voltage level of 3.3V. It must be ensured that the carrier board has the correct voltage levels for JTAG/UART signals originating from the module. For this reason, a level shifting device may be required on the carrier board to guarantee that these voltage levels are correct in order to prevent damage to the module.

More information about implementing a carrier board multiplexer can be found in the Qsever® Design Guide.

Table 23   Thermal Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	69	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	I 3.3V	PU 2.2k 3.3V	
THRMTRIP#	71	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off).	O 3.3VSB		

Table 24   Fan Control Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT /GP_PWM_OUT1	196	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V OC	PU 10k 3.3V	
FAN_TACHOIN /GP_TIMER_IN	195	Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input.	I 3.3V	PU 10k 3.3V	

8   System Resources

8.1   I/O Address Assignment

The I/O address assignment of the conga-QAF module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed in the table below.

Note

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

8.1.1   LPC Bus

On the conga-QAF the PCI Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Bus not the LPC Bus. Only specified I/O ranges are forwarded to the LPC Bus. In the congatec Embedded BIOS the following I/O address ranges are sent to the LPC Bus:

> 2Eh – 2Fh
> 4Eh – 4Fh
> 60h, 64h
> 2E8h – 2EFh
> 2F8h – 2FFh
> 378h – 37Fh
> 3E8h – 3EFh
> 3F8h – 3FFh
> 778h – 77Fh
> A00h – BFFh

Parts of these ranges are not available if a Super I/O is used on the carrier board. If a Super I/O is not implemented on the carrier board then these ranges are available for customer use. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

8.2   Interrupt Request (IRQ) Lines

Table 25   IRQ Lines in PIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		IRQ3 via SERIRQ
4	Yes		IRQ4 via SERIRQ
5	Yes		IRQ5 via SERIRQ
6	Yes		IRQ6 via SERIRQ
7	Yes		IRQ7 via SERIRQ
8	No	Real-time Clock	Not applicable
9	No	SCI	Not applicable
10	Yes		IRQ10 via SERIRQ
11	Yes		IRQ11 via SERIRQ
12	Yes		IRQ12 via SERIRQ
13	No	Math processor	Not applicable
14	Note	IDE Controller 0 (IDE0) / Generic	IRQ14 via SERIRQ
15	Note	IDE Controller 1 (IDE1) / Generic	IRQ15 via SERIRQ

Note

If the SATA interface mode configuration in BIOS setup is NOT set to legacy IDE mode, IRQ14 and 15 are free for LPC bus.

Table 26   IRQ Lines in APIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin / Function
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		IRQ3 via SERIRQ
4	Yes		IRQ4 via SERIRQ
5	Yes		IRQ5 via SERIRQ
6	Yes		IRQ6 via SERIRQ
7	Yes		IRQ7 via SERIRQ
8	No	Real-time Clock	Not applicable
9	No	SCI	Not applicable
10	Yes		IRQ10 via SERIRQ
11	Yes		IRQ11 via SERIRQ
12	Yes		IRQ12 via SERIRQ
13	No	Math processor	Not applicable
14	Note 1	IDE Controller 0 (IDE0) / Generic	IRQ14 via SERIRQ
15	Note 1	IDE Controller 1 (IDE1) / Generic	IRQ15 via SERIRQ
16	No		PIRQA, PCI Express Root Port 0/4, onboard Gigabit LAN Controller, PCI Express Port 0 (see Note 2), Main High Definition Audio Controller
17	No		PIRQB, PCI Express Root Port 1, PCI Express Port 1 (see Note 2), EHCI Host Controller 0, EHCI Host Controller 1
18	No		PIRQC, PCI Express Root Port 2, PCI Express Port 2 (see Note 2), OHCI Host Controller 0, OHCI Host Controller 1, Integrated Graphics Controller
19	No		PIRQD, PCI Express Root Port 3, PCI Express Port 3 (see Note 2), Chipset IDE Controller 0 (SATA Ports), HDMI / DisplayPort HDA Controller (for HDMI/DisplayPort integrated audio only)
20	Yes		PIRQE
21	Yes		PIRQF
22	Yes		PIRQG
23	Yes		PIRQH

In APIC mode, the PCI bus interrupt lines are connected with IRQ 20, 21, 22 and 23.

Note

1. *If the SATA interface mode configuration in BIOS setup is NOT set to legacy IDE mode IRQ14 and 15 are free for LPC bus.*

2. *Interrupt used if a single function PCI Express device is connected to the respective PCI Express port.*

8.3   PCI Configuration Space Map

Table 27   PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	01h	00h	Internal	Integrated Graphics Controller (VGA)
00h	01h	01h	Internal	HDMI / DisplayPort HDA Controller (for HDMI/DisplayPort integrated audio only)
00h (see Note 1)	04h	00h	Internal	PCI Express Root Port 0
00h (see Note 1)	05h	00h	Internal	PCI Express Root Port 1
00h (see Note 1)	06h	00h	Internal	PCI Express Root Port 2
00h (see Note 1)	07h	00h	Internal	PCI Express Root Port 3
00h	11h	00h	Internal	Chipset IDE Controller 0 (SATA Ports)
00h	12h	00h	Internal	OHCI Host Controller 0
00h	12h	02h	Internal	EHCI Host Controller 0
00h	13h	00h	Internal	OHCI Host Controller 1
00h	13h	02h	Internal	EHCI Host Controller 1
00h	14h	00h	N.A.	SMBus Host Controller
00h	14h	02h	Internal	High Definition Audio Controller
00h	14h	03h	N.A.	PCI to LPC Bridge
00h	14h	04h	N.A.	PCI to PCI Bridge
00h	15h	00h	Internal	PCI Express Root Port for on-module Gigabit LAN Controller
00h	18h	00h	N.A.	Chipset Configuration Registers
00h	18h	01h	N.A.	Chipset Configuration Registers
00h	18h	02h	N.A.	Chipset Configuration Registers
00h	18h	03h	N.A.	Chipset Configuration Registers
00h	18h	04h	N.A.	Chipset Configuration Registers
00h	18h	05h	N.A.	Chipset Configuration Registers
00h	18h	06h	N.A.	Chipset Configuration Registers
00h	18h	07h	N.A.	Chipset Configuration Registers
01h (see Note 2)	00h	00h	Internal	PCI Express Port 0
02h (see Note 2)	00h	00h	Internal	PCI Express Port 1
03h (see Note 2)	00h	00h	Internal	PCI Express Port 2
04h (see Note 2)	00h	00h	Internal	PCI Express Port 3
05h (see Note 2)	00h	00h	Internal	Onboard Gigabit LAN Controller

Note

1. *The PCI Express root ports are only visible if the PCI Express port is set to "Enabled" in the BIOS setup program and a device is attached to the corresponding PCI Express port on the carrier board.*

2. *The above table represents a case when a single function PCIe device is connected to all possible slots on the carrier board. The given bus numbers will change based on the actual configuration of the hardware .*

8.4   PCI Interrupt Routing Map

Table 28   PCI Interrupt Routing Map

PIRQ	APIC Mode IRQ	VGA	HDA (HDMI / DP)	OHCI 0	OHCI 1	EHCI 0	EHCI 1	SMBus	IDE0 (SATA)	HDA (Main)
A	16									x
B	17					x	x			
C	18	x		x	x					
D	19		x						x	
E	20									
F	21									
G	22									
H	23									

PCI Interrupt Routing Map (continued)

PIRQ	PCI-EX Root Port 0	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Root Port 3	PCI-EX Root Port 4	PCI-EX Port 0	PCI-EX Port 1	PCI-EX Port 2	PCI-EX Port 3	LAN
A	x				x	x [1]	x [4]	x [3]	x [2]	x
B		x				x [2]	x [1]	x [4]	x [3]	
C			x			x [3]	x [2]	x [1]	x [4]	
D				x		x [4]	x [3]	x [2]	x [1]	
E										
F										
G										
H										

Note

[1] *Interrupt used by single function PCI Express devices (INTA).*

[2] *Interrupt used by multifunction PCI Express devices (INTB).*

[3] *Interrupt used by multifunction PCI Express devices (INTC).*

[4] *Interrupt used by multifunction PCI Express devices (INTD).*

8.5   I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

8.6   SM Bus

System Management (SM) bus signals are connected to the AMD Controller Hub A55E and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

9   BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

9.1   Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <F2> key during POST.

9.1.1   Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used, a selection will be displayed immediately after POST allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

9.2   Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

Main	Advanced	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold print indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

9.3   Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
BIOS Information		
Main BIOS Version	no option	Displays the main BOIS version.
OEM BIOS Version	no option	Displays the additional OEM BIOS version.
Build Date	no option	Displays the date the BIOS was built.
Board Information		
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
Running Time	no option	Displays the time the board is running [in hours max. 65535].
Memory Information		
Total Memory	no option	Displays amount of installed memory.
Memory Clock	no option	Displays current memory clock.
CPU Information	no option	Displays CPU type and feature information.
System Date	Day of the week, month/day/year	Specifies the current system date. *Note: The date is in month/day/year format.*
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24 hour format.*

9.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Boot	Security	Save & Exit
	Graphics Configuration			
	Watchdog Configuration			
	PCI & PCI Express Configuration			
	ACPI Configuration			
	RTC Wake Settings			
	CPU Configuration			
	Chipset Configuration			
	Hardware Health Monitoring			
	SATA Configuration			
	USB Configuration			
	Super I/O Configuration			
	Serial Port Console Redirection			

9.4.1 Graphics Configuration Submenu

Feature	Options	Description
Primary Graphics Device	IGD **PCI/PCIe**	Select primary graphics adapter to be used during boot up. IGD: Internal Graphics Device PCI/PCIe: Try to use external standard PCI Express Graphics Device. If not present, IGD is used.
Integrated Graphics Device	**Auto Configuration** Disabled Manual Configuration	Deactivate IGD or select frame buffer configuration mode. In auto mode, the frame buffer size will be defined based on the amount of physical memory present.
IGD Framebuffer Size	32M 64M 128M **256M** 512M	Only visible if IGD is set to manual configuration. Set fixed graphics frame buffer size for IGD. The graphics driver may allocate additional memory.
Display Channel 0 Output	**LVDS** Disabled	Define output mode and connection of the integrated digital display channel 0.
Display Channel 1 Output	DisplayPort B **HDMI B** Disabled	Define output mode and connection of the integrated digital display channel 1.

Feature	Options	Description
IGD Boot Display Device	**Auto** Display Channel 0 Display Channel 1 Display Channel 0 + 1	Select the IGD display device(s) used for boot up.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the LVDS flat panel output. Only if no external EDID data set can be found, the data set selected under 'Local Flat Panel Type' will be used as fallback data set.
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. *Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.*
Backlight Inverter Type	**None** PWM I2C	Select the type of backlight inverter used. PWM = Use IGD PWM signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.
PWM Inverter Frequency (Hz)	**200**-40000	Only visible if Backlight Inverter Type is set to PWM. Set the PWM inverter frequency in Hertz.
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100%**	Actual backlight value in percent of the maximum setting.
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Setting	**No** Yes	Allow to invert backlight control values if required for the actual backlight hardware controller.

9.4.2 Watchdog Configuration Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One time Trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to '*One time Trigger'* the watchdog will be disabled after the first trigger. If set to *'Single Event'*, every stage will be executed only once, then the watchdog will be disabled. If set to *'Repeated Event'* the last stage will be executed repeatedly until a reset occurs.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	NMI ACPI Event **Reset** Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about *'ACPI Event'* see note below.
Event 2	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached. For more information about *'ACPI Event'* see note below.
Event 3	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached. For more information about *'ACPI Event'* see note below.

Feature	Options	Description
Timeout 1	0.5sec 1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

> **Note**
>
> In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason, the congatec BIOS will do one of the following:
>
> For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.
>
> For Restart: An ACPI fatal error is reported to the OS.

9.4.3   PCI &PCI Express Configuration Submenu

Feature	Options	Description
PCI ROM Priority	Legacy ROM **EFI Compatible ROM**	Specify which PCI option ROM to launch in case multiple option ROMs (legacy and EFI compatible) are present.
Launch PXE Option ROM	**Disabled** Enabled	Enable or disable start of PXE option ROMs for external legacy network devices.
Launch Storage Option ROM	Disabled **Enabled**	Enable or disable start of option ROMs for legacy mass storage devices.
PCI Settings		
PCI Latency Timer	**32**, 64, 96, 128, 160, 192, 224, 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
VGA Palette Snoop	**Disabled** Enabled	Enable or disable VGA palette registers snooping.

Feature	Options	Description
PERR# Generation	**Disabled** Enabled	Enable or disable PCI device SERR# generation.
SERR# Generation	**Disabled** Enabled	Enable or disable PCI device SERR# generation.
►PIRQ Routing	submenu	Opens the PIRQ routing submenu.
PCI Express Device & Link Settings		
Relaxed Ordering	**Disabled** Enabled	Enable or disable PCI Express device relaxed ordering.
Extended Tag	**Disabled** Enabled	If enabled a device may use an 8-bit tag filed as a requester.
No Snoop	Disabled **Enabled**	Enable or disable PCI Express device 'No Snoop' option.
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum payload of PCI Express devices or allow system BIOS to select the value.
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum read request size of PCI Express devices or allow system BIOS to select the value.
Extended Synch	**Disabled** Enabled	If enabled, the generation of extended PCI Express synchronization patterns is allowed.

9.4.3.1 PIRQ Routing Submenu

Feature	Options	Description
PIRQA	**Auto** IRQ3 IRQ4 IRQ6 IRQ7 IRQ10 IRQ11 IRQ14 IRQ15	Set interrupt for selected PIRQ. Refer to the module's resource list of devices connected to the respective PIRQ. *Note: These settings will only be effective while operating in PIC (non IOAPIC) interrupt mode.*
PIRQB	See above	See above
PIRQC	See above	See above
PIRQD	See above	See above
PIRQE	See above	See above
PIRQF	See above	See above
PIRQG	See above	See above
PIRQH	See above	See above

9.4.4 ACPI Configuration Submenu

Feature	Options	Description
Hibernation Support	Disabled **Enabled**	Enable or disable system ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system suspend.
S3 Video Repost	Disabled **Enabled**	Enable or disable video BIOS re-post on S3 resume. Required by some operating systems.
USB Device Wakeup From S3 or S4	Disabled **Enabled**	Enable or disable USB device wakeup support from S3 or S4. Additional operating systems may be required as well.
Active Trip Point	**Disabled,** 20, 30, 40, 50, 60, 70, 80, 90, 95°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Trip Point	**Disabled**, 60, 70, 80, 90, 95°C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.
LID Button Support	**Disabled** Enabled	Activate ACPI LID button support.
Sleep Button Support	**Disabled** Enabled	Activate ACPI sleep button support.

9.4.5   RTC Wake Settings Submenu

Feature	Options	Description
Wake System At Fixed Time	**Disabled** Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour		Specify wake up hour.
Wake up minute		Specify wake up minute.
Wake up second		Specify wake up second.

9.4.6   CPU Configuration Submenu

Feature	Options	Description
Limit CPUID Maximum	**Disabled** Enabled	When enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When disabled, the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
AMD PowerNow! Support	Disabled **Enabled**	Enable or disable support for AMD PowerNow! Technology. Allows operating systems to control CPU performance states.
Maximum OS P-State	**P-State 0** P-State 1 P-State 2 P-State 3 P-State 4	Select the maximum CPU performance state the operating system should support. Higher numbers mean lower performance. P-state 0 is the highest performance state.
Maximum Power Up P-State	**P-State 0** P-State 1 P-State 2 P-State 3 P-State 4	Select the maximum CPU performance state to be set at power up. Higher numbers mean lower performance. P-state 0 is the highest performance state.
NX Mode	Disabled **Enabled**	Enable or disable the 'no-execute' page protection function.
Virtualization Technology	Disabled **Enabled**	When enabled, a Virtual Machine Manager (VMM) can utilize the integrated hardware virtualization support.
C6 Support	**Disabled** Enabled	Enable or disable CPU C6 low power state support.
Core Performance Boost	**Auto** Disabled	Controls usage of boosted CPU P-states, i.e. P-states above the standard CPU P-state limit. Availability of boosted P-states depends on CPU type and revision, actual usage on total CPU/GPU power consumption.

9.4.7 Chipset Configuration Submenu

Feature	Options	Description
Memory Bank Interleaving	**Disabled** Enabled	Enable or disable memory bank interleaving.
Memory Bus Clock	**Auto** 400MHz (DDR3-800) 533MHz (DDR3-1066)	Select or limit memory frequency.
HDA Controller	Auto Disabled **Enabled**	Control activation of the High Definition Audio controller.
HDMI/DP Audio Support	Disabled **Enabled**	Enable or disable HDMI/DisplayPort integrated audio support.
Onboard LAN	Disabled **Enabled**	Enable or disable the onboard Ethernet controller.
Launch Onboard LAN PXE ROM	**Disabled** Enabled	Enable or disable PXE option ROM execution of the onboard ethernet controller.
SD Card Controller	Disabled **Enabled**	Enable or disable the onboard USB to SD card controller.
UMI (NB to SB) PCIE Gen2 Support	Disabled Enabled	Enable or disable PCIExpress generation 2 link speed for the UMI chipset interface.
PCI Express Port 0-3 Configuration	1 x4 Port 2 x2 Ports 1 x2 Port + 2 x1 Ports **4 x1 Ports**	Select configuration of PCI Express ports 0-3.
PCI Express Port 0	Disabled **Enabled**	Enable or disable PCI Express port. *Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.*
Link Speed	Auto **PCIE Gen1** PCIE Gen2	Control link speed for this PCI Express port.
Hotplug Support	**Disabled** Enabled	Enable or disable hotplug support for the respective port.
PCI Express Port 1	Disabled **Enabled**	Enable or disable PCI Express port. *Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.*
Link Speed	Auto **PCIE Gen1** PCIE Gen2	Control link speed for this PCI Express port.
Hotplug Support	**Disabled** Enabled	Enable or disable hotplug support for the respective port.
PCI Express Port 2	Disabled **Enabled**	Enable or disable PCI Express port. *Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.*

Feature	Options	Description
Link Speed	Auto **PCIE Gen1** PCIE Gen2	Control link speed for this PCI Express port.
Hotplug Support	**Disabled** Enabled	Enable or disable hotplug support for the respective port
PCI Express Port 3	Disabled **Enabled**	Enable or disable PCI Express port. *Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.*
Link Speed	Auto **PCIE Gen1** PCIE Gen2	Control link speed for this PCI Express port.
Hotplug Support	**Disabled** Enabled	Enable or disable hotplug support for the respective port.

9.4.8   Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	no option	Current CPU temperature.
Southbridge Temperature	no option	Current southbridge temperature.
Board Temperature	no option	Current board temperature.
5V Standby	no option	Current 5V standby input reading.
5V Standard	no option	Current 5V input reading.
CPU Fan Speed	no option	Current CPU fan speed reading.

9.4.9   SATA Configuration Submenu

Feature	Options	Description
SATA Interface Mode	**Native IDE** RAID AHCI Legacy IDE	Select onboard SATA controller interface mode.
SATA Port 0	**Enabled** Disabled	Enable or disable selected port.
Port Speed	**Auto** Gen1 Gen2	Select SATA speed generation for the selected port.
SATA Port 1	**Enabled** Disabled	Enable or disable selected port.
Port Speed	**Auto** Gen1 Gen2	Select SATA speed generation for the selected port.
Onboard SSD	**Enabled** Disabled	Enable or disable the optional onboard SSD.
SSD Speed	**Auto** Gen1 Gen2	Select SATA speed generation for the onboard SSD.
SSD Write Protection	**Disabled** Enabled	Enable or disable hardware write protection for the onboard SSD.

9.4.10 USB Configuration Submenu

Feature	Options	Description
USB Port 0	Disabled **Enabled**	Enable or disable selected port.
USB Port 1	Disabled **Enabled**	Enable or disable selected port.
USB Port 2	Disabled **Enabled**	Enable or disable selected port.
USB Port 3	Disabled **Enabled**	Enable or disable selected port.
USB Port 4	Disabled **Enabled**	Enable or disable selected port.
USB Port 5	Disabled **Enabled**	Enable or disable selected port.
USB Port 6	Disabled **Enabled**	Enable or disable selected port.
USB Port 7	Disabled **Enabled**	Enable or disable selected port.
USB Overcurrent Reporting	Disabled **Enabled**	Select whether activation of the USB overcurrent signals results in USB overcurrent register reporting and software event handling as well.
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
EHCI Hand-off	**Disabled** Enabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
USB Transfer Timeout	1 sec 5sec 10 sec **20 sec**	Timeout value for legacy USB control, bulk and interrupt transfers.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device Start Unit command timeout.
Device Power-Up Delay Selection	**Auto** Manual	Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value, which is 100ms for a root port or derived from the hub descriptor for a hub port.
Device Power-Up Delay Value	**5** 1-40	Actual power-up delay value in seconds.

Feature	Options	Description
USB Mass Storage Device Name *(Auto detected USB mass storage devices are listed here dynamically)*	**Auto** Floppy Forced FDD Hard Disk CD-ROM	Every USB mass storage device that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. *Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.* Select AUTO to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. Forced FDD allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. Hard Disk allows the device to be emulated as hard disk. CD-ROM assumes the CD-ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

9.4.11 Super I/O Configuration Submenu

Feature	Options	Description
Serial Port 0	Disabled **Enabled**	Enable or disable serial port 0.
Device Settings	IO=3F8h; IRQ=4;	Fixed configuration of serial port 0 if enabled.
Serial Port 1	Disabled **Enabled**	Enable or disable serial port 1.
Device Settings	IO=2F8h; IRQ=3;	Fixed configuration of serial port 1 if enabled.
Parallel Port	Disabled **Enabled**	Enable or disable parallel port.
Device Settings	IO=378h; IRQ=7;	Fixed configuration of the parallel port if enabled.
Device Mode	**Standard Parallel Mode** EPP Mode ECP Mode EPP Mode & ECP Mode	Set the parallel port mode.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

9.4.12 Serial Port Console Redirection

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
►Console Redirection Settings	submenu	Opens the console redirection configuration submenu.
COM1 Console Redirection	**Disabled** Enabled	Enable or disable serial port 1 console redirection.
►Console Redirection Settings	submenu	Opens the console redirection configuration submenu.

9.4.12.1 Console Redirection Settings Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select terminal type.
Baudrate	9600, 19200, 38400, 57600, **115200**	Select baudrate.
Data Bits	7, **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution in UEFI environment.
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.

9.5 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

9.5.1 Boot Settings Configuration

Feature	Options	Description
Quiet Boot	**Disabled** Enabled	*Disabled* displays normal POST diagnostic messages. *Enabled* displays OEM logo instead of POST messages. *Note: The default OEM logo is a dark screen.*
Setup Prompt Timeout	**1** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot, 65535 means infinite wait.
POST/Setup VGA Support	**Disabled** Enabled	Select VGA mode for setup and POST screen. Enables setup and POST screen output support for VGA and WVGA display resolutions.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The "Device Based" boot priority list allows you to select from a list of currently detected devices only. The "Type Based" boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the "Device Based" boot priority list might change dynamically in cases when devices are physically removed or added to the system. The "Type Based" boot menu is static and can only be changed by the user.
1st, 2nd, 3rd, ... Boot Device (Up to 12 boot devices can be prioritized if device based priority list control is selected. If "Type Based" priority list control is enabled only 8 boot devices can be prioritized.)	Disabled SATA 0 Drive SATA 1 Drive Onboard SSD USB Floppy USB Harddisk USB CDROM Onboard LAN External LAN Other BEV Device OEM BEV Device	This view is only available when in the default "Type Based" mode. When in "Device Based" mode you will only see the devices that are currently connected to the system.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. *Note: Only works with an ATX type power supply.*
AT Shutdown Mode	**System Reboot** Hot S5	Determines the behaviour of an AT-powered system after a shutdown.

Feature	Options	Description
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
GateA20 Active	**Upon Request** Always	Gate A20 control. Upon Request = Gate A20 can be disabled using BIOS services. Always = Do not allow disabling Gate A20.
Option ROM Messages	**Force BIOS** Keep Current	Set display mode for option ROMs.
Interrupt 19 Capture	**Disabled** Enabled	Defines whether option ROMs may trap the INT19h legacy boot vector.

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

3. *Unlike other module designs available in the embedded market, a CMOS battery is not required by congatec modules to support the 'Power Loss Control' feature.*

9.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

9.6.1 Security Settings

Feature	Options	Description
Setup Administrator Password	Enter password	Specifies the setup administrator password.
HDD Security Configuration *List of all detected hard disks supporting the security feature set.*	Select device to open device security configuration submenu	

9.6.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

9.6.3 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen.

You can display an Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Load the CMOS defaults of all the setup options.
► Boot Override *List of all boot devices currently detected.*	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to "Device Based".

10   Additional BIOS Features

The conga-QAF uses a congatec/AMI AptioEFI firmware that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as QBRAR1xx, where QBRA is the congatec internal BIOS project name for conga-QAF, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

The conga-QAF BIOS binary size is approximately 8MB.

10.1   Supported Flash Devices

The conga-QAF supports the following flash devices:

- Atmel AT25DF321-SU

- Greenliant Systems SST25VF032B-66-4I-S2AF

- Macronix MX25L3206EM2I-12G

The flash devices listed above can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.

10.2   Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

10.3   BIOS Security Features

The BIOS provides a setup administrator password that limits access to the BIOS setup menu.

10.4   Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to 'lock' and 'unlock' drives using the security password. A 'locked' drive will be detected by the system, but no data can be accessed. Accessing data on a 'locked' drive requires the proper password to 'unlock' the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within five attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

11　Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Qseven® Specification	http://www.qseven-standard.org/
Qseven® Design Guide	http://www.qseven-standard.org/
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications