

CEVA

COM Express Evaluation Backplane

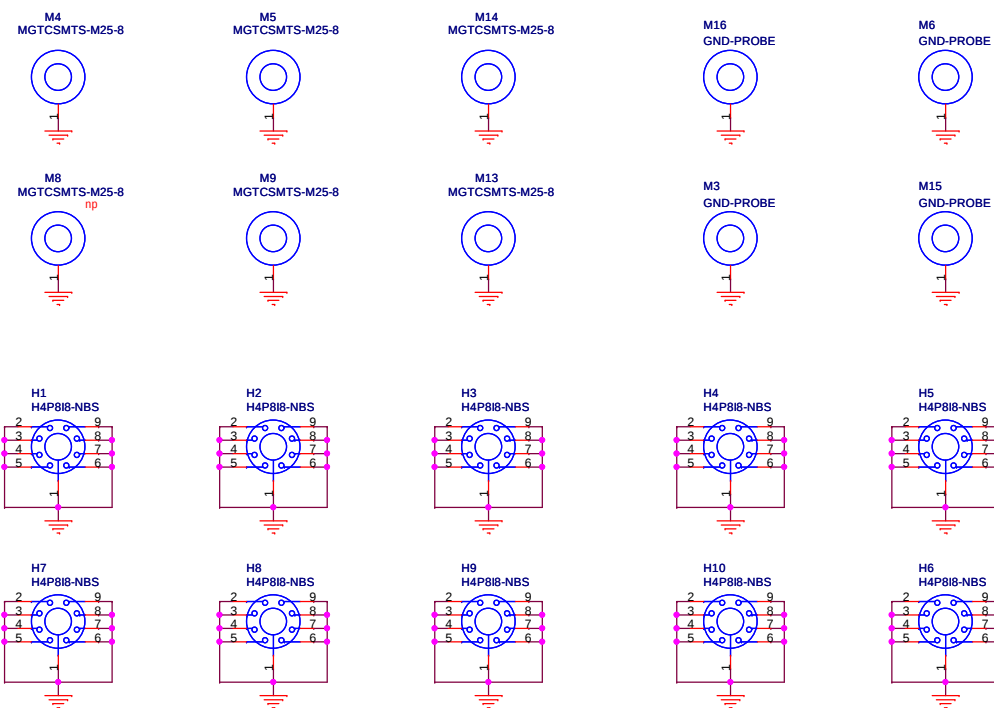
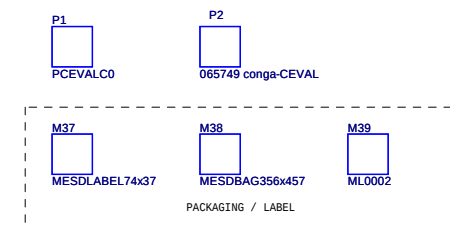
Rev. C.0

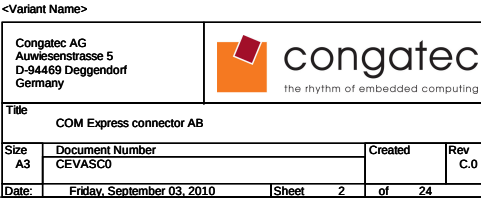
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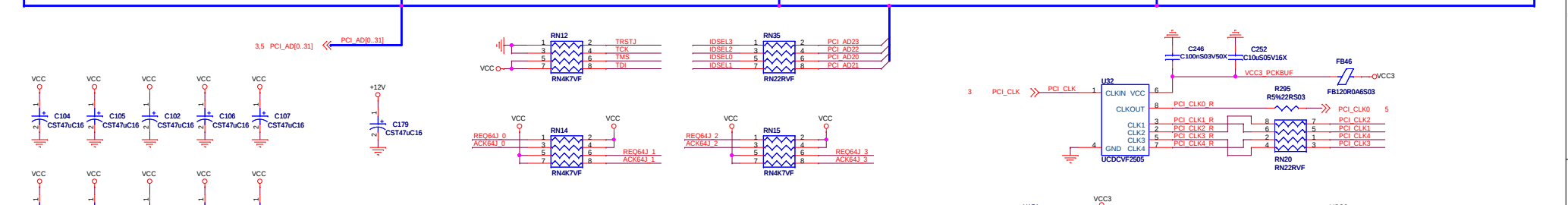
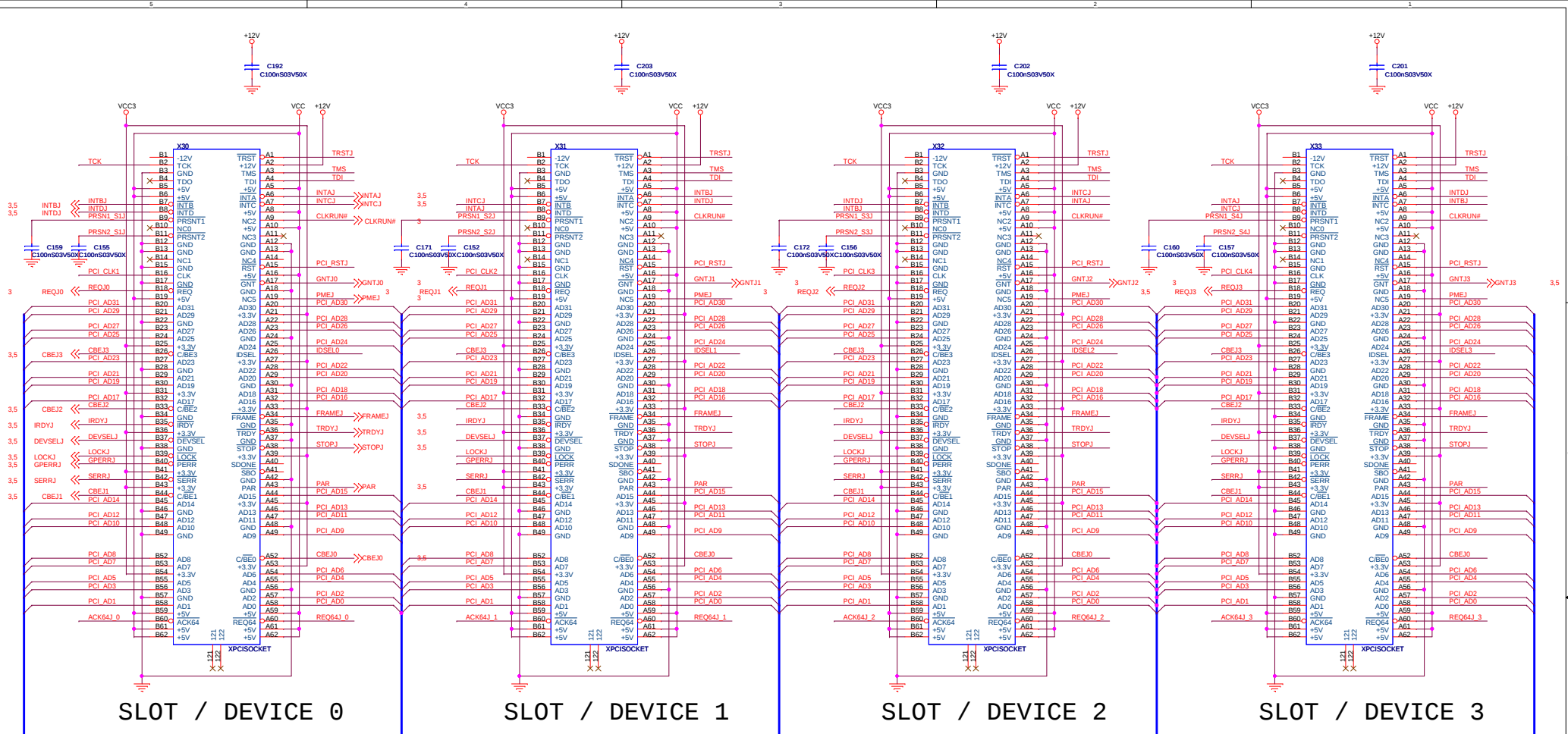
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Variants

Base LPC SuperIO W83627HG; Audio Codec ALC888

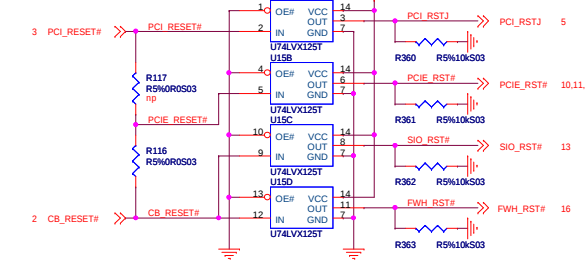


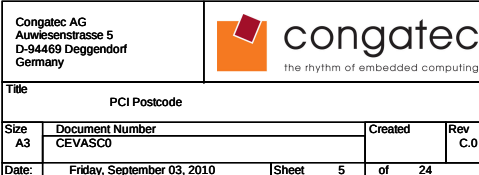


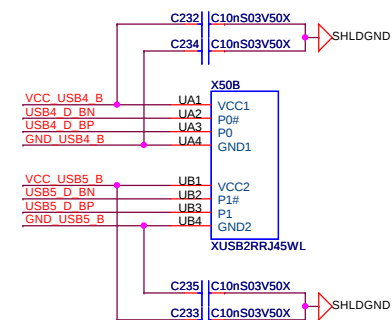
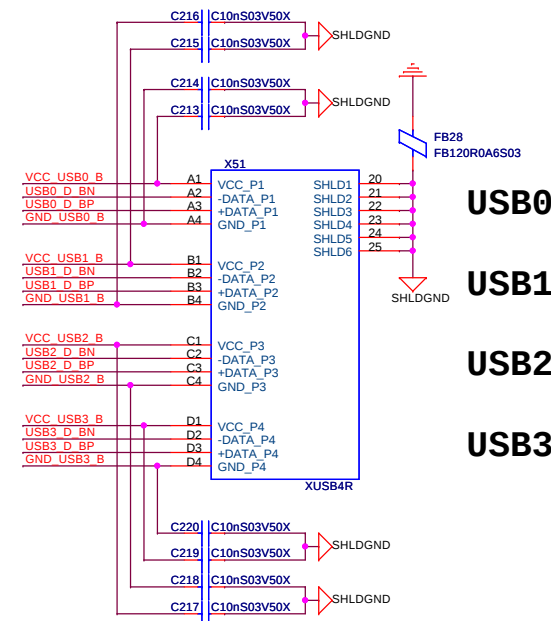
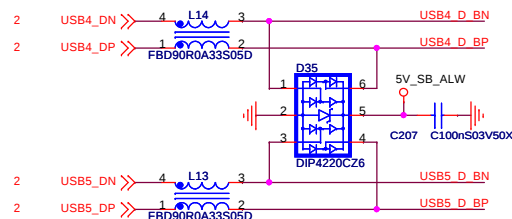
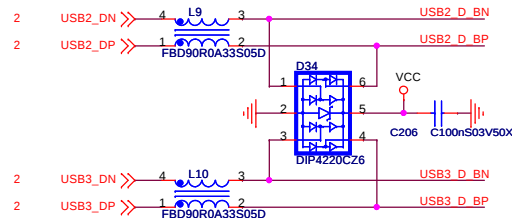
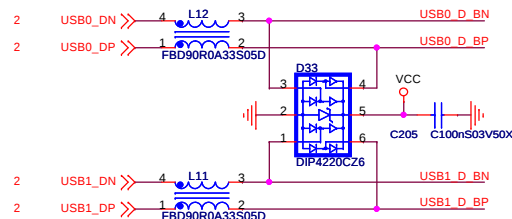
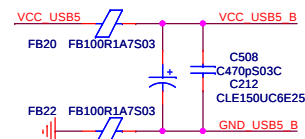
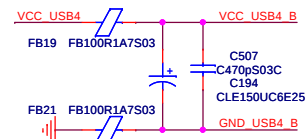
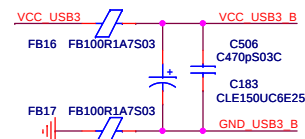
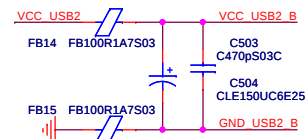
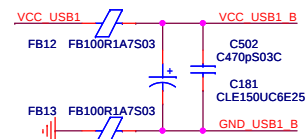
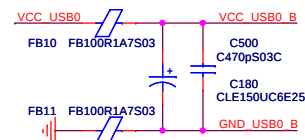
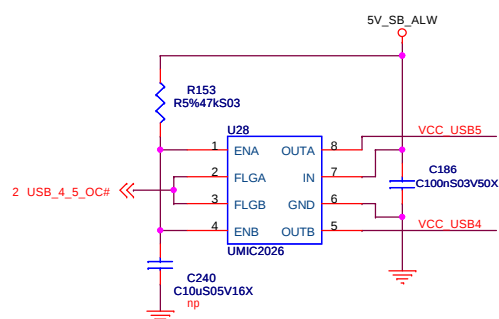
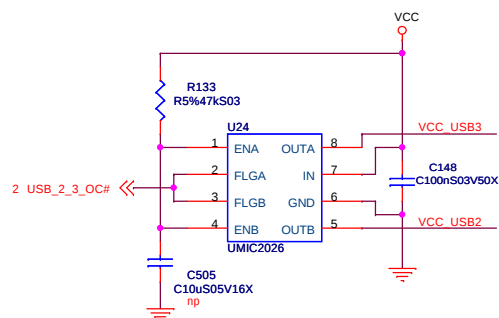
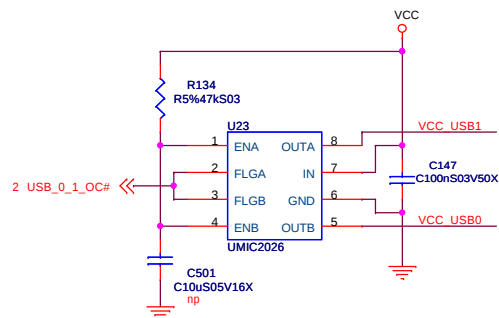


COM Express - PCI interrupt routing and IDELS

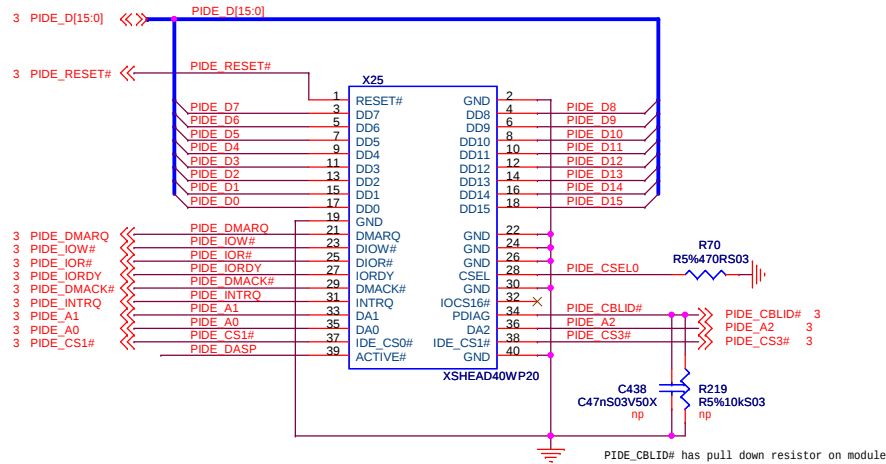
Slot / Device Signal	Slot / Device 0	Slot / Device 1	Slot / Device 2	Slot / Device 3
IDESEL	PCI_AD[20]	PCI_AD[21]	PCI_AD[22]	PCI_AD[23]
PCI Clock	PCI_CLK replica	PCI_CLK replica	PCI_CLK replica	PCI_CLK replica
INTA#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#
INTB# (if used)	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#
INTC# (if used)	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#
INTD# (if used)	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#



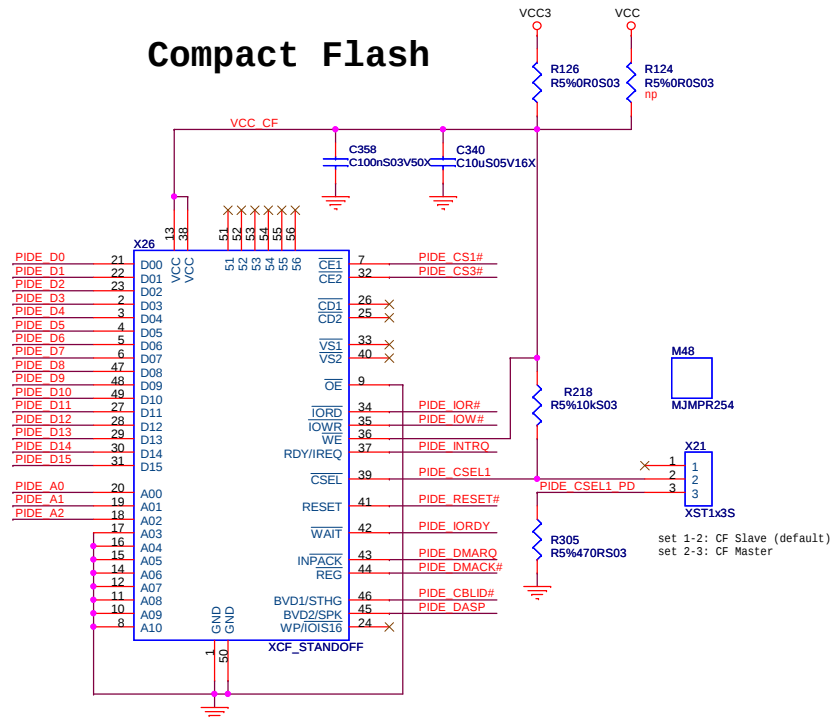




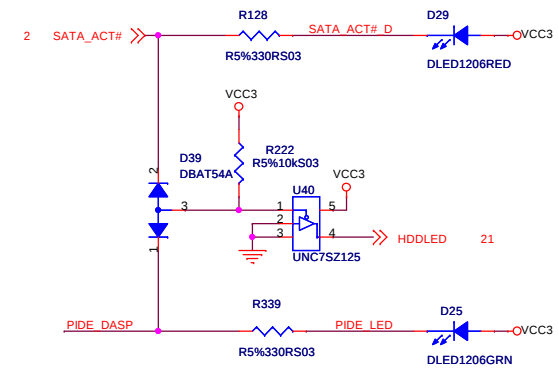
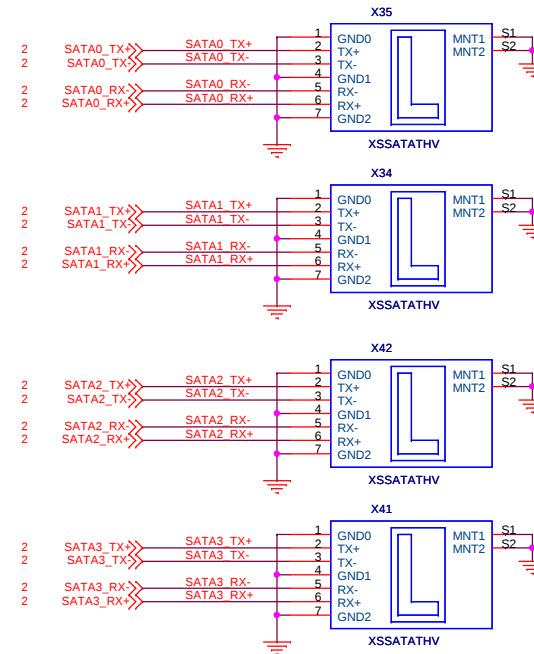
IDE



Compact Flash



SATA

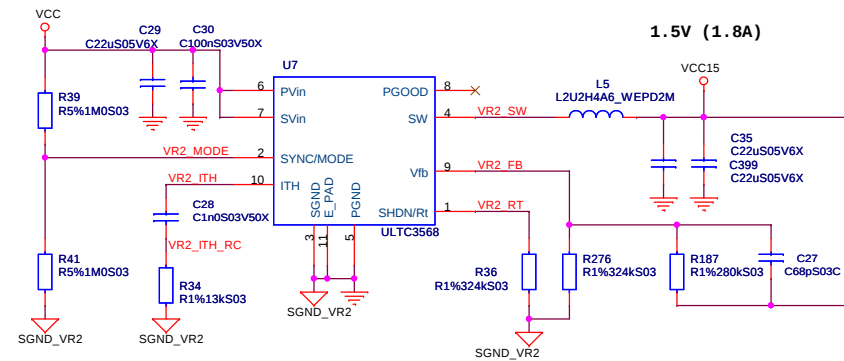
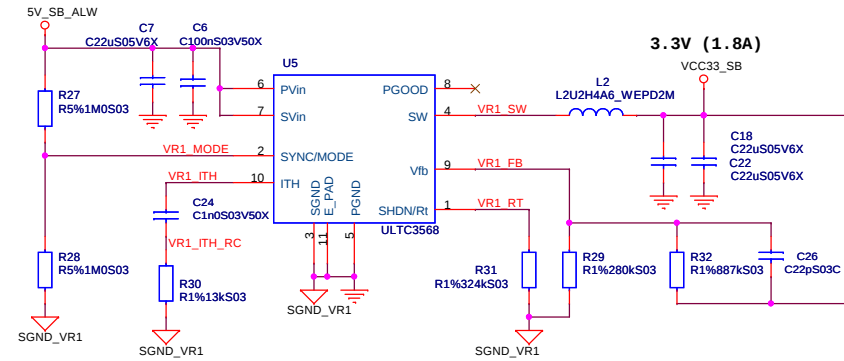
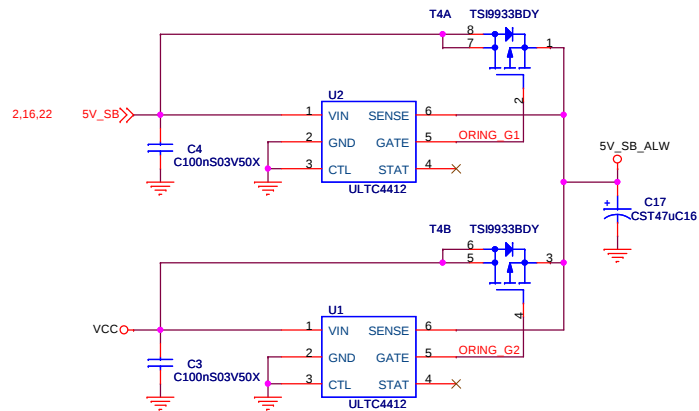


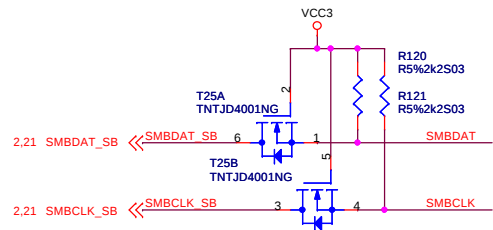
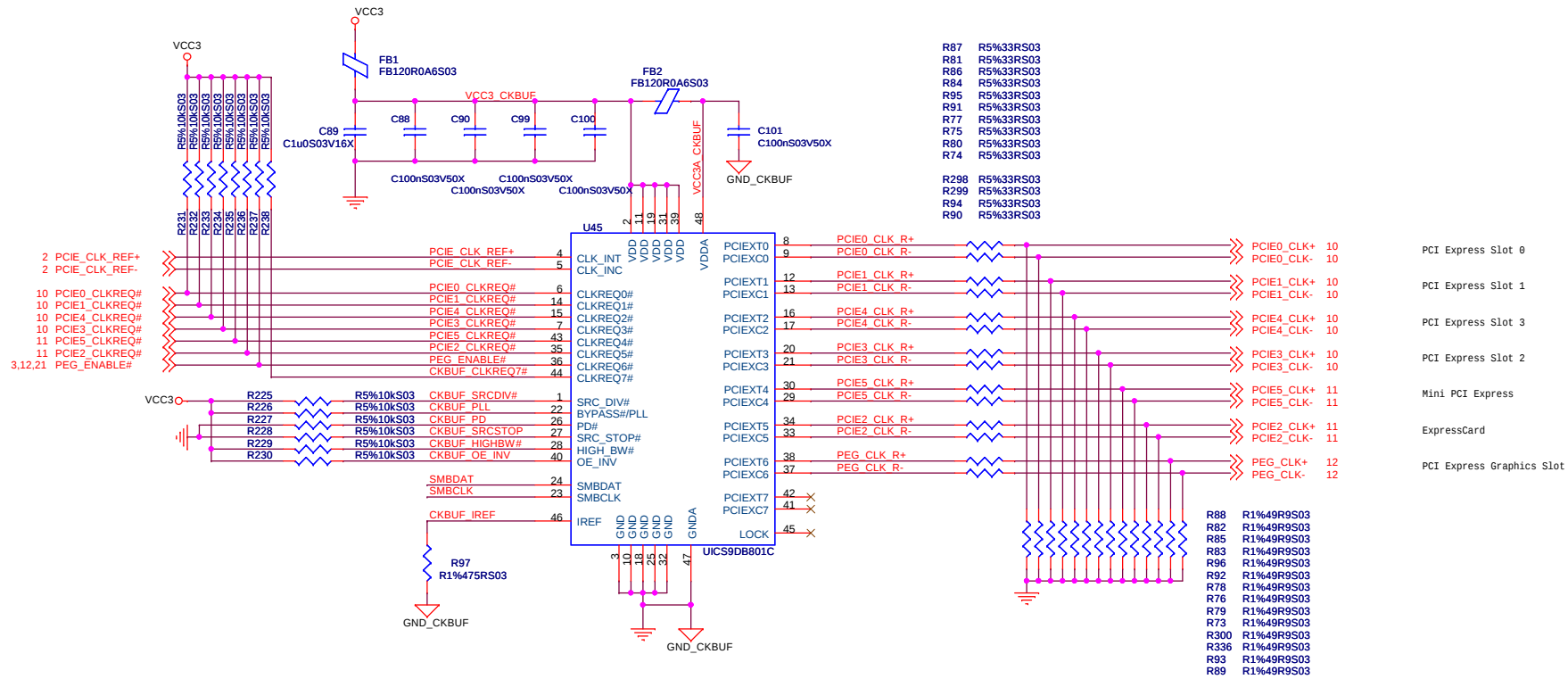
<Variant Name>

Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany



Title		SATA / IDE / CF	
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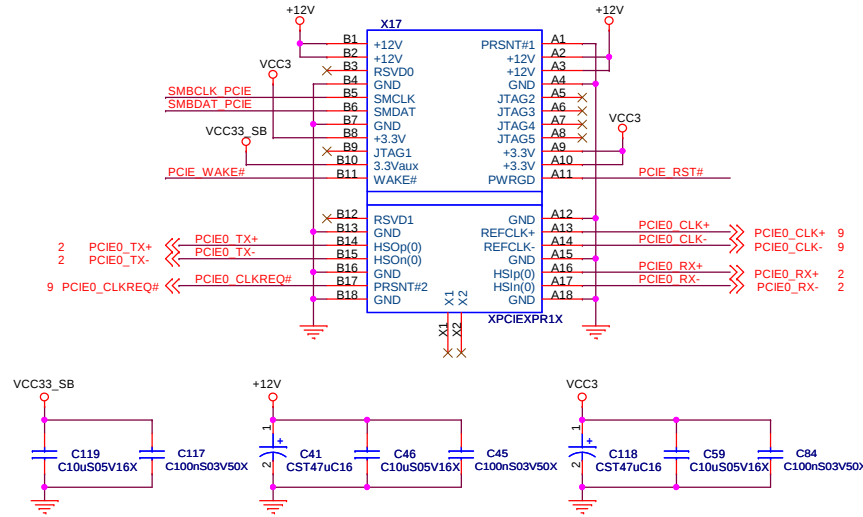
SMB BUS S5 SEGMENT from Modul
- Standby Level
- Pullups on Modul

SMB BUS S0 SEGMENT
- Main Level
- Pullups 3.3V 2.2k

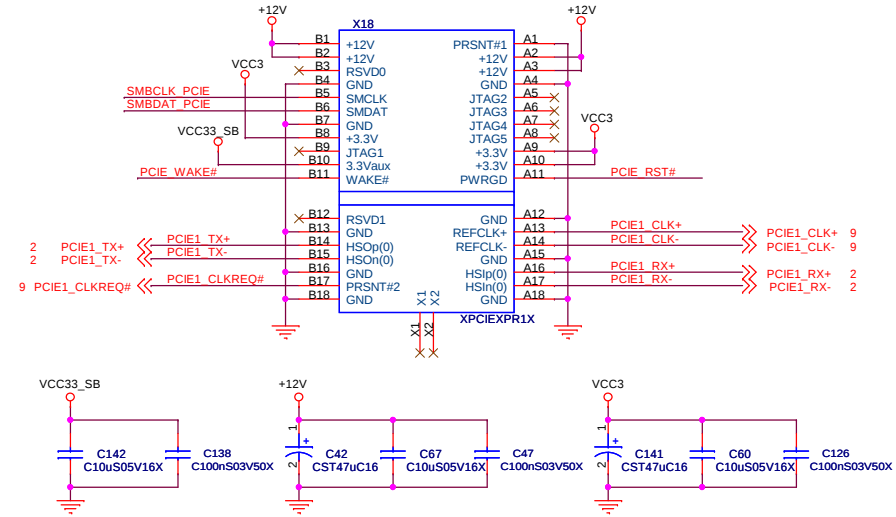


9.11.12 SMBCLK_PCIE >>> SMBCLK_PCIE
 9.11.12 SMBDAT_PCIE >>> SMBDAT_PCIE
 4.11.12 PCIE_RST# <<< PCIE_RST#
 2.11.12 PCIE_WAKE# <<< PCIE_WAKE#

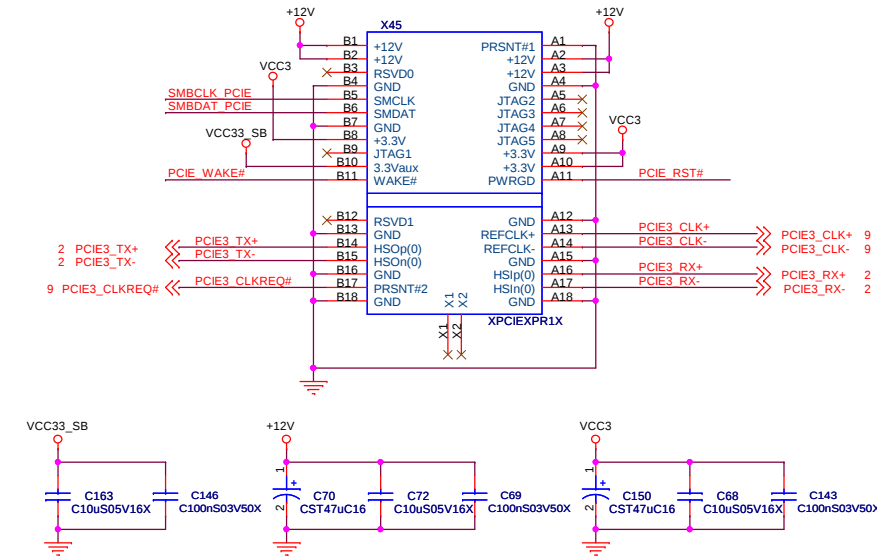
PCI Express SLOT 0 / Lane 0



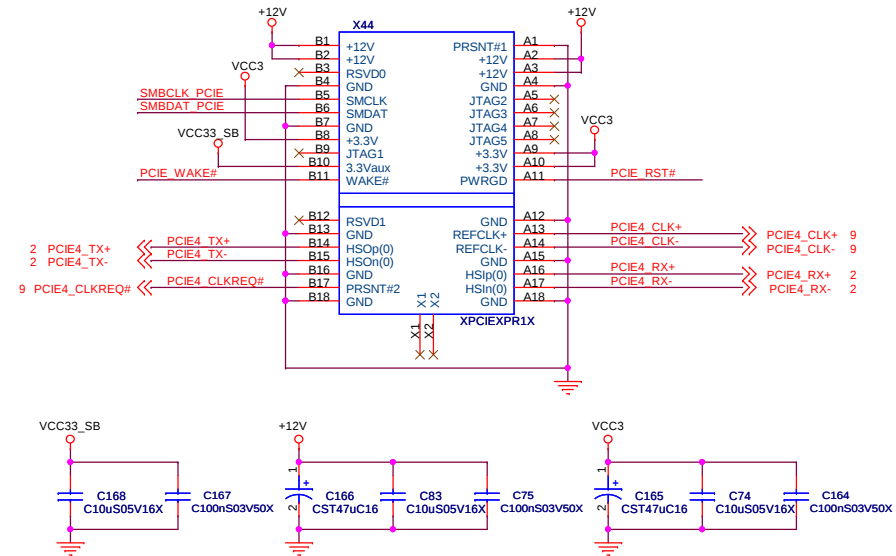
PCI Express SLOT 1 / Lane 1

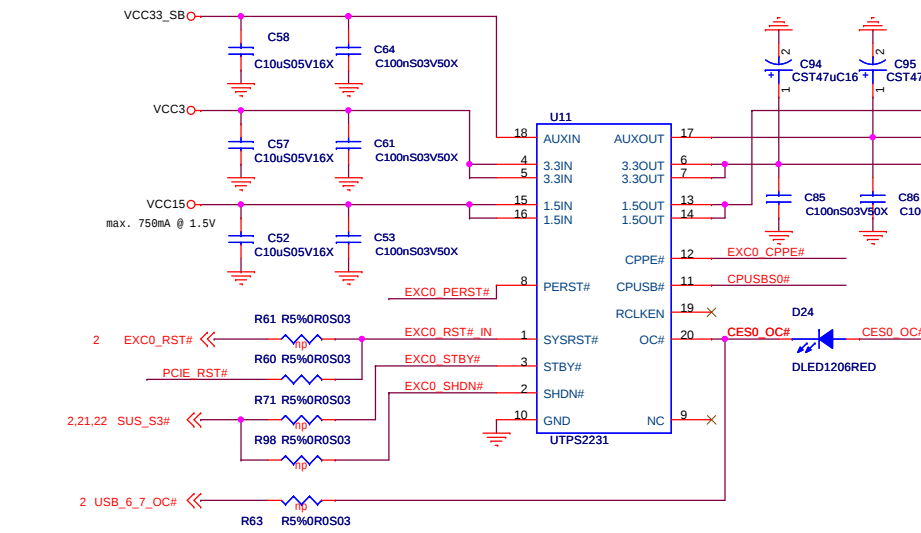


PCI Express SLOT 2 / Lane 3

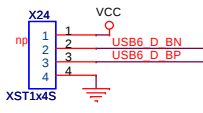


PCI Express SLOT 3 / Lane 4

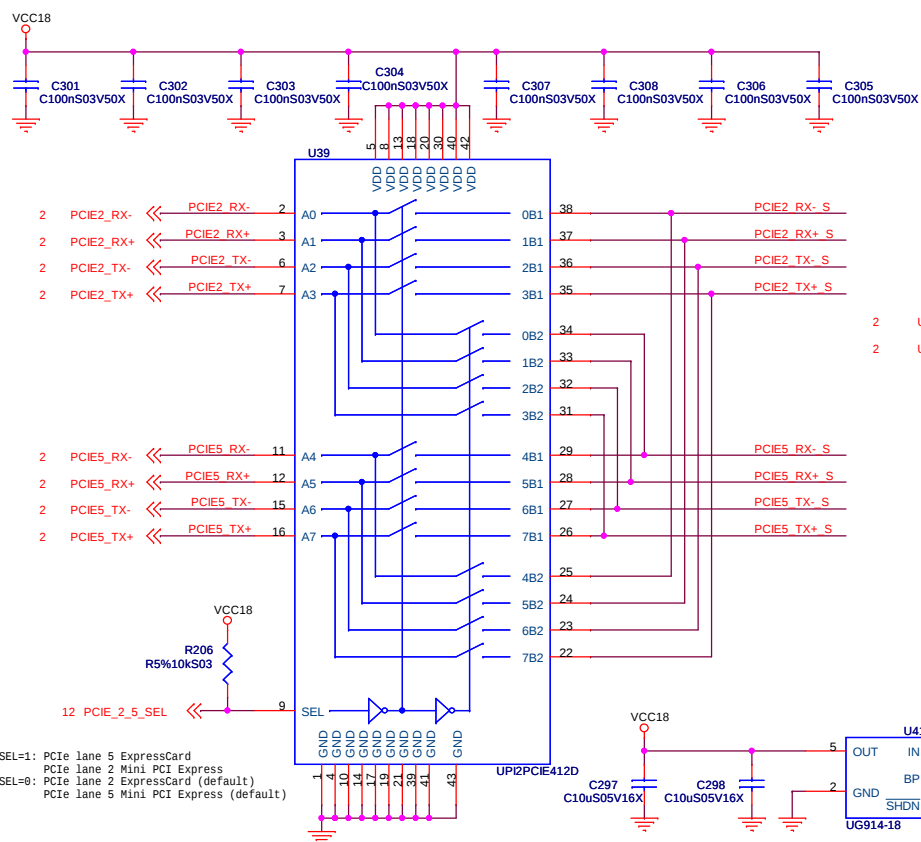
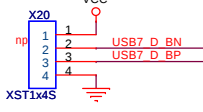




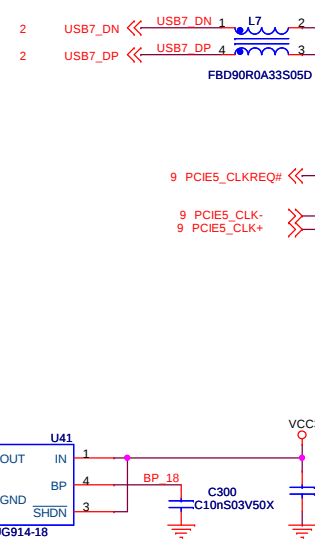
Testsocket for USB6



Testsocket for USB7



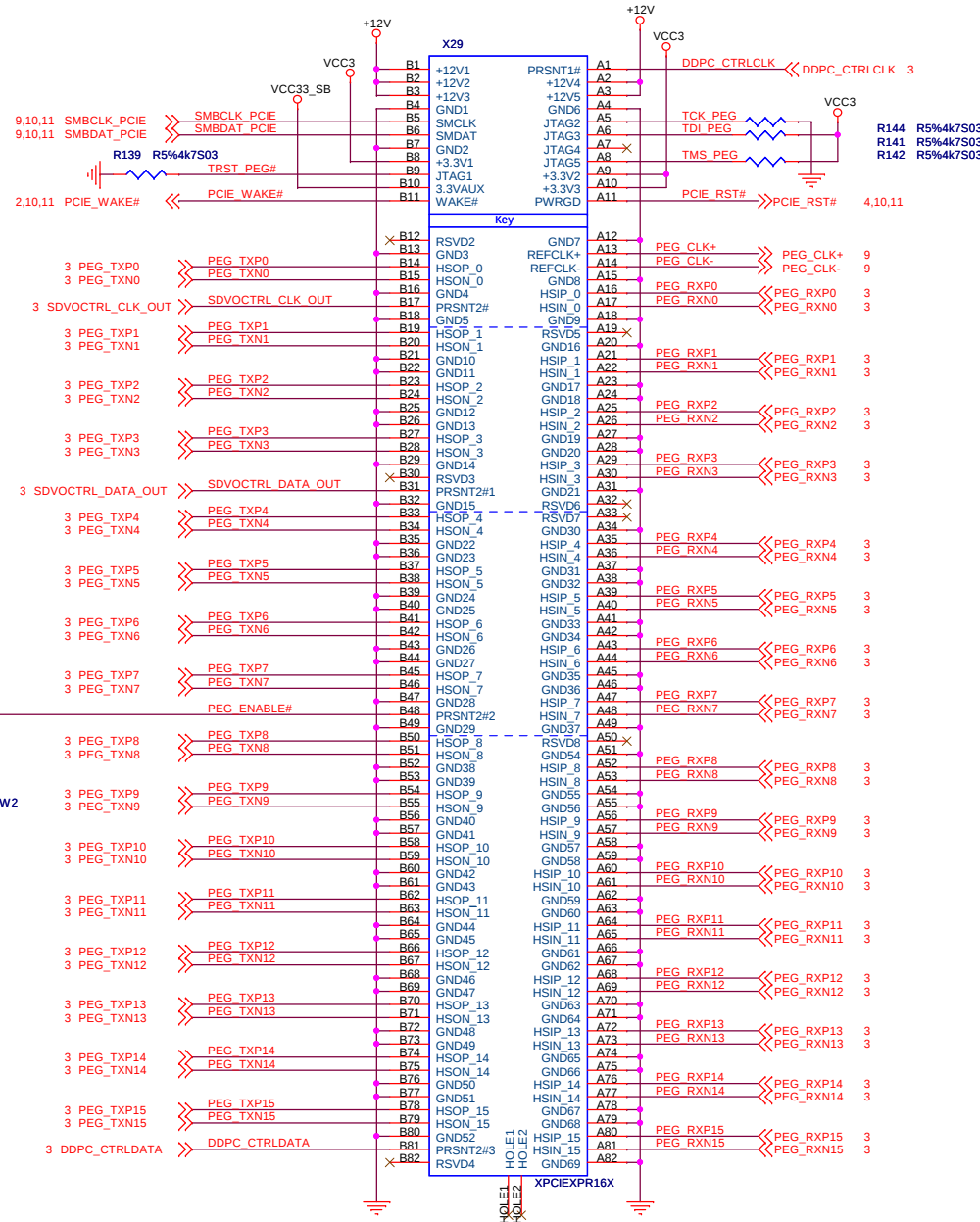
USB7



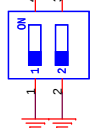
USB6 ExpressCard / LANE 2

miniCard / LANE 5

Congatec AG Auwiesenstrasse 5 D-94469 Deggendorf Germany			
Title: ExpressCard / Mini			
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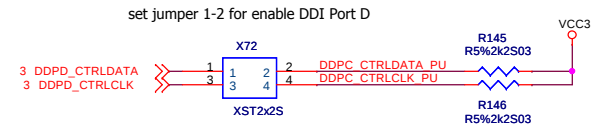
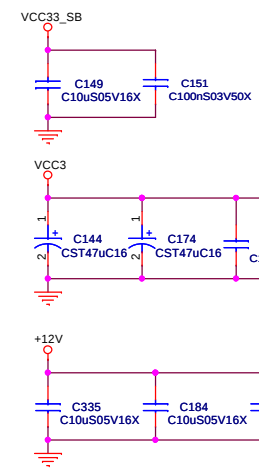


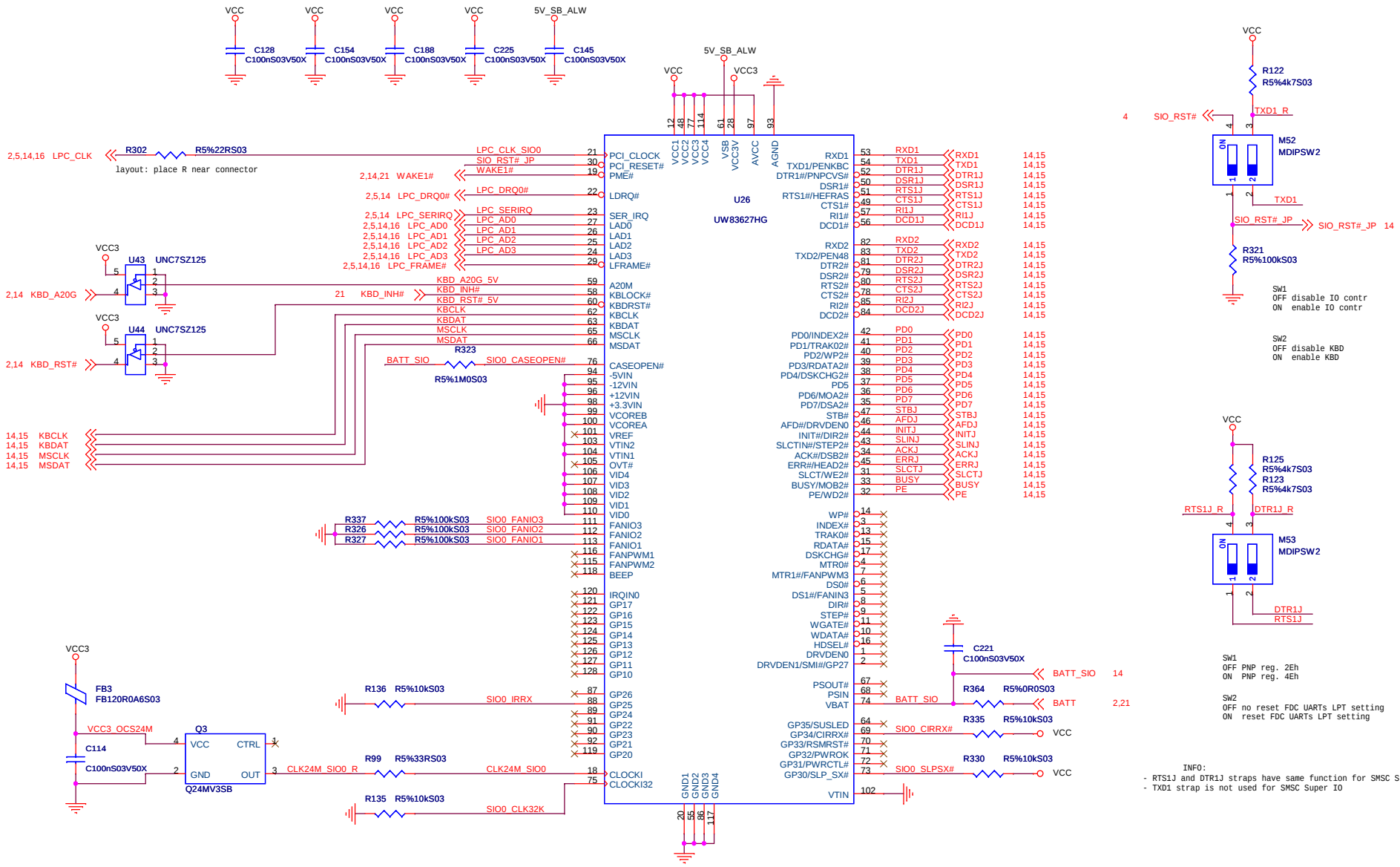
SW2-ON = Enabled PEG clock and set detect signal for Module (default)



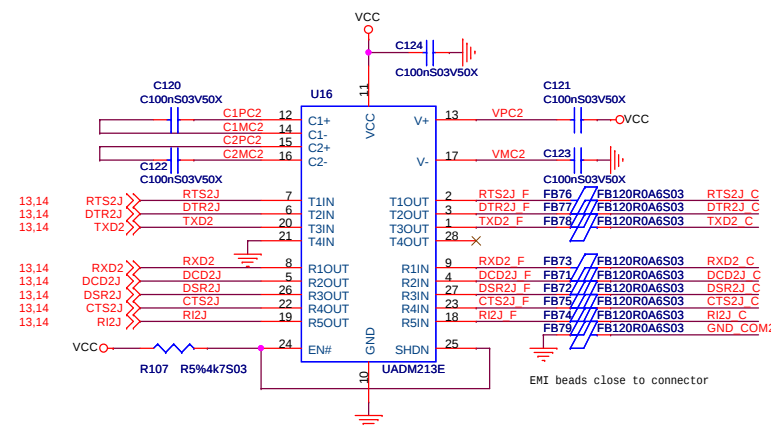
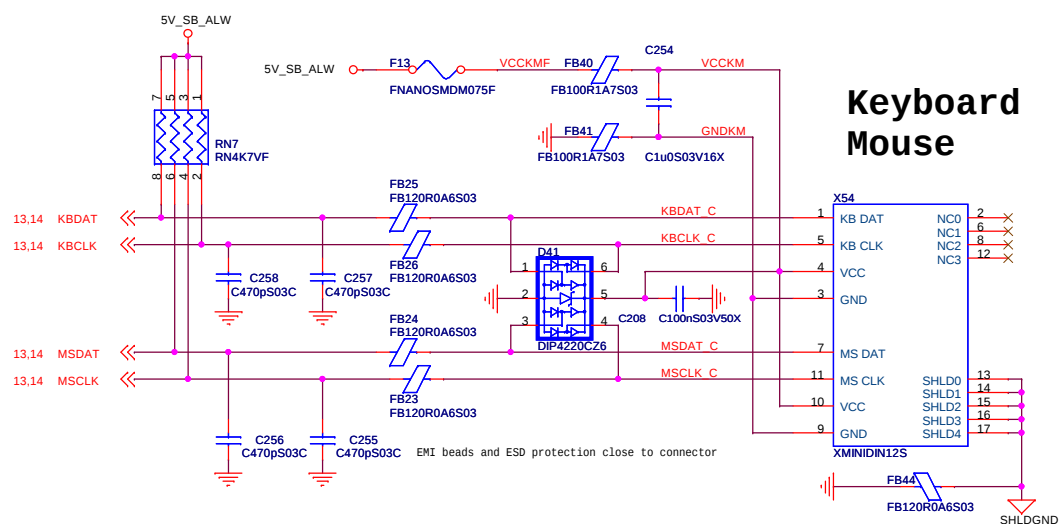
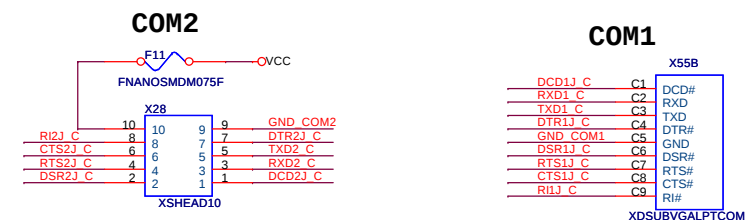
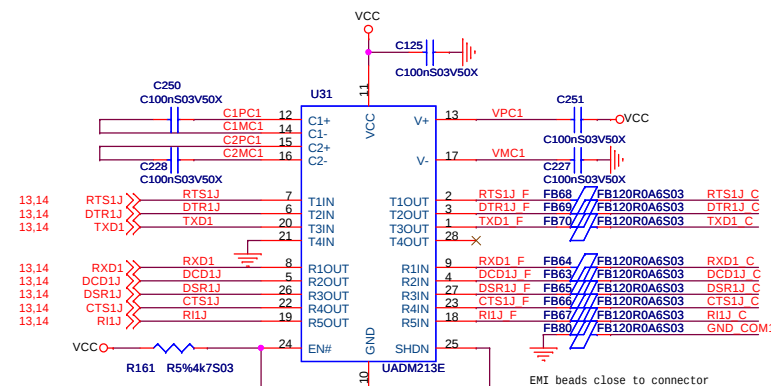
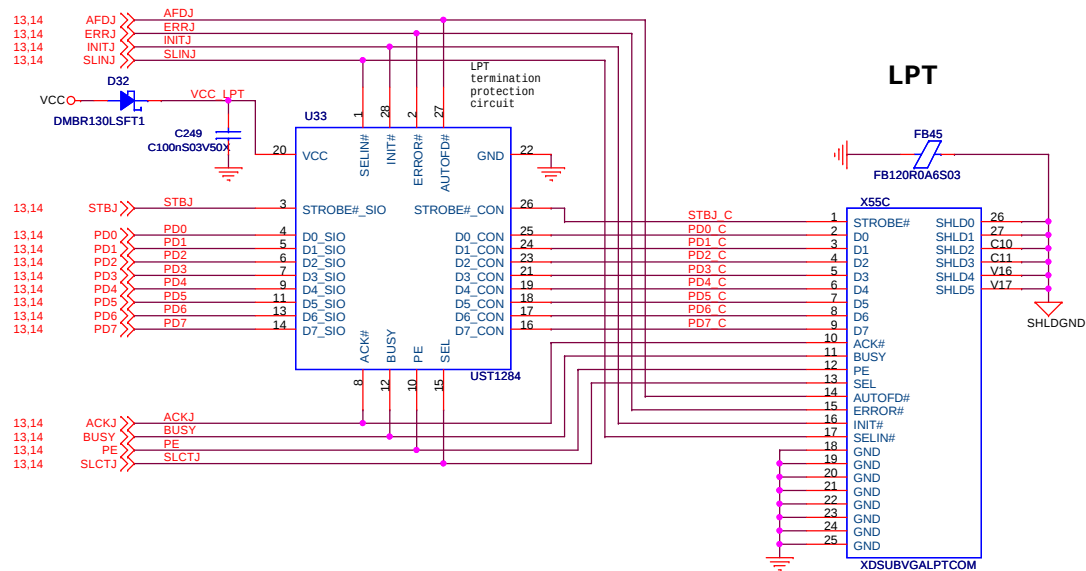
SW1-ON = PCIe lane 2 - ExpressCard (default)
PCIe lane 5 - Mini PCIe (default)

SW1-OFF = PCIe lane 5 - ExpressCard
PCIe lane 2 - Mini PCIe



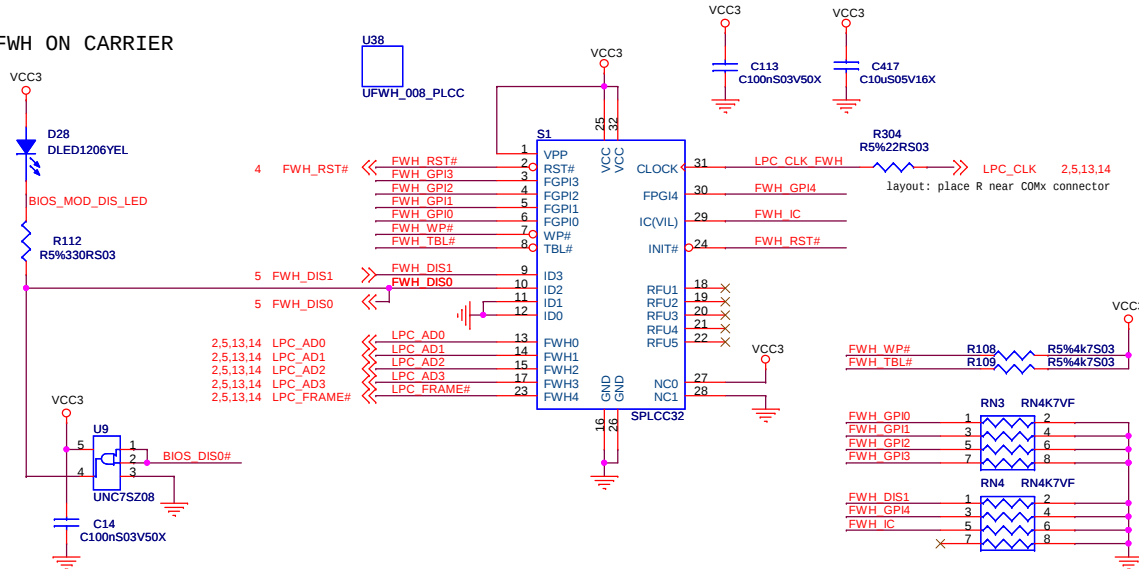


INFO:
 - RTS1J and DTR1J straps have same function for SMSC Super IO
 - TXD1 strap is not used for SMSC Super IO

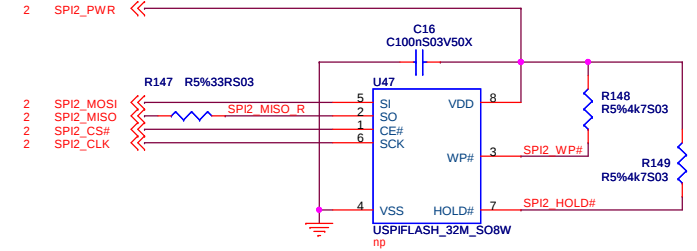


Firmware Hub

ENABLED FWH ON CARRIER

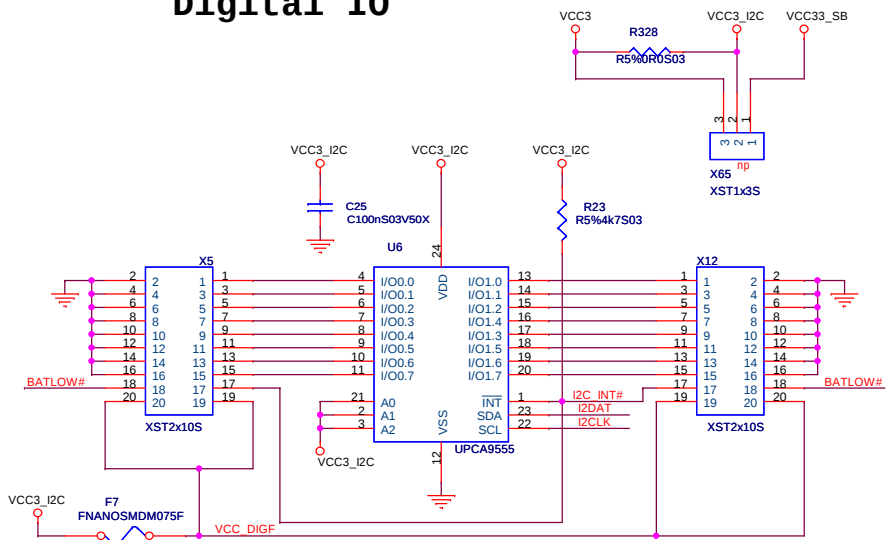


SPI BIOS Flash

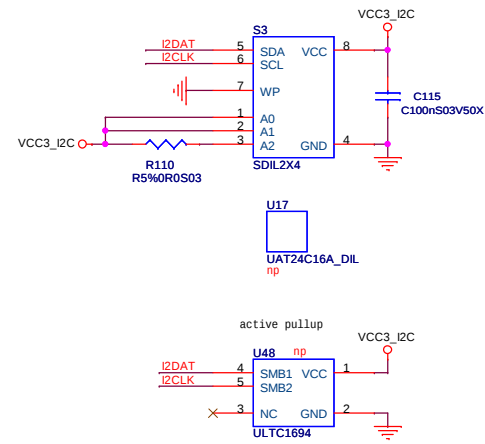


BIOS_DIS1#	BIOS_DIS0#	BIOS ENTRY / SPI_CS#
OFF	OFF	MODULE FWH OR SPI
OFF	ON	CARRIER FWH
ON	OFF	CARRIER SPI CS0#
ON	ON	CARRIER SPI CS1#

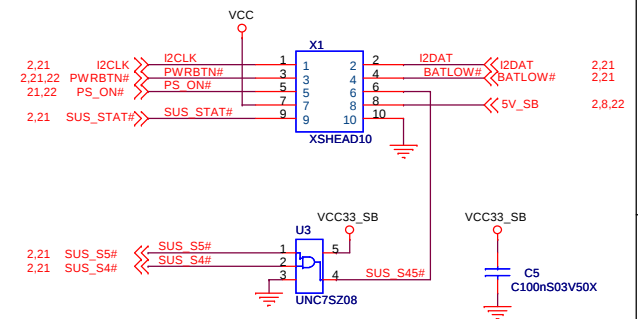
Digital IO

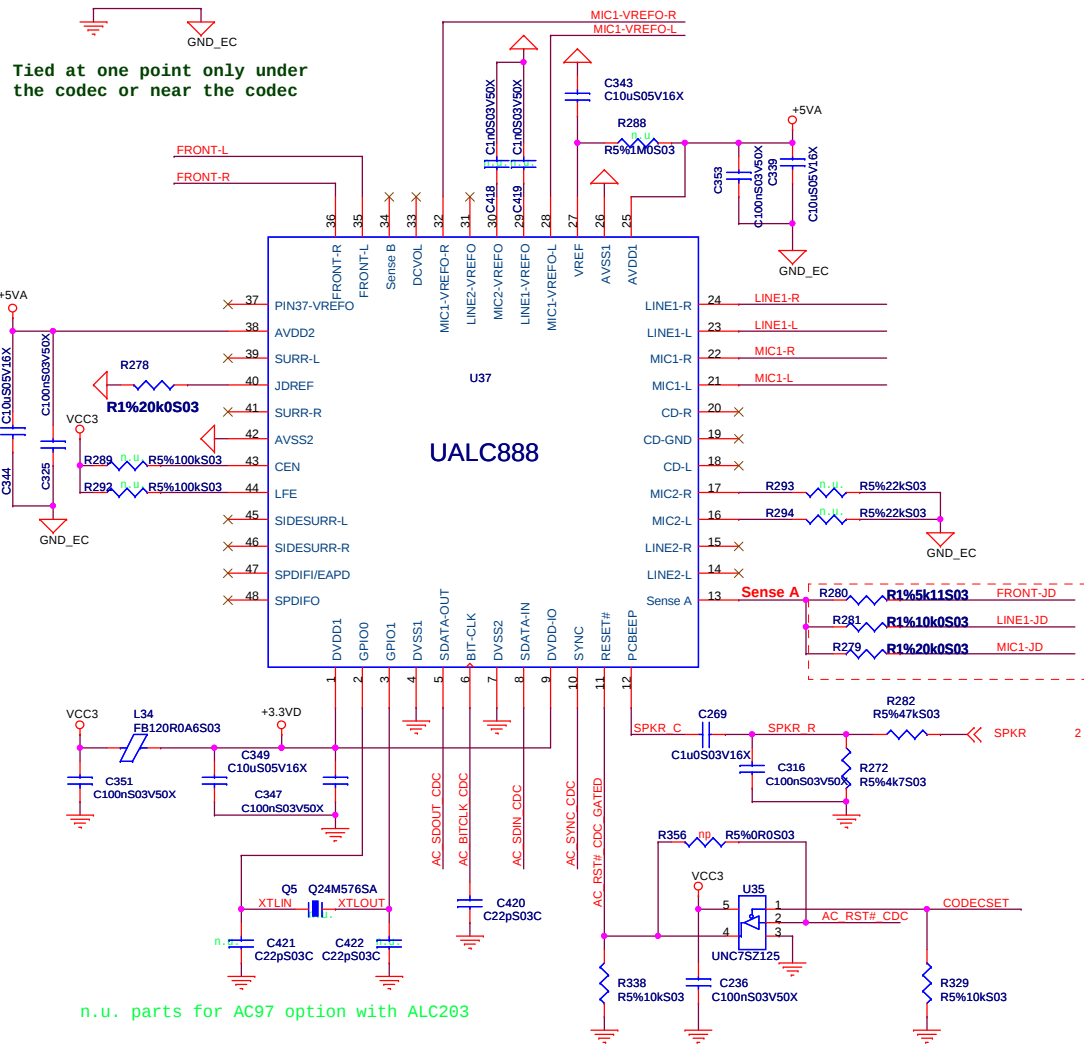


I2C Eeprom

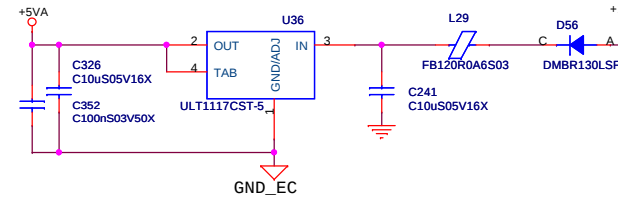


Battery Support

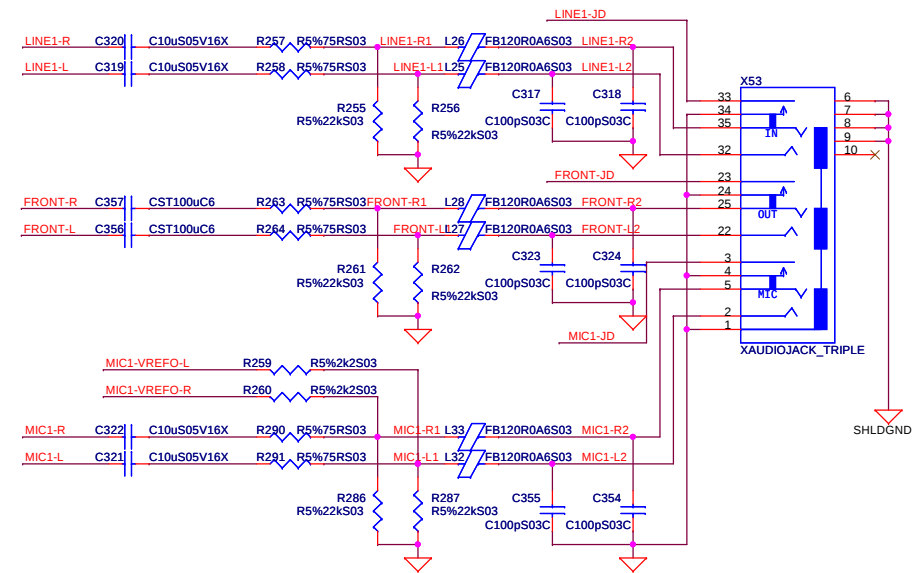




AUDIO POWER

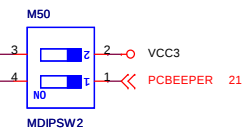


ANALOG I/O CONNECTOR

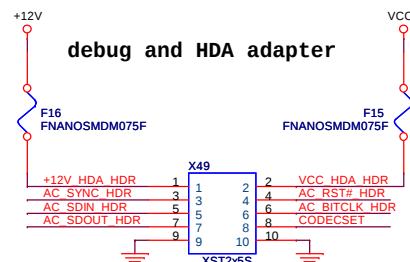


SW2
ON disable CARRIER HDA CODEC

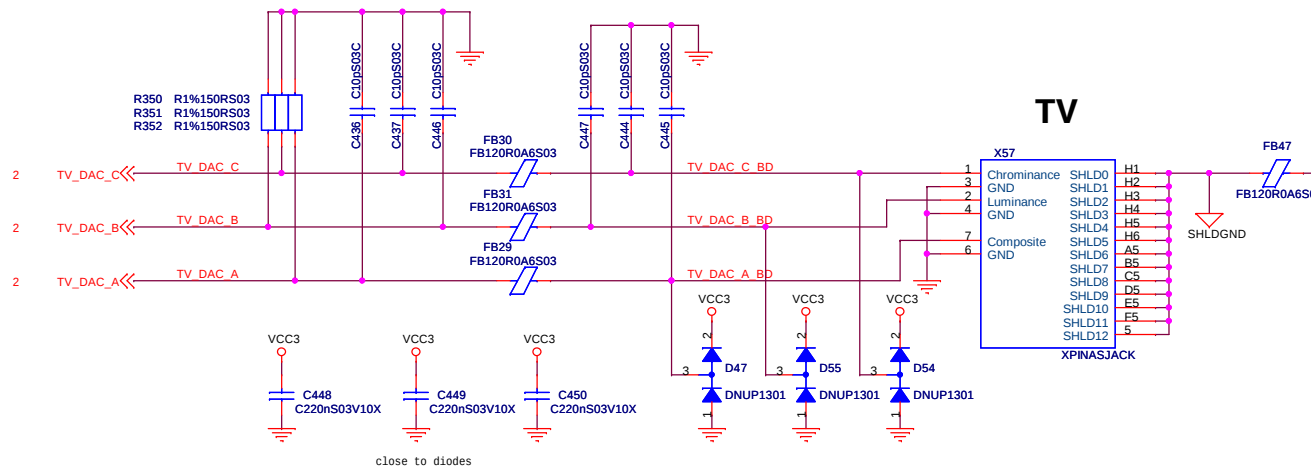
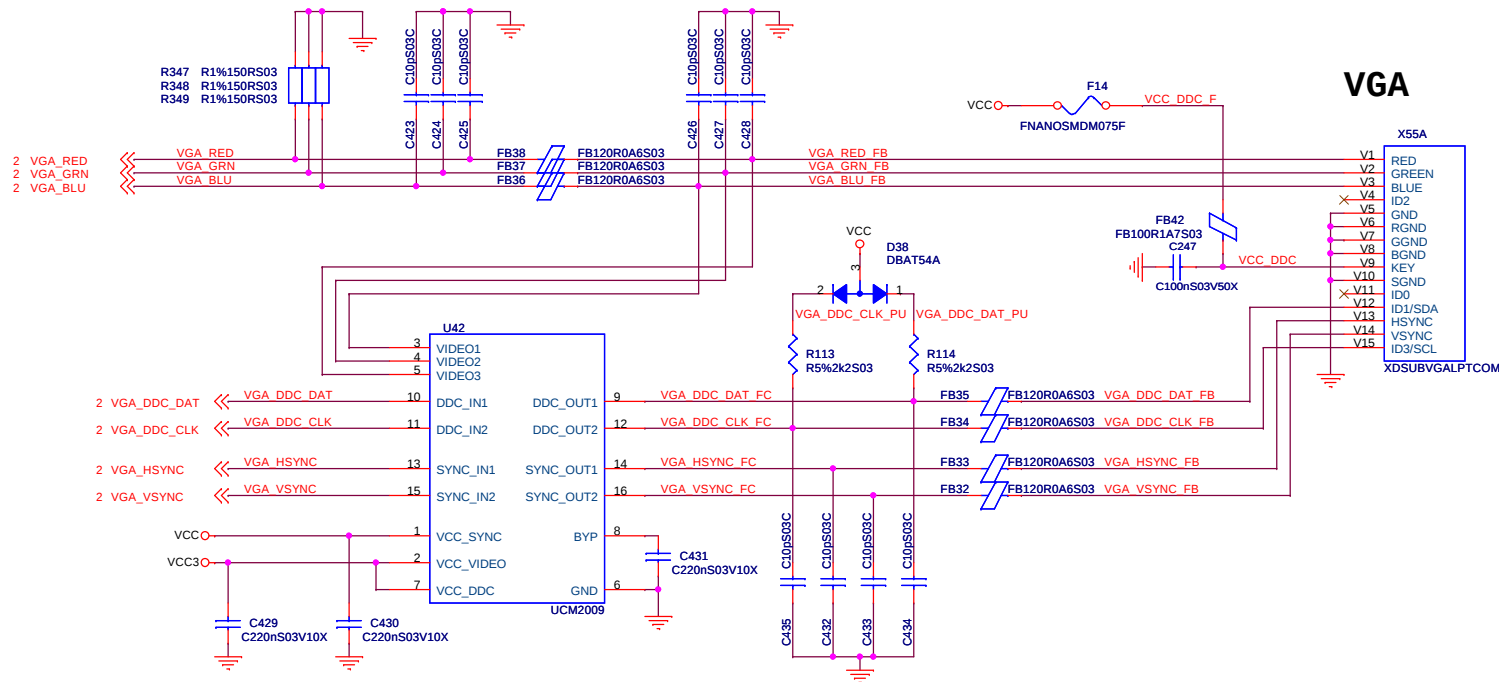
SW1
OFF disable PC BEEPER
ON enable PC BEEPER



debug and HDA adapter

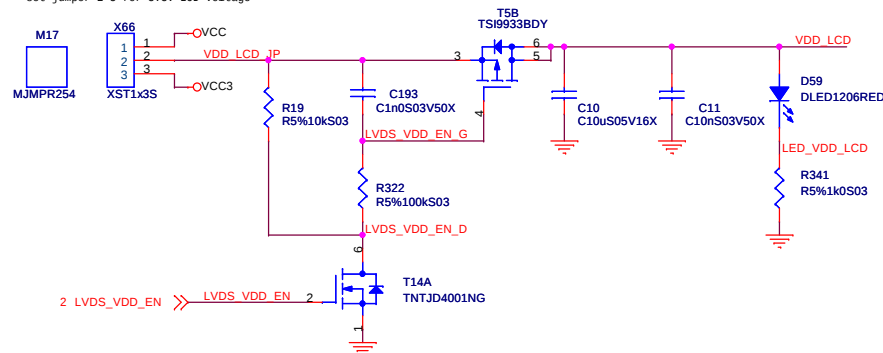


Congatec AG Auwiesenstrasse 5 D-94469 Deggendorf Germany		 congatec the rhythm of embedded computing	
Title AC97 / HDA			
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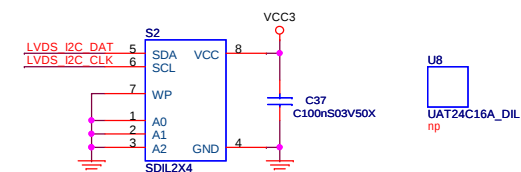
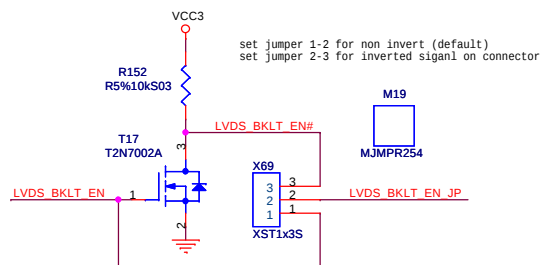
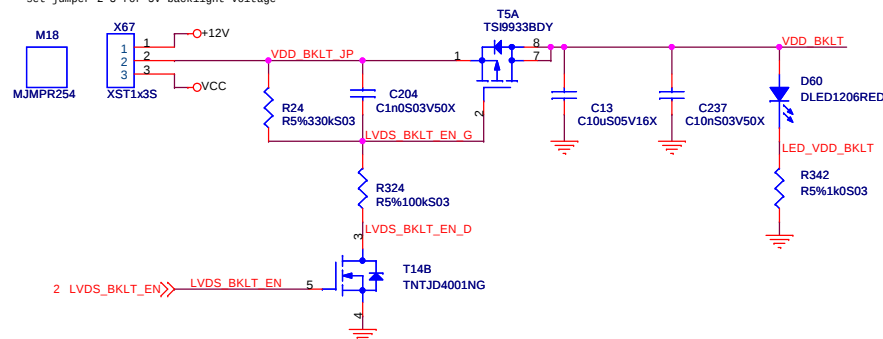


close to diodes

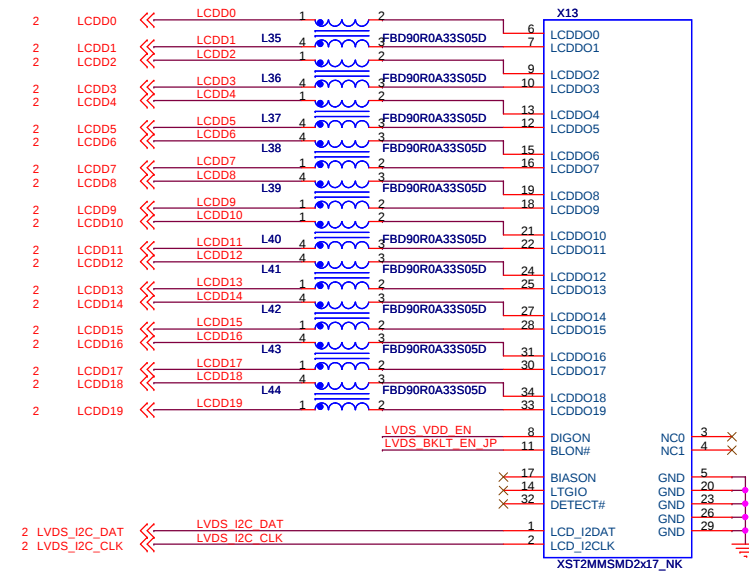
set jumper 1-2 for 5V LCD voltage (default)
set jumper 2-3 for 3.3V LCD voltage



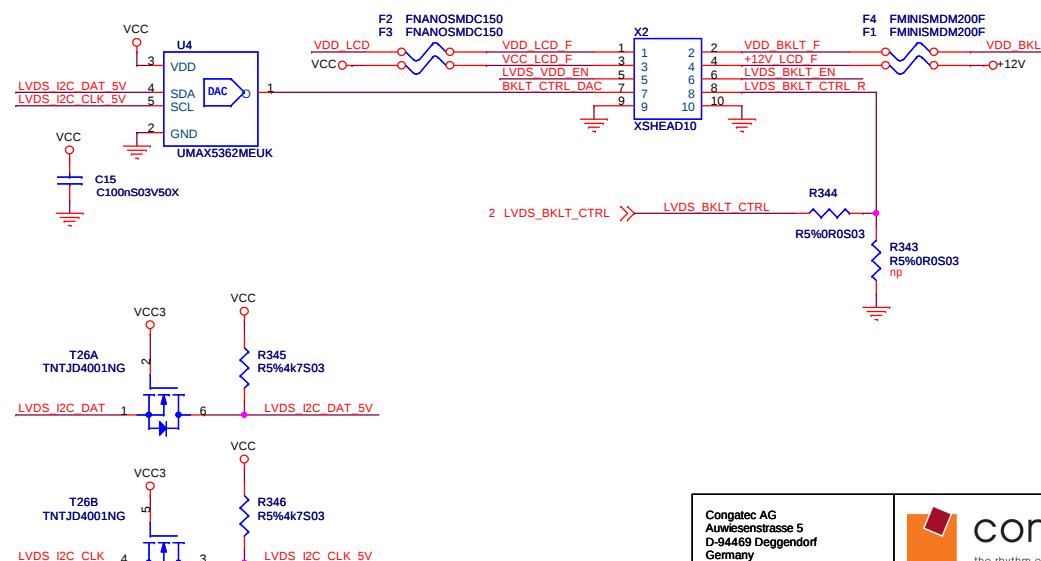
set jumper 1-2 for 12V backlight voltage (default)
set jumper 2-3 for 5V backlight voltage

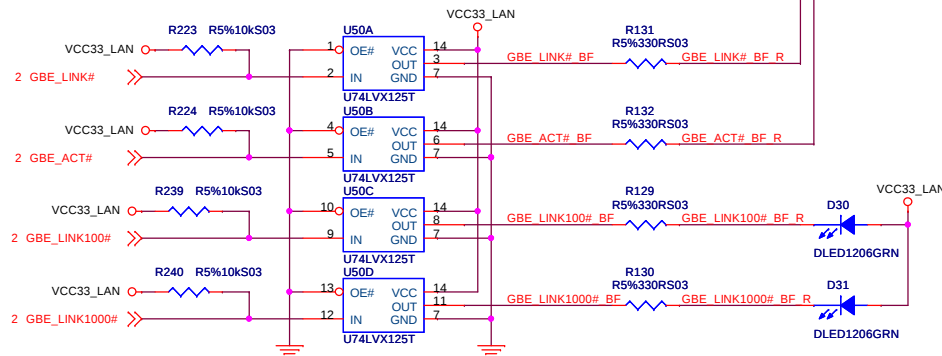
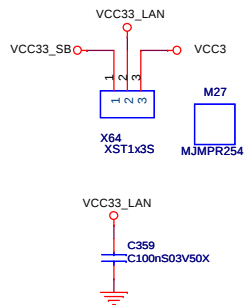
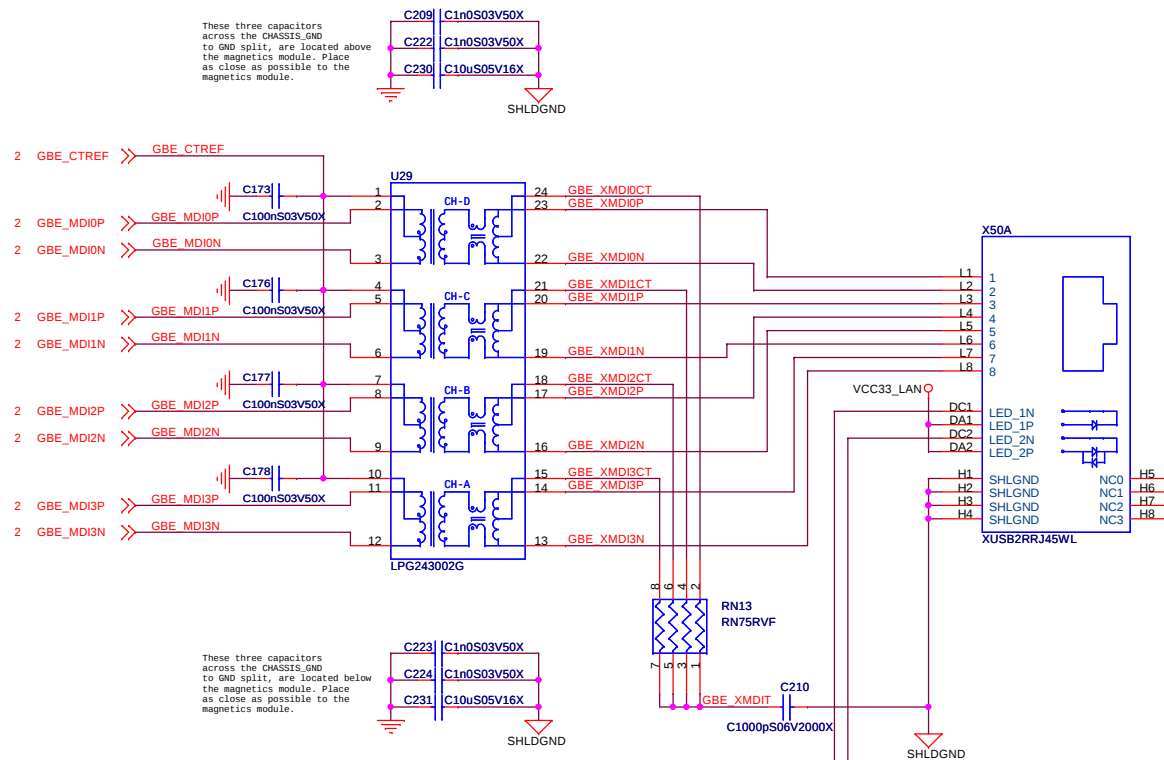


LCD



LCD / BKLT POWER





set jumper 1-2 if LAN controller is powered from standby voltage (default)
set jumper 2-3 if LAN controller is powered from main voltage

Congatec AG Auwiesenstrasse 5 D-94469 Deggendorf Germany				congatec the rhythm of embedded computing	
Title Ethernet					
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FS

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FU

FV

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LX

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MB

MC

MD

ME

MF

MG

MH

MI

MJ

MK

ML

MM

MN

MO

MP

MQ

MR

MS

MT

MU

MV

MW

MX

MY

MZ

NA

NB

NC

ND

NE

NF

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NH

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NK

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NM

NN

NO

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NT

NU

NV

NW

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NY

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OF

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5 4 3 2 1

RTC / CMOS BATTERY

2.13 BATT

BATT

C91 CST47uC16 np

D26 DBAT54A

R72 R5%1k0S03

BATT D

BATT R

M10 MBATTHOLD1

B1 BATT2032

PC BEEPER

D27 DBAT54A

VCC

M11 MPiezo1

PCBEEPER S

R102 R5%75RS03

C360 C100nS03V50X

PCBEEPER_T

T12 T2N7002A

17 PCBEEPER

R357 R5%47kS03

FAN CONTROL

VCC3

R12 R5%10kS03

3 FAN_PWMOUT

FAN_PWMOUT

T2 T2N7002A

VCC3

R26 R5%4k7S03

3 FAN_TACHOIN

FAN_TACHOIN

D15 DMBR130LSFT1

VCC_FAN_S

R17 R5%10kS03

FAN_PWMOUT_G

R18 R5%10kS03

FAN_PWMOUT_D

T7 TNTF6P02T3G

VCC_FAN_F

F6 FANANOSMDM075F

D14 DMBR130LSFT1

VCC_FAN

FAN_SENSE

X14 GNDH1 H1

VCC

SENSE

XFANHF06-3

+12V

X63 1 2 3

XST1x3S

M26 MJMPR254

set jumper 1-2 for 12V FAN (default)
set jumper 2-3 for 5V FAN

FEATURE

F10 FANANOSMDM075F

5V_SB_ALW

VCCFEA

F18 FANANOSMDM075F

R105 R5%330RS03

HLRFEA

X27 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

2.16 I2DAT

I2DAT

2.16 I2CLK

I2CLK

3 TX_CGBC

TX_CGBC

3 RX_CGBC

RX_CGBC

16,22 PS_ON#

PS_ON#

2,11,22 SUS_S3#

SUS_S3#

2 THRMTRIP#

THRMTRIP#

2 GPI1

GPI1

2,16 SUS_STAT#

SUS_STAT#

2 GPI2

GPI2

2 WDTRIG

WDTRIG

2 GPI3

GPI3

2,16 BATLOW#

BATLOW#

3,9,12 PEG_ENABLE#

PEG_ENABLE#

13 KBD_INH#

KBD_INH#

2,16,22 PWRBTN#

PWRBTN#

2,16,22 PWRBTN#

PWRBTN#

XST2x20S

2 HDDLED

HDDLED

2 SMBCLK_SB

SMBCLK_SB

2 SMBDAT_SB

SMBDAT_SB

2 GPO0

GPO0

2 GPO1

GPO1

2 GPO2

GPO2

2 GPO3

GPO3

2 SMBALRT#

SMBALRT#

2 SUS_S4#

SUS_S4#

2,16 GPIO

GPIO

2,16 SUS_S5#

SUS_S5#

2 THRM#

THRM#

2,16 PCI_M66EN

PCI_M66EN

2,13,14 WAKE1#

WAKE1#

2,13,14 PEG_LANE_RV#

PEG_LANE_RV#

2,22 SYS_RESET#

SYS_RESET#

2,22 PWGIN

PWGIN

PWR LED

R143 R5%330RS03

VCC

PWR_LED

X73 1 2

XST1x2S

R100 R5%1k0S03

PCI_M66EN

RESET

M12 1 2 3 4

MPUSHBTNSMD

SYS_RESET#

SYS_RESET# 2

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Title
BATT SPK Feature FAN

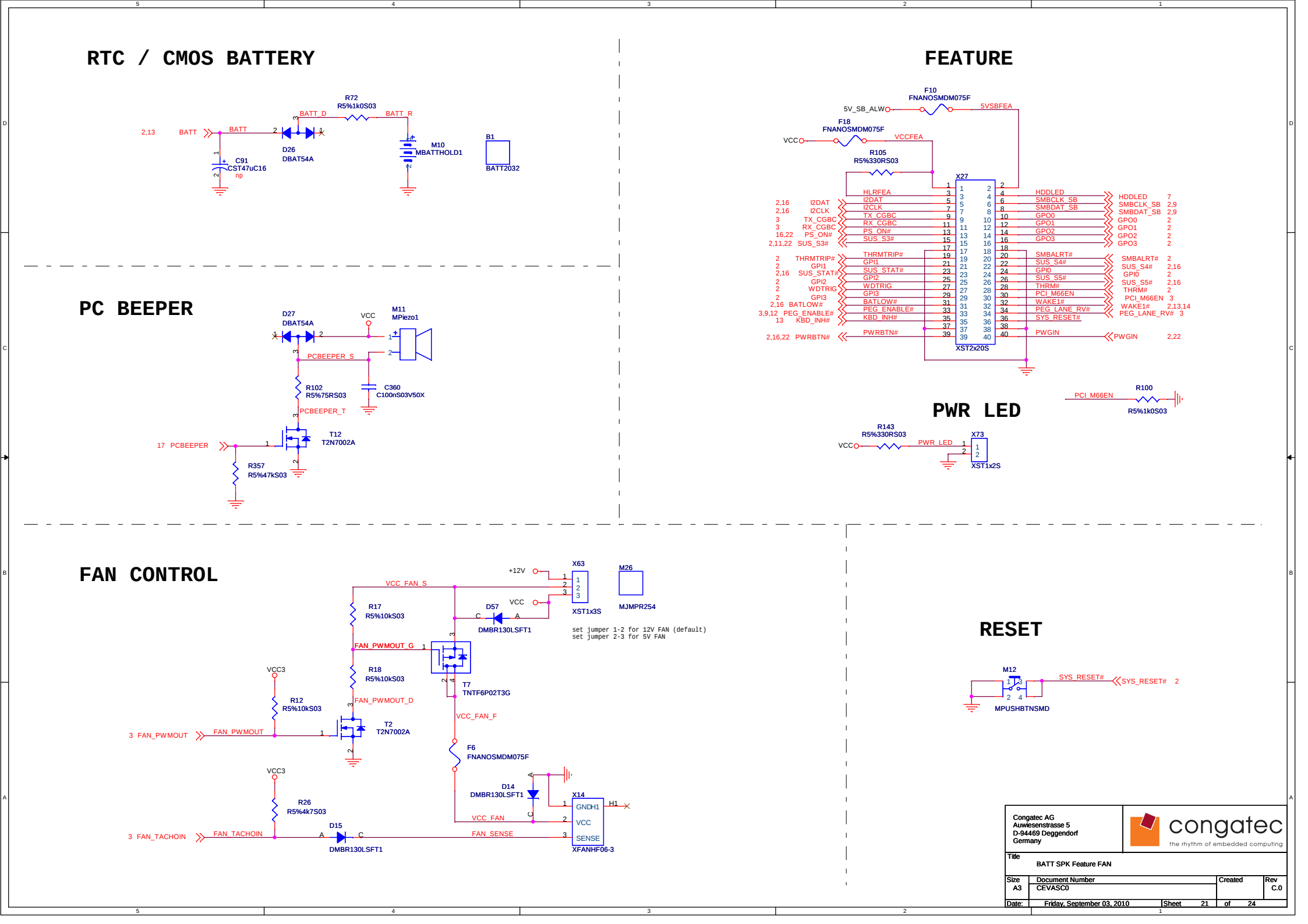
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Document Number
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Friday, September 03, 2010

Rev
C.0

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5 4 3 2 1



5 4 3 2 1

RTC / CMOS BATTERY

2.13 BATT

PC BEEPER

17 PCBEEPER

FAN CONTROL

3 FAN_PWMOUT

3 FAN_TACHOIN

FEATURE

2.16 I2DAT

2.16 I2CLK

3 TX_CGBC

3 RX_CGBC

16,22 PS_ON#

2,11,22 SUS_S3#

2 THRMTRIP#

2 GPI1

2,16 SUS_STAT#

2 GPI2

2 WDTRIG

2 GPI3

2,16 BATLOW#

3,9,12 PEG_ENABLE#

13 KBD_INH#

2,16,22 PWRBTN#

2 HDDLED

4 SMBCLK_SB

6 SMBCLK_SB

8 SMBDAT_SB

10 GPO0

12 GPO1

14 GPO2

16 GPO3

18 SMBALRT#

20 SUS_S4#

22 SUS_S4#

24 GPI0

26 SUS_S5#

28 THRM#

30 PCI_M66EN

32 WAKE1#

34 PEG_LANE_RV#

36 SYS_RESET#

38 PWGIN

40 PWGIN

PWR LED

PCI_M66EN

RESET

2

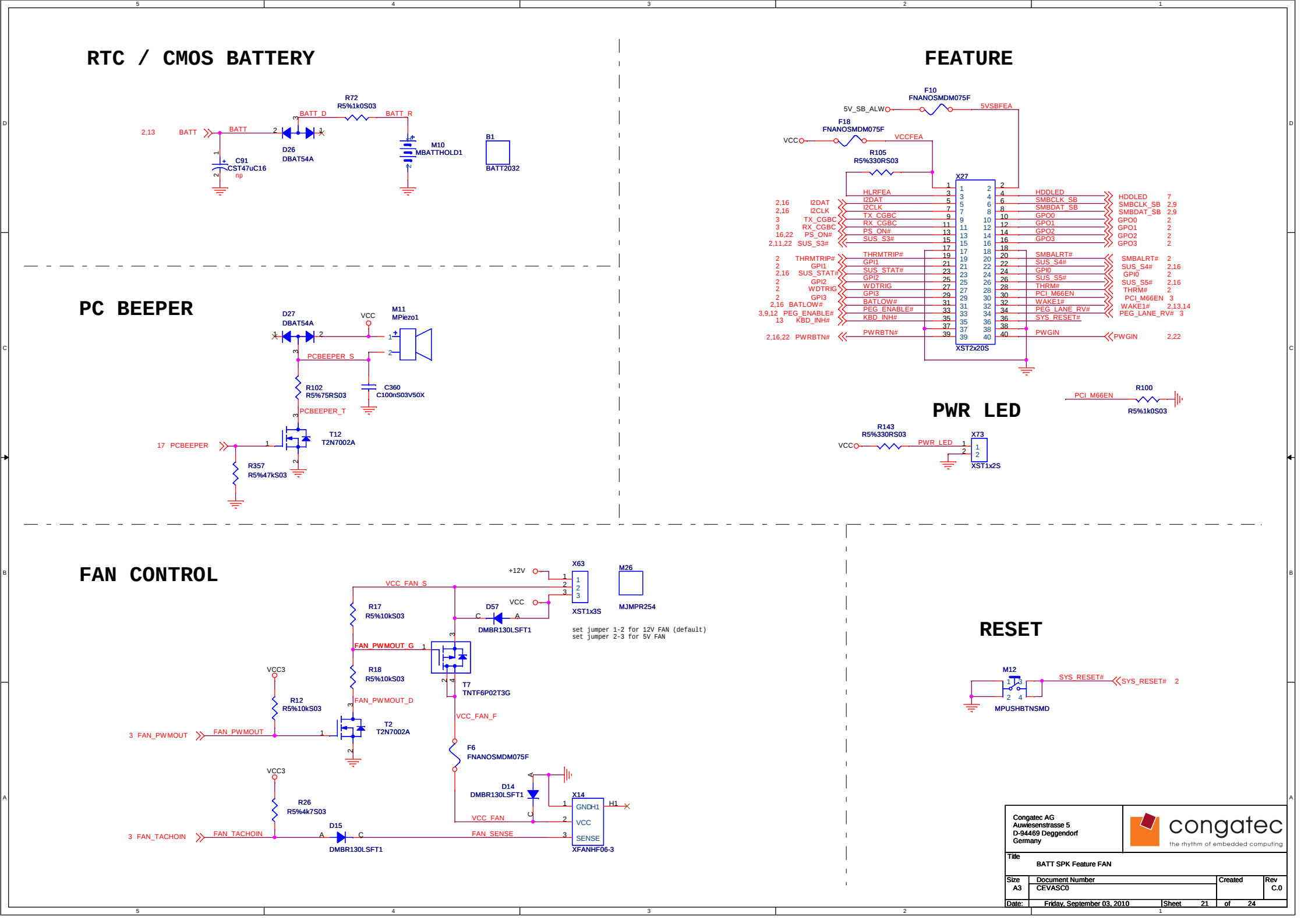
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Title: BATT SPK Feature FAN

Size A3 Document Number CEVASCO Created Rev C.0

Date: Friday, September 03, 2010 Sheet 21 of 24



5 4 3 2 1

RTC / CMOS BATTERY

2.13 BATT

BATT

C91 CST47uC16 np

D26 DBAT54A

BATT D

R72 R5%1k0S03

BATT R

M10 MBATTHOLD1

B1 BATT2032

PC BEEPER

D27 DBAT54A

VCC

M11 MPiezo1

PCBEEPER S

R102 R5%75RS03

C360 C100nS03V50X

PCBEEPER_T

T12 T2N7002A

17 PCBEEPER

R357 R5%47kS03

FAN CONTROL

VCC3

R12 R5%10kS03

3 FAN_PWMOUT

FAN_PWMOUT

T2 T2N7002A

VCC3

R26 R5%4k7S03

3 FAN_TACHOIN

FAN_TACHOIN

D15 DMBR130LSFT1

VCC_FAN_S

R17 R5%10kS03

FAN_PWMOUT_G

R18 R5%10kS03

FAN_PWMOUT_D

T7 TNTF6P02T3G

VCC_FAN_F

F6 FANANOSMDM075F

D14 DMBR130LSFT1

VCC_FAN

FAN_SENSE

X14 GNDH1 H1

VCC

SENSE

XFANHF06-3

+12V

X63

1 2 3

XST1x3S

M26 MJMPR254

set jumper 1-2 for 12V FAN (default)
set jumper 2-3 for 5V FAN

FEATURE

F10 FANANOSMDM075F

5V_SB_ALW

VCCFEA

F18 FANANOSMDM075F

R105 R5%330RS03

HLRFEA

X27

2.16 I2DAT

I2DAT

2.16 I2CLK

I2CLK

3 TX_CGBC

TX_CGBC

3 RX_CGBC

RX_CGBC

16,22 PS_ON#

PS_ON#

2,11,22 SUS_S3#

SUS_S3#

2 THRMTRIP#

THRMTRIP#

2 GPI1

GPI1

2,16 SUS_STAT#

SUS_STAT#

2 GPI2

GPI2

2 WDTRIG

WDTRIG

2 GPI3

GPI3

2,16 BATLOW#

BATLOW#

3,9,12 PEG_ENABLE#

PEG_ENABLE#

13 KBD_INH#

KBD_INH#

2,16,22 PWRBTN#

PWRBTN#

2,16,22 PWRBTN#

PWRBTN#

XST2x20S

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

HDDLED

SMBCLK_SB

SMBDAT_SB

GPO0

GPO1

GPO2

GPO3

SMBALRT#

SUS_S4#

GPI0

SUS_S5#

THRM#

PCI_M66EN

WAKE1#

PEG_LANE_RV#

SYS_RESET#

PWGIN

2.22

PWR LED

R143 R5%330RS03

VCC

PWR_LED

X73

1 2

XST1x2S

PCI_M66EN

R100 R5%1k0S03

RESET

M12

1 2 3 4

MPUSHBTNSMD

SYS_RESET#

SYS_RESET# 2

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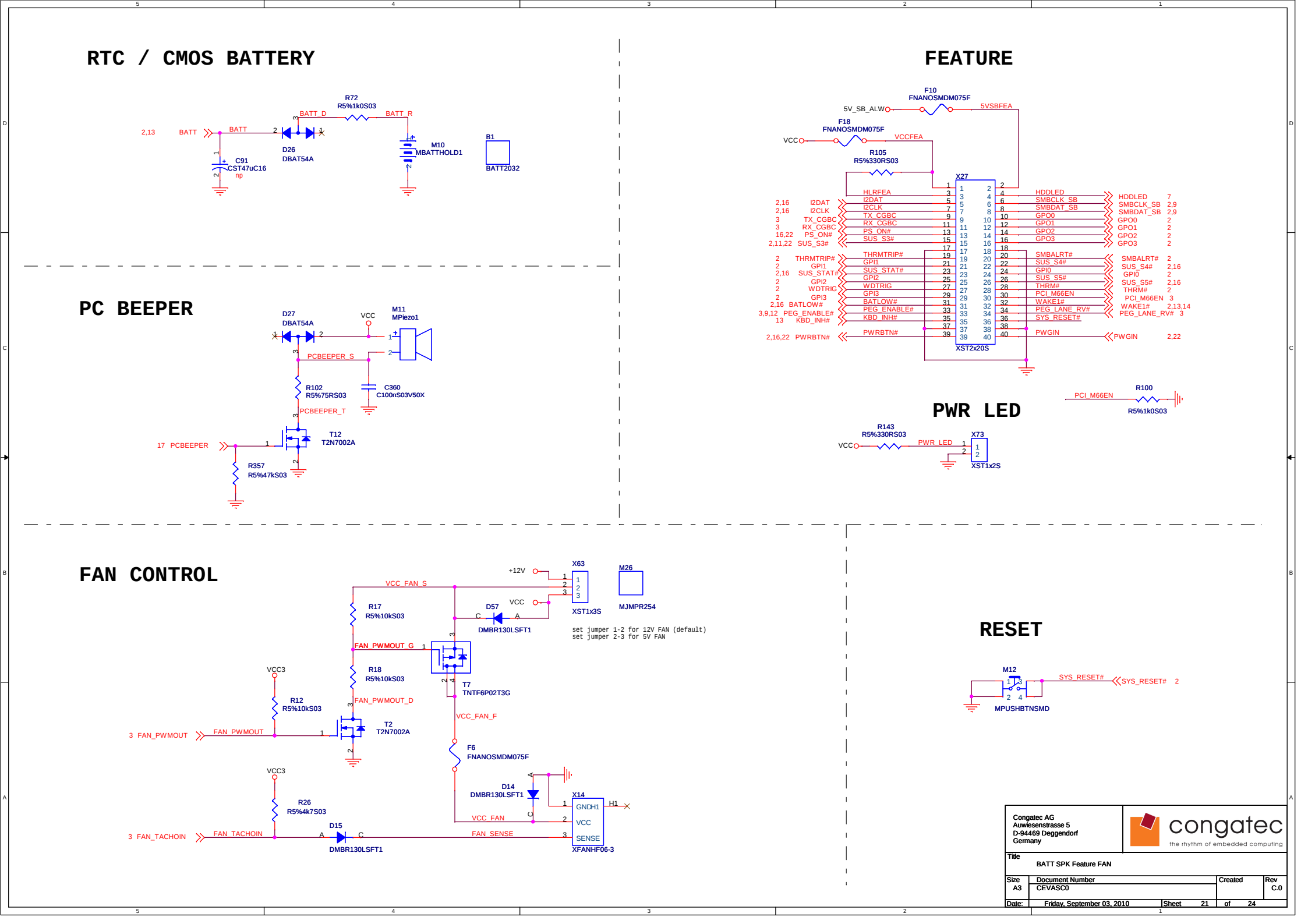
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Title
BATT SPK Feature FAN

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Date: Friday, September 03, 2010 Sheet 21 of 24

5 4 3 2 1



5 4 3 2 1

RTC / CMOS BATTERY

2.13 BATT

BATT

C91 CST47uC16 np

D26 DBAT54A

BATT D

R72 R5%1k0S03

BATT R

M10 MBATTHOLD1

B1 BATT2032

PC BEEPER

D27 DBAT54A

VCC

M11 MPiezo1

PCBEEPER S

R102 R5%75RS03

C360 C100nS03V50X

PCBEEPER_T

T12 T2N7002A

17 PCBEEPER

R357 R5%47kS03

FAN CONTROL

VCC3

R12 R5%10kS03

3 FAN_PWMOUT

FAN_PWMOUT

T2 T2N7002A

VCC3

R26 R5%4k7S03

3 FAN_TACHOIN

FAN_TACHOIN

D15 DMBR130LSFT1

VCC_FAN_S

R17 R5%10kS03

FAN_PWMOUT_G

R18 R5%10kS03

FAN_PWMOUT_D

T7 TNTF6P02T3G

VCC_FAN_F

F6 FANANOSMDM075F

D14 DMBR130LSFT1

VCC_FAN

FAN_SENSE

X14 GNDH1 H1

VCC

SENSE

XFANHF06-3

+12V

X63

1 2 3

XST1x3S

M26 MJMPR254

set jumper 1-2 for 12V FAN (default)
set jumper 2-3 for 5V FAN

FEATURE

F10 FANANOSMDM075F

5V_SB_ALW

VCCFEA

F18 FANANOSMDM075F

R105 R5%330RS03

HLRFEA

X27

2.16 I2DAT

I2DAT

2.16 I2CLK

I2CLK

3 TX_CGBC

TX_CGBC

3 RX_CGBC

RX_CGBC

16,22 PS_ON#

PS_ON#

2,11,22 SUS_S3#

SUS_S3#

2 THRMTRIP#

THRMTRIP#

2 GPI1

GPI1

2,16 SUS_STAT#

SUS_STAT#

2 GPI2

GPI2

2 WDTRIG

WDTRIG

2 GPI3

GPI3

2,16 BATLOW#

BATLOW#

3,9,12 PEG_ENABLE#

PEG_ENABLE#

13 KBD_INH#

KBD_INH#

2,16,22 PWRBTN#

PWRBTN#

2,16,22 PWRBTN#

PWRBTN#

XST2x20S

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

HDDLED

SMBCLK_SB

SMBDAT_SB

GPO0

GPO1

GPO2

GPO3

SMBALRT#

SUS_S4#

GPI0

SUS_S5#

THRM#

PCI_M66EN

WAKE1#

PEG_LANE_RV#

SYS_RESET#

PWGIN

2.22

PWR LED

R143 R5%330RS03

VCC

PWR_LED

X73

1 2

XST1x2S

PCI_M66EN

R100 R5%1k0S03

RESET

M12

1 2 3 4

MPUSHBTNSMD

SYS_RESET#

sys_reset# 2

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Title
BATT SPK Feature FAN

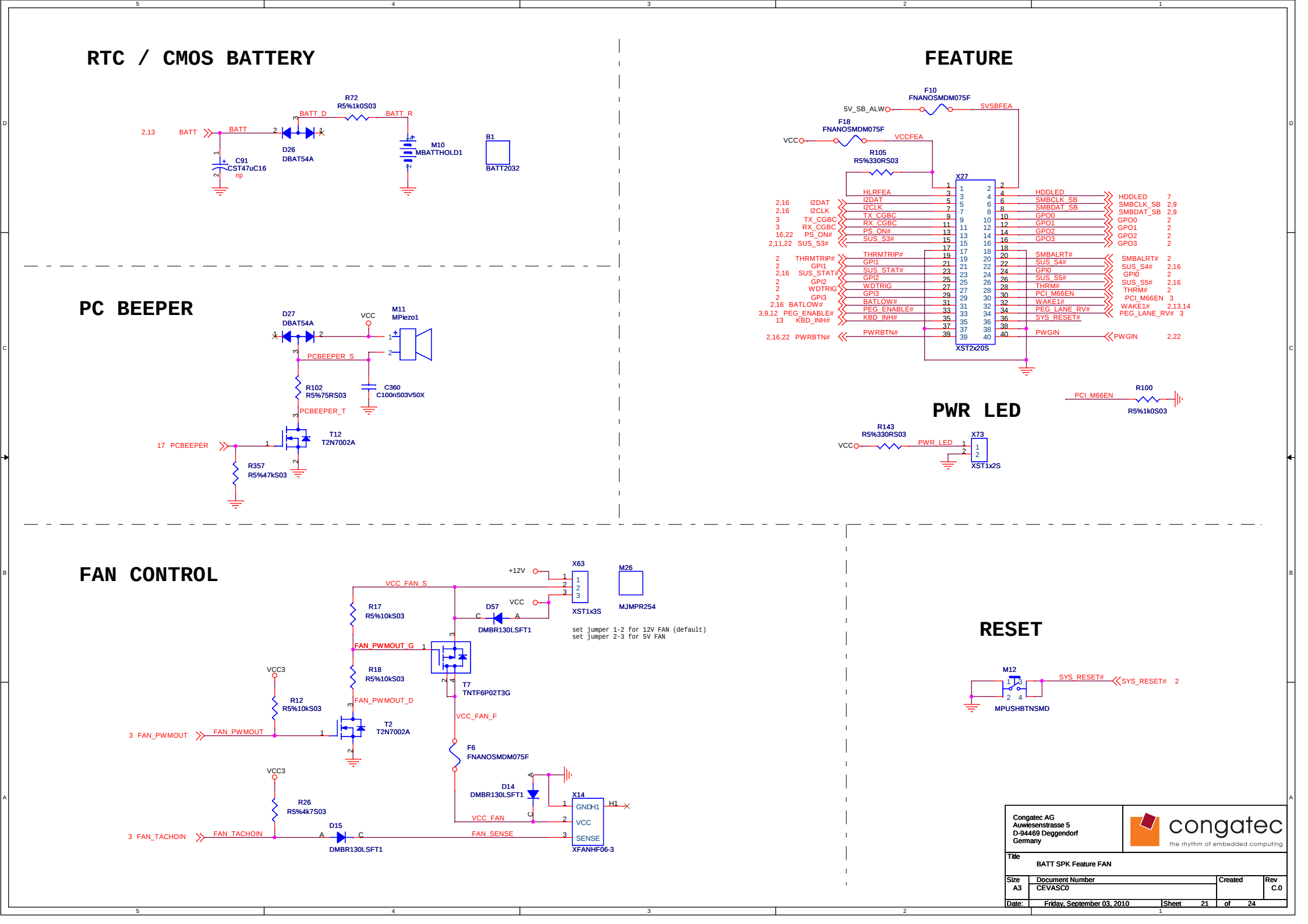
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Document Number
CEVASCO

Created
Friday, September 03, 2010

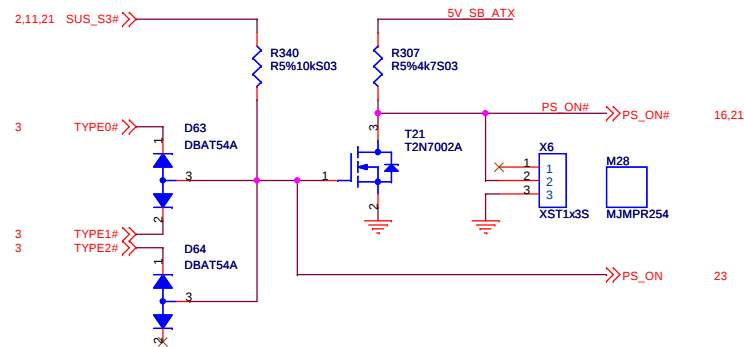
Rev
C.0

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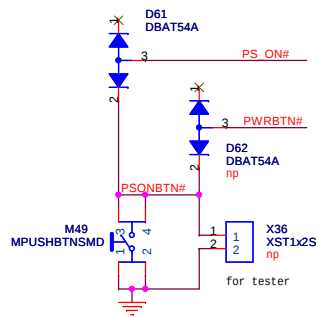
5 4 3 2 1



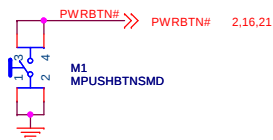
MODE1: ATX mode with jumper X6 1-2, X7 1-2, PWRBTN in function
 MODE2: AT mode with jumper X6 2-3, X7 2-3, always on
 MODE3: pseudo ATX mode with 12V only, jumper X6 1-2, X7 2-3, PS_ON# button in function
 (tester mode; not approved)



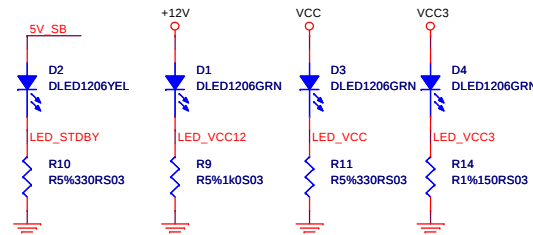
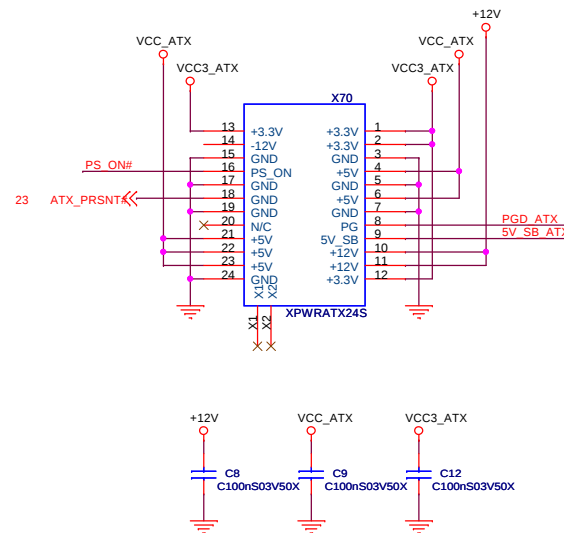
PS_ON# BUTTON for pseudo ATX mode



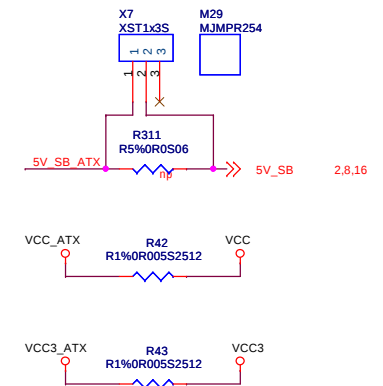
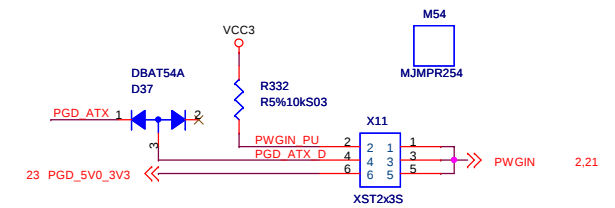
POWER BUTTON



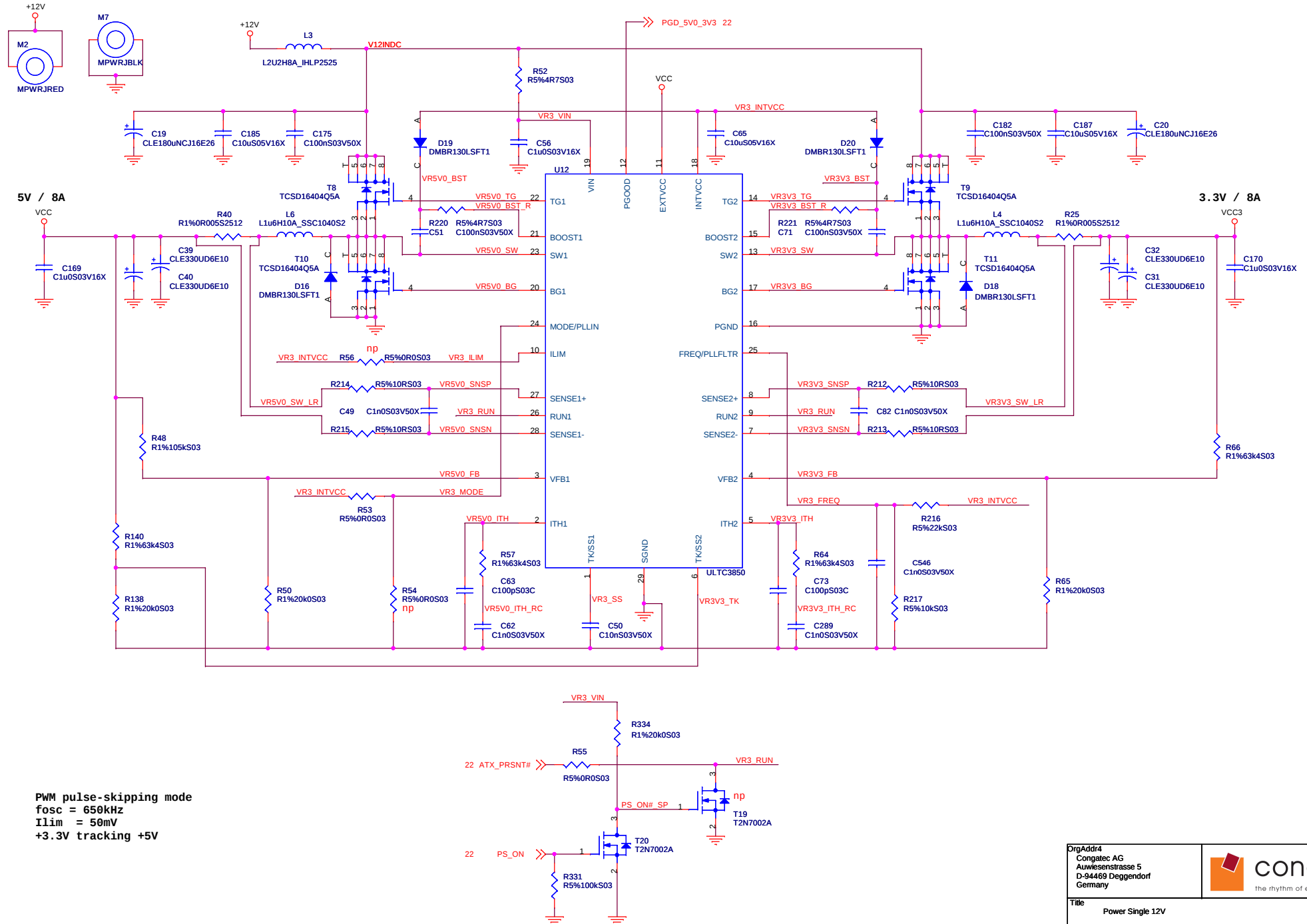
ATX POWER



SET 1-2: PU on PWGIN; ONLY FOR DEBUG - MODULE HAS INTEGRATED PU
SET 3-4: PWGIN from ATX (DEFAULT)
 SET 5-6: PWGIN from DCDC (12V PWR IN MODE); DONT SET IF ATX PSU IS USED



SINGLE 12V POWER



PWM pulse-skipping mode
fosc = 650kHz
Ilim = 50mV
+3.3V tracking +5V

Revision History

Rev. X.0	17.05.06	HMA	0	design created
Rev. A.0	30.10.06	HMA	all	changed footprints to have in general 0603 only
			4	corrected C239 to 10p
			8	added pullups to CLKREQ#s of express clock buffer
			10	added MUXer to switch between PCIe lanes 2 and 5
			12	changed standby supply on Super IO to SV_SB_ALW
				added PD to signal PSIN
				added jumper to switch between S3 and S5 for ATX power control
				added circuit to notify wrong module
			12,13,14	corrected floppy connection
			14	added 3.3V pullups for SMSC floppy connection
			16	added jumper to chose between SDIN0 and SDIN2 for codec
				added fuses to HDA connector to be consistent with UL
			17	corrected RN17 to 150R
				added diode to DDC PUS to prevent leakage
			3,20	signal PP_TPM added to COM express pinout and added feature jumper
			19	removed jumper for VCC and WE# from CF connector
				modified jumper setting for 10/100 Ethernet option
				corrected connection of IDE LED
			21	modified circuit to get better performance
Rev. B.0	04.11.08	WKA/PK0		major changes: change AC97 to HDA, POST CPLD with LPC, lot of minor changes and bugfixes
Rev. C.0	20.08.10	KDA	1	changed COMe mouting holes to COMe 8mm speacers
			2	added COMe SPI connection; remove some COMe VCC_12V pins according COMe spec 2.0
			3	added DDPD_CTRL connection
			4	added PD 10k to reset buffer outputs
			6	changed USB ESD to NXP IP4220CZ6
			11/12	changed jumper's to dual DIP switch for PEG Enable and ExpressCard/miniPCIe port selection
			12	added DDPD_CTRL header
			13/14	added BATT connection to SuperIOs
			15	changed KB/MS ESD to NXP IP4220CZ6
			16	added SPI BIOS FLASH; added isolation buffer to BISO_DIS0#; added BIOS_DIS1# to DIP switch
			17	added DIP switch for disable carrier HDA codec and PC beeper; updated PCB footprint for audiojack
			21	added PWR LED header
			22	added COMe PWGIN jumper selection