TQMLS102xA
Preliminary User's Manual

TQMLS102xA UM 0003
21.10.2015

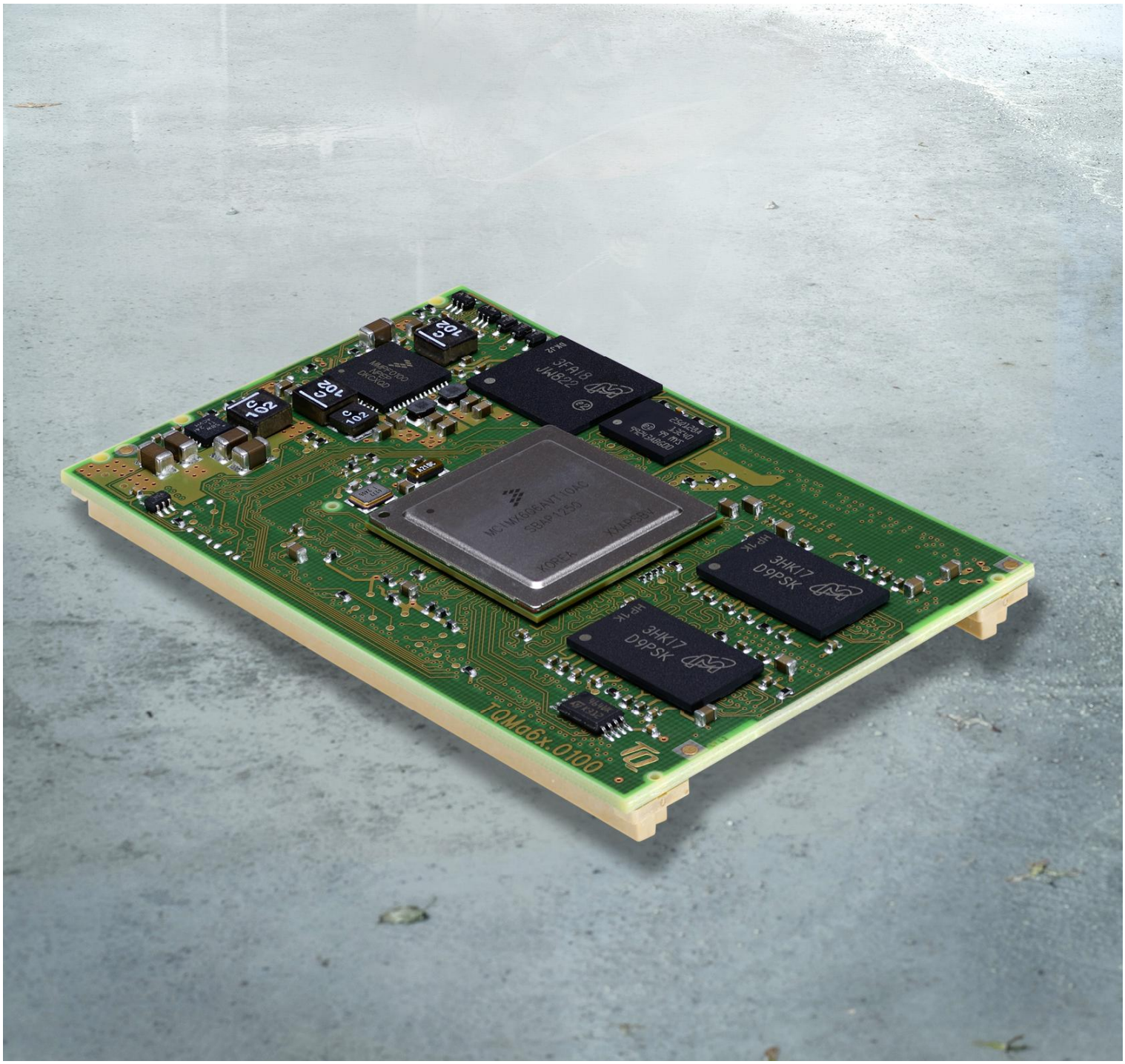


TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

TABLE DIRECTORY

ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	13.04.2015	Petz		First issue (German / English)
0002	26.05.2015	Petz		Document translated
0003	21.10.2015	Petz	All	Complete rework

1. ABOUT THIS MANUAL

1.1 Copyright and licence expenses

This Preliminary User's Manual may not be copied, reproduced, translated, changed or distributed, completely or partially in electronic, machine readable, or in any other form without the written consent of TQ-Systems GmbH.

The drivers and utilities for the components used as well as the BIOS are subject to the copyrights of the respective manufacturers. The licence conditions of the respective manufacturer are to be adhered to.

Boot loader-licence expenses are paid by TQ-Systems GmbH and are included in the price.

Licence expenses for the operating system and applications are not taken into consideration and must be separately calculated / declared.

1.2 Registered trademarks

TQ-Systems GmbH aims to adhere to the copyrights of all the graphics and texts used in all publications, and strives to use original or license-free graphics and texts.

All the brand names and trademarks mentioned in the publication, including those protected by a third party, unless specified otherwise in writing, are subjected to the specifications of the current copyright laws and the proprietary laws of the present registered proprietor without any limitation. One should conclude that brand and trademarks are rightly protected by of a third party.

1.3 Disclaimer

TQ-Systems GmbH does not guarantee that the information in this Preliminary User's Manual is up-to-date, correct, complete or of good quality. Nor does TQ-Systems GmbH assume guarantee for further usage of the information. Liability claims against TQ-Systems GmbH, referring to material or non-material related damages caused, due to usage or non-usage of the information given in the Preliminary User's Manual, or due to usage of erroneous or incomplete information, are exempted, as long as there is no proven intentional or negligent fault of TQ-Systems GmbH.

TQ-Systems GmbH explicitly reserves the rights to change or add to the contents of this Preliminary User's Manual or parts of it without special notification.

1.4 Imprint

TQ-Systems GmbH
Gut Delling, Mühlstraße 2
D-82229 Seefeld
Tel: +49 (0) 8153 9308–0
Fax: +49 (0) 8153 9308–134
Email: info@tq-group.com
Web: http://www.tq-group.com/

1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMLS102xA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- Circuit diagram MBLS102xA
- Documentation of boot loader U-Boot (http://www.denx.de/wiki/U-Boot/Documentation)
- Documentation of PTXdist (http://www.ptxdist.de)

2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the TQMLS102xA, and refers to some software settings.
A certain derivative of the TQMLS102xA does not necessarily provide all features described in this Preliminary User's Manual.
This Preliminary User's Manual does also not replace the Freescale Reference Manuals of the CPU.
The TQMLS102xA is a universal Minimodule based on the Freescale Layerscape CPU LS1020A / LS1021A / LS1022A.
The Layerscape CPU is a Dual Cortex A7 with QorIQ technology.
The TQMLS102xA extends the TQ-Systems GmbH product range and offers an outstanding computing performance.
A suitable CPU derivative (LS1020A, LS1021A, and LS1022A) can be selected for each requirement.

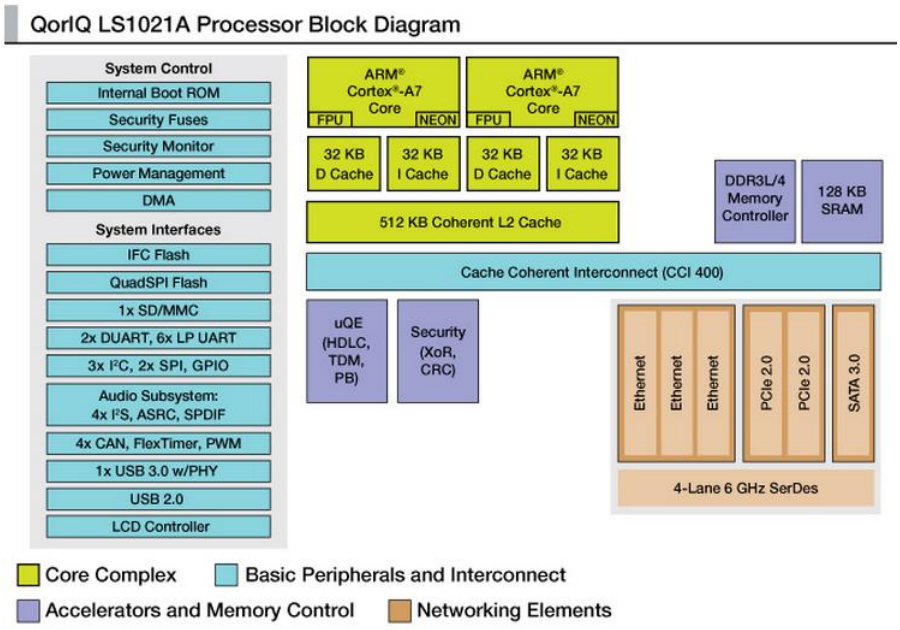


Illustration 1: Block diagram LS1021A (simplified)
(Source: Freescale)

All essential CPU pins are routed to the connectors of the TQMLS102xA.
There are therefore no restrictions for customers using the TQMLS102xA with respect to an integrated customised design.
Furthermore all components required for the CPU to function like DDR3L SDRAM, eMMC, power supply and power management are integrated on the TQMLS102xA.
The main characteristics of the TQMLS102xA are:

- CPU derivatives LS1020A, LS1021A, LS1022A
- DDR3L SDRAM incl. ECC
- eMMC and NOR flash
- Single Supply Voltage 3.3 V
- On-board RTC / EEPROM / Temperature sensor
- Extended Power Management
- Simple boot source selection

The MBLS102xA is used as a carrier board for the TQMLS102xA.

3. OVERVIEW

3.1 Block diagram

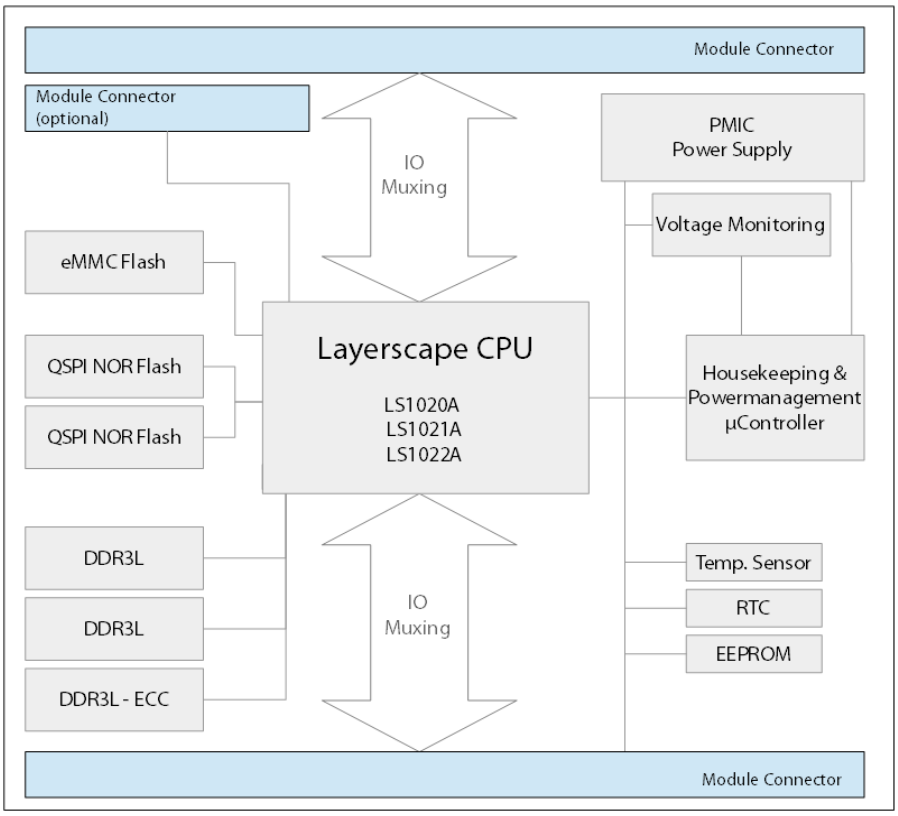


Illustration 2: Block diagram TQMLS102xA (simplified)

3.2 System components

The TQMLS102xA provides the following key functions and characteristics:

- Layerscape CPUs LS1020A / LS1021A / LS1022A
- Oscillators for CPU and DDR3L
- Reset structure and Power-Sequencing
- Power supply by PMIC
- Voltage supervision of all voltages
- Housekeeping / Power management µController (PMC)
- Temperature sensor
- RTC
- EEPROM
- DDR3L SDRAM incl. ECC
- QSPI NOR flash
- eMMC
- Three connectors (280 pins)

All essential CPU pins are routed to the connectors of the TQMLS102xA.
There are therefore no restrictions for customers using the TQMLS102xA with respect to an integrated customised design.
All versions of the TQMLS102xA are fully pin-compatible and therefore interchangeable.
The functionality of the different TQMLS102xA is mainly determined by the features provided by the respective CPU.

4. ELECTRONICS SPECIFICATION

The information in this Preliminary User's Manual is only valid in connection with the boot loader adapted for the TQMLS102xA, which is preinstalled on every TQMLS102xA (see also section 7) and the BSP provided by TQ-Systems GmbH.

4.1 CPU

4.1.1 RCW Source selection

Die CPU permits to store the RCW in the eSDHC, QSPI and several parallel flashes. See QorIQ LS1021A Reference Manual (1).
On the TQMLS102xA the RCW source is selected and time-controlled actively driven by the power management controller (PMC).
No external pin strapping is required.

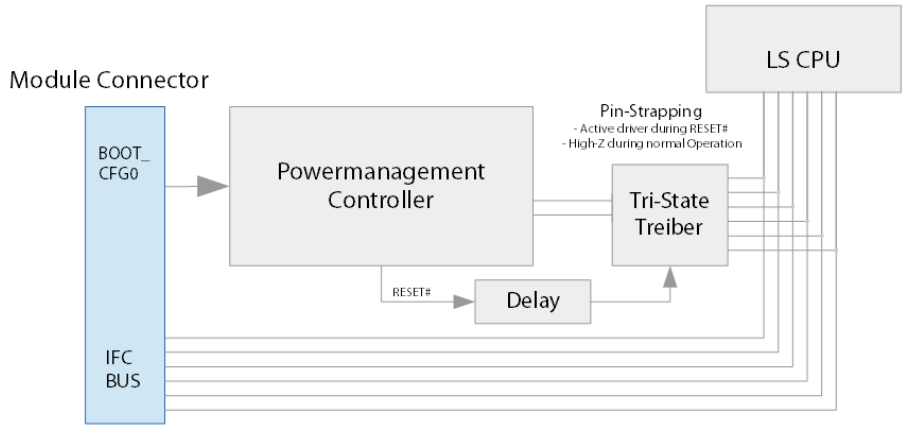


Illustration 3: Block diagram RCW source selection

The signal BOOT_CFG0 selects the boot source.

Table 2: RCW source selection

BOOT-CFG0	RCW Source	Pin strapping RCW[0:8]
Low	eSDHC	0 0100 0000
High	QSPI	0 0100 0100

A 10 kΩ pull-down at BOOT_CFG0 is assembled on the TQMLS102xA by default.
After the Power-Up of the TQMLS102xA the Power Management Controller applies the pin strapping.
The RESET# signal switches the drivers to high-impedance with a delay of +3 SYSCLOCKs, and thus removes the pin strapping from the bus.

4.1.2 RCW Word

The RCW can be taken from the QorIQ LS1021A Reference Manual (1).

4.1.3 Clock supply

The clock supply on the TQMLS102xA corresponds to the structure „Multiple Reference clocking“, described in the QorIQ LS1021A Reference Manual (1):

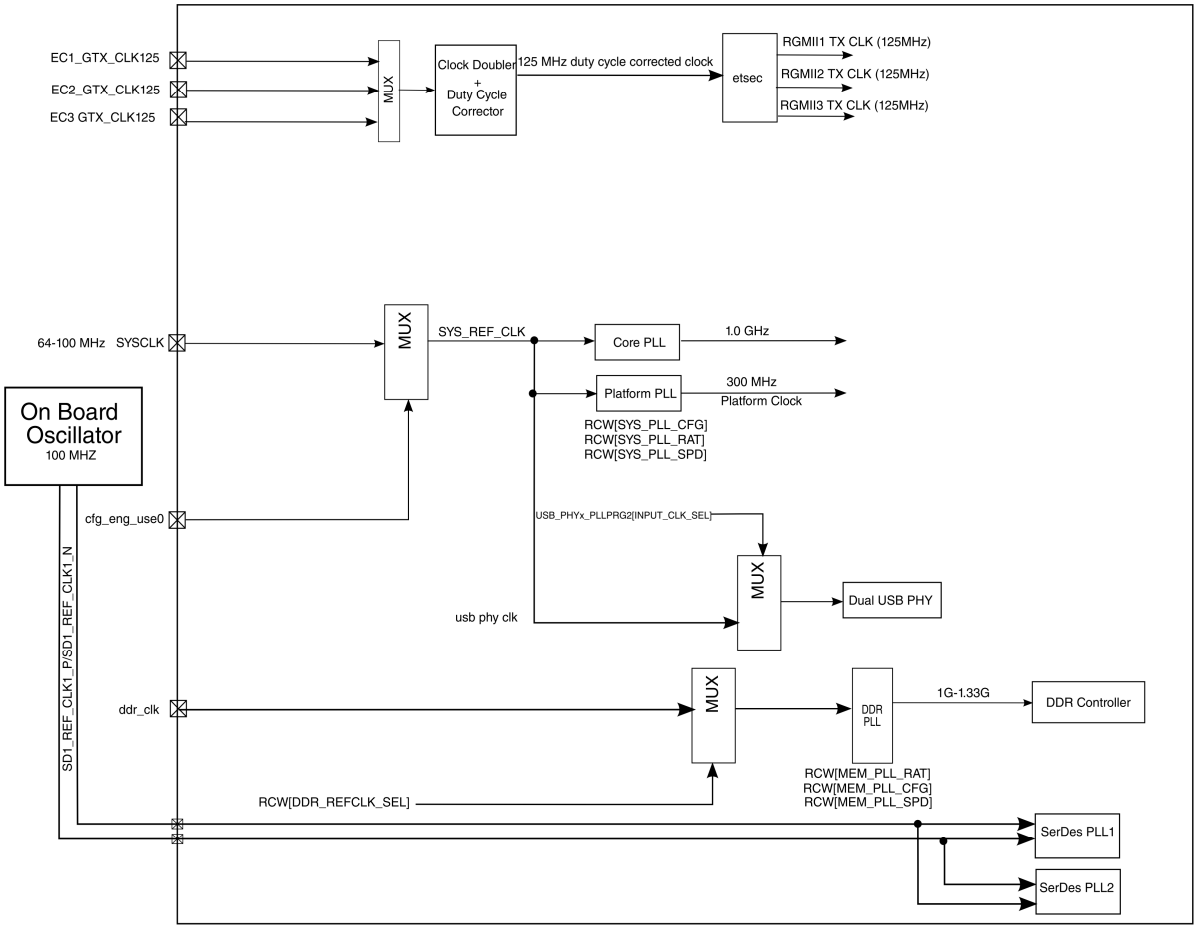


Illustration 4: Block diagram clock generation
(Source: Freescale)

- Cfg_eng_use0 is pulled “low” by the pin strapping. Thus configured to Single-Ended SYSCLK.
- SYSCLK = 100 MHz
- DDRCLK provides two options:
  - Same clock as SYSCLK (default)
  - 66.666 MHz clock independent from SYSCLK (placement option)
- ECx_GTX_CLK125 is not generated on the TQMLS102xA, has to be generated externally.
- Differential SERDES clocks are not generated on the TQMLS102xA, have to be generated externally.

4.1.4 Power Modes

- LPM20 (Sleep Mode)
- LPM35 (Deep Sleep Mode)

Deep Sleep is an especially efficient energy saving mode (LPM35), a variation of the LPM20 were parts of the Core supply are switched off.

The transition in the Deep Sleep is a complicated multistage process. It is partly controlled by software, and partly by a CPU internal State Machine, which also has to be configured by software. (Up to now this feature is not tested.)

4.1.5 JTAG

Die JTAG interface is routed to the connectors. The signals TDI, TCK, TMS, and TRST# have 10 kΩ pull-ups to OVDD (1.8 V).

Illustration 5: Block diagram JTAG interface

The signal JTAG_TRST# is connected with PORESET by resistors.

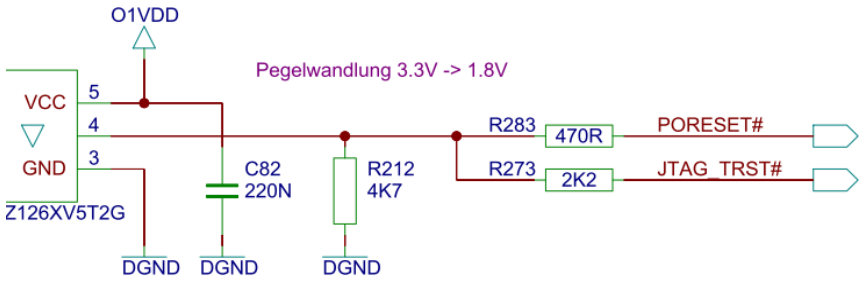


Illustration 6: Wiring of JTAG_TRST# and PORESET

JTAG_TRST# is pulled low together with PORESET#, but it can also be pulled low by an external debugger, while PORESET# remains unchanged.

4.2 Power supply

4.2.1 Input voltage

The TQMLS102xA requires a 3.3 V supply with a maximum tolerance ±3 %.

4.2.2 Power-Up sequencing

The TQMLS102xA complies with the sequencing specification defined by Freescale. It must however be ensured, that external components also comply with the sequencing specification.

External voltages have to be applied immediately or ideally after the TQMLS102xA is supplied with power.

The power management controller provides the signal PMC_PWR_STATUS at the connector of the TQMLS102xA, which can be used to activate external voltages. The signal is switched to High (3.3 V), when all voltages on the TQMLS102xA are stable.

4.3 Reset Structure

The following illustration shows the reset structure of the TQMLS102xA.

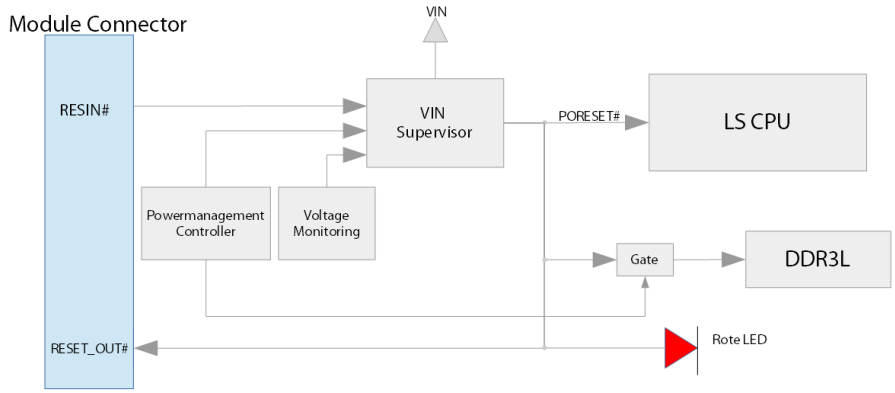


Illustration 7: Block diagram reset structure

- RESIN# keeps the TQMLS102xA in RESET#
- Further RESET# sources are:
  - VIN Power Fail
  - PMC Power Management Controller
  - Voltage Monitoring ADM1069

Table 3: RESET options

RESIN#	Reset function
Open	Self-reset possible. RESET_REQ# is switched through to RESIN# on the TQMLS102xA.
Pull-up <2.2 kΩ to VCC3V3	No self-reset possible. RESET_REQ# cannot override RESIN#.
Open Drain to DGND	Self-reset possible. A low at RESIN# triggers an external RESET.
Push/pull driver	No self-reset, but external RESET possible. Driver to High at RESIN# overrides RESET_REQ#.

4.4 Memory

4.4.1 SPI NOR Flash

Up to two QSPI NOR flash devices can be assembled on the TQMLS102xA.
The following illustration shows how the QSPI NOR flash devices are connected on the TQMLS102xA.

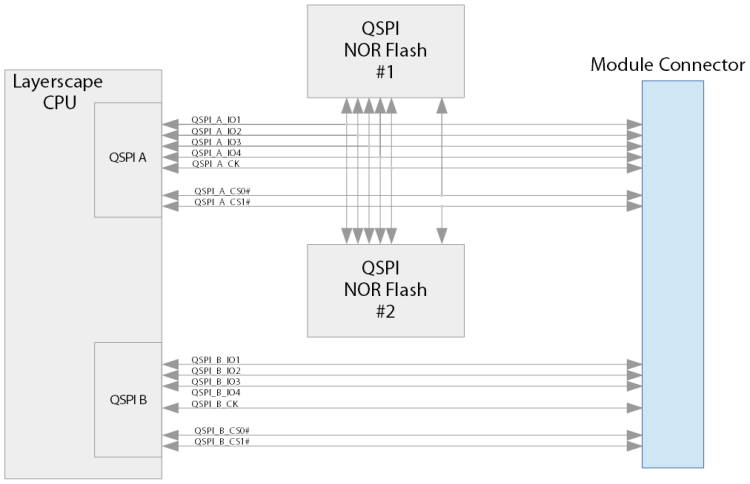


Illustration 8: Block diagram SPI NOR flash interface

- NOR flash #1 is the boot device; QSPI_A_CS0# is used as chip select.
- All QSPI signals are also routed to the connectors of the TQMLS102xA; see multiplexing options.

Table 4: SPI NOR flash

Manufacturer	Size	Remark
Micron	256 Mbit	–
Micron	512 Mbit	–
Micron	1024 Mbit	–
Micron	2048 Mbit	–

4.4.2 EEPROM

The EEPROM used is from the M24C64 series. It provides the following key features:

- 64 Kbit
- 3.3 V supply
- Max 400 kHz at the I²C bus

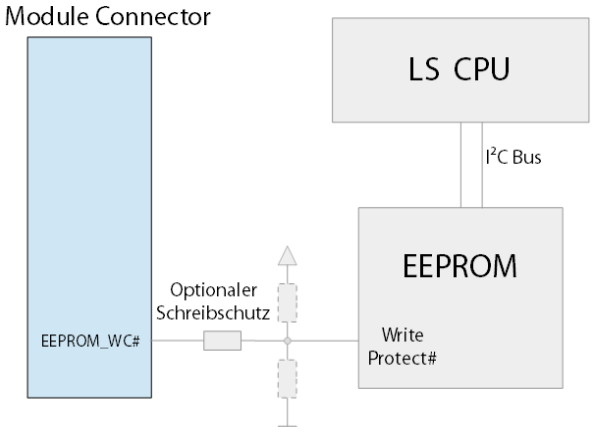


Illustration 9: Block diagram EEPROM interface

There are two options to control the write protection:

- External control by signal EEPROM_WC#, permanently pulled High or permanently pulled Low
- Default is a pull-down, thus read and write accesses are permitted

4.4.3 eMMC

The Layerscape CPUs LS102xA only provide one SDHC controller.
Therefore either the eMMC on the TQMLS102xA or an external SD card can be connected.

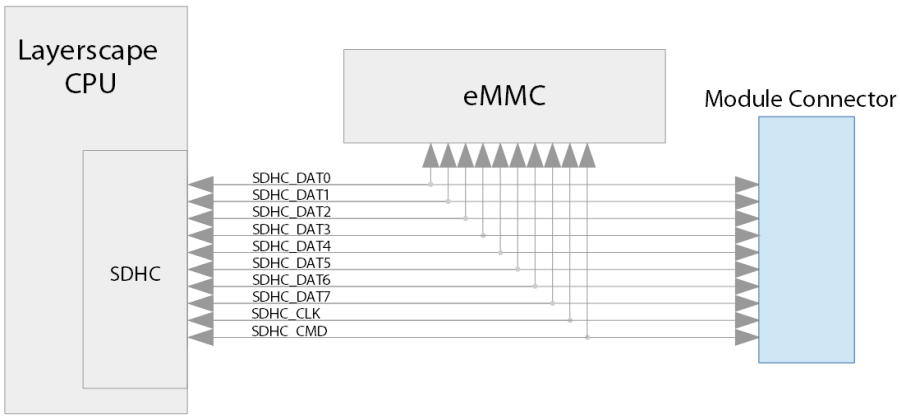


Illustration 10: Block diagram eMMC interface

The SDHC interface is routed to the connectors of the TQMLS102xA; see multiplexing options.
Micron series MTFC2GMDEA eMMC is used on the TQMLS102xA.
The following expansion stages are possible: 2 Gbyte, 4 Gbyte, 16 Gbyte or 32 Gbyte.

4.5 Temperature sensor

The temperature sensor SA56004EDP is assembled on the TQMLS102xA. The sensor measures its own housing temperature (ambient temperature) as well as a remote temperature. This remote temperature is the die temperature of the Layerscape CPU, using the internal PN junction.

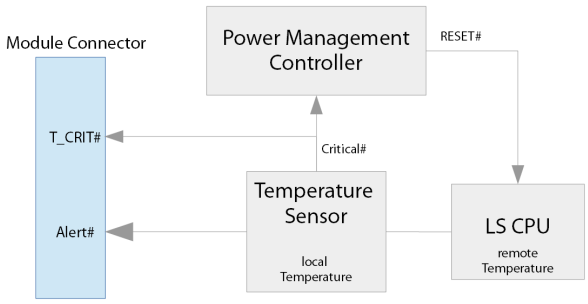


Illustration 11: Block diagram temperature sensor

- Accuracy remote: ±1 °C; accuracy local: ±2 °C
- I^2C bus (max. 400 kHz)
- 3.3 V supply
- The signal TEMP_ALERT# provides a warning with a programmed trigger level.
  It is directly routed to the connector of the TQMLS102xA.
  Since the signal has an Open Drain output, an external pull-up is required.
- The signal TEMP_CRIT_OUT# is also routed to the connector of the TQMLS102xA and signals the second programmed trigger level, which corresponds to the critical temperature. This signal is also read by the PMC, and triggers a system RESET#.
- The sensor is configured to T_CRIT_LOKAL = +95 °C and T_CRIT_REMOTE = +105 °C by the PMC during power-up. These values can later be overwritten by the boot loader U-Boot or by the application.

4.6 RTC

A PCF85063A RTC is available.

- 3.3 V or V_{BAT} supply
- Max 400 kHz at the I^2C bus

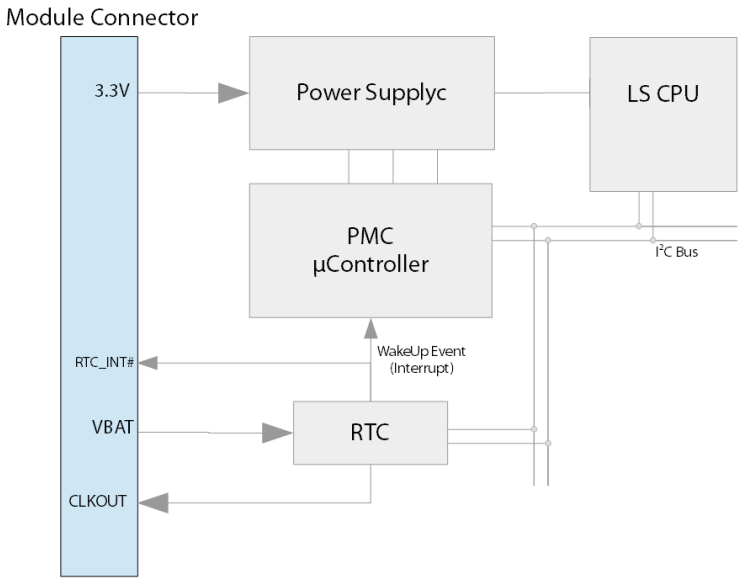


Illustration 12: Block diagram RTC interface

The signal CLKOUT of the RTC of controller is routed to the connector of the TQMLS102xA.
The interrupt signal RTC_INT# can be used in several ways.

- External use: Signal is accessible at the connector of the TQMLS102xA, pull-up to 3.3 V on the TQMLS102xA.
- When advanced power modes are used the TQMLS102xA can be put in a Stop Mode, and time-controlled restarted using the RTC interrupt.

The RTC is clocked with a 32.768 kHz crystal with an accuracy of ±20 ppm @ +25 °C. This corresponds to a deviation of 1.7 s/day.
The accuracy is ±30 ppm @ +85 °C. This corresponds to a deviation of 2.6 s/day.
The RTC is supplied by VBAT. A GoldCap® or a battery is required. The following figure shows the wiring on the TQMLS102xA:

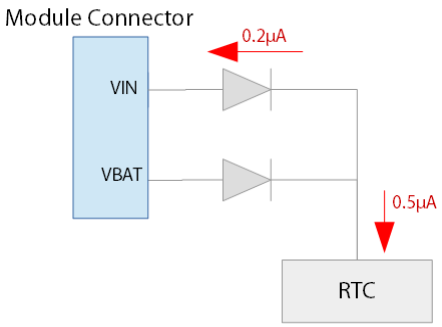


Illustration 13: Block diagram RTC buffering interface

4.7 I²C Bus

The I²C devices on the TQMLS102xA are connected to the I2C_1 bus, since the I2C_1 bus is independent of the multiplexing.

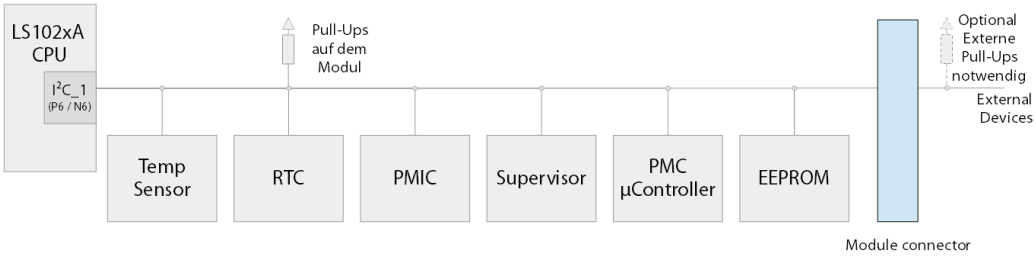


Illustration 14: Block diagram I²C bus 1

There are 2.2 kΩ pull-ups at the I²C bus on the TQMLS102xA. More devices can be connected to the bus but then additional external pull-ups are necessary on account of the relatively high capacitive load.

Table 5: Address overview

Function	Device	Reference	Address
RTC	PCF85063A	D10	1010 001b
Temperature sensor	SA56004EDP	D12	1001 100b
EEPROM	M24C64	D7	1010 000b
Supervisor	ADM1069	D39	1001 111b
PMIC	34VR500	N21	0000 100b
PMC	MKL04Z16	D37	0010 001b (freely programmable)

Except for the PMC the addresses are fixed and cannot be altered.

4.8 TQMLS102xA interface

4.8.1 Pin multiplexing

When using the processor signals the multiple pin configurations by different processor-internal function units must be taken note of. The pins assignment listed in Table 7, Table 8 and Table 9 refer to the corresponding standard BSP of TQ-Systems GmbH in combination with the Starterkit MBLS102xA.

Attention: Destruction or malfunction	
	Depending on the configuration many of the CPU pins can provide several different functions. Please take note of the information concerning the configuration of these pins in the QorIQ LS1021A Reference Manual (1), before integration or start-up of your carrier board / Starterkit.

Freescale provides an Excel Sheet, which shows the Multiplexing and simplifies the selection and configuration.
The following table shows extracts.

Table 6: Multiplexing options

Ball	Power Rail	EC1	RCW[EC1] = 3b000 RGMII 1		RCW[EC1] = 3b001 GPIO3[2:14]		RCW[EC1] = 3b010 CAN[1:2]		RCW[EC1] = 3b011 MII 1		RCW[EC1] = 3b100 SAI[1:2]		RCW[EC1] = 3b101 FTM1
W5	L1VDD		EC1_TXD3	OR	GPIO3_02	OR	CAN2_TX	OR	EC1_TXD3	OR	SAI1_TX_DATA	OR	FTM1_CH5
AA5			EC1_TXD2		GPIO3_03		CAN1_TX		EC1_TXD2		SAI2_TX_DATA		FTM1_CH7
Y6			EC1_TXD1		GPIO3_04		-		EC1_TXD1		SAI1_TX_SYNC		FTM1_CH3
AA6			EC1_TXD0		GPIO3_05		-		EC1_TXD0		SAI2_TX_SYNC		FTM1_CH2
W6			EC1_TX_EN		GPIO3_06		-		EC1_TX_EN		SAI1_TX_BCLK		FTM1_FAULT
Y7			EC1_GTX_CLK		GPIO3_07		-		EC1_TX_CLK		SAI2_TX_BCLK		FTM1_EXTCLK
AA4			EC1_GTX_CLK125		GPIO3_08		-		EC1_RX_ER		EXT_AUDIO_MCLK2		-
AB4			EC1_RXD3		GPIO3_09		CAN2_RX		EC1_RXD3		SAI1_RX_DATA		FTM1_CH4
AC4			EC1_RXD2		GPIO3_10		CAN1_RX		EC1_RXD2		SAI2_RX_DATA		FTM1_CH6
AC5			EC1_RXD1		GPIO3_11		-		EC1_RXD1		SAI1_RX_SYNC		FTM1_CH1
AB6			EC1_RXD0		GPIO3_12		-		EC1_RXD0		SAI2_RX_SYNC		FTM1_CH0
AC3			EC1_RX_CLK		GPIO3_13		-		EC1_RX_CLK		SAI1_RX_BCLK		FTM1_QD_PHA
AC6			EC1_RX_DV		GPIO3_14		-		EC1_RX_DV		SAI2_RX_BCLK		FTM1_QD_PHB

		EC2	RCW[EC2] = 3b000 RGMII 2		RCW[EC2] = 3b001 GPIO3[15:27]		RCW[EC2] = 3b010 CAN[3:4]		RCW[EC2] = 3b011 MII 1		RCW[EC2] = 3b100 USB2 (USB 2.0)		RCW[EC2] = 3b101 FTM2
R4	LVDD		EC2_TXD3	OR	GPIO3_15	OR	CAN4_TX	OR	EC2_TXD3	OR	USB2_D7	OR	FTM2_CH5
R3			EC2_TXD2		GPIO3_16		CAN3_TX		EC2_TXD2		USB2_D6		FTM2_CH7
T4			EC2_TXD1		GPIO3_17		-		EC2_TXD1		USB2_D5		FTM2_CH3
T3			EC2_TXD0		GPIO3_18		-		EC2_TXD0		USB2_D4		FTM2_CH2
T5			EC2_TX_EN		GPIO3_19		-		EC2_TX_EN		USB2_STP		FTM2_FAULT
U3			EC2_GTX_CLK		GPIO3_20		-		EC2_TX_CLK		USB2_CLK		FTM2_EXTCLK
U5			EC2_GTX_CLK125		GPIO3_21		-		EC2_RX_ER		USB2_PWRFAULT		-
R2			EC2_RXD3		GPIO3_22		CAN4_RX		EC2_RXD3		USB2_D3		FTM2_CH4
T1			EC2_RXD2		GPIO3_23		CAN3_RX		EC2_RXD2		USB2_D2		FTM2_CH6
U1			EC2_RXD1		GPIO3_24		-		EC2_RXD1		USB2_D1		FTM2_CH1
U2			EC2_RXD0		GPIO3_25		-		EC2_RXD0		USB2_D0		FTM2_CH0
R1			EC2_RX_CLK		GPIO3_26		-		EC2_RX_CLK		USB2_DIR		FTM2_QD_PHA
V1			EC2_RX_DV		GPIO3_27		-		EC2_RX_DV		USB2_NXT		FTM2_QD_PHB

		EC3	RCW[EC3] = 3b000 RGMII 3		RCW[EC3] = 3b001 GPIO3[28:31, GPIO4[0:8]		RCW[EC3] = 3b010 IEEE 1588		RCW[EC3] = 3b011 MII 1/MII 2		RCW[EC3] = 3b100 USB2_DRVVBUS		RCW[EC3] = 3b101 FTM3		RCW[EC3] = 3b110 RMII EC3
V3	LVDD		EC3_TXD3	OR	GPIO3_28	OR	TSEC_1588_ALARM_OUT2	OR	-	OR	-	OR	FTM3_CH7	OR	-
V4			EC3_TXD2		GPIO3_29		TSEC_1588_ALARM_OUT1		-		-		FTM3_CH6		-
W3			EC3_TXD1		GPIO3_30		TSEC_1588_CLK_OUT		-		-		FTM3_CH5		EC3_TXD1
W4			EC3_TXD0		GPIO3_31		TSEC_1588_PULSE_OUT2		-		-		FTM3_CH4		EC3_TXD0
Y3			EC3_TX_EN		GPIO4_00		-		EC1_TX_ER		-		FTM3_CH1		EC3_TX_EN
V5			EC3_GTX_CLK		GPIO4_01		-		EC2_TX_ER		-		FTM3_CH0		EC3_TX_CLK
Y4			EC3_GTX_CLK125		GPIO4_02		-		EC2_COL		USB2_DRVVBUS		-		EC3_RX_ER
W1			EC3_RXD3		GPIO4_03		-		EC1_CRS		-		FTM3_FAULT		-
Y1			EC3_RXD2		GPIO4_04		-		EC1_COL		-		FTM3_EXTCLK		-
Y2			EC3_RXD1		GPIO4_05		TSEC_1588_PULSE_OUT1		-		-		FTM3_CH3		EC3_RXD1
AA1			EC3_RXD0		GPIO4_06		TSEC_1588_TRIG_IN2		EC2_CRS		-		FTM3_CH2		EC3_RXD0
V2			EC3_RX_CLK		GPIO4_07		TSEC_1588_CLK_IN		-		-		FTM3_QD_PHA		EC3_RX_CLK
AA2			EC3_RX_DV		GPIO4_08		TSEC_1588_TRIG_IN1		-		-		FTM3_QD_PHB		EC3_RX_DV

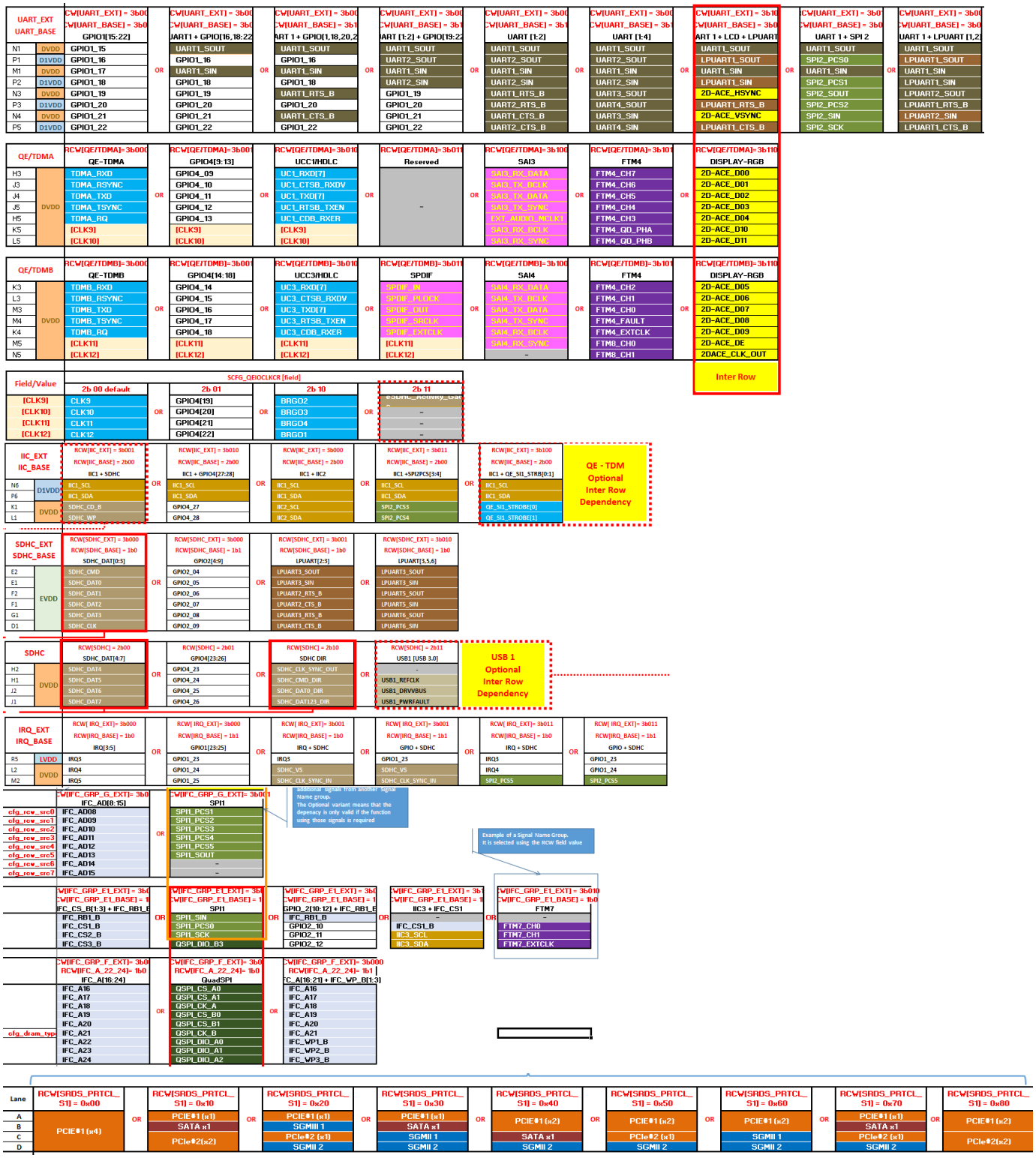
		MDC/MDIO	RCW[MDC/MDIO]= 2b00 MDC/MDIO		RCW[MDC/MDIO]= 2b01 GPIO3[0:1]
AB2	L1VDD		EMI1_MDC	OR	GPIO3_00
AB3			EMI1_MDIO		GPIO3_01

		RTC	RCW[RTC] = 1b0 RTC		RCW[RTC] = 1b1 GPIO1[14]
E10	OVDD		RTC	OR	GPIO1_14

		ASLEEP	RCW[ASLEEP] = 1b0 ASLEEP		RCW[ASLEEP] = 1b1 GPIO1[13]
E6	O1VDD		ASLEEP	OR	GPIO1_13

		EVT[9]_B	RCW[EVT[9]_B] = 1b0 EVT[9]_B		RCW[EVT[9]_B] = 1b1 GPIO_2[24]
D7	O1VDD		EVT9_B	OR	GPIO2_24

Table 6: Multiplexing options (continued)



4.8.2 Pinout connector X1

Table 7: Pinout connector X1

Ball	I/O	Description	Group	Pin name	X1		Pin name	Group	Description	I/O	Ball
-	IN		Power	VCC3V3IF	1	2	VCC3V3IF	Power		IN	-
-	IN		Power	VCC3V3IF	3	4	VCC3V3IF	Power		IN	-
-	IN		Power	VCC3V3IF	5	6	VCC3V3IF	Power		IN	-
-	IN		Power	VCC3V3IF	7	8	VCC3V3IF	Power		IN	-
-	IN		Power	L1VDD_IN	9	10	VBAT	Power		IN	-
-	OUT		Power	L1VDD_OUT	11	12	DGND				
-	OUT		Power	LVDD_OUT	13	14	USB1_D_P	USB		BI	D3
-	IN		Power	LVDD_IN	15	16	USB1_D_M	USB		BI	C3
				DGND	17	18	DGND				
-	OUT		Power	O1VDD	19	20	USB1_RX_P	USB		IN	B4
				DGND	21	22	USB1_RX_M	USB		IN	A4
-	IN		SYSTEM	RESIN#	23	24	DGND				
-	IN		SYSTEM	POWER_STBY	25	26	USB1_TX_P	USB		OUT	B2
-	IN		SYSTEM	POWER_EN	27	28	USB1_TX_M	USB		OUT	A2
				DGND	29	30	DGND				
-	OUT	For internal tests	TEST	SYSCLK_EXT	31	32	CLK_OE	TEST	For internal tests	IN	-
				DGND	33	34	I2C1_SDA	I2C	↑ 4.7 kΩ to 3.3 V	BI	P6
-	OUT	For internal tests	TEST	DDRCLK_EXT	35	36	I2C1_SCL	I2C	↑ 4.7 kΩ to 3.3 V	OUT	N6
				DGND	37	38	DGND				
N4	IN		UART	UART3_SIN	39	40	I2C2_SDA	I2C		BI	L1
N3	OUT		UART	UART3_SOUT	41	42	I2C2_SCL	I2C		OUT	K1
N1	OUT		UART	UART1_SOUT	43	44	DGND				
M1	IN		UART	UART1_SIN	45	46	GPIO4_19	GPIO		BI	K5
				DGND	47	48	DGND				
L5	IN		GPIO	GPIO4_20	49	50	GPIO4_12	GPIO		BI	J5
				DGND	51	52	GPIO4_11	GPIO		BI	J4
H5	OUT		GPIO	GPIO4_13	53	54	GPIO4_10	GPIO		BI	J3
F3	IN	↑ 1 kΩ to O1VDD	TEST	TEST_SEL#	55	56	GPIO4_09	GPIO		BI	H3
E3	IN		USB	USB1_ID	57	58	HRESET#	SYSTEM	↑ 1 kΩ to O1VDD	IN	E5
C1	IN		USB	USB1_VBUS	59	60	RESET_REQ_OUT#	SYSTEM	↑ 2.2 kΩ to 3.3 V	OUT	-
				DGND	61	62	RESET_OUT#	SYSTEM		OUT	-
L2	IN	↑ 4.7 kΩ to 3.3 V	IRQ	IRQ4	63	64	DGND				
M2	IN	↑ 4.7 kΩ to 3.3 V	IRQ	IRQ5	65	66	TEMP_CRIT_OUT#	SYSTEM	↑ 10 kΩ to 3.3 V	OUT	-
				DGND	67	68	TEMP_ALERT#	SYSTEM	Open Drain	OUT	-
-	OUT		SYSTEM	RTC_CLKOUT	69	70	BOOT_CFG0	SYSTEM	↓ 10 kΩ to GND	IN	-
-	OUT	↑ 10 kΩ to 3.3 V / VBAT	SYSTEM	RTC_INT_OUT#	71	72	DGND				
D5	BI	↑ 10 kΩ to O1VDD	SYSTEM	EVT1#	73	74	EVT0#	SYSTEM	↑ 10 kΩ to O1VDD	BI	C5
A6	BI	↑ 10 kΩ to O1VDD	SYSTEM	EVT2#	75	76	JTAG_TMS	JTAG	↑ 10 kΩ to OVDD	IN	F8
B6	BI	↑ 10 kΩ to O1VDD	SYSTEM	EVT3#	77	78	JTAG_TCK	JTAG	↑ 10 kΩ to OVDD	IN	E8
C7	BI	↑ 10 kΩ to O1VDD	SYSTEM	EVT4#	79	80	JTAG_TDO	JTAG		OUT	F7
D7	BI	↑ 10 kΩ to O1VDD	SYSTEM	EVT9#	81	82	JTAG_TDI	JTAG	↑ 10 kΩ to OVDD	IN	E7
E6	OUT	↑ 4.7 kΩ to O1VDD	SYSTEM	ASLEEP	83	84	JTAG_TRST#	JTAG	↑ 10 kΩ to OVDD	IN	F6
G6	IN	↑ 4.7 kΩ to O1VDD	IRQ	IRQ0	85	86	PMC_PWR_STATUS	SYSTEM		OUT	-
G8	IN	↑ 4.7 kΩ to OVDD	IRQ	IRQ1	87	88	EEPROM_WC#	SYSTEM	↑ or ↓ 10 kΩ to 3.3 V or GND	IN	-
				DGND	89	90	GPIO1_14 / RTC	SYSTEM		BI	E10
D15	BI		IFC	QSPI_B_IO00	91	92	DGND				
E13	BI		IFC	QSPI_B_IO01	93	94	QSPI_B_CS0	IFC		OUT	D9
C15	BI		IFC	QSPI_B_IO02	95	96	QSPI_B_CS1	IFC		OUT	C10
F18	BI		IFC	QSPI_B_IO03	97	98	QSPI_B_DQS	IFC		BI	D13
D10	OUT		IFC	QSPI_B_CK	99	100	DGND				
				DGND	101	102	SPI1_CS0#	IFC		OUT	D17
C11	BI		IFC	QSPI_A_IO00	103	104	SPI1_SCK	IFC		OUT	C18
D11	BI		IFC	QSPI_A_IO01	105	106	SPI1_CS5#	IFC	RCW config during POR	BI	A14
C12	BI	↑ 10 kΩ to 3.3 V	IFC	QSPI_A_IO02	107	108	SPI1_SIN	IFC		IN	F15
D12	BI	↑ 10 kΩ to 3.3 V	IFC	QSPI_A_IO03	109	110	SPI1_SOUT_RCW_SRC5	IFC	RCW config during POR	BI	B15
C9	OUT		IFC	QSPI_A_CK	111	112	SPI1_CS1_RCW_SRC0	IFC	RCW config during POR	BI	B12
				DGND	113	114	SPI1_CS2_RCW_SRC1	IFC	RCW config during POR	BI	A12
C8	OUT	↑ 10 kΩ to 3.3 V	IFC	QSPI_A_CS0	115	116	SPI1_CS3_RCW_SRC2	IFC	RCW config during POR	BI	A13
D8	OUT	↑ 10 kΩ to 3.3 V	IFC	QSPI_A_CS1	117	118	SPI1_CS4_RCW_SRC3	IFC	RCW config during POR	BI	B14
C13	BI		IFC	QSPI_A_DQS	119	120	DGND				

4.8.3 Pinout connector X2

Table 8: Pinout connector X2

Ball	I/O	Description	Group	Pin name	X2		Pin name	Group	Description	I/O	Ball
				DGND	1	2	SDHC_DAT4	SDHC		BI	H2
D1	OUT		SDHC	SDHC_CLK	3	4	SDHC_DAT5	SDHC		BI	H1
				DGND	5	6	SDHC_DAT6	SDHC		BI	J2
E1	BI		SDHC	SDHC_DAT0	7	8	SDHC_DAT7	SDHC		BI	J1
F2	BI		SDHC	SDHC_DAT1	9	10	SDHC_CMD	SDHC		BI	E2
F1	BI		SDHC	SDHC_DAT2	11	12	DGND				
G1	BI		SDHC	SDHC_DAT3	13	14	GPIO4_22	GPIO		BI	N5
				DGND	15	16	DGND				
M5	BI		GPIO	GPIO4_21	17	18	GPIO4_18	GPIO		BI	K4
				DGND	19	20	GPIO4_14	GPIO		BI	K3
M3	BI		GPIO	GPIO4_16	21	22	GPIO4_15	GPIO		BI	L3
M4	BI		GPIO	GPIO4_17	23	24	UART2_SIN	UART		IN	P2
P5	IN		UART	UART4_SIN	25	26	UART2_SOUT	UART		OUT	P1
P3	OUT		UART	UART4_SOUT	27	28	DGND				
R5	IN	↑ 4.7 kΩ to LVDD	IRQ	IRQ3	29	30	NC	EC2		IN	U2
				DGND	31	32	NC	EC2		IN	U1
U3	OUT		EC2	NC	33	34	CAN3_RX	EC2		IN	T1
T3	OUT		EC2	NC	35	36	CAN4_RX	EC2		IN	R2
T4	OUT		EC2	NC	37	38	NC	EC2		IN	V1
R3	OUT		EC2	CAN3_TX	39	40	NC	EC2		IN	R1
R4	OUT		EC2	CAN4_TX	41	42	DGND				
T5	OUT	↓ 1 kΩ to GND	EC2	NC	43	44	EC3_RXD0	EC3		IN	AA1
U5	IN		EC2	NC	45	46	EC3_RXD1	EC3		IN	Y2
				DGND	47	48	EC3_RXD2	EC3		IN	Y1
V5	OUT		EC3	EC3_GTX_CLK	49	50	EC3_RXD3	EC3		IN	W1
W4	OUT		EC3	EC3_TXD0	51	52	EC3_RX_DV	EC3		IN	AA2
W3	OUT		EC3	EC3_TXD1	53	54	EC3_RX_CLK	EC3		IN	V2
V4	OUT		EC3	EC3_TXD2	55	56	DGND				
V3	OUT		EC3	EC3_TXD3	57	58	MDIO	MDIO		BI	AB3
Y3	OUT	↓ 1 kΩ to GND	EC3	EC3_TX_EN	59	60	MDC	MDIO		OUT	AB2
				DGND	61	62	DGND				
Y4	IN		EC3	EC3_GTX_CLK125	63	64	EC1_RX_CLK	EC1		IN	AC3
				DGND	65	66	EC1_RX_DV	EC1		IN	AC6
AA6	OUT		EC1	EC1_TXD0	67	68	EC1_RXD0	EC1		IN	AB6
Y6	OUT		EC1	EC1_TXD1	69	70	EC1_RXD1	EC1		IN	AC5
AA5	OUT		EC1	EC1_TXD2	71	72	EC1_RXD2	EC1		IN	AC4
W5	OUT		EC1	EC1_TXD3	73	74	EC1_RXD3	EC1		IN	AB4
W6	OUT	↓ 1 kΩ to GND	EC1	EC1_TX_EN	75	76	DGND				
AA4	IN		EC1	EC1_GTX_CLK125	77	78	EC1_GTX_CLK	EC1		IN	Y7
				DGND	79	80	IRQ2	IRQ	↑ 4.7 kΩ to L1VDD	IN	W7
W10	OUT		SERDES	SD_TX0_P	81	82	DGND				
				DGND	83	84	SD_REF_CLK1_P	SERDES		IN	AC8
Y10	OUT		SERDES	SD_TX0_N	85	86	DGND				
				DGND	87	88	SD_REF_CLK1_N	SERDES		IN	AB8
W11	OUT		SERDES	SD_TX1_P	89	90	DGND				
				DGND	91	92	SD_RX0_P	SERDES		IN	AC10
Y11	OUT		SERDES	SD_TX1_N	93	94	DGND				
				DGND	95	96	SD_RX0_N	SERDES		IN	AB10
W13	OUT		SERDES	SD_TX2_P	97	98	DGND				
				DGND	99	100	SD_RX1_P	SERDES		IN	AC11
Y13	OUT		SERDES	SD_TX2_N	101	102	DGND				
				DGND	103	104	SD_RX1_N	SERDES		IN	AB11
W14	OUT		SERDES	SD_TX3_P	105	106	DGND				
				DGND	107	108	SD_RX2_P	SERDES		IN	AC13
Y14	OUT		SERDES	SD_TX3_N	109	110	DGND				
				DGND	111	112	SD_RX2_N	SERDES		IN	AB13
AC16	IN		SERDES	SD_REF_CLK2_P	113	114	DGND				
				DGND	115	116	SD_RX3_P	SERDES		IN	AC14
AB16	IN		SERDES	SD_REF_CLK2_N	117	118	DGND				
				DGND	119	120	SD_RX3_N	SERDES		IN	AB14

4.8.4 Pinout connector X3

Table 9: Pinout connector X3

Ball	I/O	Group	Pin name	X3			Pin name	Group	I/O	Ball
			DGND	1		2	DGND			
-	IN	PMC SWD	SWD_CLK	3		4	TA_BB_TMP_DETECT#	TRUST	IN	U6
-	BI	PMC SWD	SWD_DIO	5		6	TA_PROG_SFP	FUSE PROG. Power Supply	IN	F11
F10	IN	FUSE PROG. Power Supply	PROG_MTR	7		8	TA_TMP_DETECT#	TRUST	IN	F9
R6	IN	TRUST	TA_BB_RTC	9		10	DGND			
			DGND	11		12	IFC_AD00	IFC	BI	A7
B8	BI	IFC	IFC_AD01	13		14	IFC_AD02	IFC	BI	A8
B9	BI	IFC	IFC_AD03	15		16	IFC_AD04	IFC	BI	A9
A10	BI	IFC	IFC_AD05	17		18	IFC_AD06	IFC	BI	B11
A11	BI	IFC	IFC_AD07	19		20	IFC_WE0#	IFC	OUT	F14
			DGND	21		22	IFC_BTCL	IFC	OUT	E14
C14	OUT	IFC	IFC_NDDDR_CLK	23		24	DGND			
A15	BI	IFC	IFC_AD14_RCW_SRC6	25		26	IFC_TE_RCW_IFC_TE	IFC	OUT	D14
A16	BI	IFC	IFC_AD15_RCW_SRC7	27		28	IFC_AVD	IFC	OUT	C16
-	-	-	NC	29		30	IFC_NDDQS	IFC	BI	D16
C17	OUT	IFC	IFC_CS0#	31		32	DGND			
F16	IN	IFC	IFC_RB0#	33		34	IFC_OE#	IFC	OUT	E16
			DGND	35		36	IFC_CLE_RCW_SRC8	IFC	OUT	E17
A17	OUT	IFC	IFC_CLK0	37		38	DGND			
E18	OUT	IFC	IFC_WP0#	39		40	IFC_CLK1	IFC	OUT	B17

4.9 Assembly

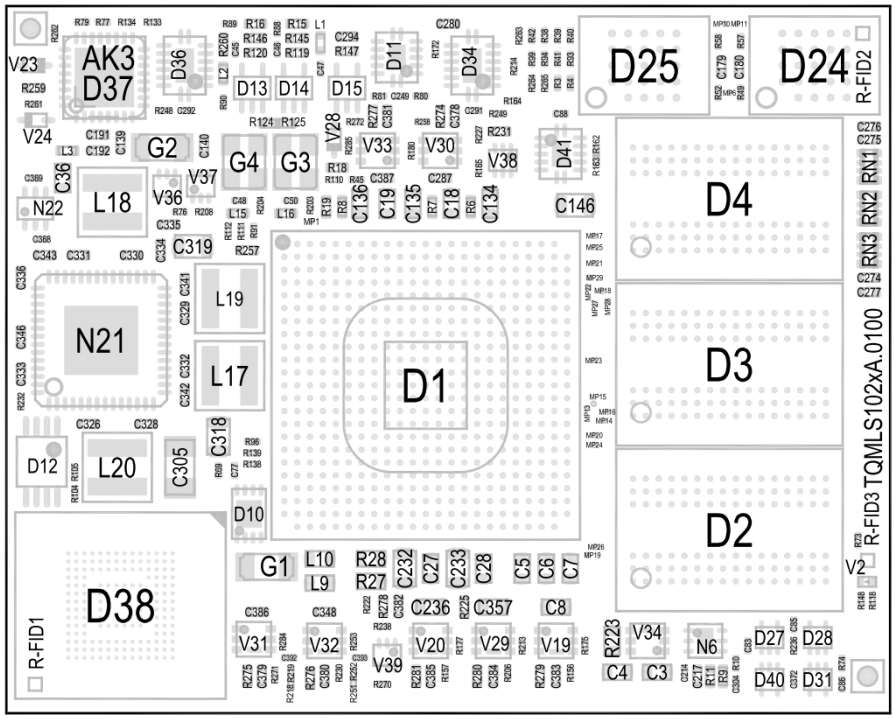


Illustration 15: TQMLS102xA assembly, top

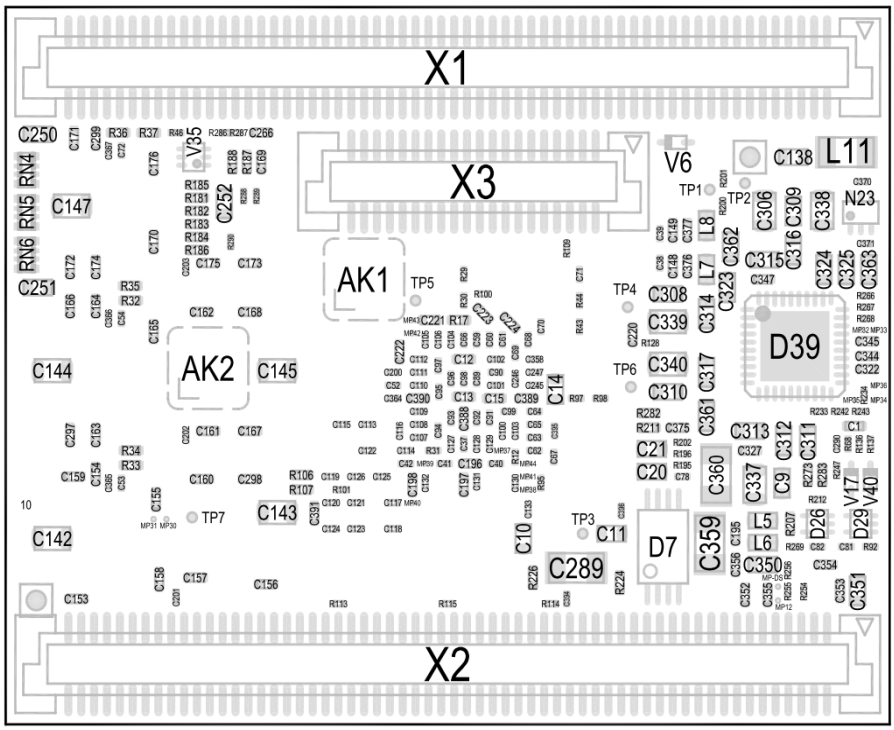


Illustration 16: TQMLS102xA assembly, bottom

5. MECHANICS

5.1 Dimensions

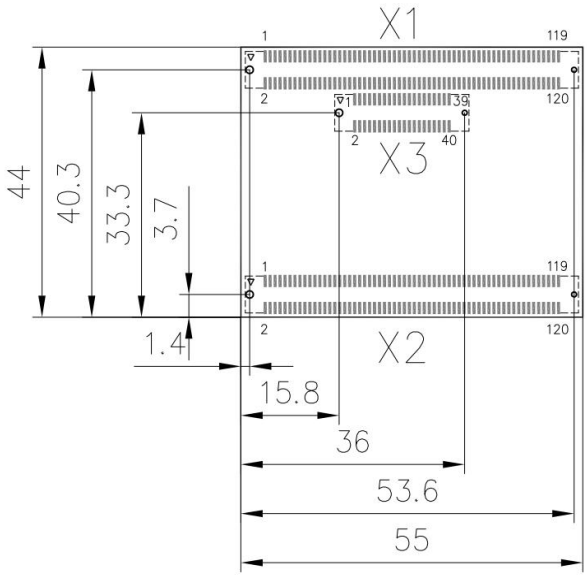


Illustration 17: TQMLS102xA dimensions, **through view**

5.2 TQMLS102xA images

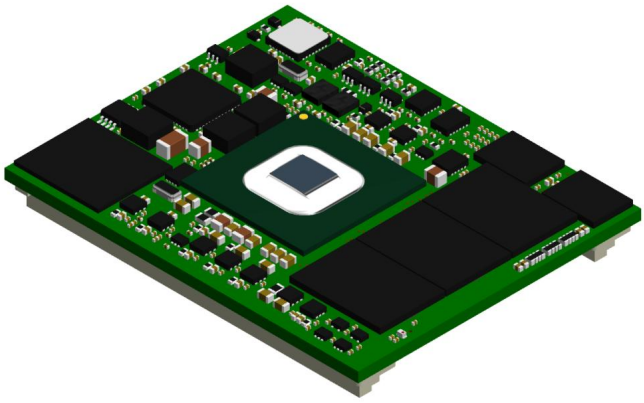


Illustration 18: TQMLS102xA, 3D, top view

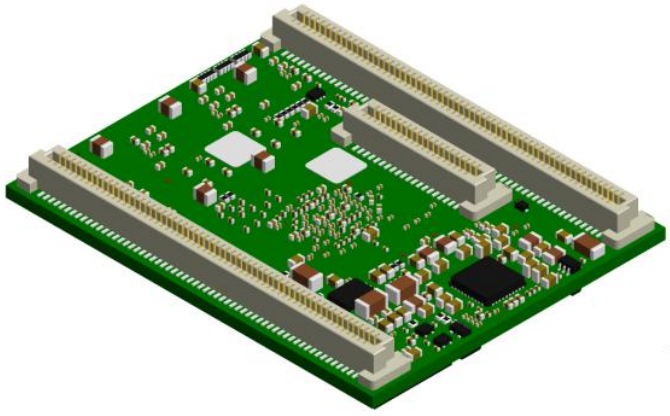


Illustration 19: TQMLS102xA, 3D, bottom view

6. TECHNICAL DATA

6.1 Connectors

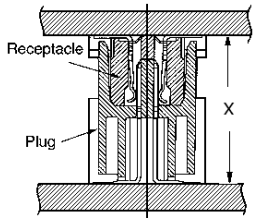
The TQMLS102xA is connected to the carrier board with 280 pins spread on three connectors.
The following table shows details of the plug connector used.

Table 10: Plug connectors on the TQMLS102xA

Manufacturer	Part number	Remark
TE connectivity	120-pin: 5177985-5	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to 125 °C
TE connectivity	40-pin: 5177985-1	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to 125 °C

The TQMLS102xA is held in the plug connectors with a considerable retention force.
To avoid damaging the plug connectors of the TQMLS102xA as well as the carrier board plug connectors while removing the TQMLS102xA the use of an extraction tool is strongly recommended. See section 6.6 for further information.
The following table shows some suitable mating plug connectors for the carrier board.

Table 11: Carrier board mating plug connectors

Manufacturer	Part number	Stack height (X)	
TE connectivity	40-pin: 5177986-1 120-pin: 5177986-5	5 mm	
TE connectivity	40-pin: 1-5177986-1 120-pin: 1-5177986-5	6 mm	
TE connectivity	40-pin: 2-5177986-1 120-pin: 2-5177986-5	7 mm	
TE connectivity	40-pin: 3-5177986-1 120-pin: 3-5177986-5	8 mm	

6.2 Adaptation to the environment

The overall dimensions (length × width) of the TQMLS102xA are 55 × 44 mm².
The maximum height of the TQMLS102xA above the carrier board is approximately 8.6 mm.

6.3 Protection against external effects

As an embedded module the TQMLS102xA is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

6.4 Thermal management

To cool the TQMLS102xA, approximately 4 W have to be dissipated.
The power dissipation originates primarily in the CPU and the DDR3L SDRAM.
The power dissipation also depends on the software used and can vary according to the application.

Attention: Destruction or malfunction	
	The CPU belongs to a performance category in which a cooling system may be essential in certain applications. It is the responsibility of the customer to define a suitable cooling method depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software).

6.5 Structural requirements

The TQMLS102xA is held in the mating plug connectors by the retention force of the pins (a total of 280). For high requirements with respect to vibration and shock firmness an additional holder has to be provided in the final product to hold the TQMLS102xA in its position. For this purpose TQ-Systems GmbH can provide a suitable solution. As no heavy and big components are used, no further requirements are given.

6.6 Notes of treatment

To avoid damage caused by mechanical stress, the TQMLS102xA may only be extracted from the carrier board by using the extraction tool MOZI8XXL that can also be obtained separately.

Attention: Note with respect to the component placement of the carrier board	
	2.5 mm should be kept free on the carrier board, along the longitudinal edges on both sides of the TQMLS102xA for the extraction tool.

6.7 Vibration

Table 12: Vibration

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 – 9 Hz, 9 – 200 Hz, 200 – 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X-Y-Z axis
Number of frequency cycles	20 frequency cycles
Amplitude	2 Hz … 9 Hz: 3.5 ms^{-2} 9 Hz … 200 Hz: 10 ms^{-2} 200 Hz … 500 Hz: 15 ms^{-2}

6.8 Shock

Table 13: Shock

Parameter	Details
Shocks	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Residence time	18 ms
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

The values shown are based on the guidelines of the standard DIN ETS 300019 (Environmental tests for telecommunications equipment).

7. SOFTWARE

The TQMLS102xA is delivered with a preinstalled boot loader and a BSP, which is configured for the Starterkit MBLS102xA.
The boot loader provides module-specific as well as board-specific settings, e.g.:

- CPU configuration
- PMIC configuration
- DDR3L SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

More information can be found in the Support Wiki for the TQMLS102xA.

8. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

8.1 EMC

The TQMLS102xA was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

The following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board.
- A sufficient number of blocking capacitors in all supply voltages.
- Fast or permanent clocked lines (e.g., clock) should be kept short;
  avoid interference of other signals by distance and / or shielding besides,
  take note of not only the frequency, but also the signal rise times.
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly).

Since the TQMLS102xA is plugged on an application-specific carrier board, EMC or ESD tests only make sense for the whole device.

8.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMLS102xA.

The following measures are recommended for a carrier board:

- Generally applicable: Shielding of the inputs
  (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering / Zener diode(s)
- Fast signal lines: Integrated protective devices (e.g., suppressor diode arrays)

8.3 Operational safety and personal security

Due to the occurring voltages (≤3.3 V DC), tests with respect to the operational and personal safety have not been carried out.

8.4 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.

In general, a reliable operation is given when following conditions are met:

Table 14: Climate and operational conditions

Parameter	Range	Remark
Permitted Environment temperature	–40 to +85 °C	–
Permitted storage temperature	–40 to +100 °C	–
Relative humidity (operating / storage)	10 to 90 %	Not condensing

Detailed information concerning the thermal characteristics of the CPU is to be taken from the Freescale QorIQ LS1021A Reference Manual (1).

8.5 Reliability and service life

No detailed MTBF calculation has been done for the TQMLS102xA.

The TQMLS102xA is designed to be insensitive to vibration and impact.

Middle grade connectors, which guarantee at least 100 mating cycles, were used for the TQMLS102xA.

8.6 Environment protection

8.6.1 RoHS

The TQMLS102xA is manufactured RoHS compliant.

- All components and assemblies used are RoHS compliant
- RoHS compliant soldering processes are used

8.6.2 WEEE

The company placing the product on the market is responsible for the observance of the WEEE® regulation.
To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

8.6.3 REACH

The EU-chemical regulation 1907/2006 (REACH regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as TQ-Systems GmbH is informed by suppliers accordingly.

8.6.4 EuP

The guideline 2005/32/EC (EuP) is the next step after WEEE® and RoHS for an environmentally friendly production of electric and electronic products. The consideration of environmental requirements with the product design "creation appropriate for the environment" ("ecological design") with the aim to improve the environmental compatibility of the product during its whole life cycle should be taken into consideration.
The guideline appropriate for the product (embedded PC) is applied.

8.6.5 Battery

No batteries are used on the TQMLS102xA.

8.6.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMLS102xA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMLS102xA is delivered in reusable packaging.

8.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
The energy consumption of this subassembly is minimised by suitable measures.
Printed PC-boards are delivered in reusable packaging.
Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.
Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 15: Acronyms

Acronym	Meaning
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DC	Direct Current
DDR3L	Double Data Rate 3 Low voltage
DIN	German industry standard (Deutsche Industrienorm)
EC	European Community
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded MultiMedia Card (Flash)
EN	European Standard (Europäische Norm)
ESD	Electrostatic Discharge
eSDHC	enhanced Secure Digital High Capacity
ETS	European Telecommunications Standards
EuP	Energy using Products
FR4	Flame Retardant-4
GPIO	General Purpose Input/Output
I	Input
I^2C	Inter-Integrated Circuit
IFC	Integrated Flash-Controller
IP00	Ingress Protection 00
JTAG	Joint Test Action Group
LPM	Low Power Mode
MOZI	Module extractor (Modulzieher)
MTBF	Mean operating Time Between Failures
NC	Not Connected
NOR	Not-Or
O	Output
PCB	Printed Circuit Board
PCMCIA	People Can't Memorize Computer Industry Acronyms
PMC	Power Management Controller
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
QSPI	Queued Serial Peripheral Interface
RC	Resistor-Capacitor
RCW	Reset Configuration Word
REACH	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
SD card	Secure Digital Card
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serializer/Deserializer
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
SWD	Serial Wire Debug
TBGA	Thin Ball Grid Array
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment

9.2 References

Table 16: Further applicable documents

No.:	Name	Rev. / Date	Company
(1)	QorIQ LS1021A Reference Manual	REV. D, 09/2014	Freescale

TQ-Systems GmbH
Mühlstraße 2 I Gut Delling I 82229 Seefeld
info@tq-group.com I www.tq-group.com

Technology in Quality