

TQMa28L User's Manual

TQMa28L UM 100 12.02.2014

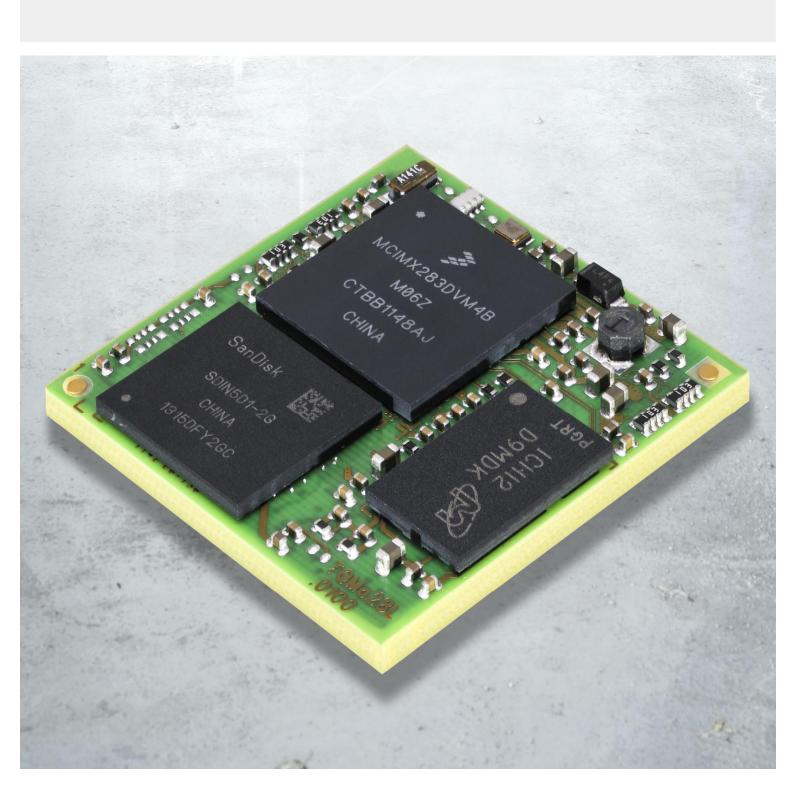




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Revision history

Rev.	Date	Name	Pos.	Modification
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1.4 Imprint

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1.5 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
4	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
<u>^</u>	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
î	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, file names, or menu items.



1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Handling and ESD tips

General handling of your TQ-products



The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.

A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off.

Violation of this guideline may result in damage / destruction of the module and be dangerous to your health.

Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling



The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal. Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.

Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring. The identification of the individual functions follows the above conventions.

Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

Specifications and manual of the modules used:

These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).

Specifications of the components used:

The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.

■ Chip errata:

It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.

Software behaviour:

No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.

■ General expertise:

Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.



1.10 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 2: Acronyms

Acronym	Meaning
A/D	Analog/Digital
ADC	Analog/Digital Converter
Al	Analog In
ARM®	Advanced RISC Machine
AUART	Application Universal Asynchronous Receiver/Transmitter
BGA	Ball Grid Array
CAN	Controller Area Network
CPU	Central Processing Unit
DC	Direct Current
DDR	Double Data Rate
DUART	Debug Universal Asynchronous Receiver/Transmitter
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electro-Magnetic Compatibility
eMMC	embedded MultiMediaCard (Flash)
ESD	Electrostatic Discharge
	Ground
GND GPIO	
	General Purpose Input/Output
GPMI	General Purpose Media Interface
1/0	Input Input
1/0	Input/Output
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
1 ² C	Inter-Integrated Circuit
I ² S	Inter Integrated Circuit Sound
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LGA	Land Grid Array
LL	Lower Left
LR	Lower Right
MTBF	Mean operating Time Between Failures
NAND	Not-And
NC NB	Not Connected
NP	Not Present
0	Output
OTG	On-The-Go
OTP	One-Time Programmable
PD	Pull-Down
PMU	Power Management Unit
PU	Pull-Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
RC	Resistor Capacitor
RGB	Red Green Blue
I Dalis	
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
ROM RTC	Read-Only Memory Real-Time Clock
ROM RTC SAIF	Read-Only Memory Real-Time Clock Serial Audio Interface
ROM RTC SAIF SD	Read-Only Memory Real-Time Clock Serial Audio Interface Secure Digital
ROM RTC SAIF SD SD card	Read-Only Memory Real-Time Clock Serial Audio Interface Secure Digital Secure Digital Card
ROM RTC SAIF SD SD card SD/MMC	Read-Only Memory Real-Time Clock Serial Audio Interface Secure Digital Secure Digital Card Secure Digital Multimedia Card
ROM RTC SAIF SD SD card SD/MMC SDRAM	Read-Only Memory Real-Time Clock Serial Audio Interface Secure Digital Secure Digital Card Secure Digital Multimedia Card Synchronous Dynamic Random Access Memory
ROM RTC SAIF SD SD card SD/MMC SDRAM SPDIF	Read-Only Memory Real-Time Clock Serial Audio Interface Secure Digital Secure Digital Card Secure Digital Multimedia Card Synchronous Dynamic Random Access Memory Sony-Philips Digital Interface Format
ROM RTC SAIF SD SD card SD/MMC SDRAM SPDIF SPI	Read-Only Memory Real-Time Clock Serial Audio Interface Secure Digital Secure Digital Card Secure Digital Multimedia Card Synchronous Dynamic Random Access Memory Sony-Philips Digital Interface Format Serial Peripheral Interface
ROM RTC SAIF SD SD card SD/MMC SDRAM SPDIF SPI SSP	Read-Only Memory Real-Time Clock Serial Audio Interface Secure Digital Secure Digital Card Secure Digital Multimedia Card Synchronous Dynamic Random Access Memory Sony-Philips Digital Interface Format Serial Peripheral Interface Synchronous Serial Port
ROM RTC SAIF SD SD card SD/MMC SDRAM SPDIF SPI SSP UART	Read-Only Memory Real-Time Clock Serial Audio Interface Secure Digital Secure Digital Card Secure Digital Multimedia Card Synchronous Dynamic Random Access Memory Sony-Philips Digital Interface Format Serial Peripheral Interface Synchronous Serial Port Universal Asynchronous Receiver/Transmitter
ROM RTC SAIF SD SD card SD/MMC SDRAM SPDIF SPI SSP UART UL	Read-Only Memory Real-Time Clock Serial Audio Interface Secure Digital Secure Digital Card Secure Digital Multimedia Card Synchronous Dynamic Random Access Memory Sony-Philips Digital Interface Format Serial Peripheral Interface Synchronous Serial Port Universal Asynchronous Receiver/Transmitter Upper Left
ROM RTC SAIF SD SD card SD/MMC SDRAM SPDIF SPI SSP UART UL UR	Read-Only Memory Real-Time Clock Serial Audio Interface Secure Digital Secure Digital Card Secure Digital Multimedia Card Synchronous Dynamic Random Access Memory Sony-Philips Digital Interface Format Serial Peripheral Interface Synchronous Serial Port Universal Asynchronous Receiver/Transmitter Upper Left Upper Right
ROM RTC SAIF SD SD card SD/MMC SDRAM SPDIF SPI SSP UART UL UR USB	Read-Only Memory Real-Time Clock Serial Audio Interface Secure Digital Secure Digital Card Secure Digital Multimedia Card Synchronous Dynamic Random Access Memory Sony-Philips Digital Interface Format Serial Peripheral Interface Synchronous Serial Port Universal Asynchronous Receiver/Transmitter Upper Left
ROM RTC SAIF SD SD card SD/MMC SDRAM SPDIF SPI SSP UART UL UR	Read-Only Memory Real-Time Clock Serial Audio Interface Secure Digital Secure Digital Card Secure Digital Multimedia Card Synchronous Dynamic Random Access Memory Sony-Philips Digital Interface Format Serial Peripheral Interface Synchronous Serial Port Universal Asynchronous Receiver/Transmitter Upper Left Upper Right



2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa28L revision 01xx.

This User's Manual does not replace the Reference Manual of the CPU.

The TQMa28L is a universal Minimodule based on the Freescale ARM-CPU i.MX283 or i.MX287.

The ARM926EJ-S core works with up to 454 MHz. The module extends the TQ-Systems GmbH product range and provides a well-balanced ratio between computing performance and graphics power.

The module provides the following key functions and characteristics:

- Freescale i.MX28 (ARM9 architecture), 454 MHz
- All functional CPU signals are routed to module contacts points
- Up to 16 Gbyte eMMC NAND flash
- Up to 256 Mbyte DDR2 SDRAM
- Up to eight 12 bit A/D converter
- PWM
- Various serial interfaces depending on multiplexing (UART, SPI, I²C, I²S)
- 2 × CAN (i.MX287)
- 2 × USB 2.0 Hi-Speed Host interface with integrated PHY
- Industrial temperature range on request
- Low power consumption (0.11 to 2 W, depending on mode of operation)
- Dimensions: 30.6 × 30.6 mm²
- Long term available
- Power supply: 5 V or Lithium-ion battery



3. TECHNICAL DATA

3.1 System architecture and functionality

3.1.1 TQMa28L, block diagram

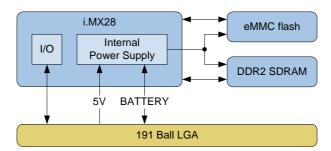


Illustration 1: TQMa28L, block diagram

3.1.2 System functionality

The following elements are implemented on the TQMa28L:

- i.MX283 or i.MX287 CPU
- DDR2 SDRAM
- eMMC NAND flash

Interfaces:

191 contact points Land Grid Array (LGA)

A detailed overview of all available user's interfaces can be found in section 4.1.

4. ELECTRONICS SPECIFICATION

The information in this User's Manual is only valid for the combination of TQMa28L and the especially adapted boot loader, which is preinstalled on every TQMa28L (also see section (5).

4.1 Interfaces to other systems and devices

The name of the module version depends on the assembled CPU:

Table 3: TQMa28L versions

Module version	Processor
TQMa28L-AA	MCIMX287CVM4B
TQMa28L-AB	MCIMX283CVM4B

4.1.1 Module connection

The TQMa28L has to be soldered onto the carrier board. It is not possible to remove the module non-destructive.

4.1.2 Module pinout

When using the processor signals the multiple pin configurations by different processor-internal function units must be taken note of.

The signals of the module are described in detail in the following tables.

The electric or pin characteristics are to be taken from the data sheet of the CPU (2).

In addition to direction, contact name and contact number, external and internal pull-up or-down wirings as well as the references to I/O voltage and processor signal characteristics are listed.



4.1.2.1 TQMa28L-AA contact points

Table 4: TQMa28L-AA contact points (**top view through module**)

		abic				027		iitac						Jugii			,											
14	9	Ž	DUART_RX	Ŋ	DUART_TX	77	USB_1_OC#	D3	USB_0_OC#	D4	USB_0_DP	B10	USB_0_DM	A10	USB_0_ID	SL	Ċ	o di di		VCC4V2	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	BALLERY) () () () () () () () () () (BALLEKY	\d\d\d\d\d\d\d\d\d\d\d\d\d\d\d\d\d\d\d	VC.5V	ğ	Ž
13	1588_EVENT2_OUT	81	1588_EVENT2_IN	Cl	ENET_RESET#	3	ENET_INT#	E3	USB_1_DP	A8	USB_1_DM	B8	i	OND O	ġ	QND	USB_1_PWR_EN	F6	USB_0_PWR_EN	F5	ğ	ONIO	PWM4	E10	ViCCEV	۷۲.53	JTAG_TDI	E12
12	CN	<u> </u>	1588_EVENT3_OUT	D1	1588_EVENT3_IN	E1	d d	GIND	LRADC2	83	LRADC3	D9		۷۲۲۱۷8	HSADC0	B14	LRADC6	C14		۷۲۲3۷3	Š	O O	PSWITCH	A11	Valley	۷۲۲.3۷	JTAG_TDO	E13
Ξ	ENET0_TXD1	F2	ENETO_TXD0 1	Ħ	ENETO_TX_EN	F4	ENET_CLK	E2	SAIF0_BITCLK	F7	LRADC1	6)	LRADCO	C15	LRADC4	D13	LRADC5	D15		۷۲۲۱۷۶	G.	פואס	PWM3	E9	G.	פאפ	JTAG_RTCK	E14
10	ENETO_RXD1	H2	ENETO_RXD0	Η	ENETO_RX_EN	E4	Ċ	פֿאַר	SAIF0_MCLK	C5		QND	i.	OND GND	Ċ	O O	SSP2_SCK	A3	SSP2_MISO	B3	JTAG_TRST#	D14	JTAG_TMS	D12	JTAG_TCK	E11	Q.	5
6	ENET1_TXD1	62	ENET1_TXD0	G1	ENET1_TX_EN	14	ENET_MDC	G4	SAIF0_LRCLK	G6	SPDIF	D7	SAIFO_SDATA0	E7	SAIF1_SDATA0	E8	SSP2_MOSI	ß	SSP2_SS0#	C4	DEBUG	89	RESET#	A14	TEST5	711	TEST6	J16
ω	ENET1_RXD1	J2	ENET1_RXD0	J1	ENET1_RX_EN	J3	ENET_MDIO	H4	GPIO0_20	9N	EMMC_CLK	P8	GPIO0_16	N7	GPIO0_26	P6	<u> </u>	O O	Ċ	GND	Ş	ם פאס	TEST8	114	Ş	פֿאַפֿ	TEST4	K16
7	LCD_WR_RW#	K1	LCD_DOTCLK	Z	ć.	GND	LCD_VSYNC	L1	LCD_HSYNC	M1		QND	LCD_BL_PWM	K8	GPI00_27	Р7	GPI00_17	6N	EMMC_CMD	N8	GPIO3_6	K5	TEST7	N14	Š	Q Q	TEST3	K17
9	CD_D00	K2	LCD_D01	83	LCD_D02	77	LCD_D03	L3	LCD_D04	M2	CCD_D05	M3	LCD_ENABLE	NS	Ċ	O O	I2C1_SDA	Н7	I2C1_SCL	H6	I2C0_SDA	D8	I2C0_SCL	7.7	TEST2	L16	TEST1	L17
7.	P00_D01	N2	LCD_D07	P1	CD_D08	P2	CCD_D09	P3	LCD_D10	R1	LCD_D11	R2	LCD_RS	M4	LCD_RESET	M6	2	פֿוּ	AUART4_RX	72	AUART4_TX	A2	AUART4_CTS#	D2	AUART4_RTS#	B2	TESTO	U15
4	LCD_D12	11	LCD_D13	T2	LCD_D14	U2	LCD_D115	U3	LCD_D16	T3	LCD_D17	R3	LCD_RD_E	P4	GPIO0_24	R6	EMMC_DATA7	T6	EMMC_DATA6	9N	Ş	O O	AUART0_CTS#	91	AUARTO_RTS#	71	AUART1_RX	L4
ю	LCD_D18	U4	LCD_D19	T4	LCD_D20	R4	LCD_D21	US	LCD_D22	T5	LCD_D23	R5	CCD_CS	P5	EMMC_DATA5	R7	EMMC_DATA4	71		U7	AUART0_RX	G5	AUART0_TX	HS	Š	O O N I O	AUART1_TX	K
2	CINU) J	Š	Ž	SD_DATA4	B5	SD_DATA6	DS	SD_DATA5	C5	SD_DATA7	B4	Ċ.	QND	EMMC_DATA2	R8	EMMC_DATA1	T8	EMMC_DATA0 EMMC_DATA3	N8	AUART3_RX	M5	AUART3_TX	1.5	AUART3_CTS#	97	AUART3_RTS#	K6
-	۵	L Z	SD_DATA3	A5	SD_DATA2	D6	SD_DATA1	9)	SD_DATA0	B6	SD_CMD	A4	SD_CLK	A6	SD_DETECT#	D10	SD_WP	67	CAN1_TX	M7	CAN1_RX	6W	CAN0_TX	M8	CAN0_RX	L8	Ç	Ž
	4	ζ	١	2		ر	۵	د		ш		ш		5	:	E		7	:	×	-	_	2	≥	Z	2	٥	



4.1.2.2 TQMa28L-AB contact points

Table 5: TQMa28L-AB contact points (**top view through module**)

	ı	able	٦.	ıQ	Ma2	OL /\	D CO	iiuci	. pon	165 (. . .	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,				uuic	,											
14	Q	Ž	DUART_RX	K7	DUART_TX	77	USB_1_OC#	D3	USB_0_OC#	D4	USB_0_DP	B10	USB_0_DM	A10	7	ر <u>ع</u>	Ş	9		VCC4V2	A TTEB V	PALLENI	>0	BATIEKY	Valley	۷۲۲۵۷	Ç	Ž
13	Z	ر <u>ح</u>	:	J	2	N N	Ž	N N	USB_1_DP	A8	USB_1_DM	B8	ć	GIND	ć	פואם	2	2	-	N N	CI	2	PWM4	E10	Valley	۸۲۲۵۷	JTAG_TDI	E12
12	CINC		:	J Z	2	NC	<u>q</u>	סווס	LRADC2	89	LRADC3	60		۸۲۲۱۷۶	HSADC0	B14	LRADC6	C14		٧٦٦٥٧٤	CIN.		PSWITCH	A11	Valley	۷۲۵۷	JTAG_TDO	E13
Ξ	ENETO_TXD1	F2	ENETO_TXD0	E	ENETO_TX_EN	F4	ENET_CLK	E2	AUART4_RX	F7	LRADC1	6)	LRADCO	C15	LRADC4	D13	LRADC5	D15		۸۵۲۱۸۶	CINC	<u> </u>	PWM3	E9	ğ	ONIO	JTAG_RTCK	E14
10	ENETO_RXD1	H2	ENETO_RXD0	Ξ	ENETO_RX_EN	E4	<u>q</u>	פֿאַס	AUART4_CTS#	CD	į	CIND	i i	פואם	Q (פֿואַס	AUART2_RX	A3	AUART3_RX	83	JTAG_TRST#	D14	JTAG_TMS	D12	JTAG_TCK	E11	<u>d</u>	פואם
6	Q	2	:	J Z	2	INC.	ENET_MDC	G4	AUART4_RTS#	G6	-	J Z	AUART4_TX	E7	GPI03_26	E8	AUART2_TX	3	AUART3_TX	C4	DEBUG	B9	RESET#	A14	TESTS	J17	TEST6	J16
ω	Z	2	:	J Z	2	N N	ENET_MDIO	H4	GPIO0_20	N6	EMMC_CLK	P8	GPIO0_16	N7	GPIO0_26	P6	Ş	5	Ċ	GIND	CN	5	TEST8	114	Š	פואט	TEST4	K16
7	LCD_WR_RW#	K1	:	J Z	Ċ	O O	Ų Ž	אַר	Ų	<u>.</u>	Ċ	OND OND	USB_0_ID	K8	GPIO0_27	P7	GPIO0_17	6N	EMMC_CMD	8N	Ų	2	TEST7	N14	Ş	פואם	TEST3	K17
9	CD_D00	K2	LCD_D01	ಬ	LCD_D02	L2	CD_D03	F3	LCD_D04	M2	CCD_D05	M3	2	N N	Č	GND	2	2	-	<u>.</u>	I2C0_SDA	D8	I2C0_SCL	77	TEST2	L16	TEST1	L17
5	PD0-D06	N2	LCD_D07	P1	RCD_D08	P2	FCD_D09	P3	LCD_D10	R1	LCD_D11	R2	LCD_RS	M4	LCD_RESET	M6	2		2) <u>P</u>	Z	2	2	<u>ا</u>	Ç	N N	TEST0	U15
4	LCD_D12	T1	LCD_D13	T2	LCD_D14	U2	LCD_D15	U3	LCD_D16	T3	LCD_D17	R3	LCD_RD_E	P4	GPI00_24	R6	EMMC_DATA7	Т6	EMMC_DATA6	9N	CN		AUART0_CTS#	ЭГ	AUARTO_RTS#	71	AUART1_RX	L4
ю	LCD_D18	U4	LCD_D19	Т4	LCD_D20	R4	LCD_D21	US	LCD_D22	T5	LCD_D23	R5	CCD_CS	P5	EMMC_DATA5	R7	EMMC_DATA4	77	EMMC_DATA0 EMMC_DATA3	U7	AUARTO_RX	65	AUART0_TX	HS	Q.	ם פו	AUART1_TX	K4
2	Q.V.		:	L Z	SSP2_MISO	B5	SSP2_MOSI	D5	SSP2_SS0	CS	SSP2_SCK	B4	Ci t	פואם	EMMC_DATA2	R8	EMMC_DATA1	Т8	EMMC_DATA0	N8	Ų	2	Ų Ž	ر <u>ال</u> ا	Q) <u>P</u>	Q	J N
-	Q	Ž	SD_DATA3	A5	SD_DATA2	D6	SD_DATA1	9)	SD_DATA0	B6	SD_CMD	A4	SD_CLK	A6	SD_DETECT#	D10	SD_WP	67		ر ع	Ž	2	Ų.	N V	Ç	N.	Ç	Ž



4.2 System components

4.2.1 Processor

4.2.1.1 Characteristics

The Freescale processor i.MX28 based on an ARM926EJ-S™ core is produced in 90 nm technology. It provides a wide range of functions. Illustration 2 gives an overview.

More information about the i.MX28 processor is provided in the following table.

Table 6: Processor information

Manufacturer	Part number	Temperature range	Package	Silicon revision
Freescale	MCIMX283CVM4B	−40 °C to +85 °C	BGA 289	1.2
Freescale	MCIMX287CVM4B	−40 °C to +85 °C	BGA 289	1.2

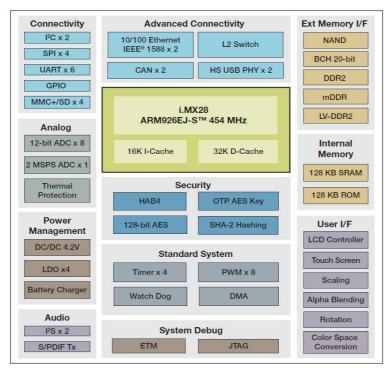


Illustration 2: i.MX28, block diagram (Source: <u>Freescale</u>)

Other functionality of the processor shown in the block diagram can be looked up in the Freescale Reference Manual (1). All essential signals of the processor, except the DDR2 SDRAM interface and the eMMC, are routed to the module's contact points.



4.2.1.2 Boot modes

The i.MX28 has of a ROM with integrated boot code. When the i.MX28 starts this boot code initializes the hardware and then loads the program image from the selected boot device.

Instead of booting from the integrated eMMC it is also possible to boot from one of the following interfaces:

- USB
- I²C
- SPI
- SSP
- GPMI

The boot device and its configuration can be defined with several boot mode registers.

For this the i.MX28 offers two possibilities:

- The settings are read from boot mode pins
- The settings are read from internal burnt OTP eFuses

The exact behaviour during the boot process depends on the value of eFuse ENABLE_PIN_BOOT_CHECK and the signal LCD_RS. The following table shows the possible combinations.

Table 7: Boot configuration

eFuse: ENABLE_PIN_BOOT_CHECK	Pin: LCD_RS	TQMa28L contact	Boot mode	Remark
0	Х		Boot configuration via boot mode pins	Default
1	0	M4	Boot configuration via OTP eFuses	_
'	1		Boot configuration via boot mode pins	-

4.2.1.3 Boot device

The eMMC is preset as the standard boot device (SD/MMC MASTER ON SSP1 3V3).

Therefore the boot mode pins on the TQMa28L are connected as follows:

Table 8: Configuration boot mode pins eMMC

i.MX28 Ball	Pin name	Boot mode name	TQMa28L	TQMa28L contact	Boot mode
K2	LCD_D00	BM0	10 kΩ Pull-Down	A6	0
K3	LCD_D01	BM1	10 kΩ Pull-Up	B6	1
L2	LCD_D02	BM2	10 kΩ Pull-Down	C6	0
L3	LCD_D03	BM3	10 kΩ Pull-Up	D6	1
M2	LCD_D04	VOLTAGE SELECT	10 kΩ Pull-Down	E6	0

4.2.1.4 Other boot devices

To boot from another source rather than the module-internal eMMC, or to use the function ENABLE_PIN_BOOT_CHECK, the default boot mode settings can be changed by resistors of about 1 k Ω at the pins LCD_D[4:0] or LCD_RS. The necessary settings for other boot device are to be taken from the Freescale Reference Manual (1).

4.2.1.5 Processor clock supply

A crystal oscillator on the TQMa28L supplies the processor with 24 MHz.

A 32.768 kHz crystal oscillator on the TQMa28L supplies the RTC domain with a clock signal.

4.2.1.6 Pin multiplexing

Depending on the configuration, the pin multiplexing enables different pins to have different functions. Freescale provides on their website the program "IOMUXCC", which supports the selection of the desired options. TQ-Systems GmbH provides an xml file created with the program "IOMUXCC", which shows the pin-multiplexing of the TQMa28L. The user can configure specific pin-multiplexing based on this xml file. The xml file can be obtained from TQ-Systems Support. The accuracy of the generated configuration cannot be guaranteed! It is the user's responsibility to conscientiously check the generated configuration.

Attention: Destruction or malfunction!



Many of the CPU pins can be used in several different ways. Please, notice the notes about the wiring of these pins in the i.MX28 Reference Manual (1) before integration / start-up of your carrier board / Starterkit.



4.2.1.7 CPU errata

Attention: Malfunction!



Please pay attention to the latest errata of the Freescale CPU (3) and the latest TechNote (5).

4.2.1.8 Freescale erratum TKT131240

Attention: Malfunction!



To fix the Freescale erratum TKT131240 and to ensure a reliable boot process an EEPROM has to be provided on the carrier board.

On account of the silicon erratum TKT131240 of the processor i.MX28 the polarity of both SSP clock domains is inverted during the boot process. The reason is a faulty boot ROM code. When executed during the system start the clock polarity is set wrong. Devices (eMMC, SD card, etc.) connected at SSP0 and SSP1 may not be recognized properly and the processor will not boot. TQ-Systems GmbH recommends using an additional SPI or I²C EEPROM containing a ROM patch. This EEPROM has to be provided on the carrier board as a boot device. If an I²C EEPROM is used, the boot mode has to be set to I2C0 (EEPROM address 0x50). In case an SPI EEPROM is used it has to be provided on SPI3. The patch executes from the EEPROM, patches the ROM SSP driver code for one SSP (SSP0 or SSP1), and switches to boot from the desired boot device. The EEPROM has to be programmed with the patch only once. This can be done using the I²C bus while the processor module TQMa28 is not plugged in the carrier board or directly using Linux. It is also possible to assemble programmed EEPROMs.

The following table shows possible boot configurations using boot EEPROMs:

Table 9: Configuration boot mode pins eMMC

TQMa28L contact	Name	Description	Remark
D6	LCD_D03		10 kΩ↑ on TQMa28L
C6	LCD_D02	D30 0001: Boot from I ² C0 0011: Boot from SPI3	10 kΩ↓ on TQMa28L
B6	LCD_D01		10 kΩ↑ on TQMa28L
A6	LCD_D00		10 kΩ↓ on TQMa28L

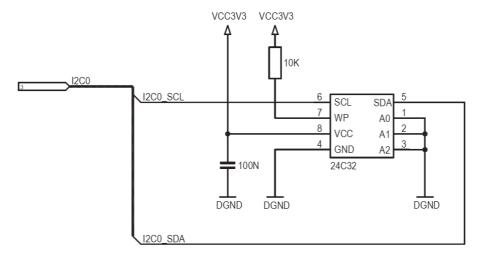


Illustration 3: EEPROM with ROM patch on carrier board



4.2.2 Memory

4.2.2.1 DDR2 SDRAM

The following illustration shows how the DDR2 SDRAM is connected to the CPU.

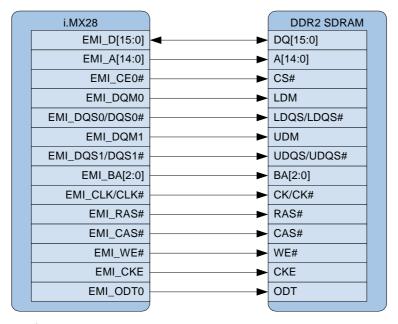


Illustration 4: Interface to DDR2 SDRAM

The following table gives an overview of the possible alternatives.

Table 10: Memory models DDR2 SDRAM

Manufacturer	Manufacturer's number	Туре	Capacity	Temp. Range	Remark
Micron	MT47H64M16HR-3IT:H	64M16	128 Mbyte	−40 to +85 °C	-
Micron	MT47H64M16HR-25EIT:H	64M16	128 Mbyte	−40 to +85 °C	Default
Micron	MT47H128M16RT-25EIT	128M16	256 Mbyte	−40 to +85 °C	-

The memory allocates the following address range:

Table 11: Address configuration DDR2 SDRAM

Start address	Size	Chip Select	Capacity
0x4000_000	0x0800_000	CE0#	128 Mbyte
0x4000_000	0x1000_000	CE0#	256 Mbyte

4.2.2.2 eMMC

The TQMa28L is equipped with an eMMC flash to store programs and data (boot loader and operating system). It is controlled via the SD card controller SSP1 of the i.MX28.

The following illustration shows how the eMMC is connected to the processor. $\label{eq:matter}$

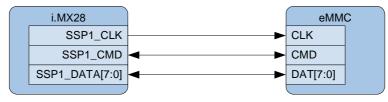


Illustration 5: Interface to eMMC



4.2.3 RTC

The TQMa28L provides a processor internal RTC. The current consumption of the RTC is approximately 30 μ A. A 32.768 kHz crystal oscillator clocks the RTC.

In the following table the parameters of the crystal oscillator are shown.

Table 12: Parameters of 32.768 kHz crystal oscillator

Parameter	Value	Unit	Remark
Frequency tolerance	±20	ppm	@ 25 °C
Frequency ageing	±3 max.	ppm	First year, @ 25 °C
Parabolic Coefficient	-0.04 x 10 ⁻⁶	°C²	Additional deviation @ temp ≠ 25 °C

When the power supply is switched off the CPU internal RTC has to be buffered by a lithium-ion battery to maintain its function. As the RTC in the CPU is supplied by the same power plane than the CPU in normal operation the whole system supplies itself from this power plane. For this reason the RTC cannot be buffered with a normal button cell. If the characteristics of the internal RTC are not suitable, the DS1339 is proposed as an external RTC on the carrier board.

4.2.4 Graphics interfaces / LCD bus

Parallel displays with a maximum frame size of up to 800×480 pixels can be connected to the TQMa28L. The parallel data interface can be up to 24 bits wide. The LCD bus is directly routed to the module's contact points.

Table 13: Display signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
LCD_D[23:0]	LCD_D[23:0]	A:F – 3:6	0	LCD-Interface RGB-Data
LCD_HSYNC	LCD_HSYNC	E7	0	LCD-Interface Horizontal Sync
LCD_VSYNC	LCD_VSYNC	D7	0	LCD-Interface Vertical Sync
LCD_ENABLE	LCD_ENABLE	G6	0	LCD-Interface Enable
LCD_DOTCLK	LCD_DOTCLK	В7	0	LCD-Interface Dot clock
LCD_CS	LCD_CS#	G3	0	LCD-Interface Chip Select
LCD_RS	LCD_RS	G5	0	LCD-Interface Register Select
LCD_WR_RWN	LCD_WR_RW#	A7	0	LCD-Interface 6800 R/W# / 8080 W
LCD_RD_E	LCD_RD_E	G4	0	LCD-Interface 6800 Enable / 8080 RD
LCD_RESET	LCD_RESET	H5	0	LCD-Interface Reset Out



4.2.5 Ethernet

The i.MX283 (TQMa28L-AB) provides one; the i.MX287 (TQMa28L-AA) provides two built-in Fast Ethernet controllers, which are designed for 10 and 100 Mbps. Each Ethernet interfaces requires a PHY on the carrier board.

Table 14: Ethernet signals ENET0

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
ENETO_MDIO	ENET_MDIO	D8	I/O	Ethernet Management Data
ENETO_MDC	ENET_MDC	D9	0	Ethernet Output Management Data Clock
ENETO_TXD[0:1]	ENETO_TXD[0:1]	B11:A11	0	Ethernet Output Transmit Data
ENETO_TX_EN	ENETO_TX_EN	C11	0	Ethernet Output Transmit Enable
ENETO_RXD[0:1]	ENETO_RXD[0:1]	B10:A10	I	Ethernet Input Receive Data
ENETO_RX_EN	ENETO_RX_EN	C10	I	Ethernet Data Valid / Carrier Sense
ENET_CLK	ENET_CLK	D11	I/O	Reference Clock
GPIO4_5	ENET_INT#	D13	I Ethernet Input Interrupt (GPIO)	
GPIO4_13	ENET_RESET#	C13	0	Ethernet Output Reset (GPIO)

Table 15: Ethernet signals ENET1 (TQMa28L-AA)

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
ENET1_TXD[0:1]	ENET1_TXD[0:1]	B9:A9	0	Ethernet Output Transmit Data
ENET1_TX_EN	ENET1_TX_EN	C9	0	Ethernet Output Transmit Enable
ENET1_RXD[0:1]	ENET1_RXD[0:1]	B8:A8	I	Ethernet Input Receive Data
ENET1_RX_EN	ENET1_RX_EN	C8	I	Ethernet Data Valid / Carrier Sense

The processor-internal clock generator of the i.MX28 does not meet the clock jitter values required by most Ethernet PHYs. This may cause Ethernet connection problems during link-up.

It is recommended to provide an external clock generator with suitable precision on the carrier board to generate the clock signal for the input ENET_CLK. This can be achieved by using a quartz crystal or a crystal oscillator.

The CPU supplies additional functions according to IEEE® 1588.

The following signals are available at the module's contact points:

Table 16: IEEE1588 signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
ENET0_1588_EVENT2_OUT	1588_EVENT2_OUT	A13	0	-
ENETO_1588_EVENT2_IN	1588_EVENT2_IN	B13	I	-
ENET0_1588_EVENT3_OUT	1588_EVENT3_OUT	B12	0	-
ENETO_1588_EVENT3_IN	1588_EVENT3_IN	C12	I	-

By turning off pre-set functions and switching on 1588-features, more 1588_Events can be provided.

4.2.6 SD card

The TQMa28L provides an SD card controller (SSP0), whose signals are available at the module's contact points. The following table shows the signals used for the SD card interface.

Table 17: SD card interface signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
SSP0_SCK	SD_CLK	G1	0	SD Card Output Clock
SSP0_CMD	SD_CMD	F1	I/O	SD Card Command
SSP0_D[7:4]	SD_D[7:4]	F2:D2:E2:C2	I/O	SD Card Data / only TQMa28L-AA
SSP0_D[3:0]	SD_D[3:0]	B1:E1	I/O	SD Card Data
SSP0_CARD_DETECT	SD_DETECT#	H1	I	SD Card Input Card-Detect
GPIO0_28	SD_WP	J1	I	SD Card Input Write-Protection



4.2.7 Serial interfaces

The supported standards, transmission modes and transfer rates of the following interfaces are to be taken from the Freescale Reference Manual (1).

4.2.7.1 CAN

The TQMa28L-AA provides two integrated CAN controllers. All four signals are routed to the module's contact points. The corresponding drivers have to be provided on the carrier board.

The following table shows the signals used for the CAN interfaces.

Table 18: CAN signals TQMa28L-AA

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
CAN0_TX	CAN0_TX	M1	0	TQMa28L-AA
CAN0_RX	CANO_RX	N1	I	TQMa28L-AA
CAN1_TX	CAN1_TX	K1	0	TQMa28L-AA
CAN1_RX	CAN1_RX	L1	I	TQMa28L-AA

4.2.7.2 I²C

Depending on the version the TQMa28L provides up to two I²C interfaces.

The following tables show the signals used for the I²C interfaces.

Table 19: I²C signals TQMa28L-AA

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
I2C0_SDA	I2C0_SDA	L6	I/O	Pull-Up 10 kΩ to 3.3 V on TQMa28L-AA
I2C0_SCL	I2C0_SCL	M6	0	Pull-Up 10 kΩ to 3.3 V on TQMa28L-AA
I2C1_SDA	I2C1_SDA	J6	I/O	Pull-Up 10 kΩ to 3.3 V on TQMa28L-AA
I2C1_SCL	I2C1_SCL	K6	0	Pull-Up 10 kΩ to 3.3 V on TQMa28L-AA

Table 20: I²C signals TQMa28L-AB

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
I2C0_SDA	I2C0_SDA	L6	I/O	Pull-Up 10 kΩ to 3.3 V on TQMa28L-AB
I2C0_SCL	I2C0_SCL	M6	0	Pull-Up 10 kΩ to 3.3 V on TQMa28L-AB

Attention: pull-up resistors



Pull-up resistors for the I^2C buses are already assembled on the module. If more devices are connected on the carrier board the maximum capacitive bus load according to the I^2C standard has to be observed. If necessary additional pull-ups have to be assembled on the carrier board.



4.2.7.3 I²S

To connect an audio-codec via I²S the signals of the Serial Audio Interface (SAIF) are routed to the module's contact points.

The following table shows the signals used for the SAIF interface.

Table 21: I²S signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
SAIF0_MCLK	SAIF0_MCLK	E10	0	System Master Clock
SAIF0_LRCLK	SAIF0_LRCLK	E9	I/O	I ² S Frame Clock
SAIF0_BITCLK	SAIF0_BITCLK	E11	I/O	I ² S Bit Clock
SAIF0_SDATA0	SAIF0_SDATA0	G9	I	I ² S Data Input
SAIF1_SDATA0	SAIF1_SDATA0	H9	0	I ² S Data Output

The SAIF allows to connect 3, 4 or 5-wire interface, e.g., via I²S. Details are to be taken from the Freescale Reference Manual (1).

4.2.7.4 SPDIF

The TQMa28L-AA provides an SPDIF interface with transmit functionality.

The following table shows the signals used for the SPDIF interface.

Table 22: SPDIF signal

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
SPDIF	SPDIF	F9	0	-

4.2.7.5 SPI

The following table shows the signals used for the SPI interface.

Table 23: SPI signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
SSP2_SCK	SSP2_SCK	J10	0	-
SSP2_MOSI	SSP2_MOSI	J9	0	-
SSP2_MISO	SSP2_MISO	K10	I	-
SSP2_SS0	SSP2_SS0#	K9	0	-

More SPI interfaces can be made available by adapting the multiplexing.



4.2.7.6 UART

The i.MX28 provides five Application UART interfaces (AUART) and one Debug UART (DUART). The following table shows the signals used for the AUART0 interface.

Table 24: AUARTO signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
AUARTO_TX	AUARTO_TX	M3	0	-
AUARTO_RX	AUARTO_RX	L3	I	-
AUARTO_RTS	AUARTO_RTS#	N4	0	-
AUARTO_CTS	AUARTO_CTS#	M4	I	-

The following table shows the signals used for the AUART1 interface.

Table 25: AUART1 signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
AUART1_TX	AUART1_TX	P3	0	-
AUART1_RX	AUART1_RX	P4	I	_

The following table shows the signals used for the AUART2 interface.

Table 26: AUART2 signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
AUART2_TX	AUART2_TX	J9	0	TQMa28L-AB
AUART2_RX	AUART2_RX	J10	I	TQMa28L-AB

The following table shows the signals used for the AUART3 interface.

Table 27: AUART3 signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
AUART3_TX	AUART3_TX	M2	0	_
AUART3_RX	AUART3_RX	L2	I	-
AUART3_RTS	AUART3_RTS#	P2	0	Only TQMa28L-AA
AUART3_CTS	AUART3_CTS#	N2	I	Only TQMa28L-AA

The following table shows the signals used for the AUART4 interface.

Table 28: AUART4 signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
AUART4_TX	AUART4_TX	L5	0	-
AUART4_RX	AUART4_RX	K5	I	-
AUART4_RTS	AUART4_RTS#	N5	0	-
AUART4_CTS	AUART4_CTS#	M5	I	_

The following table shows the signals used for the DUART interface.

Table 29: DUART signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
DUART_TX	DUART_TX	C14	0	-
DUART_RX	DUART_RX	B14	I	Pull-Up 10 kΩ to 3.3 V on TQMa28L required



4.2.7.7 USB

The i.MX8 provides two USB-High-Speed controller. Controller USB0 is OTG capable. The second port exclusively provides a Hi-Speed host. For both ports the PHY is integrated in the i.MX28. The 5 V supply for the USB ports has to be implemented on the carrier board. In addition, filtering and EMC protection for the USB signals has to be provided on the carrier board. Notes are to be found in the USB standard.

The following table shows the signals used for the USB0 interface.

Table 30: USB0 signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
USBODM	USB_0_DM	G14	I/O	-
USB0DP	USB_0_DP	F14	I/O	-
USB0_ID	USB_0_ID	H14	I	-
GPIO3_9	USB_0_PWR_EN	K13	0	Only TQMa28L-AA
USB0_OVERCURRENT	USB_0_OC#	E14	ı	-

The following table shows the signals used for the USB1 interface.

Table 31: USB1 signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
USB1DM	USB_1_DM	F13	I/O	-
USB1DP	USB_1_DP	E13	I/O	-
GPIO3_8	USB_1_PWR_EN	J13	0	Only TQMa28L-AA
USB1_OVERCURRENT	USB_1_OC#	D14	I	-

4.2.8 PWM

Three of the eight PWM outputs of the i.MX28 are directly available at the module's contact points. More PWMs are available if the pin multiplexing is adapted.

The following table shows the available PWM signals.

Table 32: PWM signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
PWM2	LCD_BL_PWM	G7	0	-
PWM3	PWM3	M11	0	-
PWM4	PWM4	M13	0	_



4.2.9 GPIO

Besides their interface function most of the pins of the i.MX28 can also be used as GPIOs. All these GPIOs are interrupt and therefore wake-up capable. The configuration can be taken from the Freescale Reference Manual (1). Some of the GPIOs are directly named as GPIO and directly routed to the module's contact points.

The following table shows the GPIO signals which can be used.

Table 33: GPIO signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
BANK0_PIN16	GPIO0_16	G8	I/O	-
BANK0_PIN17	GPIO0_17	J7	I/O	-
BANK0_PIN20	GPIO0_20	E8	I/O	-
BANK0_PIN24	GPIO0_24	H4	I/O	-
BANK0_PIN26	GPIO0_26	H8	I/O	-
BANK0_PIN27	GPIO0_27	H7	I/O	-
BANK3_PIN06	GPIO3_6	L7	I/O	Only TQMa28L-AA
BANK3_PIN26	GPIO3_26	H9	I/O	Only TQMa28L-AB

4.2.10 JTAG

The i.MX28 provides two JTAG modes. The mode is defined with the signal DEBUG.

To change the JTAG mode, the default can be changed by a pull-down resistor of approximately 1 k Ω at the pin DEBUG.

The following table shows the available modes. The default mode used on the TQMa28L is printed in **bold**.

Table 34: JTAG modes

Debug	Name	TQMa28L contact	Remark	
0	JTAG interface works for boundary scan	L9	-	
1	JTAG interface works for ARM debugging		Pull-Up 10 kΩ to 3.3 V on TQMa28L	

The JTAG signals are directly routed from the CPU to the module's contact points. All necessary pull-up and pull-down resistors are already assembled on the TQMa28L.

The following table shows the signals used for the JTAG interface.

Table 35: JTAG signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
JTAG_TCK	JTAG_TCK	N10	I	Pull-Up 10 kΩ to 3.3 V on TQMa28L
JTAG_TMS	JTAG_TMS	M10	I	Pull-Up 10 kΩ to 3.3 V on TQMa28L
JTAG_TDI	JTAG_TDI	P13	I	Pull-Up 10 kΩ to 3.3 V on TQMa28L
JTAG_TDO	JTAG_TDO	P12	0	-
JTAG_TRST	JTAG_TRST#	L10	I	Pull-Up 10 kΩ to 3.3 V on TQMa28L
JTAG_RTCK	JTAG_RTCK	P11	0	Pull-Up 10 kΩ to 3.3 V on TQMa28L



4.2.11 ADC

The TQMa28L provides eight ADC inputs. All inputs are blocked to GND with 10 nF.

The ADC supports resistive 4- or 5-wire touch screens.

An adequate protection circuit has to be implemented on the carrier board.

The following table describes the ADC signals available at the module's contact points:

Table 36: ADC signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	4-wire touch	5-wire touch	Remark
LRADC0	LRADC0	G11	Al			-
LRADC1	LRADC1	F11	Al			-
LRADC2	LRADC2	E12	Al	Touch Right / X+	UL	-
LRADC3	LRADC3	F12	Al	Touch Top / Y+	LL	-
LRADC4	LRADC4	H11	Al	Touch Left / X–	UR	-
LRADC5	LRADC5	J11	Al	Touch Bottom / Y-	LR	-
LRADC6	LRADC6	J12	Al		Common	-
HSADC0	HSADC0	H12	AI			High-Speed ADC (not qualified)

4.2.12 Reset

There are two ways to reset the TQMa28L:

- Power-on reset
- RESET# input

The following table describes the Reset signal available at the module's contact points:

Table 37: RESET signal

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
RESETN	RESET#	M9	I	 Pull-Up 10 kΩ to 3.3 V on TQMa28L Minimum required Low-Time: ≥100 ms

To improve the stability in case of voltage drops we recommend to provide a supervisor on the carrier board.

A supervisor with a minimum reset time of 200 ms should be used.

The following illustration shows a possible implementation.

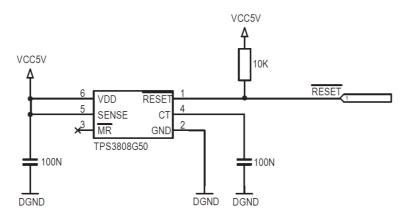


Illustration 6: Optional supervisor on carrier board



4.2.13 Power supply

4.2.13.1 Module supply

The TQMa28L works with a single supply of 5 V that must be provided by the carrier board.

Alternatively a lithium-ion battery can supply the TQMa28L.

If a lithium-ion battery is connected at the BATTERY pin it is charged if the module is supplied with 5 V. Software settings can be done in the registers HW_LRADC_CONVERSION and HW_POWER_CHARGE.

Attention: Lithium primary batteries and lithium-ion secondary batteries



Lithium primary batteries may not be used at the i.MX28 or TQMa28L (pin BATTERY) because of the charging function of the CPU!

The following table shows the permitted ranges of the supply voltages.

Table 38: Supply voltages

Parameter	Min.	Тур.	Max.	Unit
Supply voltage V _{IN} VCC5V	4.75	5.00	5.25	V
Supply voltage V _{IN} BATTERY	3.10	-	4.20	V

The calculated current consumption (worst case) is at most 0.4 A. The current consumption strongly depends on component placement, software and wiring options. The values given are to be seen as indicative values.

Table 39: Current consumption

Parameter	V _{IN}	I _{ITYP}	Remark
Current consumption in Linux idle mode	5.0 V	147 mA	-
Current consumption in Linux boot mode	5.0 V	234 mA	-
Switch-on current	5.0 V	3.56 A	Peak current for approximately 1.2 μs.



4.2.13.2 Power Management Unit

The i.MX28 has an integrated Power Management Unit (PMU). All voltages required on the TQMa28L are generated by the PMU. The following illustration shows the internal structure of the PMU.

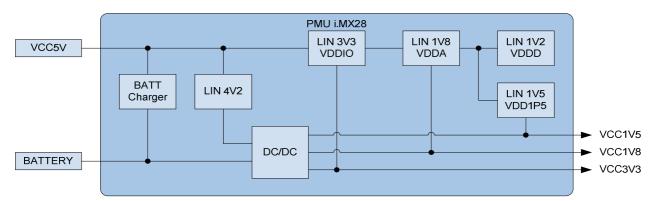


Illustration 7: i.MX28 PMU, block diagram

The internal power supply consists of a chain of linear regulators a DC/DC converter and a battery charger.

If the TQMa28L is supplied via VCC5V the processor starts with the voltages generated by its internal linear regulators. During the boot process the linear regulator LIN 4V2 is switched on and supplies the DC/DC converter. From this point the DC/DC converter provides the necessary system voltages instead of the linear regulators. In BATTERY mode the DC/DC converter starts directly.

The i.MX28 provides an extensive set of registers to configure the PMU. Among other things the output voltages of all voltage regulators, the brown-out level, the start behaviour, the charging currents, the trigger levels, etc. can be configured.

The settings of these registers have to be checked or set for the respective design. Further information is to be taken from the Freescale Reference Manual (1), the i.MX28 data sheet (2) and the Application Note for the power management (4) of the i.MX28.

4.2.13.3 Power-up/down

The start behaviour of the TQMa28L depends on the selected voltage source (VCC5V or BATTERY).

- Module supply with VCC5V: Power-up sequence of the CPU starts immediately
- Module supply with BATTERY: Power-up sequence of the CPU only starts when PSWITCH is supplied with a valid start-up voltage between 0.65 V and 1.5 V.

The function of PSWITCH depends on the applied voltage (see Freescale Reference Manual (1)).

In case the function "Fast Falling Edge" is not used (which could be used to power-down the CPU) it is recommended to disable this function using the circuitry suggested by Freescale (see Illustration 8).

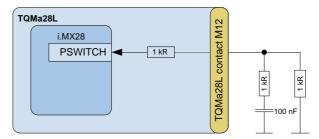


Illustration 8: Wiring of PSWITCH

Attention: Power-up sequence



To avoid across supply and errors in the power-up sequence, no I/O pins may be driven by external components during boot-time.



5. SOFTWARE SPECIFICATION

The TQMa28L comes with a preinstalled especially tailored boot loader.

The boot loader contains module specific adaptions as for example

- CPU/PMU configuration
- RAM configuration
- RAM timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strength

These settings have to be adapted if a different boot loader is used. More details can be requested from the TQ-Support.



6. MECHANICS SPECIFICATION

6.1 TQMa28L dimensions

Dimensions (L x W): $30.6 \times 30.6 \text{ mm}^2$ Maximum height: Maximum 3.5 mm

6.2 TQMa28L views



Illustration 9: TQMa28L top view (3D)

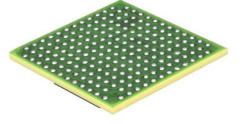


Illustration 10: TQMa28L bottom view (3D)

6.3 TQMa28L component placement

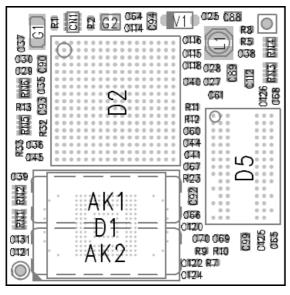


Illustration 11: TQMa28L component placement top

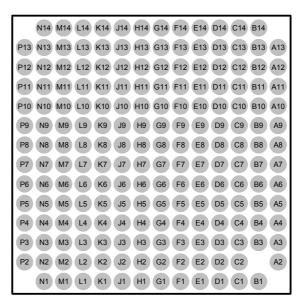


Illustration 12: TQMa28L bottom view



6.4 TQMa28L footprint

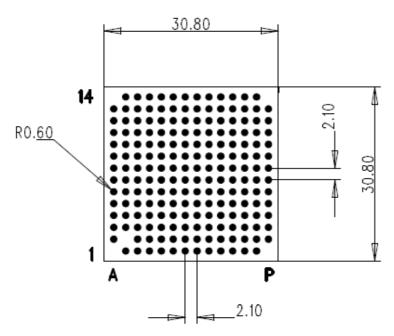


Illustration 13: Recommended footprint for carrier board

Attention: Note with respect to the placement of the carrier board



The free space at position B2 serves as indicator for automatic placement detection.

6.5 Requirements for the superior system

6.5.1 Protection against external effects

As an embedded module it is not protected against dust, external impact and contact (IP00). An adequate protection has to be guaranteed by the surrounding system.

6.5.2 Thermal management

Up to 2 W (worst case) have to be dissipated to cool the TQMa28L. The power dissipation originates primarily in the CPU and in the DDR2 SDRAM. The user is responsible for an adequate cooling system in his application. In most cases a passive cooling should be sufficient.

Attention: Destruction or malfunction!



The CPU belongs to a performance category with which in certain applications cooling can become necessary. It is the task of the user, to define a heat sink suitable for the specific case of operation (e.g., by clock frequency, stack height and airflow).

6.5.3 Structural requirements

The TQMa28L is soldered on the carrier board. As no heavy and big components are used, no further requirements are given.



7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The module was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system. Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding besides, notice not only the frequency, but also the signal rise times
- Filtering of all signals which can be connected externally (also "slow signals" and DC can radiate RF indirectly)

7.2 **ESD**

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system.

As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa28L.

Following measures are recommended for a carrier board:

■ Generally applicable: Shielding of the inputs

(shielding connected well to ground / housing on both ends)

Supply voltages: Protection by suppressor diode(s)Slow signal lines: RC filtering, perhaps Zener diode(s)

Fast signal lines: Integrated protective devices (suppressor diode arrays)

7.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety haven't been carried out.

7.4 Reliability and service life

No detailed MTBF calculation has been done for the TQMa28L.

It was designed to be insensitive to vibration and impact.

Product life limiting components like electrolyte capacitors were not used.



7.5 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly. In general, a reliable operation is given when following conditions are met:

Table 40: Climate and operating conditions "Commercial temp. range" 0 °C to +70 °C

Parameter	Range	Remark
Die temperature CPU	−40 °C to +105 °C	Environment: -40 °C to +85 °C
Housing temperature DDR2 SDRAM	0 °C to +85 °C	-
Housing temperature other ICs	0 °C to +70 °C	-
Permitted storage temperature TQMa28L	−40 °C to +85 °C	-
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

Table 41: Climate and operating conditions "Extended temp. range" –25 °C to +85 °C

Parameter	Range	Remark
Die temperature CPU	−40 °C to +105 °C	Environment: -40 °C to +85 °C
Housing temperature DDR2 SDRAM	−40 °C to +95 °C	-
Housing temperature other ICs	−25 °C to +85 °C	-
Permitted storage temperature TQMa28L	−40 °C to +85 °C	-
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

Table 42: Climate and operating conditions "Industrial temp. range" –40 °C to +85 °C

Parameter	Range	Remark
Die temperature CPU	−40 °C to +105 °C	Environment: -40 °C to +85 °C
Housing temperature DDR2 SDRAM	−40 °C to +95 °C	Environment: –40 °C to +85 °C
Housing temperature other ICs	−40 °C to +85 °C	-
Permitted storage temperature TQMa28L	−40 °C to +85 °C	-
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

7.6 Environment protection

7.6.1 RoHS compliance

The TQMa28L is manufactured RoHS compliant.

- All components used and assemblies are RoHS compliant
- RoHS compliant soldering processes are used

7.6.2 WEEE regulation

The company placing the product on the market is responsible for the observance of the WEEE regulation.

7.6.3 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.



8. APPENDIX

8.1 References

Table 43: Further applicable documents

No.	Description	Rev. / Date	Company
(1)	i.MX28 Applications Processor Reference Manual	Rev. 2, 08/2013	<u>Freescale</u>
(2)	Datasheet i.MX28 Applications Processors for Consumer Products	Rev. 3, 07/2012	<u>Freescale</u>
(3)	Chip Errata for the i.MX28	Rev. 2, 09/2012	<u>Freescale</u>
(4)	Application Note AN4199	Rev. 1, 03/2013	<u>Freescale</u>
(5)	TQMa28-MBa28 Tech Note	Rev. 0102	TQ-Systems