COM Express™ conga-TCA3

3rd Generation Intel® Atom™ and Intel® Celeron® SoC

User's Guide

Revision 1.1

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2014.01.09	AEM	• Preliminary release
0.2	2014.07.04	AEM	• Deleted the variant equipped with Intel Celeron N2920 (PN: 047306) from sections 1, 2.1 and 2.5. • Added industrial variant with PN: 047312 to conga-TCA3 Options Information in section 1 "Introduction". • Updated the notes in section 2.1 "Feature List" and section 6.1.2 "Low Voltage Memory". Added note in section 2.2 "Supported OS". • Updated caution notes in sections 2.7 "Environmental Specifications" and 4 "Heatspreader". Updated section 7.3 "USB Port Mapping". • Deleted support for MIPI interfaces from the whole document.
1.0	2014.09.23	AEM	• Added UART interface to the block diagram and to section 2.1 "Feature List". • Updated section 5.1.13 "General Purpose Serial Interface". • Deleted the conga-TCA3 PWR_OK input circuitry in section 5.1.14 "Power Control" because the circuitry is not implemented in conga-TCA3. • Added note about the configuration of fan_pwm pin as push-pull in section 6.1.3.3 "Fan Control" and table 14 "Miscellaneous Signal Description". • Updated section 7.1.1.1 "Intel Virtualization Technology". • Deleted the active cooling sub-section from section 7.1.1.3 "Thermal Management" because the BIOS does not support this feature. • Added sections 9 "System Resources", 10 "BIOS Setup Description" and 11 "Additional BIOS Features". • Official release
1.1	2015.04.15	AEM	• Updated the note in section 2.2 "Supported Operating Systems". • Added note about Intel's HSIC errata (USB ports 4-7 reset) to sections 5.1.4 "USB 2.0" and 7.3 "USB Port Mapping".

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-TCA3. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide

COM Express™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHz	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
DDC	Display Data Channel
SoC	System On Chip
LVDS	Low-Voltage Differential Signaling
Gbe	Gigabit Ethernet
eMMC	Embedded Multi-media Controller
HDA	High Definition Audio
cBC	congatec Board Controller
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

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1 Introduction

COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available today. COM Express™ modules are available in following form factors:

- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x 110mm

The COM Express™ specification 2.1 defines seven different pinout types.

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports	USB 2.0/ USB 3.0	Display Interfaces
Type 1	A-B	Up to 6			1	8 / 0	VGA, LVDS
Type 2	A-B C-D	Up to 22	32 bit	1	1	8 / 0	VGA, LVDS,PEG/SDVO
Type 3	A-B C-D	Up to 22	32 bit		3	8 / 0	VGA,LVDS,PEG/SDVO
Type 4	A-B C-D	Up to 32		1	1	8 / 0	VGA,LVDS,PEG/SDVO
Type 5	A-B C-D	Up to 32			3	8 / 0	VGA,LVDS,PEG/SDVO
Type 6	A-B C-D	Up to 24			1	8 / 4	VGA,LVDS,PEG, 3x DDI
Type 10	A-B	Up to 4			1	8 / 2	1x DDI, Single 24bit LVDS/eDP

conga-TCA3 module is based on the Type 6 pinout definition. They are equipped with two high performance connectors that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are a legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 6 pinout provides the ability to offer PCI Express, Serial ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use

of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

conga-TCA3 Options Information

The conga-TCA3 is available in 10 variants (six commercial and four industrial).This user's guide describes all of these variants. The table below shows the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

conga-TCA3 (commercial variants)

Part-No.	047302	047303	047305	047300	047301	047304
Processor	Intel® Atom™ E3826 (Dual Core, 1.46 GHz)	Intel® Atom™ E3825 (Dual Core, 1.33 GHz)	Intel® Celeron® J1900 (Quad Core, 2.0 GHz)	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Atom™ E3827 (Dual Core, 1.75 GHz)	Intel® Atom™ E3815 (Single Core, 1.46 GHz)
L2 Cache	1 MB	1 MB	2 MB	2 MB	1 MB	512kB
Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics
GFX Normal/Burst	533 / 667	533 / N/A	688 / 854	542 / 792	542 / 792	400 / N/A
LVDS	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit
DDI	DP / HDMI / DVI	DP / HDMI / DVI	DP / HDMI / DVI	DP / HDMI / DVI	DP / HDMI / DVI	DP / HDMI / DVI
Memory (DDR3L)	1066 MT/s dual channel	1066 MT/s single channel	1333 MT/s dual channel	1333 MT/s dual channel	1333 MT/s dual channel	1066 MT/s single channel
Max. TDP / SDP	7 W	6 W	10 W	10 W	8 W	5 W

conga-TCA3 (Industrial variants)

Part-No.	047310	047311	047312	047314
Processor	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Atom™ E3827 (Dual Core, 1.75 GHz)	Intel® Atom™ E3826 (Dual Core, 1.46 GHz)	Intel® Atom™ E3815 (Single Core, 1.46 GHz)
L2 Cache	2 MB	1 MB	1 MB	512kB
Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics
GFX Normal/Burst	542 / 792	542 / 792	533 / 667	400 / N/A
LVDS	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit
DDI	DP / HDMI / DVI	DP / HDMI / DVI	DP / HDMI / DVI	DP / HDMI / DVI
Memory (DDR3L)	1333 MT/s dual channel	1333 MT/s dual channel	1066 MT/s dual channel	1066 MT/s single channel
Max. TDP	10 W	8 W	7 W	5 W

2 Specifications

2.1 Feature List

Table 1 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 6 Rev. 2.1 (Compact size 95 x 95mm)	
Processor	Intel®Atom™ E3845 1.91GHz Quad Core processor with 2MB L2 cache and 10W TDP Intel® Atom™ E3827 1.75GHz Dual Core processor, with 1MB L2 cache and 8W TDP Intel® Atom™ E3826 1.46GHz Dual Core processor, with 1MB L2 cache and 7W TDP Intel® Atom™ E3825 1.33GHz Dual Core processor, with 1MB L2 cache and 6W TDP Intel® Atom™ E3815 1.46GHz Single Core processor, with 512kB L2 cache and 5W TDP Intel® Celeron J1900 2 GHz Quad Core processor, with 2MB L2 cache and 10W TDP	
Memory	Single or dual channel non-ECC DDR3L memory interface (up to two SO-DIMM sockets) with up to 8 GB and data rates up to 1333 MT/s. Variants equipped with Intel Atom E3815 and E3825 feature single channel memory interface and therefore support only one memory socket. For more information, see conga-TCA3 Options Information table on page 11.	
Chipset	Integrated in SoC	
Onboard Storage	Optional eMMC 4.5 onboard flash up to 64 GB (optional only for Intel® Atom™ variants)	
Audio	High Definition Audio (HDA)/digital audio interface with support for multiple codecs.	
Ethernet	Gigabit Ethernet via the onboard Intel® I210 Gigabit Ethernet controller.	
Graphics Options	Intel® HD Graphics Gen. 7, full hardware acceleration for MPEG2, H.264, DirectX11, OCL 1.2, OGL 3.2, WMV9 and VC1. Dual simultaneous display support.	
	LVDS (Integrated flat panel interface with 25-112MHz single/dual-channel LVDS transmitter) Supports: - Single-channel LVDS interface: 1 x 18 bpp or 1 x 24 bpp. - Dual-channel LVDS interface : 2 x 18 bpp or 2 x 24 bpp. - VESA LVDS color mappings - Automatic Panel Detection via Embedded Panel Interface based on VESA EDID™ 1.3. - Resolution up to 1920x1200 in dual LVDS bus mode. Optional eDP interface **NOTE**: Either eDP or LVDS signals supported. Both not supported.	2x DDI (Digital Display Interface) with support for - 2x DisplayPort 1.1. Multiplexed with HDMI/DVI ports. Supports Hot-Plug detect. - 2x HDMI 1.4 port. Multiplexed with DisplayPort (DP)/DVI. Supports Hot-Plug detect - 2x DVI ports. Multiplexed with HDMI/DP ports. Supports Hot-Plug detect. **NOTE**: The second DDI channel is only available if LVDS is not used.
Peripheral Interfaces	2x Serial ATA® up to 3Gb/s 5x PCI Express® Gen2 links up to 5.0 GT/s per lane USB Interfaces - 8x USB 2.0 - 1x USB 3.0 1x SD/MMC	2x UART GPIOs muxed with SD card SPI Bus LPC Bus I²C Bus, multimaster

BIOS	AMI Aptio® UEFI 2.x firmware; 8 MByte serial SPI with congatec Embedded BIOS features (OEM Boot Logo, OEM Default Settings, LCD Control, Display Auto Detection, Backlight Control, Flash Update)
Power Management	ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).
congatec Board Controller	Multi Stage Watchdog, non-volatile User Data Storage, Manufacturing and Board Information, Board Statistics, BIOS Setup Data Backup, I²C bus (fast mode, 400 kHz, multi-master), Power Loss Control

Note

Some of the features mentioned in the above Feature Summary are optional and requires customized article. Check the part number of your module and compare it to the option information list on page 11 to determine what options are available on your particular module. For more information, contact congatec support.

The conga-TCA3 supports only DDR3L memory modules and the memory modules in the sockets must be symmetrical - that is, same raw cards and same memory sizes. This is because the Bay Trail SoC on the conga-TCA3 does not support mixed raw cards or same raw cards with mixed memory sizes. Although the conga-TCA3 might boot up with asymmetrical memory modules, this may however cause memory errors or instabilities. Therefore use only symmetrical DDR3L memory modules on the conga-TCA3 and also make sure the memory module supports the data transfer rate of the particular variant.

In addition, if you use only one memory module then you must insert this memory module only in the first memory slot of the conga-TCA3 (top side). Due to the Bay Trail architecture, the conga-TCA3 will ignore the second memory socket (bottom side) if the first memory slot is not populated. This means that you cannot boot up the conga-TCA3 if the first memory slot is empty. See Bay Trail datasheet for more information.

2.2 Supported Operating Systems

The conga-TCA3 supports the following operating systems:

- Microsoft® Windows® 8
- Microsoft® Windows® Embedded Standard 8
- Microsoft® Windows® 7
- Microsoft® Windows® Embedded Standard 7
- Microsoft® Windows® Embedded Compact 7
- Linux (Timesys Fedora 18)

Note

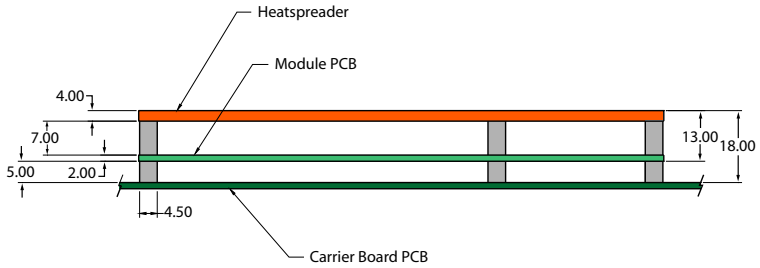
Intel does not currently provide validated eMMC and SD drivers for Win 7/WES7.

For the installation of Windows 7/8 and WES7/8, congatec AG requires a minimum storage capacity of 16 GB. congatec will not offer

installation support for systems with less than 16 GB storage space.

2.3 Mechanical Dimensions

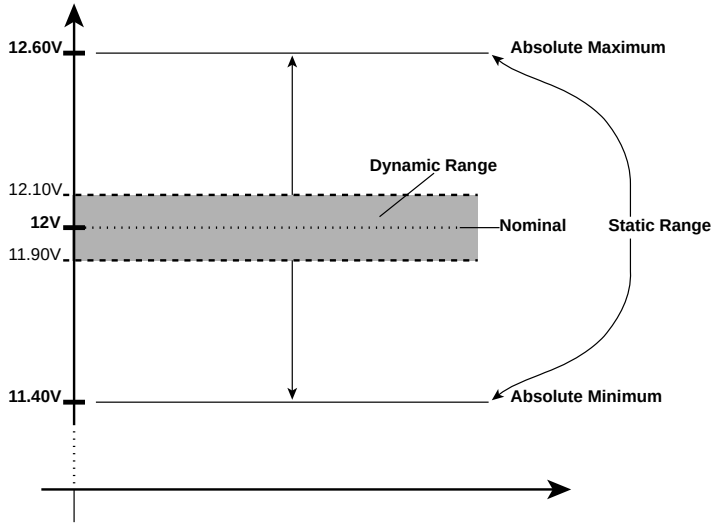
- 95.0 mm x 95.0 mm (3.75" x 3.75")
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm



2.4 Supply Voltage Standard Power

- 12V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used for testing includes a conga-TCA3 module, congatec debug carrier board, TFT monitor, SATA drive, and USB keyboard. The SATA drive was powered externally by an ATX power supply so that it does not influence the power consumption value that is measured for the module. The USB keyboard was detached once the module was configured within the OS. All recorded values were averaged over a 30 second time period. Cooling of the module was done by the module specific heatspreader and a fan cooled heatsink to measure the power consumption under normal thermal conditions.

Each module was measured while running Windows 7 Professional 32Bit, Hyper Threading enabled, Speed Step enabled and Power Plan set to “Power Saver”. This setting ensures that Core processors run in LFM (lowest frequency mode) with minimal core voltage during desktop idle. Each module was tested while using 2GB symmetrical memory modules (congatec AG does not recommend asymmetrical memory modules).

To measure the worst case power consumption the cooling solution was removed and the CPU core temperature was allowed to run up to between 95° and 100°C while running 100% workload with the Power Plan set to “Balanced”. The peak current value was then recorded. This value should be taken into consideration when designing the system's power supply to ensure that the power supply is sufficient during worst case scenarios.

Power consumption values were recorded during the following stages:

Windows 7 (32 bit)

- Desktop Idle (power plan = Power Saver)
- 100% CPU workload (see note below, power plan = Power Saver)
- 100% CPU workload at approximately 100°C peak power consumption (power plan = Balanced)
- Suspend to RAM. Supply power for S3 mode is 5V.

Note

A software tool was used to stress the CPU to maximum frequency.

Processor Information

The tables below provide additional information about the power consumption data for each of the conga-TCA3 variants offered. The values are recorded at various operating modes.

2.5.1 conga-TCA3 Intel® Atom™ E3845 Quad Core 1.91 GHz 2MB Cache

With dual memory sockets (10W Max. TDP)

conga-TCA3 Art. No. 047300 (Commercial) conga-TCA3 Art. No. 047310 (Industrial)	Intel® Atom™ E3845 Quad Core 1.91 GHz 2MB L2 Cache (22nm). Layout Rev. TA30LA0 /BIOS Rev. TA30R000				
Memory Size	2GB				
Operating System	**Windows 7 (64 bit)**				
Power State	Desktop Idle	100% CPU Workload [W]	100% CPU & 100% GPU Workload [W]	Max. Power Consumption (Worst Case)	Suspend to Ram (S3) 5V SB Input
Power Consumption (Amps. /Watts)	0.40A / 4.79 W	0.69A / 8.23 W	1.01A / 12.13 W	1.08A / 12.90 W	0.17A / 0.85 W

2.5.2 conga-TCA3 Intel® Atom™ E3827 Dual Core 1.75 GHz 1MB Cache

With dual memory sockets (8W Max. TDP)

conga-TCA3 Art. No. 047301 (Commercial) conga-TCA3 Art. No. 047311 (Industrial)	Intel® Atom™ E3827 Dual Core 1.75 GHz 1MB L2 Cache (22nm) Layout Rev. TA30LA0 /BIOS Rev. TA30R000				
Memory Size	2GB				
Operating System	**Windows 7 (64 bit)**				
Power State	Desktop Idle	100% CPU Workload [W]	100% CPU & 100% GPU Workload [W]	Max. Power Consumption (Worst Case)	Suspend to Ram (S3) 5V SB Input
Power Consumption (Amps./Watts)	0.39A / 4.70 W	0.48A / 5.73 W	0.81A / 9.74 W	0.84A / 10.10 W	0.17A / 0.85 W

2.5.3 conga-TCA3 Intel® Atom™ E3826 Dual Core 1.46 GHz 1MB Cache

With dual memory sockets (7W Max. TDP)

conga-TCA3 Art. No. 047302	Intel® Atom™ E3826 Dual Core 1.46 GHz 1MB L2 Cache (22nm) Layout Rev. TA30LA0 /BIOS Rev. TA30R000				
Memory Size	2GB				
Operating System	**Windows 7 (64 bit)**				
Power State	Desktop Idle	100% CPU Workload [W]	100% CPU & 100% GPU Workload [W]	Max. Power Consumption (Worst Case)	Suspend to Ram (S3) 5V SB Input
Power Consumption (Amps./Watts)	0.38A / 4.54 W	0.47A / 5.69 W	0.75A / 8.94 W	0.75A / 8.94 W	0.17A / 0.86 W

2.5.4 conga-TCA3 Intel® Atom™ E3825 Dual Core 1.33 GHz 1MB Cache

With single memory socket (6W Max. TDP)

conga-TCA3 Art. No. 047303	Intel® Atom™ E3825 Dual Core 1.33 GHz 1MB L2 Cache (22nm) Layout Rev. TA30LA0 /BIOS Rev. TA30R000				
Memory Size	2GB				
Operating System	**Windows 7 (64 bit)**				
Power State	Desktop Idle	100% CPU Workload [W]	100% CPU & 100% GPU Workload [W]	Max. Power Consumption (Worst Case)	Suspend to Ram (S3) 5V SB Input
Power Consumption (Amps./Watts)	0.36A / 4.28 W	0.43A / 5.19 W	0.63A / 7.54 W	0.65A / 7.82 W	0.17A / 0.84 W

2.5.5 conga-TCA3 Intel® Atom™ E3815 Single Core 1.46 GHz 512KB Cache

With single memory socket (5W Max. TDP)

conga-TCA3 Art. No. 047304 (Commercial) conga-TCA3 Art. No. 047314 (Industrial)	Intel® Atom™ E3815 Single Core 1.46 GHz 512KB L2 Cache (22nm) Layout Rev. TA30LA0 /BIOS Rev. TA30R000				
Memory Size	2GB				
Operating System	**Windows 7 (64 bit)**				
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V SB Input	Max. Power Consumption (Worst Case)	Suspend to Ram (S3) 5V SB Input
Power Consumption (Amps./Watts)	0.35A / 4.22 W	0.40A / 4.75 W	0.53A / 6.38 W	0.59A / 7.11 W	0.18A / 0.90 W

2.5.6 conga-TCA3 Intel® Celeron® J1900 Quad Core 2.0 GHz 2MB Cache

With dual memory sockets (10W Max. TDP)

conga-TCA3 Art. No. 047305	Intel® Celeron® J1900 Quad Core 2.0 GHz 2MB L2 Cache (22nm) Layout Rev. TA30LA0 /BIOS Rev. TA30R000				
Memory Size	2GB				
Max. Turbo Freq.	2.42 GHz				
Operating System	**Windows 7 (64 bit)**				
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V SB Input	Max. Power Consumption (Worst Case)	Suspend to Ram (S3) 5V SB Input
Power Consumption (Amperes/Watts)	0.40A / 4.74 W	0.89A / 10.73 W	1.33A / 15.92 W	1.33A / 15.92 W	0.18A / 0.88 W

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Supply power for S3 mode is 5V while all other measured modes are supplied with 12V power. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

2.6 Supply Voltage Battery Power

- 2.0V-3.5V DC
- Typical 3V DC

2.6.1 CMOS Battery Power Consumption

RTC @ 20°C	Voltage	Current
Integrated in the SoC	3V DC	1.85 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

2.7 Environmental Specifications

Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -45° to +85°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

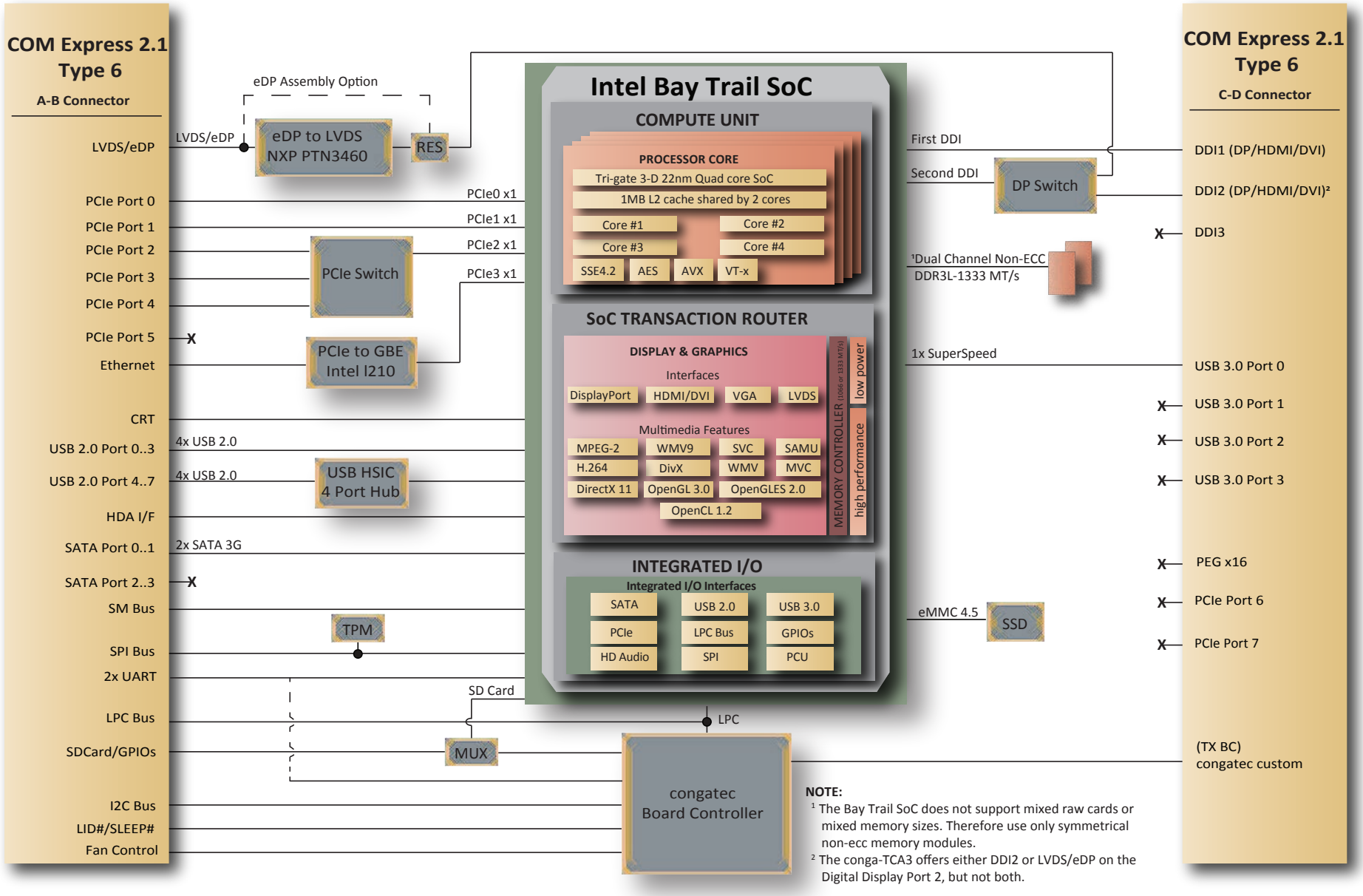
Caution

The above operating temperatures must be strictly adhered to at all times. The congatec heatspreader is only suitable for use within commercial temperature ranges (0° to 60°). It is not designed to be used within industrial temperature ranges (-40° to 85°). When using a heatspreader with conga-TCA3 commercial grade variants, the max. operating temperature refers to any measurable spot on the heatspreader's surface.

congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution when used in a commercial temperature range. If for some reason it is not possible to use the appropriate congatec module heatspreader as a thermal interface for conga-TCA3 commercial grade variants or if an industrial grade variant of conga-TCA3 is being used within industrial temperature ranges, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



NOTE:

[1] The Bay Trail SoC does not support mixed raw cards or mixed memory sizes. Therefore use only symmetrical non-ecc memory modules.

[2] The conga-TCA3 offers either DDI2 or LVDS/eDP on the Digital Display Port 2, but not both.

4 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module and The heatspreader acts as a thermal coupling device to the module and is thermally coupled to the CPU via a thermal gap filler. On some modules, it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis thereby using the whole chassis as a heat dissipater.

For additional information about the conga-TCA3 heatspreader, refer to section 4.1 of this document.

Caution

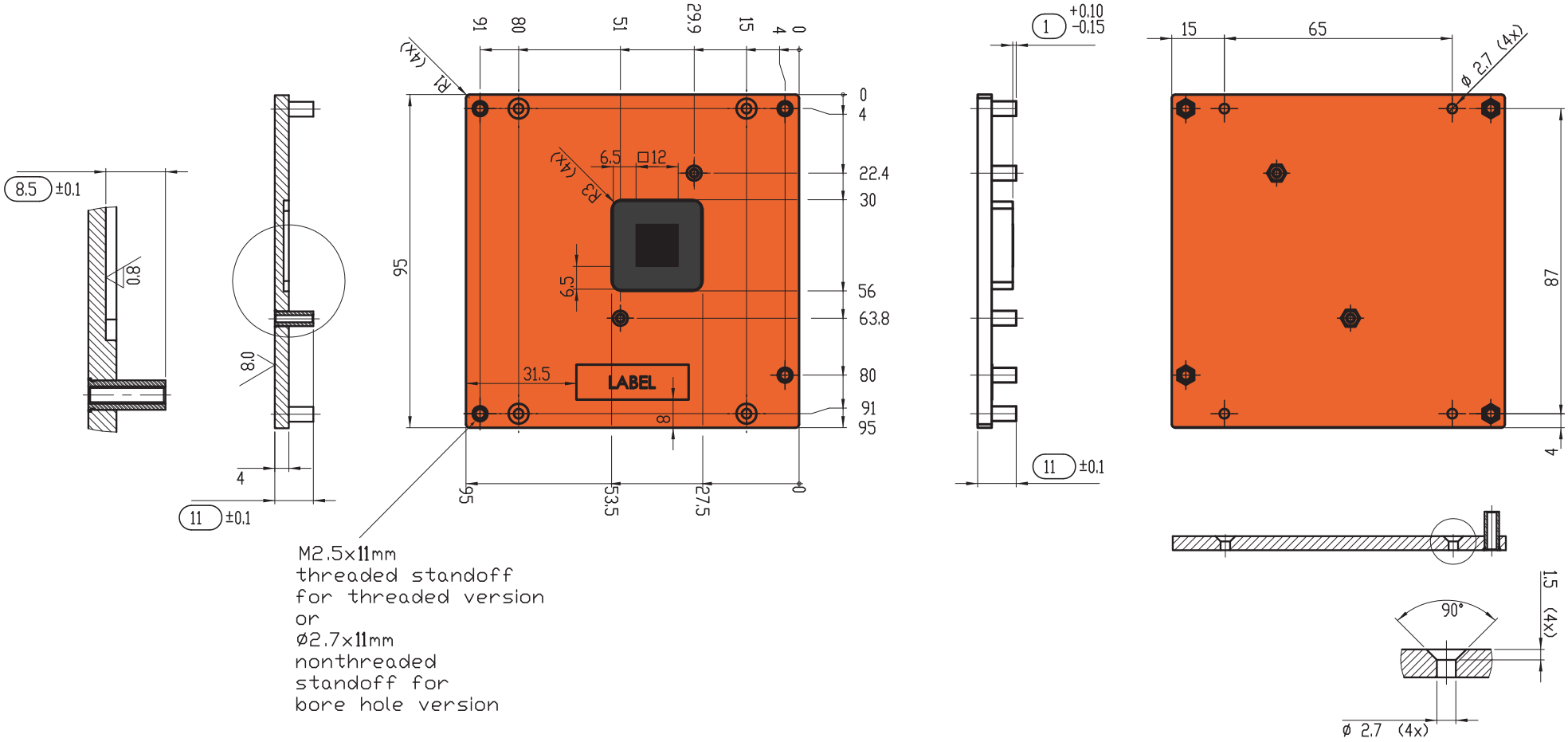
congatec heaspreaders have been specifically designed for use within commercial temperature ranges (0° to 60°C) only. When using industrial temperature variants of the conga-TCA3 in industrial temperature ranges (-40° to 85°C), use of the conga-TCA3 heatspreaders is not recommended by congatec. Its use is at the risk of the end user.

It is the responsibility of the end user to design an optimized thermal solution that meets the needs of their application within the industrial environmental conditions it is required to operate in. Attention must be given to the mounting solution used to mount the heatspreader and module to the system carrier board. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

Only heatspreaders that feature fixing post that secure the thermal stacks should be used for applications that require the heatspreader to be mounted vertically. It cannot be guaranteed that the thermal stacks will not move if a heatspreader that does not have the fixing post feature is used in applications mounted vertically.

Additionally, the gap pad material used on all heatspreaders contains silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.

4.1 Heatspreader Dimensions



Note

All measurements are in millimeters. Torque specification for heatspreader screws is 0.3 Nm. Mechanical system assembly mounting shall follow the valid DIN/IS0 specifications.

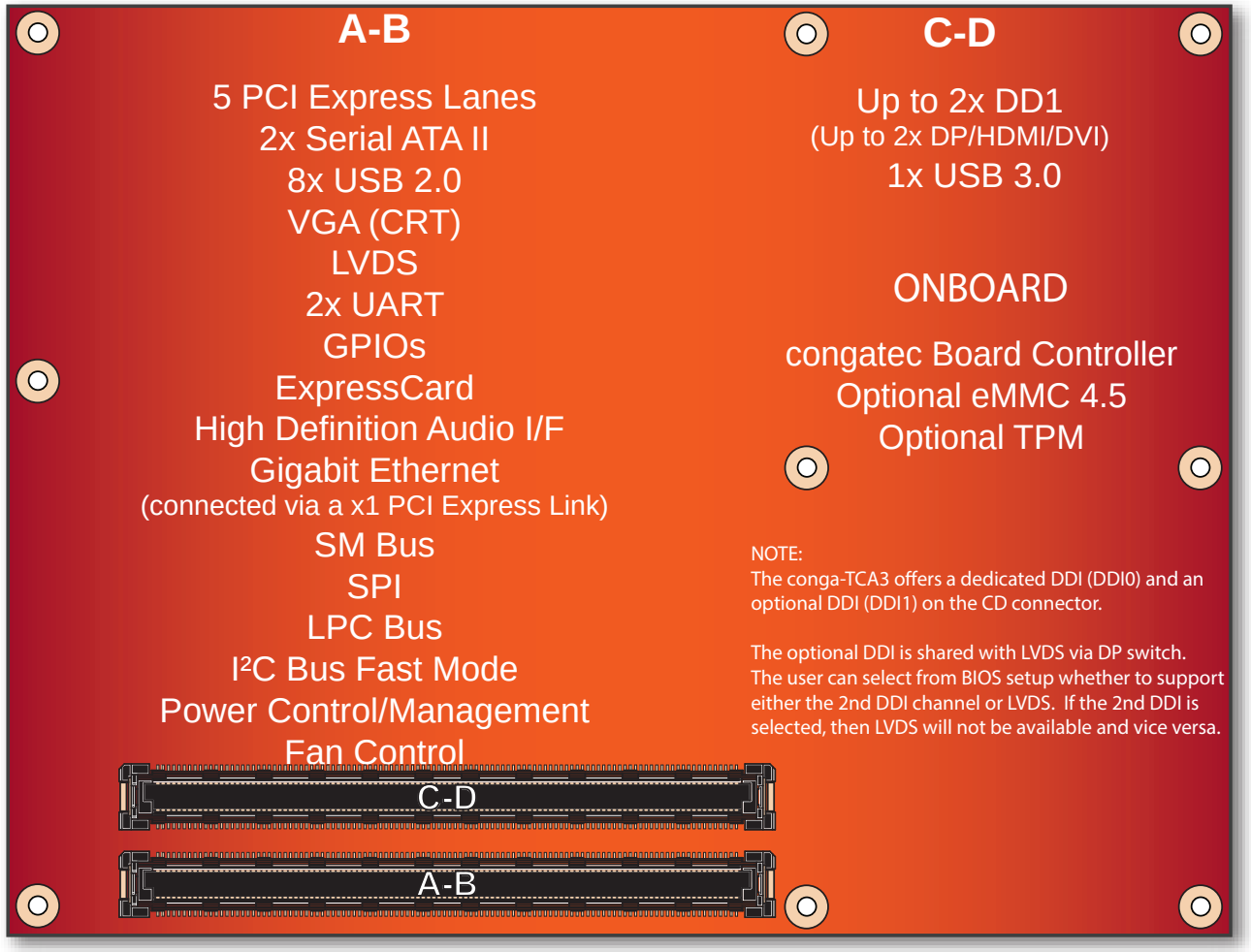
Caution

When using the heatspreader in a high shock and/or vibration environment, congatec recommends the use of a thread-locking fluid on the heatspreader screws to ensure the above mentioned torque specification is maintained.

5 Connector Subsystems Rows A, B, C, D

The conga-TCA3 is connected to the carrier board via two 220-pin connectors (COM Express Type 6 pinout) for a total of 440 pins connectivity. These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.

In this view the connectors are seen “through” the module.



top view

5.1 Primary Connector Rows A and B

The following subsystems can be found on the primary connector rows A and B.

5.1.1 PCI Express™

The conga-TCA3 offers 5 PCI Express externally on connector rows A-B. The lanes are Gen 2 compliant and offer support for full 5 Gb/s bandwidth in each direction per x1 link. Default configuration for the lanes on the A-B connector is 5 x1 link. A 3 x1 + 1 x2 link configuration is also possible but requires a special/customized BIOS firmware. Contact congatec technical support for more information about this subject.

The PCI Express interface is based on the PCI Express Specification 2.0 with Gen 1 (2.5Gb/s) and Gen 2 (5 Gb/s) speed. For more information refer to the conga-TCA3 pinout table in section 8 "Signal Descriptions and Pinout Tables."

5.1.2 Gigabit Ethernet

The conga-TCA3 offers a Gigabit Ethernet interface on connector rows A-B via the onboard Intel® I210 Gigabit Ethernet controller. This controller is connected to the Intel® Bay Trail SoC through the fourth PCI Express lane. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

5.1.3 Serial ATA™ (SATA)

The conga-TCA3 offers two SATA interfaces on connector rows A-B via a SATA host controller integrated in the Intel® Bay Trail SoC. The controller supports independent DMA operation and data transfer rates of 1.5 Gb/s and 3.0 Gb/s. It also supports two modes of operation - a legacy mode and AHCI mode. Software that uses legacy mode will not have AHCI capabilities.

For more information, refer to section 10 "BIOS Setup Description".

5.1.4 USB 2.0

The conga-TCA3 offers 8 USB 2.0 interfaces on connector rows A-B. Four of these ports are routed directly from the SoC to the A-B connector. The other four are routed to the A-B connector via a 4-port USB HSIC hub.

The EHCI host controller in the SoC supports these interfaces with high-speed, full-speed and low-speed USB signalling. The controller complies with USB standard 1.1 and 2.0. For more information about how the USB host controllers are routed, see section 7.3.

Note

According to an Intel Errata, the SoC's HSIC port 0 is reset and re-enumerated when a device is connected or disconnected from USB port 0 during runtime. For this reason, end users should not disconnect or connect any USB device to USB port 0 at runtime. Doing so may cause USB ports 4-7 (ports routed via USB 2.0 hub) to malfunction.

5.1.5 High Definition Audio (HDA) Interface

The conga-TCA3 provides an interface that supports the connection of HDA audio codecs.

5.1.6 LPC Bus

The conga-TCA3 offers the LPC (Low Pin Count) bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals and functionality. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific carrier board using this bus. Only certain devices such as Super I/O or TPM 1.2 chips can be implemented on the carrier board. See section 9.1.1 for more information about the LPC Bus

Note

The conga-TCA3 Atom variants operate at a frequency of 33 MHz and the Celeron variants at 25 MHz.

5.1.7 I²C Bus

The I²C bus is implemented through the congatec board controller. It provides a Fast Mode multi-master I²C Bus at runs at fast mode.

5.1.8 ExpressCard™

The conga-TCA3 supports the implementation of ExpressCards, which requires the dedication of one USB port and a x1 PCI Express link for each ExpressCard used.

5.1.9 Graphics Output (VGA/CRT)

The conga-TCA3 offers one VGA interface on the A-B connector rows. The VGA port provides RGB signal output as well as HSYNC and VSYNC signal, with dedicated DDC signal pair. The analog VGA display interface has a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics engine to analog data for the VGA monitor. The 320 MHz RAMDAC integrated in the SoC

supports resolution up to 2560 x 1600 at 60 Hz refresh rate.

5.1.10 LVDS

The conga-TCA3 offers a single/dual channel LVDS interface on the A-B connector rows. The interface is provided by routing the onboard PTN3460 to the SoC's second Digital Display Interface, via a DisplayPort switch. With the integration of the DisplayPort switch, the conga-TCA3 can be configured in the BIOS to support either LVDS on the A-B connector or a second Digital Display Interface on the C-D connector.

The PTN3460 processes incoming DisplayPort stream, converts the DP protocol to LVDS protocol and transmits the processed stream in LVDS format. It supports single and dual channel signalling with color depths of 18 bits or 24 bits per pixel and pixel clock frequency up to 112 MHz. It also supports automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3, with resolution up to 1920x1200 in dual LVDS mode.

Note

The LVDS interface is available only if the optional COM Express Digital Display Interface (DDI2) is not used.

5.1.11 SPI

An SPI interface that supports booting from an external SPI flash is available on the conga-TCA3 via the Intel® Bay Trail SoC . The conga-TCA3 implements an SPI interface as an alternative interface for the BIOS flash device. An SPI flash device can be used as a replacement for the Firmware Hub.

5.1.12 SD Card

The conga-TCA3 offers a 4-bit SD interface for SD/MMC cards on the A-B connector. The SD signals are multiplexed with GPIO signals and controlled by the congatec Board controller. The SD card controller in the Storage Control Cluster of the SoC supports the SD interface with up to 832 Mb/s data rate using 4 parallel data lines.

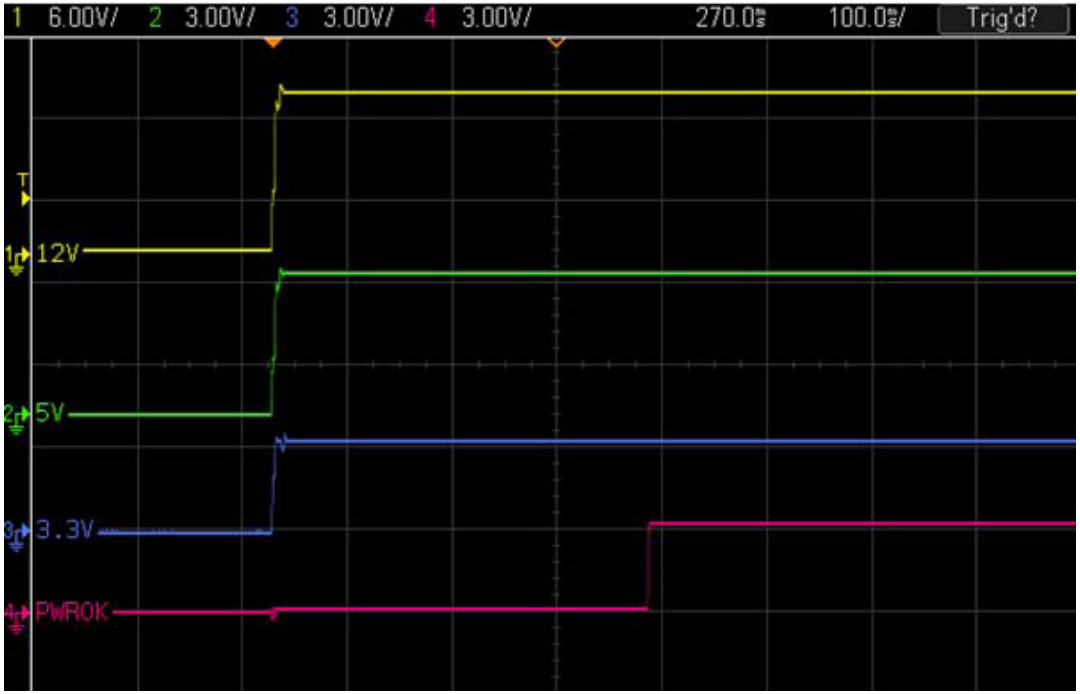
5.1.13 General Purpose Serial Interface (UART)

The conga-TCA3 offers two UART interfaces. The pins are designated SER0_TX, SER0_RX, SER1_TX and SER1_RX. Data out of the module is on the _TX pins. Hardware handshaking and hardware flow control are not supported. See table 17 of section 8 "Signal Descriptions and Pinout Tables" for the signal description.

5.1.14 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system. See screenshot below.



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The conga-TCA3 provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-TCA3's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

12 volt input power is the sole operational power source for the conga-TCA3. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-TCA3 application:

- It has also been noticed that on some occasions, problems occur when using a 12V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document “ATX12V Power Supply Design Guide V2.2”.

5.1.15 Power Management

ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

5.2 Secondary Connector Rows C and D

The following subsystems can be found on the secondary connector rows C and D.

5.2.1 USB 3.0

The conga-TCA3 offers one USB 3.0 interface on the C-D connector. This interface is controlled by an xHCI host controller in the SoC. The host controller allows data transfers of up to 5 Gb/s and supports SuperSpeed, high-speed, full-speed and low-speed USB signalling. See section 7.3 for more information about USB port mapping.

Note

The USB 3.0 port should be paired with USB 2.0 port 0 on the carrier board.

5.2.2 Digital Display Interface

The conga-TCA3 offers up to two Digital Display interfaces - a dedicated DDI (DDI1) and an optional DDI (DDI2). The dedicated DDI is available by default and is provided by routing the first Digital Display Interface of the SoC directly to the conga-TCA3 C-D connector rows. The optional DDI is provided via an onboard DisplayPort switch, connected to the SoC's second DDI port. With this switch, the SoC's second DDI port can be configured via BIOS to either support a second DDI interface on the C-D connector or an LVDS interface on the A-B connector.

The conga-TCA3 supports eDP 1.3, DP 1.1a, DVI or HDMI 1.4a, audio on DP and HDMI, High-bandwidth Digital Content Protection 1.4/2.1 and up to two independent displays. The display combinations supported are shown below:

Table 2 Display Combination

Display 1	Display 2	Display 1 (Max. Resolution)	Display 2 (Max. Resolution)
DDI	LVDS or Optional DDI	1920x1200 @60Hz (HDMI/DVI) 2560x1600 @60Hz (DP)	1920x1200 @60Hz (dual LVDS mode)
DDI	VGA	1920x1200 @60Hz (HDMI/DVI) 2560x1600 @60Hz (DP)	2560x1600 @60Hz
LVDS or Optional DDI	DDI	1920x1200 @60Hz (dual LVDS mode).	1920x1200 @60Hz (HDMI/DVI) 2560x1600 @60Hz (DP)
LVDS or Optional DDI	VGA	1920x1200 @60Hz (dual LVDS mode).	2560x1600 @60Hz
VGA	DDI	2560x1600 @60Hz	1920x1200 @60Hz (HDMI/DVI) 2560x1600 @60Hz (DP)
VGA	LVDS or Optional DDI	2560x1600 @60Hz	1920x1200 @60Hz (dual LVDS mode)

5.2.3 HDMI

High-Definition Multimedia Interface (HDMI) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video.

The conga-TCA3 can support up to two HDMI interfaces - a dedicated HDMI interface and an optional HDMI interface. The dedicated interface is supported by default while the optional interface requires the BIOS setup configuration. If the BIOS is configured to support the optional HDMI interface, then conga-TCA3 will not support LVDS. See section 5.2.2 "Digital Display Interface" for more information.

The supported resolution is up to 1920x1200@60Hz.

Note

See table 2 above for possible display combinations.

5.2.4 DVI

The DVI is similar to HDMI in the way it uses TMDS for transmitting data from transmitter to the receiver but unlike the HDMI, does not support audio and CEC.

The conga-TCA3 can support up to two DVI interfaces - a dedicated DVI and an optional DVI interface. The dedicated interface is supported by default while the optional interface requires the BIOS setup configuration. If the BIOS is configured to support the optional DVI interface, then conga-TCA3 will not support LVDS. See section 5.2.2 "Digital Display Interface" for more information.

The supported resolution is up to 1920x1200@60Hz.

Note

See table 2 above for possible display combinations.

5.2.5 DisplayPort (DP)

DisplayPort is an open, industry standard digital display interface, that has been developed within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

The conga-TCA3 can support up to two DP interfaces - a dedicated DP interface and an optional DP interface. The dedicated interface is

supported by default while the optional interface requires the BIOS setup configuration. If the BIOS is configured to support the optional DP interface, then conga-TCA3 will not support LVDS. See section 5.2.2 "Digital Display Interface" for more information.

The supported resolution is up to 2560x1600@60Hz.

Note

See table 2 above for possible display combinations.

6 Additional Features

6.1 Onboard Interfaces

6.1.1 eMMC 4.5

The conga-TCA3 offers an optional eMMC 4.5 flash onboard the Intel Atom variants, with up to 64 GB capacity. The conga-TCA3 celeron variants do not offer eMMC.

6.1.2 Low Voltage Memory (DDR3L)

The Bay Trail on the conga-TCA3 supports low voltage system memory interface. The memory interface I/O voltage is 1.35V and supports unbuffered DDR3L SO-DIMMs. With this low voltage system memory interface on the processor, the conga-TCA3 offers a system optimized for lowest possible power consumption. The reduction in power consumption due to lower voltage subsequently reduces the heat generated.

Note

The conga-TCA3 supports only DDR3L memory modules and the memory modules in the sockets must be symmetrical - that is, same raw cards and same memory sizes. This is because the Bay Trail SoC on the conga-TCA3 does not support mixed raw cards or same raw cards with mixed memory sizes. Although the conga-TCA3 might boot up with asymmetrical memory modules, this may however cause memory errors or instabilities. Therefore use only symmetrical DDR3L memory modules on the conga-TCA3 and also make sure the memory module supports the data transfer rate of the particular variant.

In addition, if you use only one memory module then you must insert this memory module only in the first memory slot of the conga-TCA3 (top side). Due to the Bay Trail architecture, the conga-TCA3 will ignore the second memory socket (bottom side) if the first memory slot is not populated. This means that you cannot boot up the conga-TCA3 if the first memory slot is empty. For more information, consult the Bay Trail datasheet.

6.1.3 congatec Board Controller (cBC)

The conga-TCA3 is equipped with a Texas Instruments Tiva™ TM4E1231H6ZRBI microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

6.1.3.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.1.3.2 General Purpose Input/Output

The conga-TCA3 offers general purpose inputs and outputs for custom system design. These GPIOs are multiplexed with SD signals and are controlled by the cBC.

6.1.3.3 Fan Control

The conga-TCA3 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

A four wire fan must be used to generate the correct speed readout.

The congatec COM Express Type 6 and Type 10 modules use a Push-Pull output for the fan_pwm signal instead of the open drain output specified in the COM Express specification. Although this does not comply with the COM Express specification 2.0, the benefits are obvious. The Push-Pull output optimizes the power consumed by the fan_pwm signal without functional change.

6.1.3.4 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

6.1.3.5 Watchdog

The conga-TCA3 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-TCA3 does not support external hardware triggering. For more information about the Watchdog feature see the BIOS setup description section 10.4.2 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

Note

The conga-TCA3 module does not support the watchdog NMI mode. COM Express type 6 modules do not support the PCI bus and therefore the PCI_SERR# signal is not available. There is no way to drive a NMI to the processor without the presence of the PCI_SERR# PCI bus signal.

6.1.3.6 I²C Bus

The conga-TCA3 offers support for the frequently used I²C bus. Thanks to the I²C host controller in the cBC the I²C bus is multimaster capable and runs at fast mode.

6.1.3.7 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behaviour of the system after a AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

6.1.4 Embedded BIOS

The conga-TCA3 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. These are the most important embedded PC features:

6.1.4.1 CMOS Backup in Non Volatile Memory

A copy of the CMOS memory (SRAM) is stored in the BIOS flash device. This prevents the system from not booting up with the correct system configuration if the backup battery (RTC battery) has failed. Additionally, it provides the ability to create systems that do not require a CMOS backup battery.

6.1.4.2 OEM CMOS Default Settings and OEM BIOS Logo

This feature allows system designers to create and store their own CMOS default configuration and BIOS logo (splash screen) within the BIOS flash device. Customized BIOS development by congatec for these changes is no longer necessary because customers can easily do these changes by themselves using the congatec system utility CGUTIL.

6.1.4.3 OEM BIOS Code

With the congatec embedded BIOS it is even possible for system designers to add their own code to the BIOS POST process. Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table, verb tables for HDA codecs, rare graphic modes and Super I/O controllers.

For more information about customizing the congatec embedded BIOS refer to the congatec System Utility user's guide, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com or contact congatec technical support.

6.1.5 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-TCA3 BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

6.2 API Support (CGOS/EAPI)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

Other COM (Computer on Modules) vendors offer similar driver solutions for these kind of embedded PC features, which are by nature proprietary. All the API solutions that can be found on the market are not compatible to each other. As a result, writing application software that can run on more than one vendor's COM is not so easy. Customers have to change their application software when switching to another COM vendor. EAPI (Embedded Application Programming Interface) is a programming interface defined by the PICMG that addresses this problem.

With this unified API, it is now possible to run the same application on all vendor's COMs that offer EAPI driver support. Contact congatec technical support for more information about EAPI.

6.3 Security Features

The conga-TCA3 can be equipped optionally with a "Trusted Platform Module" (TPM1.2). This TPM 1.2 includes coprocessors to calculate efficient hash and RSA algorithms with key lengths up to 2,048 bits as well as a real random number generator. Security sensitive applications like gaming and e-commerce will benefit also with improved authentication, integrity and confidence levels.

6.4 Suspend to Ram

The Suspend to RAM feature is available on the conga-TCA3.

7 conga Tech Notes

The conga-TCA3 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the system resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

7.1 Intel Bay Trail SoC Features

7.1.1 Processor Core

The Intel Bay Trail Soc features Single, Dual or Quad Out-of-Order Execution processor cores. The cores are sub-divided into dual-core modules with each module sharing a 1 MB L2 cache (512 KB per core). Some of the features supported by the core are:

- Intel 64 architecture
- Intel Streaming SIMD Extensions 4.1 and 4.2
- Support for Intel VT-x
- Thermal management support vial Intel Thermal Monitor
- Uses Power Aware Interrupt Routing
- Uses 22 nm process technology

Note

Intel Hyper-Threading technology is not supported (four cores execute four threads)

7.1.1.1 Intel Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel® VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

7.1.1.2 AHCI

The Intel Bay Trail SoC provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

Legacy Mode

When operating in legacy mode, the SATA controllers need two legacy IRQs (14 and 15) and are unable to share these IRQs with other devices. This is because the SATA controllers emulate the primary and secondary legacy IDE controllers.

Native Mode

Native mode allows the SATA controllers to operate as true PCI devices and therefore do not need dedicated legacy resources. This means they can be configured anywhere within the system. When either SATA controller 1 or 2 runs in native mode it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system. Setting "Native IDE" mode in the BIOS setup program will automatically enable Native mode. See section 10.4.9 for more information about this. Running in native mode frees up interrupt resources (IRQs 14 and 15) and decreases the chance that there may be a shortage of interrupts when installing devices.

Note

If your operating system supports native mode then congatec AG recommends you enable it.

7.1.1.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-TCA3 ACPI thermal solution offers three different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.2 ACPI Suspend Modes and Resume Events

conga-TCA3 supports S3 (STR= Suspend to RAM). For more information about S3 wake events see section 10.4.4 "ACPI Configuration Submenu".

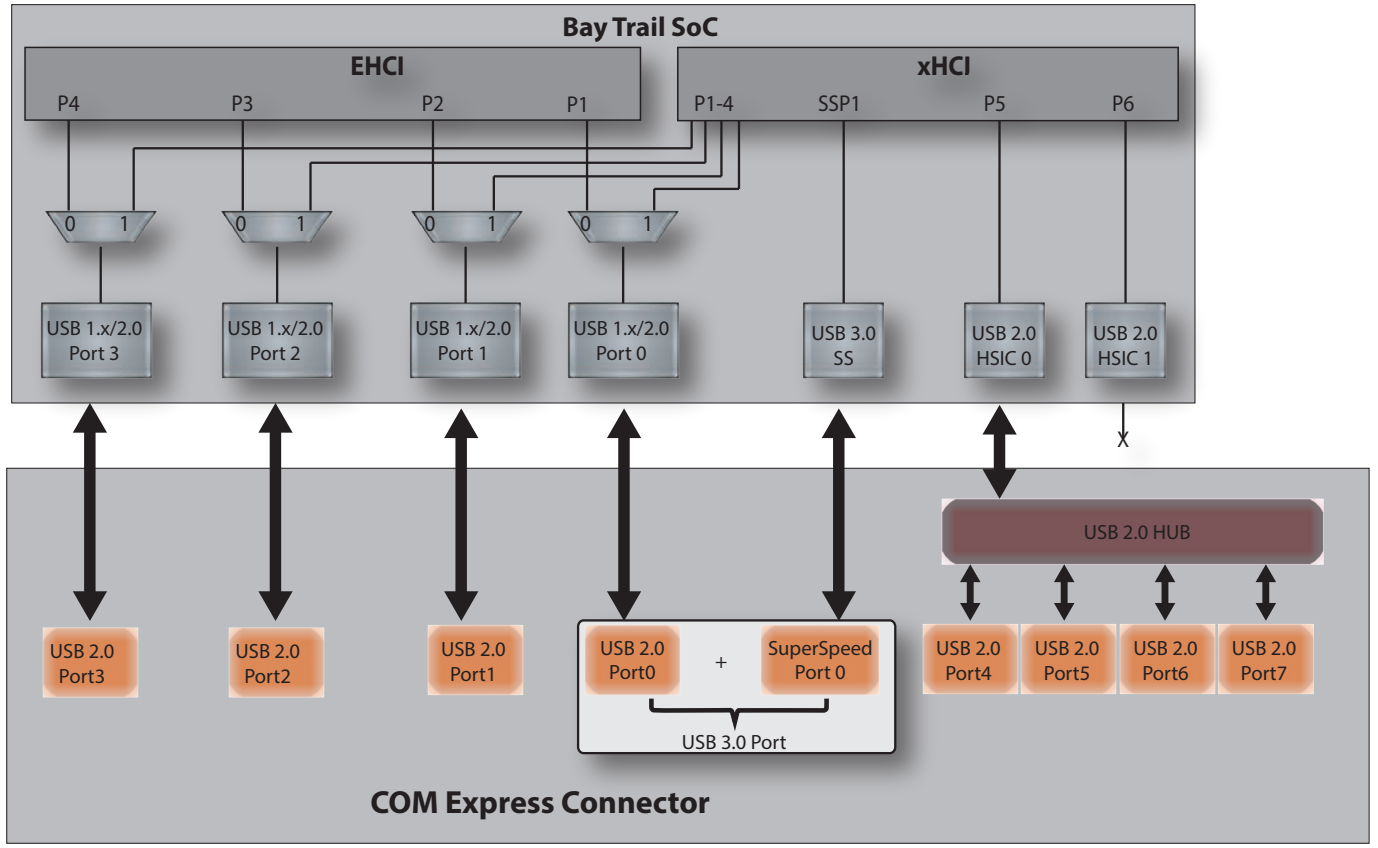
S4 (Suspend to Disk, S4_OS= Hibernate) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems:

- Windows 7, Windows Vista, Windows XP and Linux

This table lists the "Wake Events" that resume the system from S3 unless otherwise stated in the "Conditions/Remarks" column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

7.3 USB Port Mapping



NOTE:

Possible USB configurations are:

(*) Up to 8x USB 2.0
(*) Up to 7x USB 2.0 and 1x USB 3.0

Note

According to an Intel Errata, the SoC's HSIC port 0 is reset and re-enumerated when a device is connected or disconnected from USB port 0 during runtime. For this reason, end users should not disconnect or connect any USB device to USB port 0 at runtime. Doing so may cause USB ports 4-7 (ports routed via USB 2.0 hub) to malfunction.

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type VI connectors used for congatec AG modules. The pinout of the modules complies with COM Express Type 6.0 Rev. 2.1.

Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 3 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.0a
SATA	In compliance with Serial ATA specification, Revision 3.0
REF	Reference voltage output. May be sourced from a module power plane

PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

8.1 A-B Connector Signal Descriptions

Table 4 Intel® High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC/HDA_RST#	A30	**Intel® High Definition Audio Reset:** This signal is the master hardware reset to external codec(s).	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SYNC	A29	**Intel® High Definition Audio Sync:** This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_BITCLK	A32	**Intel® High Definition Audio Bit Clock Output:** This signal is a 24.000MHz serial data clock generated by the Intel® High Definition Audio controller.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SDOUT	A33	**Intel® High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SDIN[1:0]	B29-B30	**Intel® High Definition Audio Serial Data In [1:0]:** These signals are serial TDM data inputs from the two codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.	I 3.3V	100k PD	AC'97 codecs are not supported. AC/HDA_SDIN2 is not supported

Table 5 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:				I/O Analog		Twisted pair signals for external transformer.
			1000	100	10			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.				O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.				O 3.3VSB		

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.			Not connected

Table 6 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA II specification, up to 3 Gb/s
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA II specification, up to 3 Gb/s
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA II specification, up to 3 Gb/s
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA II specification, up to 3 Gb/s
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Not supported
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Not supported
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Not supported
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Not supported
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	I/O 3.3v	PU 4.99k 3.3V	

Table 7 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0.
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Not supported
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 8 ExpressCard Support Pins Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE#	A49	ExpressCard 0 capable card request.	I 3.3V	PU 10k 3.3V	
EXCD0_PERST#	A48	ExpressCard 0 Reset	O 3.3V	PU 10k 3.3V	
EXCD1_CPPE#	B48	ExpressCard 1 capable card request	I 3.3V	PU 10k 3.3V	
EXCD1_PERST#	B47	ExpressCard 1 Reset	O 3.3V	PU 10k 3.3V	

Table 9 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V		Not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3V		
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V		33 MHz with Bay Trail-I SoC (Intel Atom series) 25 MHz with Bay Trail-M/D SoC (Intel Celeron series)

Table 10 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1

Signal	Pin #	Description	I/O	PU/PD	Comment
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+	A37	USB Port 6, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6-	A36	USB Port 6, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+	B37	USB Port 7, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7-	B36	USB Port 7, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 4.99k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 4.99k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

Table 11 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/O OD 5V	PU 4k02 3.3V	
VGA_I2C_DAT	B96	DDC data line.	I/O OD 5V	PU 4k02 3.3V	

Table 12 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10k	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10k	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k0 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k0 3.3V	

Note

The LVDS signals are available only if the optional DDI (DDI2) is not used.

Table 13 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 69k8 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	+ 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10k 3.3VSB	Carrier shall pull to GND or leave no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10k 3.3VSB	Carrier shall pull to GND or leave no-connect.

Table 14 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O 3.3V	PU 2k0 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O 3.3V	PU 2k0 3.3VSB	
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V	PU 4k99 3.3V	
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PD 10k	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V		
FAN_TACHIN	B102	Fan tachometer input.	I OD	PU 10k 3.3V	Requires a fan with a two pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V		Trusted Platform Module chip is optional.

Note

The congatec COM Express Type 6 and Type 10 modules use a Push-Pull output for the fan_pwm signal instead of the open drain output specified in the COM Express specification. Although this does not comply with the COM Express specification 2.0, the benefits are obvious. The Push-Pull output optimizes the power consumed by the fan_pwm signal without functional change.

Table 15 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins. Shared with SD_CLK. Output from COM Express, input to SD	O 3.3V		
GPO1	B54	General purpose output pins. Shared with SD_CMD. Output from COM Express, input to SD	O 3.3V		
GPO2	B57	General purpose output pins. Shared with SD_WP. Output from COM Express, input to SD	O 3.3V		
GPO3	B63	General purpose output pins. Shared with SD_CD. Output from COM Express, input to SD	O 3.3V		
GPI0	A54	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal	I 3.3V	PU 10K 3.3V	Pull-up only active in GPIO mode
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3V	PU 10K 3.3V	Pull-up only active in GPIO mode
GPI2	A67	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal	I 3.3V	PU 10K 3.3V	Pull-up only active in GPIO mode
GPI3	A85	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3V	PU 10K 3.3V	Pull-up only active in GPIO mode

Table 16 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on rising edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V		Set by resistor divider to accept 3.3V.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB	PU 10k 3.3VSB	
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON#") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		

Signal	Pin #	Description	I/O	PU/PD	Comment
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		Not supported by chipset. Shorted with SUS_S4#.
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 4.99k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 4.99k 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 4.99k 3.3VSB	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 10k 3.3V	
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 10k 3.3V	
SMB_CK	B13	System Management Bus bidirectional clock line.	I/O 3.3VSB	PU 4.99k 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line.	I/O OD 3.3VSB	PU 4.99k 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3VSB	PU 10k 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch.	I OD 3.3V	PU 10k 3.3VSB	
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3V	PU 10k 3.3VSB	

Table 17 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O 3.3V		
SER1_TX	A101	General purpose serial port transmitter	O 3.3V		
SER0_RX	A99	General purpose serial port receiver	I 3.3V	43.2k 3.3V	
SER1_RX	A102	General purpose serial port receiver	I 3.3V	43.2k 3.3V	

Table 18 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

8.2 A-B Connector Pinout

Table 19 Connector A-B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#	A73	LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+ (*)	B22	SATA3_TX+ (*)	A77	LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX- (*)	B23	SATA3_TX- (*)	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	SATA2_RX+ (*)	B25	SATA3_RX+ (*)	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX- (*)	B26	SATA3_RX- (*)	A81	LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2 (*)	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	AC/HDA_BITCLK	B32	SPKR	A87	RSVD	B87	VCC_5V_SBY
A33	AC/HDA_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	RSVD
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	RSVD
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	EXCD1_PERST#	A102	SER1_RX	B102	FAN_TACHIN
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+ (*)	B52	PCIE_RX5+ (*)	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5- (*)	B53	PCIE_RX5- (*)	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga TCA3.

8.3 C-D Connector Signal Descriptions

Table 20 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		Not supported.
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		Not supported.
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		Not supported.
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		Not supported.

Table 21 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX0-	C3		I		
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX0-	D3		O		
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I		Not supported.
USB_SSRX1-	C6		I		Not supported.
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not supported.
USB_SSTX1-	D6		O		Not supported.
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I		Not supported.
USB_SSRX2-	C9		I		Not supported.
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not supported.
USB_SSTX2-	D9		O		Not supported.
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I		Not supported.
USB_SSRX3-	C12		I		Not supported.
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not supported.
USB_SSTX3-	D12		O		Not supported.

Table 22 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs. *Note: Can also be used as PCI Express Receive Input differential pairs 16 through 31 known as PCIE_RX[16-31] + and -.*	I PCIE		Not supported.
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_TX0+ PEG_TX0- PEG_TX1+ PEG_TX1- PEG_TX2+ PEG_TX2- PEG_TX3+ PEG_TX3- PEG_TX4+ PEG_TX4- PEG_TX5+ PEG_TX5- PEG_TX6+ PEG_TX6- PEG_TX7+ PEG_TX7- PEG_TX8+ PEG_TX8- PEG_TX9+ PEG_TX9- PEG_TX10+ PEG_TX10- PEG_TX11+ PEG_TX11- PEG_TX12+ PEG_TX12- PEG_TX13+ PEG_TX13- PEG_TX14+ PEG_TX14- PEG_TX15+ PEG_TX15-	D52 D53 D55 D56 D58 D59 D61 D62 D65 D66 D68 D69 D71 D72 D74 D75 D78 D79 D81 D82 D85 D86 D88 D89 D91 D92 D94 D95 D98 D99 D101 D102	PCI Express Graphics Transmit Output differential pairs. *Note: Can also be used as PCI Express Transmit Output differential pairs 16 through 31 known as PCIE_TX[16-31] + and -.*	O PCIE		Not supported.
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I		Not supported.

Note

PCI Express Graphics is not supported on conga-TCA3 modules

Table 23 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with SDVO1_RED+, DP1_LANE0+ and TMDS1_DATA2+. Multiplexed with SDVO1_RED-, DP1_LANE0- and TMDS1_DATA2-.	O PCIE		Only TMDS/DP option, no SDVO.
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with SDVO1_GRN+, DP1_LANE1+ and TMDS1_DATA1+. Multiplexed with SDVO1_GRN-, DP1_LANE1- and TMDS1_DATA1-.	O PCIE		Only TMDS/DP option, no SDVO.
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with SDVO1_BLU+, DP1_LANE2+ and TMDS1_DATA0+. Multiplexed with SDVO1_BLU-, DP1_LANE2- and TMDS1_DATA0-.	O PCIE		Only TMDS/DP option, no SDVO.
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with SDVO1_CK+, DP1_LANE3+ and TMDS1_CLK+. Multiplexed with SDVO1_CK-, DP1_LANE3- and TMDS1_CLK-.	O PCIE		Only TMDS/DP option, no SDVO.
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	Multiplexed with SDVO1_INT+. Multiplexed with SDVO1_INT-.			Not supported due to missing SDVO support.
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	Multiplexed with SDVO1_TVCLKIN+. Multiplexed with SDVO1_TVCLKIN-.			Not supported due to missing SDVO support.
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	Multiplexed with SDVO1_FLDSTALL+. Multiplexed with SDVO1_FLDSTALL-.			Not supported due to missing SDVO support.
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD.	I 3.3V	PD 1M	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with SDVO1_CTRLCLK, DP1_AUX+ and HDMI1_CTRLCLK. DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PD100k @ DP mode, PU 3.0k 3.3V @ HDMI/DVI mode	
DDI1_CTRLDATA_AUX-	D16	Multiplexed with SDVO1_CTRLDATA, DP1_AUX- and HDMI1_ CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PU 100k 3.3V@ DP mode, PU 3.0k 3.3V @ HDMI/DVI mode	DDI1_CTRLDATA_AUX- is a boot strap signal (see note below). DDI enable strap already populated.
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_ AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1M	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+ and TMDS2_DATA2+. Multiplexed with DP2_LANE0- and TMDS2_DATA2-.	O PCIE		
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+ and TMDS2_DATA1+. Multiplexed with DP2_LANE1- and TMDS2_DATA1-.	O PCIE		
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+ and TMDS2_DATA0+. Multiplexed with DP2_LANE2- and TMDS2_DATA0-.	O PCIE		
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+ and TMDS2_CLK+. Multiplexed with DP2_LANE3- and TMDS2_CLK-.	O PCIE		
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD.	I 3.3V	PD 1M	

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+ and HDMI2_CTRLCLK. DP AUX+ function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PD100k @ DP mode, PU 3.0k 3.3V @ HDMI/DVI mode	
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA. DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3V	PU 100k 3.3V@ DP mode, PU 3.0k 3.3V @ HDMI/DVI mode	DDI2_CTRLCLK_AUX- is a boot strap signal (see note below). DDI enable strap already populated.
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_ AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V	PD 1M	
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+. Multiplexed with DP3_LANE0- and TMDS3_DATA2-.	O PCIE		Not supported.
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+. Multiplexed with DP3_LANE1- and TMDS3_DATA1-.	O PCIE		Not supported.
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+. Multiplexed with DP3_LANE2- and TMDS3_DATA0-.	O PCIE		Not supported.
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+. Multiplexed with DP3_LANE3- and TMDS3_CLK-.	O PCIE		Not supported.
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3_HPD.	I 3.3V		Not supported.
DDI3_CTRLCLK_AUX+	C36	Multiplexed with DP3_AUX+ and HDMI3_CTRLCLK. DP AUX+ function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V		Not supported.
DDI3_CTRLDATA_AUX-	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA. DP AUX- function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3V		Not supported.
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_ AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V		Not supported.

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.5 of this user's guide.

The second DDI channel (DDI2) is only available if LVDS is not used. Refer to the HDMI and DisplayPort signal description tables in this section for information about the signals routed to the DDI interface of the COM Express connector.

Table 24 HDMI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS1_CLK + TMDS1_CLK -	D36 D37	HDMI/DVI TMDS Clock output differential pair. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
TMDS1_DATA0+ TMDS1_DATA0-	D32 D33	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
TMDS1_DATA1+ TMDS1_DATA1-	D29 D30	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-..	O PCIE		
TMDS1_DATA2+ TMDS1_DATA2-	D26 D27	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
HDMI1_HPD	C24	HDMI/DVI Hot-plug detect. Multiplexed with DDI1_HPD.	I PCIE	PD 1M	
HDMI1_CTRLCLK	D15	HDMI/DVI I²C Control Clock Multiplexed with DDI1_CTRLCLK_AUX+	I/O OD 3.3V	PU 3.0k 3.3V	
HDMI1_CTRLDATA	D16	HDMI/DVI I²C Control Data Multiplexed with DDI1_CTRLDATA_AUX-	I/O OD 3.3V	PU 3.0k 3.3V	HDMI1_CTRLDATA is a boot strap signal (see note below). HDMI enable strap already populated
TMDS2_CLK + TMDS2_CLK -	D49 D50	HDMI/DVI TMDS Clock output differential pair.. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-.	O PCIE		
TMDS2_DATA0+ TMDS2_DATA0-	D46 D47	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-.	O PCIE		
TMDS2_DATA1+ TMDS2_DATA1-	D42 D43	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-.	O PCIE		
TMDS2_DATA2+ TMDS2_DATA2-	D39 D40	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-..	O PCIE		
HDMI2_HPD	D44	HDMI/DVI Hot-plug detect. Multiplexed with DDI2_HPD	I PCIE	PD 1M	
HDMI2_CTRLCLK	C32	HDMI/DVI I²C Control Clock Multiplexed with DDI2_CTRLCLK_AUX+	I/O OD 3.3V	PU 3.0k 3.3V	
HDM12_CTRLDATA	C33	HDMI/DVI I²C Control Data Multiplexed with DDI2_CTRLDATA_AUX-	I/O OD 3.3V	PU 3.0k 3.3V	HDMI2_CTRLDATA is a boot strap signal (see note below). HDMI enable strap is already populated.
TMDS3_CLK + TMDS3_CLK -	C49 C50	HDMI/DVI TMDS Clock output differential pair.. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		Not supported
TMDS3_DATA0+ TMDS3_DATA0-	C46 C47	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		Not supported
TMDS3_DATA1+ TMDS3_DATA1-	C42 C43	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-..	O PCIE		Not supported
TMDS3_DATA2+ TMDS3_DATA2-	C39 C40	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		Not supported

Signal	Pin #	Description	I/O	PU/PD	Comment
HDMI3_HPD	C44	HDMI/DVI Hot-plug detect. Multiplexed with DDI3_HPD.	I PCIE		Not supported
HDMI3_CTRLCLK	C36	HDMI/DVI I²C Control Clock Multiplexed with DDI3_CTRLCLK_AUX+	I/O OD 3.3V		Not supported
HDMI3_CTRLDATA	C37	HDMI/DVI I²C Control Data Multiplexed with DDI3_CTRLDATA_AUX-	I/O OD 3.3V		Not supported

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.5 of this user's guide.

The second HDMI interface is only available if LVDS is not used.

Table 25 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP1_LANE3+ DP1_LANE3-	D36 D37	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
DP1_LANE2+ DP1_LANE2-	D32 D33	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
DP1_LANE1+ DP1_LANE1-	D29 D30	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-.	O PCIE		
DP1_LANE0+ DP1_LANE0-	D26 D27	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
DP1_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI1_HPD.	I 3.3V	PD 1M	
DP1_AUX+	D15	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP1_AUX-	D16	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	DP1_AUX- is a boot strap signal (see note below). DP enable strap is already populated.
DP2_LANE3+ DP2_LANE3-	D49 D50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
DP2_LANE2+ DP2_LANE2-	D46 D47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O PCIE		
DP2_LANE1+ DP2_LANE1-	D42 D43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O PCIE		
DP2_LANE0+ DP2_LANE0-	D39 D40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR0+ and DDI1_PAIR0-	O PCIE		
DP2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI2_HPD.	I 3.3V	PD 1M	
DP2_AUX+	C32	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP2_AUX-	C33	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	DP2_AUX- is a boot strap signal (see note below). DP enable strap already populated.
DP3_LANE3+ DP3_LANE3-	C49 C50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		Not supported
DP3_LANE2+ DP3_LANE2-	C46 C47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		Not supported
DP3_LANE1+ DP3_LANE1-	C42 C43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-.	O PCIE		Not supported
DP3_LANE0+ DP3_LANE0-	C39 C40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		Not supported
DP3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI3_HPD.	I 3.3V		Not supported
DP3_AUX+	C36	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE		Not supported
DP3_AUX-	C37	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE		Not supported

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.5 of this user's guide.

The second DP interface is only available if LVDS is not used

Table 26 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# / TYPE1# / TYPE0# / X / X / X / Pinout Type 1 NC / NC / NC / Pinout Type 2 NC / NC / GND / Pinout Type 3 (no IDE) NC / GND / NC / Pinout Type 4 (no PCI) NC / GND / GND / Pinout Type 5 (no IDE, no PCI) GND / NC / NC / Pinout Type 6 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.	PDS	TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard. The conga-TCA3 is based on the COM Express Type 6 pinout therefore the pins 0 and 1 are not connected and pin 2 is connected to GND.
TYPE10#	A97	Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed. TYPE10# NC – Pinout R2.0 PD – Pinout Type 10 pull down to ground with 4.7k resistor 12V – Pinout R1.0 This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7k resistor.	PDS	Not connected to indicate "Pinout R2.0".

Table 27 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

8.4 C-D Connector Pinout

Table 28 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1- (*)	D56	PEG_TX1- (*)
C2	GND	D2	GND	C57	TYPE1#	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PEG_RX2+ (*)	D58	PEG_TX2+ (*)
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PEG_RX2- (*)	D59	PEG_TX2- (*)
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1- (*)	D6	USB_SSTX1- (*)	C61	PEG_RX3+ (*)	D61	PEG_TX3+ (*)
C7	USB_SSRX1+ (*)	D7	USB_SSTX1+ (*)	C62	PEG_RX3- (*)	D62	PEG_TX3- (*)
C8	GND	D8	GND	C63	RSVD	D63	DDPC_CTRLCLK
C9	USB_SSRX2- (*)	D9	USB_SSTX2- (*)	C64	RSVD	D64	DDPC_CTRLDATA
C10	USB_SSRX2+ (*)	D10	USB_SSTX2+ (*)	C65	PEG_RX4+ (*)	D65	PEG_TX4+ (*)
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4- (*)	D66	PEG_TX4- (*)
C12	USB_SSRX3- (*)	D12	USB_SSTX3- (*)	C67	RSVD	D67	GND
C13	USB_SSRX3+ (*)	D13	USB_SSTX3+ (*)	C68	PEG_RX5+ (*)	D68	PEG_TX5+ (*)
C14	GND	D14	GND	C69	PEG_RX5- (*)	D69	PEG_TX5- (*)
C15	DDI1_PAIR6+ (*)	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	DDI1_PAIR6- (*)	D16	DDI1_CTRLDATA_AUX-	C71	PEG_RX6+ (*)	D71	PEG_TX6+ (*)
C17	RSVD	D17	RSVD	C72	PEG_RX6- (*)	D72	PEG_TX6- (*)
C18	RSVD	D18	RSVD	C73	GND	D73	GND
C19	PCIE_RX6+ (*)	D19	PCIE_TX6+ (*)	C74	PEG_RX7+ (*)	D74	PEG_TX7+ (*)
C20	PCIE_RX6- (*)	D20	PCIE_TX6- (*)	C75	PEG_RX7- (*)	D75	PEG_TX7- (*)
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+ (*)	D22	PCIE_TX7+ (*)	C77	RSVD	D77	RSVD
C23	PCIE_RX7- (*)	D23	PCIE_TX7- (*)	C78	PEG_RX8+ (*)	D78	PEG_TX8+ (*)
C24	DDI1_HPD	D24	RSVD	C79	PEG_RX8- (*)	D79	PEG_TX8- (*)
C25	DDI1_PAIR4+ (*)	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)
C26	DDI1_PAIR4- (*)	D26	DDI1_PAIR0+	C81	PEG_RX9+ (*)	D81	PEG_TX9+ (*)
C27	RSVD	D27	DDI1_PAIR0-	C82	PEG_RX9- (*)	D82	PEG_TX9- (*)
C28	RSVD	D28	RSVD	C83	RSVD	D83	RSVD
C29	DDI1_PAIR5+ (*)	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	DDI1_PAIR5- (*)	D30	DDI1_PAIR1-	C85	PEG_RX10+ (*)	D85	PEG_TX10+ (*)

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- (*)	D86	PEG_TX10- (*)
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+	C87	GND	D87	GND
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-	C88	PEG_RX11+ (*)	D88	PEG_TX11+ (*)
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11- (*)	D89	PEG_TX11- (*)
C35	RSVD	D35	RSVD	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+ (*)	D36	DDI1_PAIR3+	C91	PEG_RX12+ (*)	D91	PEG_TX12+ (*)
C37	DDI3_CTRLDATA_AUX- (*)	D37	DDI1_PAIR3-	C92	PEG_RX12- (*)	D92	PEG_TX12- (*)
C38	DDI3_DDC_AUX_SEL (*)	D38	RSVD	C93	GND	D93	GND
C39	DDI3_PAIR0+ (*)	D39	DDI2_PAIR0+	C94	PEG_RX13+ (*)	D94	PEG_TX13+ (*)
C40	DDI3_PAIR0- (*)	D40	DDI2_PAIR0-	C95	PEG_RX13- (*)	D95	PEG_TX13- (*)
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+ (*)	D42	DDI2_PAIR1+	C97	RVSD	D97	RSVD
C43	DDI3_PAIR1- (*)	D43	DDI2_PAIR1-	C98	PEG_RX14+ (*)	D98	PEG_TX14+ (*)
C44	DDI3_HPD (*)	D44	DDI2_HPD	C99	PEG_RX14- (*)	D99	PEG_TX14- (*)
C45	RSVD	D45	RSVD	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+ (*)	D46	DDI2_PAIR2+	C101	PEG_RX15+ (*)	D101	PEG_TX15+ (*)
C47	DDI3_PAIR2- (*)	D47	DDI2_PAIR2-	C102	PEG_RX15- (*)	D102	PEG_TX15- (*)
C48	RSVD	D48	RSVD	C103	GND	D103	GND
C49	DDI3_PAIR3+ (*)	D49	DDI2_PAIR3+	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3- (*)	D50	DDI2_PAIR3-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+ (*)	D52	PEG_TX0+ (*)	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0- (*)	D53	PEG_TX0- (*)	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV#	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+ (*)	D55	PEG_TX1+ (*)	C110	GND (FIXED)	D110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-TCA3.

8.5 Boot Strap Signals

Table 29 Boot Strap Signal Descriptions

Signal	Pin #	Description of Boot Strap Signal	I/O	PU/PD	Comment
DDI1_CTRLDATA_AUX- DP1_AUX- HDMI_CTRLDATA	D16	Multiplexed with DP1_AUX- and HDMI1_CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3V	PU100k 3.3V	DDI1_CTRLDATA_AUX- is a boot strap signal (see caution statement below).
DDI2_CTRLDATA_AUX- DP2_AUX- HDM2_CTRLDATA	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA. DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3V	PU100k 3.3V	DDI2_CTRLDATA_AUX- is a boot strap signal (see caution statement below).

Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either COM Express™ internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM Express™ module to malfunction and/or cause irreparable damage to the module.

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-TCA3 module is functionally identical with a standard PC/AT. The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.1.1 LPC Bus

On the conga-TCA3, the Platform Controller Hub (PCH) acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCH and the LPC Bus. Some fixed I/O space ranges seen by the processor are:

Device	IO Address
8259 Master	20h-21h, 24h-25h, 28h-29h, 2Ch-2Dh, 30h-31h, 34h-35h, 38h-39h, 3Ch-3Dh
8254s	40h-43h, 50h-53h
Ps2 Control	60h, 64h
NMI Controller	61h, 63h, 65h, 67h
RTC	70h-77h
Port 80h	80h-83h
Init Register	92h
8259 Master	A0h- A1h, A4h-A5h, A8h-A9h, Ach-ADh, B0h-B1h, B4h-B5h, B8h-B9h, Bch-BDh, 4D0h-4D1h
PCU UART	3F8h-3FFh
Reset Control	CF9h
Active Power Management	B2h-B3h

Some of these ranges are used by a Super I/O if implemented on the carrier board or are occupied by the COM Express on-module UARTs if these are enabled in the setup. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 30 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00h	00h	00h	SoC Transaction Router
00h	02h	00h	Graphics and Display
00h	12h	00h	SD Port
00h	13h	00h	SATA
00h	14h	00h	XHCI USB
00h	17h	01h	eMMC 4.5 Port
00h	1Ah	00h	Trusted Execution Engine
00h	1Bh	00h	HD Audio
00h	1Ch	00h	PCI Express Root Port 0
00h	1Ch	01h	PCI Express Root Port 1
00h	1Ch	02h	PCI Express Root Port 2
00h	1Ch	03h	PCI Express Root Port 3
00h	1Dh	00h	EHCI USB
00h	1Fh	00h	LPC: Bridge to Intel Legacy Port
00h	1Fh	03h	SMBus Port
03h	00h	00h	PLX PE8605 PCI Express Bridge
04h	01h	00h	PLX PCI Express Port 0
04h	02h	00h	PLX PCI Express Port 1
04h	03h	00h	PLX PCI Express Port 2
08h	00h	00h	Intel I210 Ethernet Network

Note

1. *The PCI Express Ports are visible only if they are set to "Enabled" in the BIOS setup program and a device attached to the corresponding PCI Express port on the carrier board.*

2. *The above table represents a case when a single function PCI Express device is connected to all possible slots on the carrier board. The given bus numbers will change based on the actual configuration of the hardware.*

9.3 PCI Interrupt Routing Map

Table 31 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line [1]	APIC Mode IRQ	Graphic	SD Card	SATA	XHCI	eMMC 4.5 Port	TXE	HD Audio	PCI-EX Root Port 0	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Root Port 3	EHCI USB	SMBus Port	I210 Ethernet Network
A	INTA	16	x	x	x	x	x	x	x	x				x		x [3]
B	INTB	17									x				x	x [4]
C	INTC	18										x				x [5]
D	INTD	19											x			x [2]
E		20														
F		21														
G		22														
H		23														

Note

[1] *These interrupt lines are virtual (message based).*

[2] *Interrupt used by single function PCI Express devices (INTA).*

[3] *Interrupt used by multifunction PCI Express devices (INTB).*

[4] *Interrupt used by multifunction PCI Express devices (INTC).*

[5] *Interrupt used by multifunction PCI Express devices (INTD).*

9.4 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.5 SM Bus

System Management (SM) bus signals are connected to the Intel® Baytrail SoC and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

10 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

10.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <F2> key during POST.

10.1.1 Boot Selection Popup

Press the <F11> key during POST to access the Boot Selection Popup menu. A selection menu displays immediately after POST, allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

10.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar, left frame and right frame. The menu bar is shown below:

Main	Advanced	Chipset	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

10.3 Main Setup Screen

When you first enter the BIOS setup, you will see the main setup screen. The main setup screen reports BIOS, processor, memory and board information and is for configuring the system date and time. You can always return to the main setup screen by selecting the 'Main' tab.

Feature	Options	Description
Main BIOS Version	no option	Displays the main BIOS version.
OEM BIOS Version	no option	Displays the additional OEM BIOS version.
Build Date	no option	Displays the date the BIOS was built.
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Revision	no option	Displays the firmware revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
Microcode Patch	no option	Displays the microcode patch loaded for the onboard CPU
Baytrail SoC	no option	B3 Stepping
Total Memory	no option	Total amount of low voltage DDR3 present on the system
System Date	Day of week, month/day/year	Specifies the current system date *Note: The date is in month/day/year format.*

Feature	Options	Description
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24 hour format.*

10.4 Advanced Setup

Select the advanced tab from the setup menu to enter the advanced BIOS setup screen. The menu is used for setting advanced features and only features described within this user's guide are listed.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Watchdog				
	Graphics				
	Hardware Health Monitoring				
	RTC Wake				
	Module Serial Ports				
	ACPI				
	Intel(R) Smart Connect Technology				
	Serial Port Console Redirection				
	CPU Configuration				
	PPM Configuration				
	Thermal Configuration				
	IDE Configuration				
	Miscellaneous Configuration				
	SCC Configuration				
	Network Stack				
	CSM				
	SDIO				
	Trusted Computing				
	USB				
	Platform Trust Technology				
	Security Configuration				
	Intel(R) I210 Gigabit Network				

10.4.1 Watchdog Submenu

Feature	Options	Description
POST Watchdog	Disabled 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup of the boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	Disabled One-time Trigger Single Event Repeated Event	Select the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to 'One-time Trigger' the watchdog will be disabled after the first trigger. If set to 'Single Event', every stage will be executed only once, then the watchdog will be disabled. If set to 'Repeated Event' the last stage will be executed repeatedly until a reset occurs.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	ACPI Event **Reset** Power Button	Select the type of event that will be generated when timeout 1 is reached. For more information about ACPI Event, see note below.
Event 2	Disabled ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 2 is reached.
Event 3	Disabled ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 3 is reached.

Feature	Options	Description
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Select the timeout value for the first stage watchdog event.
Timeout 2	see above	Select the timeout value for the second stage watchdog event.
Timeout 3	see above	Select the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

Note

In ACPI mode, it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

Additionally, the conga-TCA3 module does not support the watchdog NMI mode. COM Express type 6 modules do not support the PCI bus and therefore the PCI_SERR# signal is not available. There is no way to drive a NMI to the processor without the presence of the PCI_SERR# PCI bus signal.

10.4.2 Graphics Submenu

Feature	Options	Description
Boot Display Device	VBIOS Default	
CRT	**Enabled** Disabled	Enable CRT Video Interface.
Active LFP	No LVDS **LVDS**	Select the active local flat panel configuration.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel. If no external EDID data set is found, the data set selected under 'Local Flat Panel Type' will then be used as a fallback data set.

Feature	Options	Description
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 2x24 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.
Backlight Inverter Type	None **PWM** I2C	Select the type of backlight inverter used. PWM = Use IGD PWM signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.
PWM Inverter Polarity	**Normal** Inverted	Select PWM inverter polarity. Only visible if 'Backlight Inverter Type' is set to 'PWM' .
PWM Inverter Frequency (Hz)	**200** - 40000	Set the PWM inverter frequency in Hz. Only visible if 'Backlight Inverter Type' is set to 'PWM'.
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100%**	Actual backlight value in percent of the maximum setting.
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Setting	**No** Yes	Allow to invert backlight control values if required for the actual I2C type backlight hardware controller.
Digital Display Interface 1 (DDI1)	Disabled **DisplayPort** HDMI/DVI Auto	Select the output type of the Digital Display Interface 1.
Digital Display Interface 2 (DDI2)	Disabled **DisplayPort** HDMI/DVI Auto	Select the output type of the Digital Display Interface 2. This interface is visible and configurable only when 'Active LFP' is set to 'No LVDS' because DDI2 and LFP interface are shared on conga-TCA3.

10.4.3 Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	no option	Displays the actual CPU Temperature in °C.
CPU Fan Speed	no option	Displays the actual CPU Fan Speed in RPM.

10.4.4 RTC Wake Submenu

Feature	Options	Description
Wake System At Fixed Time	**Disabled** Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour		Specify wake up hour. For example, enter "3" for 3am and "15" for 3pm.
Wake up minute		Specify wake up minute.
Wake up second		Specify wake up second.

10.4.5 Module Serial Ports Submenu

Feature	Options	Description
Serial Port 0	**Disabled** Enabled	Enable or disable module's serial port 0.
Serial Port 1	**Disabled** Enabled	Enable or disable module's serial port 1.

10.4.6 ACPI Submenu

Feature	Options	Description
Enable ACPI Auto Configuration	Disabled Enabled	Enable or disable BIOS ACPI Auto Configuration
Enable Hibernation	Disabled **Enabled**	Enable or disable system's ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system sleep/suspend.
Lock Legacy Resources	**Disabled** Enabled	Enable or disable locking of legacy resources.

Feature	Options	Description
LID Support	Disabled **Enabled**	Configure COM Express LID# signal to act as ACPI lid
Sleep Button Support	Disabled **Enabled**	Configure COM Express SLEEP# signal to act as ACPI sleep button.

10.4.7 Intel(R) Smart Connect Technology Submenu

Feature	Options	Description
ISCT Support	**Disabled** Enabled	Enable or disable Intel(R) Smart Connection Support. When this setup node is set to Disabled, all the other Nodes will not be visible.
ISCT Notification Control	Disabled **Enabled**	Enable or Disable ISCT Notification Control.
ISCT WLAN Power Control	Disabled **Enabled**	Enable or Disable ISCT WLAN Power Control.
ISCT WWAN Power Control	Disabled **Enabled**	Enable or Disable ISCT WWAN Power Control
ISCT Sleep Duration Value Format	**Duration in Seconds**	ISCT Sleep Duration in seconds.
ISCT RF Kill Switch Type	Software **Hardware**	Select ISCT RF Kill Switch Type
ISCT RTC Timer Support	**Disabled** Enabled	Enable ISCT RTC Timer

10.4.8 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
►Console Redirection Settings	submenu	Opens console redirection configuration sub menu.
Serial Port for Out-of-Band Management / EMS Console Redirection	**Disabled** Enabled	Enable or disable Serial Port for Out-of-Band Management / Windows Emergency Management Services.
►Console Redirection Settings	submenu	Opens console redirection configuration sub menu.

Note

The Serial Port Console Redirection can be enabled (functional) only if an external Super I/O offering UARTs has been implemented on the

10.4.8.1 Console Redirection Settings COM0 Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select terminal type.
Baudrate	9600, 19200, 38400, 57600, **115200**	Select baud rate.
Data Bits	7, **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enable or disable extended terminal resolution.
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select Function Key and Key Pad on Putty.

10.4.8.2 Console Redirection Settings Out-of-Band Management Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ **VT-UTF8** ANSI	Select terminal type.
Bits Per Second	9600, 19200, 38400, 57600, **115200**	Select baud rate.
Data Bits	**8**	Set number of data bits.
Parity	**None**	Select parity.
Stop Bits	**1**	Set number of stop bits.

10.4.9 CPU Configuration Submenu

Feature	Options	Description
▶Socket 0 CPU Information	submenu	Socket specific CPU information
▶CPU Thermal Configuration	submenu	CPU thermal configuration options
CPU Speed	no option	Displays the CPU clock frequency
64-bit	no option	Displays whether 64-bit is supported.
Active Processor Cores	**All** 1	Set the number of cores to be enabled.
Limit CPUID Maximum	**Disabled** Enabled	When enabled, the processor limits the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When disabled, the processor returns the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Execute Disable Bit	Disabled **Enabled**	Enable or disable the Execute Disable Bit (XD) of the processor. With the XD bit set to enabled, certain classes of malicious buffer overflow attacks can be prevented when combined with a supporting OS.
Hardware Prefetcher	Disabled **Enabled**	Enable or disable the Mid Level Cache (MLC) streamer prefetcher.
Adjacent Cache Line Prefetch	Disabled **Enabled**	Enable or disable prefetching of adjacent cache lines.
Intel Virtualization Technology	Disabled **Enabled**	Enable or disable support for the Intel virtualization technology.
Power Technology	Disable **Energy Efficient** Custom	Configure the power technology schema for the CPU

10.4.9.1 Socket 0 CPU Information Submenu

Feature	Options	Description
CPU Name	no option	Displays socket specific CPU name
CPU Signature	no option	Displays CPU signature number
Microcode Patch	no option	Displays the CPU microcode patch number
Max. CPU Speed	no option	Displays the maximal CPU clock frequency
Min. CPU Speed	no option	Displays the minimal CPU clock frequency
Processor Cores	no option	Displays the number of CPU core on Socket CPU
Intel HT Technology	no option	Displays the Intel HT Technology support information.
Intel VT-x Technology	no option	Displays the Intel VT-x Technology support information
L1 Data Cache	no option	Displays the Socket L1 data cache information
L1 Code Cache	no option	Displays the Socket L1 code cache information
L2 Cache	no option	Displays the Socket L2 data cache information
L3 Cache	no option	Displays the Socket L3 data cache information

10.4.9.2 CPU Thermal Configuration Submenu

Feature	Options	Description
DTS	Enabled **Disabled**	Enable or Disable CPU Digital Thermal Sensor (DTS). DTS is used on ACPI functions to read the CPU temperature. This value is read from MSR.

10.4.10 PPM Configuration Submenu

Feature	Options	Description
EIST	Disabled **Enabled**	Enable or disable Enhanced Intel SpeedStep Technology (EIST).
CPU C state Report	Disabled **Enabled**	Enable/Disable CPU state Report to Operating System.
Enhanced CPU C-state	Disabled **Enabled**	Enable/Disable enhanced CPU C states
Max CPU C state	C7 C6 **C1**	Maximal CPU C state supported by the CPU
SOix	**Disabled** Enabled	Enable/Disable CPU SOix state support

10.4.11 Thermal Configuration

Feature	Options	Description
Critical Trip Point	**90 C** 87 C 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	Temperature of the ACPI critical Trip Point in which the OS will shut the system off.
Passive Trip Point	90 C 87 C **85 C** 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	Temperature of the ACPI passive Trip Point in which the OS will begin throttling the processor.

Note

The conga-TCA3 does not support active trip point.

10.4.12 IDE Configuration Submenu

Feature	Options	Description
Serial-ATA (SATA)	**Enabled** Disabled	Enable or disable the onboard SATA controller.
SATA Test Mode	Enabled **Disabled**	Should be set to Disabled. Test Mode is used just for verification measurements.
SATA Speed Support	Gen1 **Gen2**	Indicates the maximum speed the SATA controller can support.
SATA ODD Port	Port 0 ODD Port 1 ODD **No ODD**	Configure which SATA Port is ODD.
SATA Mode	IDE Mode **AHCI Mode**	Configure SATA Port Mode
Serial-ATA Port 0	**Enabled** Disabled	Enable or disable the SATA Port 0.
SATA Port 0 Hot Plug	**Disabled** Enabled	Select hot plug support for SATA Port 0. Not possible in Native IDE mode.
Serial-ATA Port 1	**Enabled** Disabled	Enable or disable the SATA Port 1.
SATA Port 1 Hot Plug	**Disabled** Enabled	Select hot plug support for SATA Port 1. Not possible in Native IDE mode.
SATA Port 0 Information	No Option	Displays Information of device detected on SATA Port 0.
SATA Port 1 Information	No Option	Displays Information of device detected on SATA Port 1.

10.4.13 Miscellaneous Configuration Submenu

Feature	Options	Description
High Precision Timer	**Enabled** Disabled	Enable or disable the high precision event timer.
Boot Timer with HPET Timer	Enabled **Disabled**	Allow boot timer calculation with the high precision event timer.
PCI Express Dynamic Clock Gating	Enabled **Disabled**	Enable dynamic clock gating.

10.4.14 SCC Configuration Submenu

Feature	Options	Description
SCC Device Mode	ACPI Mode PCI Mode	Configure the storage control cluster working mode.
SCC eMMC Support	Enable eMMC 4.5 Support Enable eMMC 4.41 Support **eMMC AUTO MODE** Disable	Enable SCC eMMC support and configure eMMC mode.
SCC 4.5 DDR50 eMMC Support	**Enabled** Disabled	Enable DDR50 eMMC support.
SCC 4.5 HS200 eMMC Support	Enabled **Disabled**	Enable DDR50 eMMC support.
eMMC Secure Erase	Enabled **Disabled**	Enable eMMC secure erase support.
SCC SD Card Support	**Enabled** Disabled	Enable storage control cluster SD Card support
SDR25 Support for SD Card	Enabled **Disabled**	Enable SDR25 Support for SD Card
DDR50 Support for SD Card	**Enabled** Disabled	Enable DDR50 Support for SD Card

10.4.15 Network Stack

Feature	Options	Description
Network Stack	Enabled **Disabled**	Enable or disable the UEFI network stack.
Ipv4 PXE Support	Enabled **Disabled**	Enable Ipv4 PXE boot support. If disabled IPV6 PXE boot option will not be created.
Ipv6 PXE Support	Enabled **Disabled**	Enable Ipv4 PXE boot support. If disabled IPV6 PXE boot option will not be created.
PXE boot wait time	0-5	Wait time to press ESC to abort PXE Boot

10.4.16 CSM Submenu

Feature	Options	Description
Launch CSM	**Enabled** Disabled	Enable the Compatibility Support Module.
CSM16 Module Version	No option	Display CSM Module Version number.
Gate A20 Active	**Upon Request** Always	Configure legacy Gate A behavior.
Option ROM Messages	**Force BIOS** Keep Current	Enable Option ROM message
INT19 Trap Response	**Immediate** Postponed	Define BIOS reaction on INT19 trapping by Option ROM: Immediate executes the trap right away. Postpone executes the trap during legacy boot.
Boot Option Filter	UEFI and Legacy **Legacy Only** UEFI Only	Controls which devices / boot loaders the system should boot to.
Network	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and legacy Network option ROMs.
Storage	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and legacy Storage option ROMs.
Video	Do not launch UEFI only **Legacy only**	Controls the execution of UEFI and legacy Video option ROMs
Other PCI Devices	**UEFI only** Legacy only	Controls the execution of UEFI and legacy option ROMs for any other PCI device different to Network, Video and Storage.

10.4.17 SDIO Submenu

Feature	Options	Description
SDIO Access Mode	**Auto** DMA PIO	Controls the SDIO Access mode to the device.

10.4.18 Trusted Computing Submenu

Feature	Options	Description
Security Device Support	**Disabled** Enabled	Enable or disable TPM support. System reset is required after change.
User Confirmation	Disabled **Enabled**	Enable or disable user confirmation requests for certain transactions.
TPM State	**Disabled** Enabled	Enable or disable TPM chip. Note: System might restart several times during POST to acquire target state.
Pending operation	**None,** Enable Take Ownership, Disable Take Ownership, TPM Clear	Perform selected TPM chip operation. Note: System might restart several times during POST to perform selected operation.

10.4.19 USB Submenu

Feature	Options	Description
USB Module Version	no option	Displays the version of the USB module.
USB Devices	no option	Displays the detected USB devices.
xHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without xHCI hand-off support. The xHCI ownership change should be claimed by xHCI OS driver.
EHCI Hand-off	**Disabled** Enabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI OS driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable Mass Storage Driver Support.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device start unit command timeout.
USB Transfer Timeout	1 sec 5 sec 10 sec **20 sec**	The timeout value for control, bulk, and interrupt transfers.
Device Power -Up Delay Selection	**Auto** Manual	Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.
Device Power -Up Delay Value	0-40 Default : 5	Actual power-up delay value in seconds.

10.4.20 Platform Trust Technology

Feature	Options	Description
fTPM	**Disable** Enable	Enable Trusted Platform Module support.

10.4.21 Security Configuration

Feature	Options	Description
TXE	**Enabled** Disabled	Enable Trusted Execution Engine.
TXE HMRFPO	Enable **Disable**	Enable Host ME Region Flash Protection Overwrite.
TXE Firmware Update	**Enabled** Disabled	Enable Firmware update.
TXE EOP Message	**Enabled** Disabled	Enable TXE End of Post Message.
TXE Unconfiguration Perform	No option	Execute a TXE unconfiguration command
Intel(R) Anti-Theft Technology Configuration	No option	
Intel(R) AT	Enable **Disable**	Enable Anti-Theft technology.
Intel(R) AT Platform PBA	Enable **Disable**	Enable Anti-Theft Platform Pre-boot Authentication.
Intel(R) AT Suspend Mode	Enable **Disable**	Enable Anti-Theft Suspend Mode.

10.4.22 SIO Submenu

Feature	Options	Description
AMI SIO Driver Version		
▶Serial Port 1	No option	Serial Port 1 Submenu
▶Serial Port 2	No option	Serial Port 2 Submenu
▶Parallel Port	No option	Parallel Port Submenu
▶PS2 Controller (KB&MS)	No Option	PS2 configuration Submenu

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

10.4.22.1 Serial Port 1 Submenu

Feature	Options	Description
Use this Device	Enable **Disable**	Enable Logical Device.
Logical Device Settings	No option	Show current Logical Device Settings.
Possible	**Use Automatic Settings** IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11, 12; DMA;	Serial Port 1 configuration options.

10.4.22.2 Serial Port 2 Submenu

Feature	Options	Description
Use this Device	Enable **Disable**	Enable Logical Device.
Logical Device Settings	No option	Show current Logical Device Settings.
Possible	**Use Automatic Settings** IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11, 12; DMA;	Serial Port 2 configuration options.

10.4.22.3 Parallel Port Submenu

Feature	Options	Description
Use this Device	Enable **Disable**	Enable Logical Device.
Logical Device Settings	No option	Show current Logical Device Settings.
Possible	**Use Automatic Settings** IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11, 12; DMA;	Parallel Port configuration options.

10.4.22.4 PS2 Controller (KB&MS) Submenu

Feature	Options	Description
Use this Device	Enable Disable	Enable Logical Device.
Logical Device Settings	No option	Show current Logical Device Settings.
Possible	Use Automatic Settings IO=60h; IO=64h; IRQ=1;	PS2 configuration options.

10.4.23 Intel(R) Ethernet Connection I210 Submenu

At this submenu additionally to its title the MAC address is displayed at the end of the title.

Feature	Options	Description
► NIC Configuration	submenu	Opens the NIC Configuration submenu.
Blink LEDs	0-15 Default : 0	The Ethernet LEDs will blink so many seconds long as entered.
UEFI Driver	no option	Displays the UEFI Driver version.
Adapter PBA	no option	Displays the Adapter PBA.
Chip Type	no option	Displays the type of the Chip in which the Ethernet controller is integrated.
PCI Device ID	no option	Displays the PCI Device ID of the Ethernet controller.

Feature	Options	Description
Bus:Device:Function	no option	Displays the PCI Bus:Device:Function number of the Ethernet controller.
Link Status	no option	Displays the Link Status.
MAC Address	no option	Displays the MAC Address.

10.4.23.1 NIC Configuration Submenu

Feature	Options	Description
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Specifies the port speed used for the selected boot protocol.
Wake on LAN	Disabled **Enabled**	Enables Wake on LAN (WOL) feature

10.4.24 Driver Health Submenu

Feature	Options	Description
▶Intel(R) PRO/1000	No option	Provides Health Status for the drivers/Controllers connected to the System

10.4.24.1 Intel(R) PRO/1000 Submenu

Feature	Options	Description
Controller Information	No option	Provides Health Status of the controller

10.5 Chipset Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.5.1 North Bridge Submenu

Feature	Options	Description
Memory Information		
Total Memory	No option	Total amount of memory detected by the system
Memory Slot 0	No option	Memory detected by the system on Slot 0
Memory Slot 1	No option	Memory detected by the system on Slot 1

10.5.2 South Bridge Submenu

Feature	Options	Description
▶ Azalia HD Audio	Submenu	Azalia HD Audio Submenu.
▶ USB	Submenu	USB Submenu.
▶ PCI Express Configuration	Submenu	PCI Express Configuration Submenu.
High Precision Timer	**Enabled** Disabled	Enable High Precision Event Timer.
Restore AC Power Loss	Power Off Power On **Last State**	Configure the State of the system after a Power Loss when running in AT Mode
Serial IRQ	**Quiet** Continuous	Configure IRQ Serial Mode
SB CRID	**Revision ID** CRID 0 CRID 1 CRID 2	Select the Revision ID showed on the PCI configuration space.
Global SMI Lock	**Enabled** Disabled	Enable or Disable SMI Lock
BIOS Read/Write Protection	Enable **Disable**	Enable BIOS SPI Region read/write protection.

10.5.2.1 Azalia HD Audio

Feature	Options	Description
LPE Audio Support	**Disable** LPE Audio PCI Mode LPE Audio ACPI Mode	Enable LPE Audio Support.
Audio Controller	**Enabled** Disabled	Enable Audio Controller.
Azalia Vci Enable	**Enabled** Disabled	Enable Azalia Vci.
Azalia Docking Support Enable	Enable **Disable**	Enable Azalia Docking support.
Azalia PME Enable	**Enabled** Disabled	Enable Azalia PME support.
Azalia HDMI Codec	**Enabled** Disabled	Enable Azalia HDMI Codec
HDMI Port B	**Enabled** Disabled	Enable HDMI Port B Audio.
HDMI Port C	Enable **Disable**	Enable HDMI Port C Audio.

10.5.2.2 USB Submenu

Feature	Options	Description
USB OTG Support	**Disabled** Enabled	Enable USB OTG support.
USB VBUS	**On** Off	VBUS should be On in Host Mode and it should be Off in OTG device Mode.

Feature	Options	Description
XHCI Mode	Enable Disable Auto **Smart Auto**	USB3.0 mode support on USB0, USB1, USB2 and USB3 ports. Enabled – USB ports will function correctly in BIOS but the ports on which the USB3.0 mode is enabled (see USB0 port USB3.0 item) will not function at all under OS if the USB3.0 OS driver is not installed. USB ports will not function in pre-OS time if USB3.0 Support in BIOS is disabled (see the USB3.0 Support in BIOS item). Disabled – USB ports will function in USB2.0 mode only. No USB3.0 OS driver required. The USB ports will be routed to EHCI1 controller. Auto – USB ports are initially set to operate in USB2.0 Mode and the USB3.0 OS driver (if available) will switch them to USB3.0 mode. If USB3.0 OS driver is not available, the ports will function correctly but will operate in USB2.0 mode. Smart Auto – The BIOS will store the USB mode set by the OS and at next boot the BIOS will set this previously used mode. At G3 boot (first boot after mechanical disconnection of the power supply) the USB ports will function identically as in Auto mode. This mode is not available when 'Disabled' is selected at USB3.0 Support in BIOS item.
USB2 Link Power Management	Disabled **Enabled**	Enable USB2 Link Power Management
USB 2.0(EHCI) Support	**Disabled** Enabled	Control USB EHCI (USB 2.0) functions.
USB Per Port Control	Disabled **Enabled**	Control each of the USB ports (0-3).
USB Port 0	Disabled **Enabled**	Enable Port 0
USB Port 1	Disabled **Enabled**	Enable Port 1
USB Port 2	Disabled **Enabled**	Enable Port 2
USB Port 3	Disabled **Enabled**	Enable Port 3

Note

The USB ports originating from the HSIC hub behave differently from the EHCI USB 2.0 ports. For this reason, it is necessary to set the 'XHCI mode' correctly. See the congatec technical note 'CTN-20140702-001' for more information on the configuration that suits your requirement .

10.5.2.3 PCI Express Configuration Submenu

Feature	Options	Description
PCIe noncompliance Card	**Not Supported** Supported	Enable PCIe 1.0 Device Support
PCI Express Port 0	Disabled **Enabled**	Enable PCIe Port 0.
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 0 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
PCI Express Port 1	Disabled **Enabled**	Enable PCIe Port 1.
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 1 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
PCI Express Port 2	Disabled **Enabled**	Enable PCIe Port 2.
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 2 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
PCI Express Port 3	Disabled **Enabled**	Enable PCIe Port 3.
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 3 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.

10.6 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.6.1 Boot Settings Configuration

Feature	Options	Description
Setup Prompt Timeout	**2** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot (not recommended), 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.

Feature	Options	Description
Quiet Boot	**Disabled** Enabled	Disabled displays normal POST diagnostic messages. Enabled displays OEM logo instead of POST messages. Note: The default OEM logo is a dark screen.
Enter Setup If No Boot Device	No **Yes**	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The "Device Based" boot priority list allows you to select from a list of currently detected devices only. The "Type Based" boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the "Device Based" boot priority list might change dynamically in cases when devices are physically removed or added to the system. The "Type Based" boot menu is static and can only be changed by the user.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. Note: Only works with an ATX type power supply.
AT Shutdown Mode	System Reboot **Hot S5**	Determines the behavior of an AT-powered system after a shutdown.
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
Fast Boot	**Disabled** Enabled	Enable or disable boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS / legacy boot options.

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

10.7 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

10.7.1 Security Settings

Feature	Options	Description
Administrator Password	enter password	Specifies the setup administrator password.
HDD Security Configuration		
List of all detected hard disks supporting the security feature set	Select device to open device security configuration submenu	

10.7.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

10.8 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen. You can display a Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.

Feature	Description
Boot Override	
List of all boot devices currently detected	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to "Device Based".

11 Additional BIOS Features

The conga-TCA3 uses a congatec/AMI AptioEFI that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility (version 1.5.0 and later), which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as TA31R1xx or TA32R1xx where:

- TA31 is the BIOS for modules with Baytrail Single Channel Memory SoC
- TA32 is the BIOS for modules with Baytail Dual Channel Memory SoC
- R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

The TA31 and TA32 BIOS binary size is 8MB.

11.1 Supported Flash Devices

The conga-TC87 supports the following flash devices:

- Winbond W25Q64CVSSIG (8MB)

The flash device listed above has been tested and can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.

11.2 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

12 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.3	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0	http://www.serialata.org
PICMG® COM Express Module™ Base Specification	http://www.picmg.org/
PCI Express Base Specification, Revision 1.0a	http://www.pcisig.com/specifications