Qseven® conga-QG

AMD Embedded G-Series SoC

User's Guide

Revision 1.0

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2014.03.19	AEM	• Preliminary release.
1.0	2014.07.16	AEM	• Updated section 2.5 “Power Consumption”. Renamed Pin 153 signal name according to the Qseven specification. • Updated caution notes in sections 2.7 “Environmental Specifications“ and 4 “Heatspreader”. • Added section 9 “System Resources” and 10 “BIOS Setup Description”. • Official release.

Preface

This user's guide provides information about the components, features, connector and BIOS Setup menus available on the conga-QG. It is one of three documents that should be referred to when designing a Qseven® application. The other reference documents that should be used include the following:

Qseven® Design Guide

Qseven® Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

Disclaimer

The information contained within this user's guide, including but not limited to any product specification, is subject to change without notice.

congatec AG provides no warranty with regard to this user's guide or any other information contained herein and hereby expressly disclaims any implied warranties of merchantability or fitness for any particular purpose with regard to any of the foregoing. congatec AG assumes no liability for any damages incurred directly or indirectly from any technical or typographical errors or omissions contained herein or for discrepancies between the product and the user's guide. In no event shall congatec AG be liable for any incidental, consequential, special, or exemplary damages, whether based on tort, contract or otherwise, arising out of or in connection with this user's guide or any other information contained herein or the use thereof.

Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Copyright Notice

Trademarks

Product names, logos, brands, and other trademarks featured or referred to within this user's guide, or the congatec website, are the property of their respective trademark holders. These trademark holders are not affiliated with congatec AG, our products, or our website.

Warranty

congatec AG makes no representation, warranty or guaranty, express or implied regarding the products except its standard form of limited warranty (“Limited Warranty”) per the terms and conditions of the congatec entity, which the product is delivered from. These terms and conditions can be downloaded from www.congatec.com. congatec AG may in its sole discretion modify its Limited Warranty at any time and from time to time.

The products may include software. Use of the software is subject to the terms and conditions set out in the respective owner’s license agreements, which are available at www.congatec.com and/or upon request.

Beginning on the date of shipment to its direct customer and continuing for the published warranty period, congatec AG represents that the products are new and warrants that each product failing to function properly under normal use, due to a defect in materials or workmanship or due to non conformance to the agreed upon specifications, will be repaired or exchanged, at congatec’s option and expense.

Customer will obtain a Return Material Authorization (“RMA”) number from congatec AG prior to returning the non conforming product freight prepaid. congatec AG will pay for transporting the repaired or exchanged product to the customer.

Repaired, replaced or exchanged product will be warranted for the repair warranty period in effect as of the date the repaired, exchanged or replaced product is shipped by congatec, or the remainder of the original warranty, whichever is longer. This Limited Warranty extends to congatec’s direct customer only and is not assignable or transferable.

Except as set forth in writing in the Limited Warranty, congatec makes no performance representations, warranties, or guarantees, either express or implied, oral or written, with respect to the products, including without limitation any implied warranty (a) of merchantability, (b) of fitness for a particular purpose, or (c) arising from course of performance, course of dealing, or usage of trade.

congatec AG shall in no event be liable to the end user for collateral or consequential damages of any kind. congatec shall not otherwise be liable for loss, damage or expense directly or indirectly arising from the use of the product or from any other cause. The sole and exclusive remedy against congatec, whether a claim sound in contract, warranty, tort or any other legal theory, shall be repair or replacement of the product only..

Certification

congatec AG is certified to DIN EN ISO 9001:2008 standard.

Technical Support

congatec AG technicians and engineers are committed to providing the best possible technical support for our customers so that our products can be easily used and implemented. We request that you first visit our website at www.congatec.com for the latest documentation, utilities and drivers, which have been made available to assist you. If you still require assistance after visiting our website then contact our technical support department by email at support@congatec.com

Terminology

Term	Description
PCIe	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4, x8, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4, x8, or x16 link.
SSD	Solid State Drive
SD card	Secure Digital card is a non-volatile memory card format developed for use in portable devices.
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial-interface standard for hard disks
HDA	High Definition Audio
DDI	Digital Display Interface. DDI can operate as DisplayPort, HDMI or DVI.
DP	DisplayPort is a VESA open digital communications interface.
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
LPC	Low Pin-Count is a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy device support into a single IC.
I²C Bus	Inter-Integrated Circuit Bus is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system.
SM Bus	System Management Bus is a popular derivative of the I²C-bus.
SPI Bus	Serial Peripheral Interface is a synchronous serial data link standard that operates in full duplex mode.
GbE	Gigabit Ethernet
LVDS	Low-Voltage Differential Signaling
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

Contents

List of Tables

1 Introduction

Qseven® Concept

The Qseven® concept is an off-the-shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm and a specified pinout based on the high speed MXM system connector. The pinout remains the same regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

With the Qseven® evaluation carrier board, carrier board designers are provided with a reference design platform and the opportunity to test all the Qseven® I/O interfaces available and then choose the interfaces suitable for their application.

Qseven® applications are scalable, which means once a carrier board has been created, there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another - no need to redesign the carrier board.

This document describes the features available on the conga-QG, a congatec module based on AMD Embedded G-Series SoC. Additional information and schematic for the congatec Qseven® evaluation board can be found on the congatec website.

conga-QG Options Information

The conga-QG is available in four variants (three commercial and one industrial). This user's guide describes all of these variants and the table below shows the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

conga-QG (commercial variants)

Part-No.	015600	015601	015602
SoC	AMD Embedded GX-210HA SoC	AMD Embedded GX-210JA SoC	AMD Embedded GX-210HA SoC
CPU Freq.	1.0 GHz Dual Core	1.0 GHz Dual Core	1.0 GHz Dual Core
L2 Cache	1 MB (Shared)	1 MB (Shared)	1 MB (Shared)
GPU Freq.	300 MHz	225 MHz	300 MHz
Graphics Engine	AMD Radeon™ HD 8210E	AMD Radeon™ HD 8180E	AMD Radeon™ HD 8210E
Onboard Memory	2 GB ECC DDR3L-1333	2 GB ECC DDR3L-1066	2 GB ECC DDR3L-1333
PCIe	4x Gen2	3x Gen2	4x Gen2
USB 3.0	1x	1x	1x
DDI	Dual-mode DP 1.2	Dual-mode DP 1.2	Dual-mode DP 1.2
LVDS/eDP	LVDS	LVDS	LVDS
SSD	N/A	N/A	4 GB
SoC TDP	9 W	6 W	9 W

conga-QG (Industrial variants)

Part-No.	015610
SoC	AMD Embedded GX-209HA SoC
CPU Freq.	1.0 GHz Dual Core
L2 Cache	1 MB (Shared)
GPU Freq.	225 MHz
Graphics Engine	AMD Radeon™ HD 8180E
Onboard Memory	2 GB ECC DDR3L-1066
PCIe	4x Gen2
USB 3.0	1x
DDI	Dual-mode DP 1.2
LVDS/eDP	LVDS
SSD	N/A
SoC TDP	9 W (Ext Temp)

2 Specifications

2.1 Feature List

Table 1 Feature Summary

Form Factor	Based on Qseven® form factor specification revision 2.0	
SoC	AMD Embedded G-Series SoC up to 9W TDP	
Memory	Up to 8GB onboard ECC DDR3L-1600	
Chipset	Integrated in the SoC	
Audio	High Definition Audio (HDA) interface	
Ethernet	Gigabit Ethernet via Intel® Ethernet Controller I210.	
Graphics Options	AMD Radeon™ HD 8000E Series Graphics with support for Video Compressing Engine (VCE 2.0), Unified Video Decoder (UVD 4.2), OpenGL 4.2, OpenCL™ 1.2, DirectX®11.2 and up to two independent displays.	

	• LVDS (Integrated flat panel interface with 25-112MHz single/dual-channel Transmitter). Supports::
	  * Single-channel LVDS interface: 1 x 18 bpp or 1 x 24 bpp.
	  * Dual-channel LVDS interface : 2 x 18 bpp or 2 x 24 bpp.
	  * VESA standard or JEIDA data mapping
	  * Automatic Panel Detection via Embedded Panel Interface based on VESA EDID™ 1.3.
	  * Resolution up to 1920x1200 in dual channel LVDS mode.
	• Optional eDP interface
	NOTE: Either eDP or LVDS signals supported. Both not supported.
		• 1x DDI (Digital Display Interface) with support for
		  * 1x DisplayPort 1.2 (resolution up to 2560x1600 @ 60Hz).
		  * 1x HDMI 1.4a port (requires external level shifter)
		  * 1x DVI port (requires external level shifter).
		
		NOTE: To support HDMI/DVI, an external level shifter (e.g PTN 3360D) should be implemented on the user's carrier board.

Peripheral Interfaces	• 2x Serial ATA® up to 3Gb/s (1x SATA if the optional SSD is implemented) • Optional onboard SSD up to 64 GB • Up to 4x PCI Express® Gen2 ports (5 Gb/s) • 5x USB 2.0 • 1x USB 3.0	• UART • SD/SDIO • LPC Bus • SM Bus • I²C Bus, multimaster
BIOS	AMI Aptio® UEFI 2.x firmware, 8 MB serial flash memory with congatec Embedded BIOS features	
Power Management	ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).	

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 11 of this user's guide to determine what options are available on your particular module.

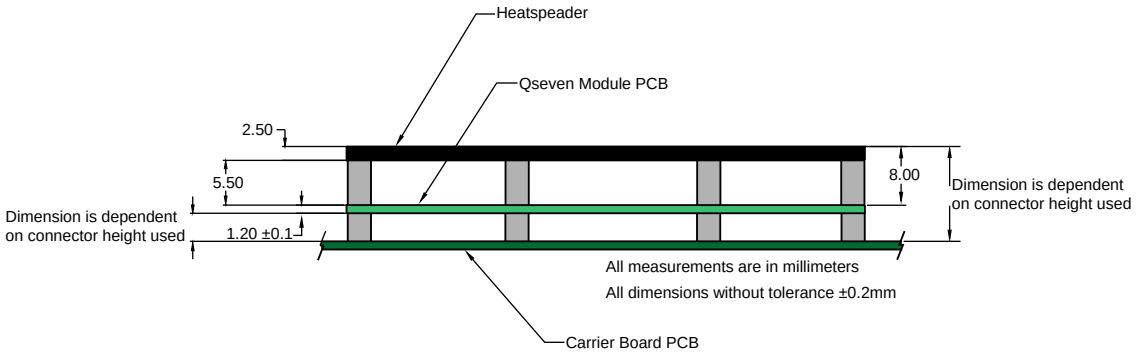
2.2 Supported Operating Systems

The conga-QG supports the following operating systems.

- Microsoft® Windows® 8
- Microsoft® Windows® 7
- Microsoft® Windows® 7 Embedded
- Linux

2.3 Mechanical Dimensions

- 70.0 mm x 70.0 mm @ (2 ¾" x 2 ¾")
- The Qseven® module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12mm thick.

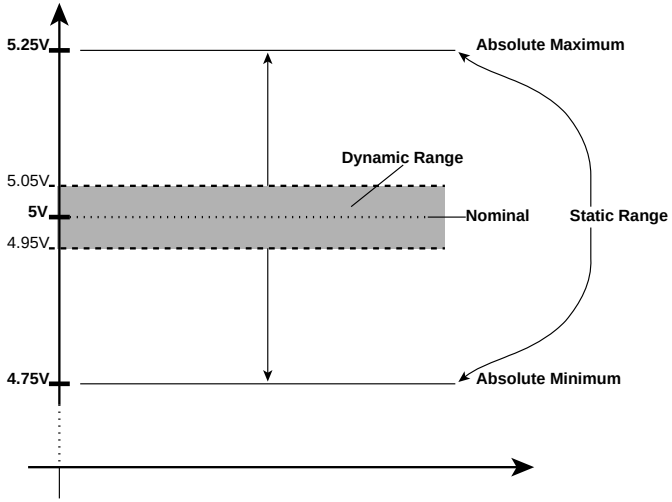


Rear View of Qseven Module

2.4 Supply Voltage Standard Power

- 5V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Characteristics			Min.	Typ.	Max.	Units	Comment
5V	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	± 50	mV_{PP}	0-20MHz
	Current						
5V_SB	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple				± 50	mV_{PP}	

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

Note

For information about the input power sequencing of the Qseven® module, refer to the Qseven® specification.

2.5 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used for testing includes a conga-QG module, conga-QEVAL, SATA drive, USB keyboard and USB mouse. The SATA drive, USB Keyboard, USB mouse were powered separately so that they do not influence the power consumption value that is measured for the module. To ensure that only the power consumption of the CPU module is measured, the conga-QEVAL power consumption was determined before the measurement and subtracted from the overall power consumption value measured.

The USB keyboard/mouse were detached once the module was configured within the OS. All recorded values were averaged over a 30 second time period. Cooling of the module was done by the module specific heatspreader and a fan cooled heatsink to measure the power consumption under normal thermal conditions

Each module was measured while running Windows 7 Professional 64Bit, Hyper Threading enabled, Speed Step enabled and Power Plan set to “Power Saver”. This setting ensures that core processors run in LFM (lowest frequency mode) with minimal core voltage during desktop idle. Each module tested was equipped with onboard dual channel memory and 1GB memory size per channel.

To measure the worst case power consumption the cooling solution was removed and the CPU core temperature was allowed to run up to between 90° and 95°C while running 100% workload with the Power Plan set to “Balanced”. The peak current value was then recorded. This value should be taken into consideration when designing the system’s power supply to ensure that the power supply is sufficient during worst case scenarios.

Power consumption values were recorded during the following stages:

Windows 7

- Desktop Idle (power plan = Power Saver)
- 100% CPU workload (see note below, power plan = Power Saver)
- 100% CPU workload at approximately 100°C peak power consumption (power plan = Balanced)
- Suspend to RAM. Supply power for S3 mode is 5V. Desktop Idle

Note

A software tool was used to stress the CPU to 100% workload.

Processor Information

The tables below provide additional information about the power consumption data for each of the conga-QG variants offered. The values are recorded at various operating mode.

Commercial Variants

2.5.1 conga-QG AMD Embedded GX-210HA SoC 1.0 GHz Dual Core 1MB L2 Cache

SoC TDP: 9 W

conga-QG Art. No. 015600	AMD Embedded GX-210HA SoC 1.0 GHz Dual Core 1MB L2 Cache 28nm Layout Rev. QFT3LX1 /BIOS Rev. QFT3R002				
Turbo Frequency	n/a				
Memory Size	2GB				
Operating System	**Windows 7 (64 bit)**				
Power State	Desktop Idle	100% CPU Workload [W]	100% CPU & 100% GPU Workload [W]	Max. Power Consumption (Worst Case)	Suspend to Ram (S3) 5V SB Input
Power consumption (Amperes/Watts)	**0.46 A / 2.30 W**	**1.64 A / 8.21 W**	**1.91 A / 9.56 W**	**2.09 A / 10.43 W**	**0.09 A / 0.43 W**

2.5.2 conga-QG AMD Embedded GX-210JA SoC 1.0 GHz Dual Core 1MB L2 Cache

SoC TDP: 6 W

conga-QG Art. No. 015601	AMD Embedded GX-210JA SoC 1.0 GHz Dual Core 1MB L2 Cache 28nm Layout Rev. QFT3LX1 /BIOS Rev. QFT3R002				
Turbo Frequency	n/a				
Memory Size	2GB				
Operating System	**Windows 7 (64 bit)**				
Power State	Desktop Idle	100% CPU Workload [W]	100% CPU & 100% GPU Workload [W]	Max. Power Consumption (Worst Case)	Suspend to Ram (S3) 5V SB Input
Power consumption (Amperes/Watts)	**0.44 A / 2.21 W**	**1.44 A / 7.20 W**	**1.46 A / 7.29 W**	**1.65 A / 8.25 W**	**0.08 A / 0.41 W**

2.5.3 conga-QG AMD Embedded GX-210HA SoC 1.0 GHz Dual Core 1MB L2 Cache

With 4GB SSD and 9W SoC TDP

conga-QG Art. No. 015602	AMD Embedded GX-210HA SoC 1.0 GHz Dual Core 1MB L2 Cache 28nm Layout Rev. QFT3LX1 /BIOS Rev. QFT3R002				
Turbo Frequency	n/a				
Memory Size	2GB				
Operating System	Windows 7 (64 bit)				
Power State	Desktop Idle	100% CPU Workload [W]	100% CPU & 100% GPU Workload [W]	Max. Power Consumption (Worst Case)	Suspend to Ram (S3) 5V SB Input
Power consumption (Amperes/Watts)	0.68 A / 3.42 W	A / 8.33 W	1.67 A / 9.91 W	2.13 A / 10.65 W	0.08 A / 0.39 W

Industrial Variant

2.5.4 conga-QG AMD Embedded GX-209HA SoC 1.0 GHz Dual Core 1MB L2 Cache (ext. temp)

SoC TDP: 9 W

conga-QG Art. No. 015610	AMD Embedded GX-209HA SoC 1.0 GHz Dual Core 1MB L2 Cache 28nm Layout Rev. QFT3LX1 /BIOS Rev. QFT3R002			
Turbo Frequency	n/a			
Memory Size	2GB			
Operating System	Windows 7 (64 bit)			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	TBD	TBD	TBD	TBD

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

2.6 Supply Voltage Battery Power

- 2.5V-3.6V DC
- Typical 3V DC

2.6.1 CMOS Battery Power Consumption

RTC @ 20ºC	Voltage	Current
Integrated in the SoC	3V DC	3.0 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found at www.congatec.com.

2.7 Environmental Specifications

Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -45° to +85°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

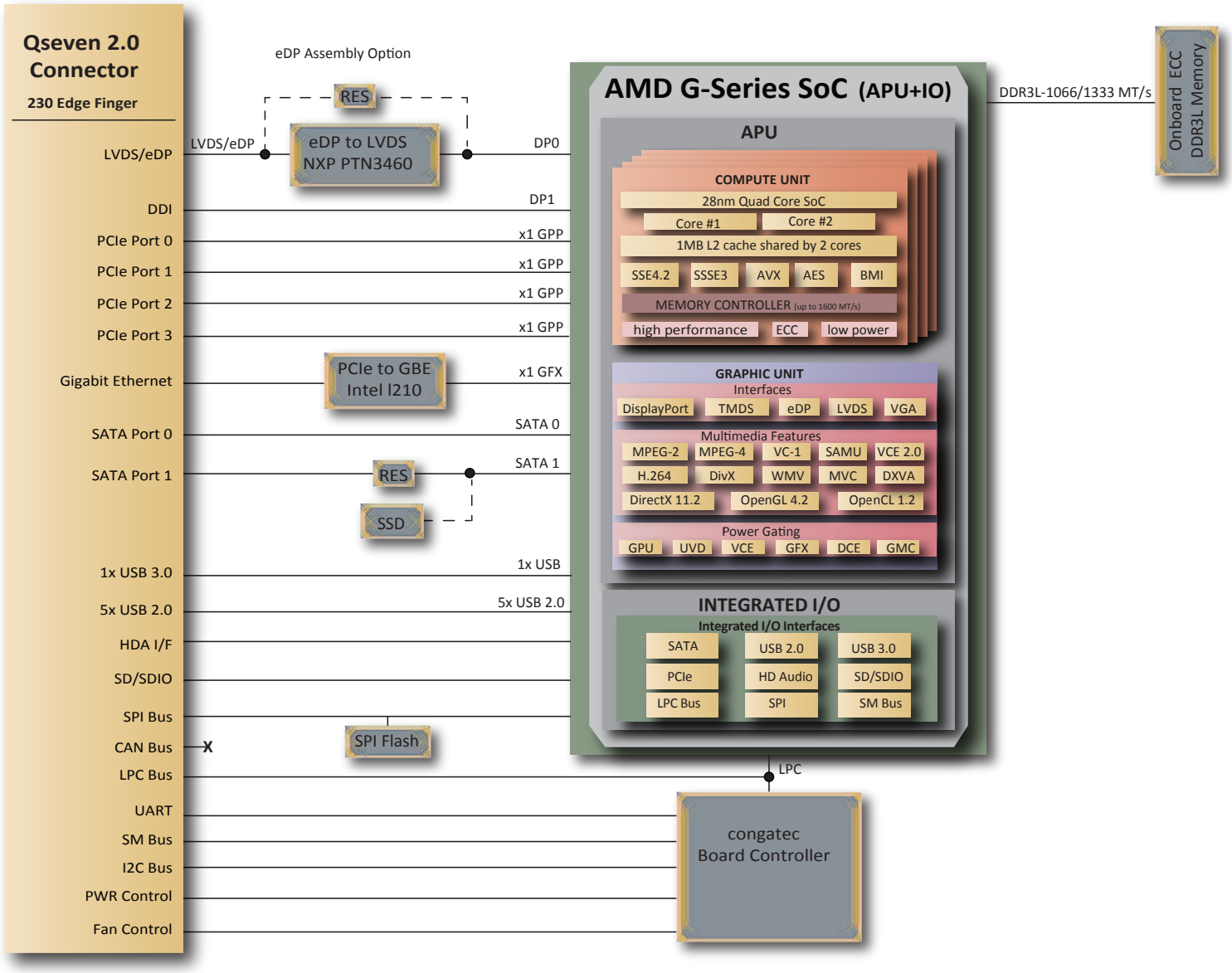
Caution

The above operating temperatures must be strictly adhered to at all times. The congatec heatspreader is only suitable for use within commercial temperature ranges (0° to 60°C). It is not designed to be used within industrial temperature ranges (-40° to 85°C). When using a heatspreader with conga-QG commercial grade variants, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution when used in a commercial temperature range. If for some reason it is not possible to use the appropriate congatec module heatspreader as a thermal interface for conga-QG commercial grade variants or if an industrial grade variant of conga-QG is being used within industrial temperature ranges, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



4 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module and is thermally coupled to the CPU via a thermal gap filler. On some modules, it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis thereby using the whole chassis as a heat dissipater.

Caution

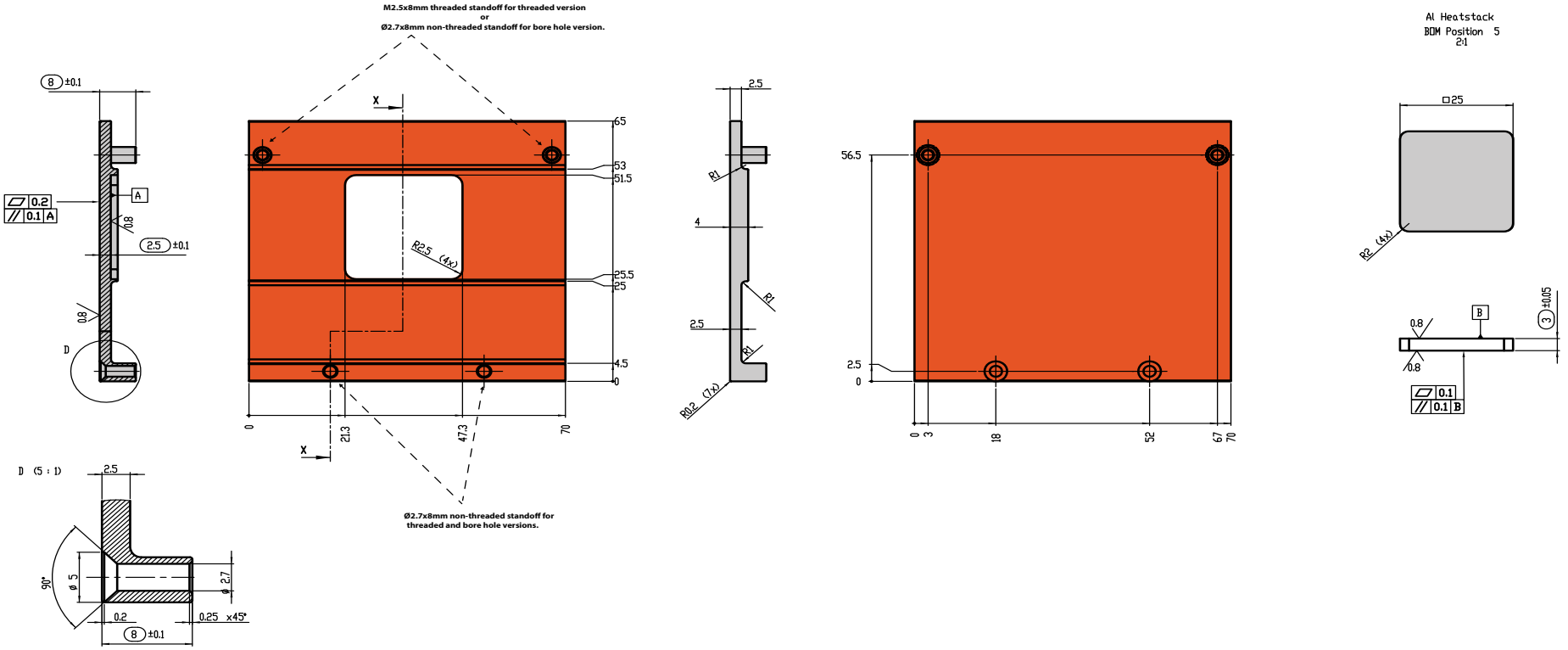
congatec Qseven® heaspreaders have been specifically designed for use within commercial temperature ranges (0° to 60°C) only. When using industrial temperature variants of the conga-QG in industrial temperature ranges (-40° to 85°C), use of the conga-QG heatspreaders is not recommended by congatec. Its use is at the risk of the end user.

It is the responsibility of the end user to design an optimized thermal solution that meets the needs of their application within the industrial environmental conditions it is required to operate in. Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

Only heatspreaders that feature fixing post that secure the thermal stacks should be used for applications that require the heatspreader to be mounted vertically. It cannot be guaranteed that the thermal stacks will not move if a heatspreader that does not have the fixing post feature is used in vertically mounted applications.

Additionally, the gap pad material used on all heatspreaders contains silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.

4.1 Heatspreader Dimensions



Note

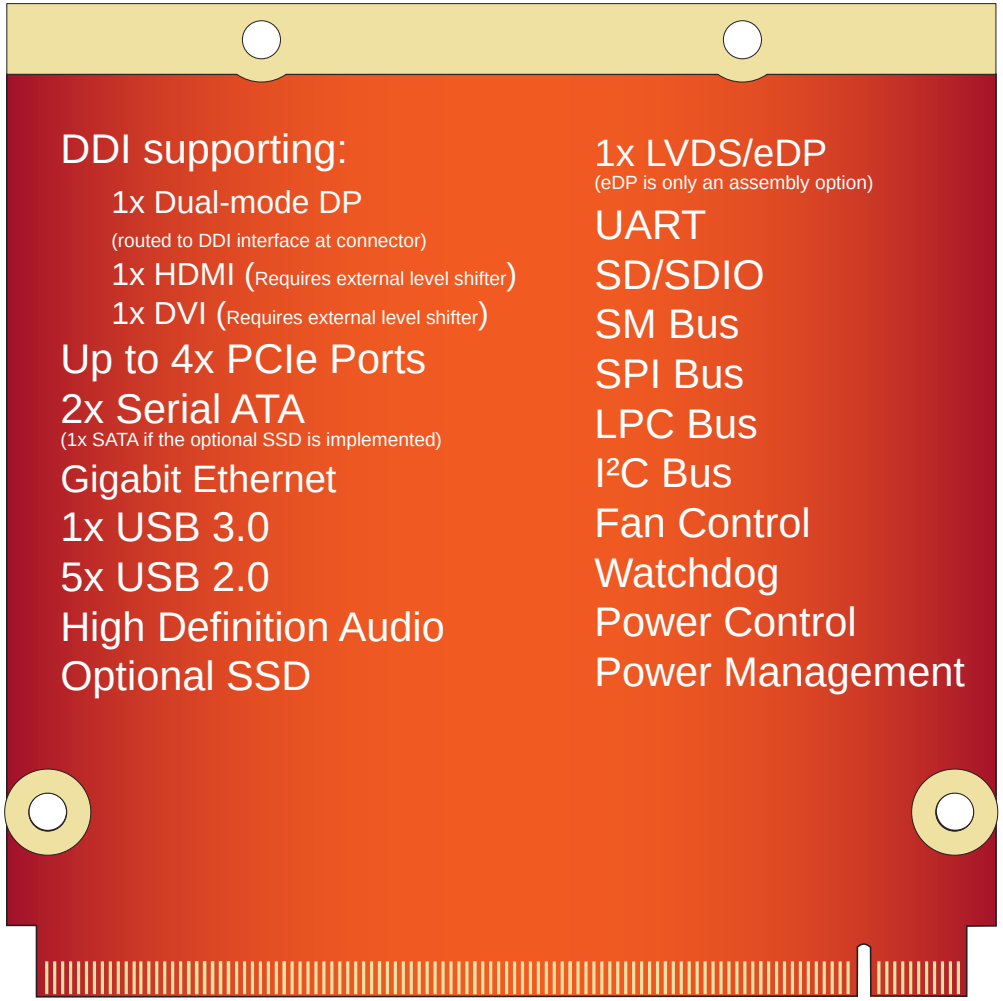
All measurements are in millimeters. Torque specification for heatspreader screws is 0.3 Nm. Mechanical system assembly mounting shall follow the valid DIN/IS0 specifications. The cooling strip found on the conga-QG is connected directly to the ground plane when mounted in the conga-QEVAL evaluation carrier board. For more information about connecting the conga-QG's PCB cooling plate to the carrier board ground plane, refer to the Qseven® Design Guide.

Caution

When using the heatspreader in a high shock and/or vibration environment, congatec recommends the use of a thread-locking fluid on the heatspreader screws to ensure the above mentioned torque specification is maintained.

5 Connector Subsystems

The conga-QG is based on the Qseven® standard and therefore has 115 edge fingers on the top and bottom side of the module that mate with the 230-pin card-edge MXM connector located on the carrier board. This connector is able to interface the available signals of the conga-QG with the carrier board peripherals.



5.1 PCI Express™

The controller hub integrated in the AMD G-Series SoC provides four x1 general purpose PCI Express ports. The conga-QG offers these four PCI Express™ ports externally on the edge finger. These ports are PCI Express™ Gen. 2 compliant and can be configured as 4x1, 1x2 + 2x1, 2x2 or 1x4 links.

The PCI Express interface is based on the PCI Express Specification 2.0 with Gen 1 and Gen 2 speeds.

Note

Some conga-QG variants do not support PCIe3 differential pair.

5.2 ExpressCard™

The Qseven® specification 2.0 does not support ExpressCard.

5.3 Gigabit Ethernet

The conga-QG offers Gigabit Ethernet with the integration of Intel i210 Ethernet Controller. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MDI0± to GBE0_MDI3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

Note

The GbE Controller on the conga-QG supports only three LEDs outputs:

GBE_LINK100# *100Mb/s link indicator*

GBE_LINK1000# *1000Mb/s link indicator*

GBE_LINK#/ACT *Combined all speed link with the link activity that is connected to GBE_LINK# pin on Qseven connector.*

Additionally, the conga-QG can drive gigabit ethernet LEDs directly with up to 10mA.

5.4 Serial ATA™ (SATA)

The conga-QG offers two Serial ATA ports (SATA 0-1) on the edge finger. These SATA ports are Gen 2 compliant, capable of up to 3.0 Gb/s transfer rate. Any of the ports can be configured to a lower transfer rate of 1.5 Gb/s for saving power.

The SATA controller supports two modes of operation - IDE and AHCI mode.

Note

The second SATA port (SATA 1) is not supported if the optional SSD is implemented.

5.5 USB 2.0

The conga-QG offers five USB 2.0 (USB 1-5) via the OHCI and EHCI controllers provided by the integrated controller hub. These controllers comply with USB 1.1 and 2.0 specifications. The USB ports are capable of supporting USB 1.1 and 2.0 compliant devices. See section 7.5 for more information about xHCI and EHCI port mapping.

Note

USB 2.0 ports 0 and 1 are connected to XHCI controller when USB 3.0 ports are enabled.

5.6 USB 3.0

The conga-QG offers one USB 3.0 interface on the edge finger. This interface is controlled by an xHCI host controller in the SoC. The host controller allows data transfers of up to 5 Gb/s and supports SuperSpeed, high-speed, full-speed and low-speed USB signalling. To support this interface on the conga-QG, ports 6-7 should be paired with USB port 0 signals. See section 7.5 for more information about xHCI and EHCI port mapping.

5.7 SD/SDIO

The conga-QG offers a 4-bit SD/SDIO interface on the edge finger.

5.8 High Definition Audio (HDA)

The conga-QG provides an interface that supports the connection of high definition audio codec.

5.9 Digital Display Interface

The conga-QG supports Digital Display Interface on the edge finger. This interface supports dual-mode DisplayPort 1.2 on the conga-QG. To support HDMI/DVI, customers should implement an external level shifter e.g PTN3360D on their carrier board.

The processor on the conga-QG supports High-bandwidth Digital Content Protection (HDCP) for playing high definition content over digital interfaces. Integrated in the processor is a dedicated mini HD audio controller which drives audio on integrated digital display interfaces such as HDMI and DisplayPort.

The conga-QG supports up to two independent displays. Any combination of DDI and LVDS is possible as shown in the table below:

Table 2 Display Combination

Display 1	Display 2	Display 1 Max. Resolution	Display 2 Max. Resolution
DDI (DP/HDMI/DVI)	LVDS/eDP	DP: 2560x1600 @60Hz HDMI/DVI: 1920x1200 @60Hz	1920x1200 @60Hz
LVDS/eDP	DDI (DP/HDMI/DVI)	1920x1200 @60Hz	DP: 2560x1600 @60Hz HDMI/DVI: 1920x1200 @60Hz

5.9.1.1 HDMI

The conga-QG offers an HDMI interface on the Digital Display Interface of the Qseven® edge finger connector. The interface is based on HDMI 1.4a specification with support for 3D, 4K, Deep Color, maximum display resolution of 1920x1200 at 60Hz. Supported audio formats are AC-3 Dolby Digital, Dolby Digital Plus, Dolby TrueHD, DTS-HD, DTS-HD Master Audio.

To support two independent displays, the user can combine the HDMI interface with the LVDS/eDP interface.

Note

To support the HDMI interface, customers should implement an external level translator/shifter (e.g PTN3360D) on their baseboard.

5.9.1.2 DVI

The conga-QG offers one single-link DVI interface on the Digital Display Interface of the Qseven® edge finger connector. The interface supports a maximum display resolution of 1920x1200 at 60 Hz and can be combined with LVDS/eDP to support two independent displays.

Note

To support the DVI interface, customers should implement an external level translator/shifter (e.g PTN3360D) on their baseboard.

5.9.1.3 DisplayPort (DP)

The conga-QG offers one dual-mode DisplayPort 1.2 interface on the DDI of the Qseven® edge finger connector. The interface supports all mandatory features of the VESA DisplayPort Standard, versions 1.2 including Multi-Stream Transport (MST) for monitor daisy-chaining, stereoscopic 3D frame transport, maximun bit rate of 5.4 Gbps and maximum display resolution of 2560x1600 at 60 Hz. Supported audio formats are linear PCM, Dolby Digital (AC-3), Dolby TrueHD, DTS, DTS-HD Master Audio and up to 8 channels.

To support two independent displays, the user can combine the DP interface with the LVDS/eDP interface.

5.10 LPC

The conga-QG offers the Low Pin Count (LPC) bus via the integrated controller hub. The LPC bus is similar to a serialized ISA bus but with fewer signals. Due to the software compatibility with the ISA bus, it is easy to implement I/O extensions such as additional serial ports on an application specific baseboard using the LPC bus. Many devices are available for this cost-efficient, low-speed interface designed to support low bandwidth and legacy devices.

The LPC host bus controller supports one master DMA device. TPM version 1.1/1.2 devices are also supported. See section 9.1.1 for more information about the LPC Bus.

5.11 SPI

The conga-QG offers the SPI interface on the edge finger connector. This interface is only used to boot a BIOS from an SPI Flash device placed on the carrier board.

5.12 CAN Bus

The conga-QG does not support CAN bus.

5.13 Power Control

The conga-QG supports ATX-style power supplies control. To do this, the power supply must provide a constant source of VCC_5V_SB power. The conga-QG also supports AT-style power supply (5V only). In this case, the conga-QG's pin PWRBTN# should be left unconnected. Pin SUS_S3# should control the main power regulators on the carrier board (+3.3V) and pins VCC_5V_SB should be connected to the 5V input power rail according to the Qseven® specification.

PWGIN

PWGIN (pin 26) can be connected to an external power good circuit. This input is optional and should be left unconnected when not used. By using an internal monitor on the +5V input voltage and/or the internal power supplies, the conga-QG module can generate its own power-on good.

SUS_S3#

The SUS_S3# (pin 18) signal is an active-low output that can be used to control the main 5V rail of the power supply for module and all other main power supplies on carrier board. To do this, the inverter/transistor on the carrier board must invert the signal and you can power the inverter/transistor with either standby voltage (ATX-style) or system input voltage (AT-style).

PWRBTN#

When using ATX-style power supplies, PWRBTN# (pin 20) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3.3V_SB using a 10k resistor. When PWRBTN# is asserted, it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Note

To initiate an ACPI event, the SoC expects a rising edge on the PWRBTN# signal.

Power Supply Implementation Guidelines

5 volt input power is the only operational power source for the conga-QG. The remaining necessary voltages are internally generated on the module with onboard voltage regulators.

A carrier board designer should be aware of the important information below when designing a power supply for a conga-QG application:

- We have noticed that on some occasions, problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction. This problem though rare, has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through an oscilloscope. This will help to determine if the rise is indeed monotonic and does not have any dips. You should do this during the power supply qualification phase to ensure that the problem does not occur in the application. For more information about this issue, visit www.formfactors.org and view page 25 figure 7 of the document “ATX12V Power Supply Design Guide V2.2”.

Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush-current on the conga-QG VCC_5V_SB power rail (8ms soft-start) can go up as high as 0.4A for a maximum of 100µs. Sufficient decoupling capacitance must be implemented to ensure proper power-up sequencing.

The maximum peak-current on the conga-QG VCC (5V) power rail can be as high as 5A for a maximum of 100µs. You should therefore ensure the power supply and decoupling capacitors provide enough power to drive the module.

Note

For more information about power control event signals refer to the Qseven® specification.

5.14 Power Management

ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3). No support for legacy APM.

5.15 I²C Bus

The conga-QG supports I²C bus via the congatec board controller (cBC). The I²C host controller in the cBC provides a multi-master I²C Bus and runs at fast mode.

5.16 UART

The conga-QG supports UART interface via the congatec Board controller. The UART interface offered is fully featured with control signals. For the UART description, see table 6 of section 8 “Signal Descriptions and Pinout Tables”.

6 Additional Features

6.1 SSD

The conga-QG offers an optional 64GB SSD onboard. The second SATA port (SATA 1) is not supported if the optional SSD is implemented.

6.2 congatec Board Controller (cBC)

The conga-QG is equipped with a Texas Instruments Tiva™ TM4E1231H6ZRBI microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

6.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.2.2 Fan Control

The conga-QG has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

A four wire fan must be used to generate the correct speed readout.

6.2.3 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are "Always On", "Remain Off" and "Last State".

6.2.4 Watchdog

The conga-QQ is equipped with a multi stage watchdog solution that is triggered by software. The Qseven® Specification does not provide support for external hardware triggering of the watchdog, which means the conga-QG does not support external hardware triggering.

For more information about the watchdog feature, see the BIOS setup description in section 10.4.2 of this document and the application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

6.3 Embedded BIOS

The conga-QG is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. This provides important features to embedded systems.

6.3.1 CMOS Backup in Non Volatile Memory

A copy of the CMOS memory (SRAM) is stored in the BIOS flash device. This prevents the system from booting up with incorrect system configuration if the backup battery (RTC battery) fails. Additionally, it provides the ability to create systems that do not require a CMOS backup battery.

6.3.2 OEM CMOS Default Settings and OEM BIOS Logo

This feature allows system designers to create and store their own CMOS default configuration and BIOS logo (splash screen) within the BIOS flash device. Customized BIOS development by congatec for these changes is no longer necessary because customers can easily do these changes by themselves using the congatec system utility CGUTIL.

6.3.3 OEM BIOS Code

With the congatec embedded BIOS it is possible for system designers to add their own code to the BIOS POST process. Except for custom specific code, this feature can also be used to support Window 7 SLIC table, verb tables for HDA codecs, rare graphic modes and Super I/O controllers.

For more information about customizing the congatec embedded BIOS, refer to the congatec system utility user's guide (CGUTLm1x.pdf) and can be found on the congatec AG website at www.congatec.com or contact congatec technical support.

6.4 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec AG defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a smart battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI-capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for additional modifications to the system BIOS.

The conga-QG BIOS fully supports this interface. For more information about this subject, visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

6.4.1 API Support (CGOS/EAPI)

To allow customers benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux and QNX. The architecture of the CGOS API driver makes it possible to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

Other COM (Computer on Modules) vendors offer similar driver solutions for these kind of embedded PC features, which are by nature proprietary. All the API solutions that can be found on the market are not compatible to each other. As a result, writing application software that can run on more than one vendor's COM is complicated. Customers have to change their application software when switching to another COM vendor. However, with EAPI (Embedded Application Programming Interface), this problem of portability is now solved

EAPI (Embedded Application Programming Interface) is a programming interface defined by the PICMG. With this unified API, it is now possible to run the same application on all vendor's COMs that offer EAPI driver support. Contact congatec technical support for more information about EAPI.

6.5 Suspend to RAM

The Suspend to RAM feature is available on the conga-QG.

7 conga Tech Notes

The conga-QG has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help the user to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

7.1 AHCI

The integrated controller hub in the AMD G-Series SoC provides hardware support for Advanced Host Controller Interface (AHCI), a new programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

7.2 AMD Processor Features

7.2.1 AMD64 Technology

- AMD64 technology instruction-set extensions
- 64-bit integer registers, 48-bit virtual addresses, and 40-bit physical addresses
- Sixteen 64-bit integer registers
- Sixteen 128-bit SSE/SSE2/SSE3/SSE4a registers

For more information about AMD64 Technology, visit http://www.amd.com.

7.2.2 Power Management

- Multiple low-power states
- AMD AllDay™ power technology
- System Management Mode (SMM)
- ACPI-compliant, including support for processor performance states (P-states)

- Supports processor power states C0, C1, CC6, and PC6
- Supports sleep states including S0, S3, S4, and S5
- PCIe® core power gating
- PCIe speed power policy

For more information about AMD64 Technology, visit http://www.amd.com.

7.2.3 AMD Virtualization™ Technology

- SVM pause count capability
- SVM disable and lock
- Rapid virtualization indexing (nested paging)
- Improved world-switch speed

For more information about AMD64 Technology, visit http://www.amd.com.

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not to congatec technical support.

7.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This helps the operating system to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-QG ACPI thermal solution offers three different cooling policies:

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not

produce any noise. Use the “passive cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy, the operating system turns the fan on/off. Although active cooling devices consume power and produce noise, they are able to cool the thermal zone without reducing the overall system performance. Use the “active cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion to ensure that high temperatures do not damage the system. Use the “critical trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points. If passive cooling is activated and the processor temperature is above the trip point, the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.4 ACPI Suspend Modes and Resume Events

conga-QG supports S3 (STR= Suspend to RAM). For more information about S3 wake events see section 10.4.7 “ACPI Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

- Windows 7, Windows 8, Linux

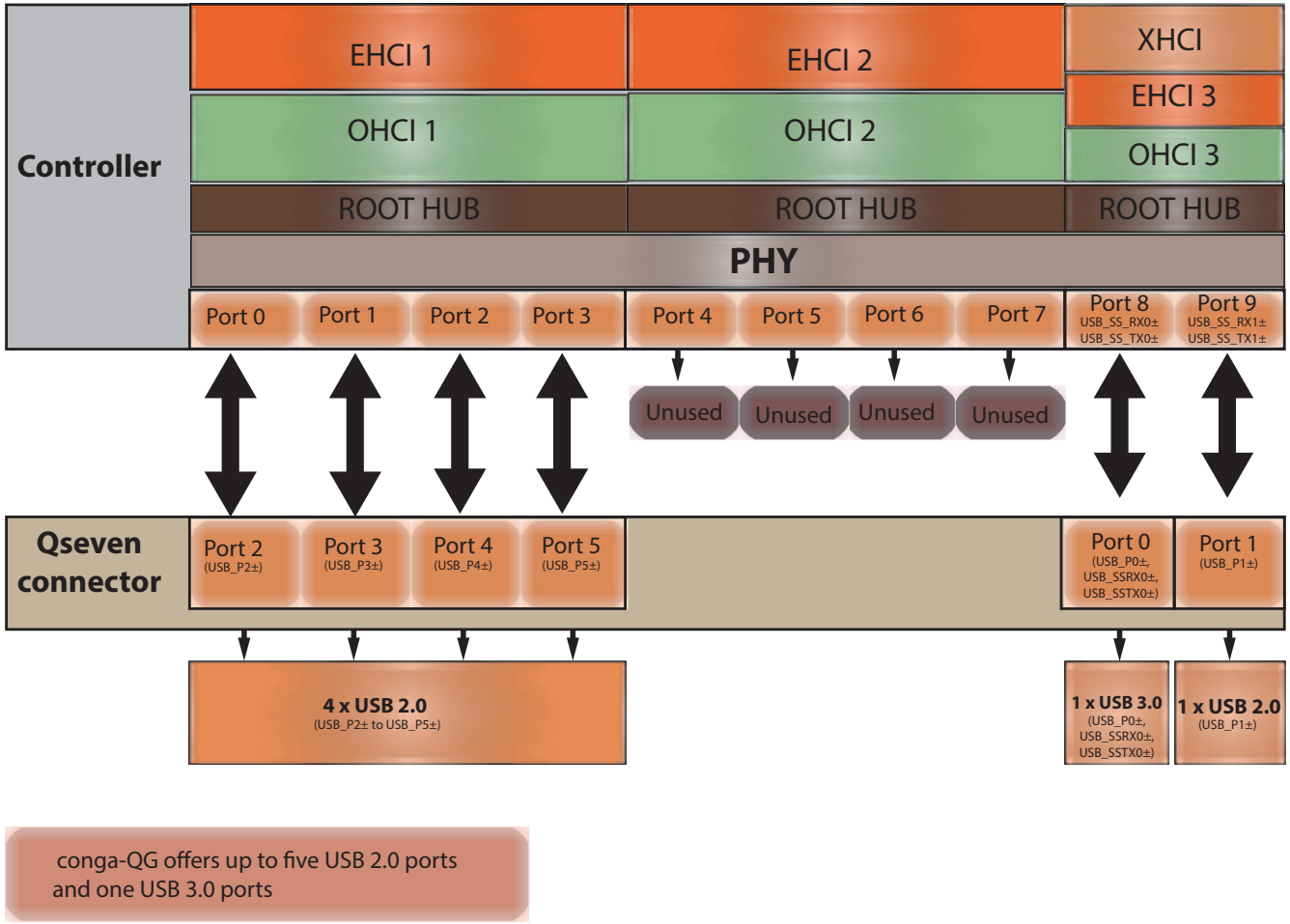
This table lists the “Wake Events” that resume the system from S3 unless otherwise stated in the “Conditions/Remarks” column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
SMBALERT#	Wakes unconditionally from S3-S5.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
USB Mouse/Keyboard Event	When Standby mode is set to S3, the following must be done for a USB Mouse/Keyboard Event to be used as a Wake Event. USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). Under Windows XP add following registry entries: Add this key: HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\usb Under this key add the following value: “USBBIOSx“=DWORD:00000000 *Note that Windows XP disables USB wakeup from S3, so this entry has to be added to re-enable it.* Configure USB keyboard/mouse to be able to wake up the system: In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check ‘Allow this device to bring the computer out of standby’. *Note: When the standby state is set to S3 in the ACPI setup menu, the power management tab for USB keyboard /mouse devices only becomes available after adding the above registry entry and rebooting to allow the registry changes to take affect.*
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

7.5 USB Host Controller

The conga-QG offers up to five USB 2.0 ports and one USB 3.0 port. The integrated controller hub in the SoC supports these ports with one xHCI controller and two OHCI/EHCI controller pairs. The routing diagram is shown below:

Routing Diagram



conga-QG offers up to five USB 2.0 ports and one USB 3.0 ports

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on Qseven® module's edge fingers.

Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

Not all the signals described in this section are available on all conga-QG variants. Use the article number of the module and refer to the "conga-QG Options Information table" in section 1 to determine the options available on the module.

Table 3 Signal Tables Terminology Descriptions

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PP	Push Pull
I/O	Bi-directional Input/Output Pin
P	Power Input
DP	DisplayPort
NA	Not applicable
NC	Not Connected
PCIE	PCI Express differential pair signals. In compliance with the PCI Express Base Specification 2.0
GB_LAN	Gigabit Ethernet Media Dependent Interface differential pair signals. In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet Specification.
USB	Universal Serial Bus differential pair signals. In compliance with the Universal Serial Bus Specification 2.0
USBSS	USB Superspeed signals
SATA	Serial Advanced Technology Attachment differential pair signals. In compliance with the Serial ATA High Speed Serialized AT Attachment Specification 2.6.
SPI	Serial Peripheral Interface bus is a synchronous serial data link that operates in full duplex mode.
CAN	Controller Area Network bus is a vehicle bus standard that allows microcontrollers and devices to communicate with each other within a vehicle without a host computer.
LVDS	Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0.
TMDS	Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0.
CMOS	Logic input or output.

Table 4 Edge Finger Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Power Ground	2	GND	Power Ground
3	GBE_MDI3-	Gigabit Ethernet MDI3-	4	GBE_MDI2-	Gigabit Ethernet MDI2-
5	GBE_MDI3+	Gigabit Ethernet MDI3+	6	GBE_MDI2+	Gigabit Ethernet MDI2+
7	GBE_LINK100#	100 Mbps link speed	8	GBE_LINK1000#	1000 Mbps link speed
9	GBE_MDI1-	Gigabit Ethernet MDI1-	10	GBE_MDI0-	Gigabit Ethernet MDI0-
11	GBE_MDI1+	Gigabit Ethernet MDI1+	12	GBE_MDI0+	Gigabit Ethernet MDI0+
13	GBE_LINK#	Gigabit Ethernet Link indicator	14	GBE_ACT#	Gigabit Ethernet Activity indicator
15	GBE_CTREF	Reference voltage for GBE	16	SUS_S5#	S5 (Soft OFF) – shutdown state
17	WAKE#	External system wake event	18	SUS_S3#	S3 (Suspend to RAM) – SLP
19	SUS_STAT#	Suspend status	20	PWRBTN#	Power button
21	SLP_BTN#	Sleep button	22	LID_BTN#	LID button
23	GND	Power Ground	24	GND	Power Ground
25	GND	Power Ground	26	PWGIN	Power good input
27	BATLOW#	Battery low input	28	RSTBTN#	Reset button input
29	SATA0_TX+	Serial ATA Channel 0 TX+	30	SATA1_TX+	Serial ATA Channel 1 TX+
31	SATA0_TX-	Serial ATA Channel 0 TX-	32	SATA1_TX-	Serial ATA Channel 1 TX-
33	SATA_ACT#	Serial ATA Activity	34	GND	Power Ground
35	SATA0_RX+	Serial ATA Channel 0 RX+	36	SATA1_RX+	Serial ATA Channel 1 RX+
37	SATA0_RX-	Serial ATA Channel 0 RX-	38	SATA1_RX-	Serial ATA Channel 1 RX-
39	GND	Power Ground	40	GND	Power Ground
41	BIOS_DISABLE# /BOOT_ALT#	BIOS Module disable Boot Alternative Enable	42	SDIO_CLK	SDIO Clock Output
43	SDIO_CD#	SDIO Card Detect	44	SDIO_LED	SDIO LED
45	SDIO_CMD	SDIO Command/Response	46	SDIO_WP	SDIO Write Protect
47	SDIO_PWR#	SDIO Power Enable	48	SDIO_DAT1	SDIO Data Line 1
49	SDIO_DAT0	SDIO Data Line 0	50	SDIO_DAT3	SDIO Data Line 3
51	SDIO_DAT2	SDIO Data Line 2	52	SDIO_DAT5 (*)	SDIO Data Line 5
53	SDIO_DAT4 (*)	SDIO Data Line 4	54	SDIO_DAT7 (*)	SDIO Data Line 7
55	SDIO_DAT6 (*)	SDIO Data Line 6	56	USB_DRIVE_VBUS (*)	USB Power enable pin for USB Port 1. Enables the Power for the USB-OTG port on the carrier board.
57	GND	Power Ground	58	GND	Power Ground
59	HDA_SYNC / I2S_WS	HD Audio/AC'97 Synchronization. Multiplexed with I2S Word Select from Codec	60	SMB_CLK / GP1_I2C_CLK	SMBus Clock line. Multiplexed with General Purpose I²C bus #1 clock line
61	HDA_RST# / I2S_RST#	HD Audio/AC'97 Codec Reset. Multiplexed with I2S Codec Reset	62	SMB_DAT / GP1_I2C_DAT	SMBus Data line. Multiplexed with General Purpose I²C bus #1 data line.
63	HDA_BITCLK / I2S_CLK	HD Audio/AC'97 Serial Bit Clock. Multiplexed with I2S Serial Data Clock from Codec.	64	SMB_ALERT#	SMBus Alert input
65	HDA_SDI / I2S_SDI	HD Audio/AC'97 Serial Data In. Multiplexed with I2S Serial Data Input from Codec	66	GP0_I2C_CLK	General Purpose I2C Bus No 0 clock line

Pin	Signal	Description	Pin	Signal	Description
67	HDA_SDO / I2S_SDO	HD Audio/AC'97 Serial Data Out. Multiplexed with I2S Serial Data Output from Codec	68	GP0_I2C_DAT	General Purpose I2C Bus No 0 data line
69	THRM#	Thermal Alarm active low	70	WDTRIG#	Watchdog trigger signal
71	THRMTRIP# (*)	Thermal Trip indicates an overheating condition	72	WDOUT	Watchdog event indicator
73	GND	Power Ground	74	GND	Power Ground
75	USB_P7- / USB_SSTX0-	USB Port 7 Differential Pair- . Multiplexed with Superspeed USB transmit differential pair-	76	USB_P6- / USB_SSRX0-	USB Port 6 Differential Pair-. Multiplexed with Superspeed USB receive differential pair-
77	USB_P7+ / USB_SSTX0+	USB Port 7 Differential Pair+. Multiplexed with Superspeed USB transmit differential pair+	78	USB_P6+ / USB_SSRX0+	USB Port 6 Differential Pair+.Multiplexed with Superspeed USB receive differential pair+
79	USB_6_7_OC#	Over current detect input 6/7 USB	80	USB_4_5_OC#	Over current detect input 4/5 USB
81	USB_P5- / USB_SSTX1-	USB Port 5 Differential Pair-. Multiplexed with Superspeed USB transmit differential pair-	82	USB_P4- / USB_SSRX1-	USB Port 4 Differential Pair-. Multiplexed with Superspeed USB receive differential pair-
83	USB_P5+ / USB_SSTX1+	USB Port 5 Differential Pair+. Multiplexed with Superspeed USB transmit differential pair+	84	USB_P4+ / USB_SSRX1+	USB Port 4 Differential Pair+. Multiplexed with Superspeed USB receive differential pair+
85	USB_2_3_OC#	Over current detect input 2/3 USB	86	USB_0_1_OC#	Over current detect input 0/1 USB
87	USB_P3-	USB Port 3 Differential Pair-	88	USB_P2-	USB Port 2 Differential Pair-
89	USB_P3+	USB Port 3 Differential Pair+	90	USB_P2+	USB Port 2 Differential Pair+
91	USB_VBUS (*)	USB Port 1 VBUS pin	92	USB_ID (*)	USB ID pin
93	USB_P1-	USB Port 1 Differential Pair-	94	USB_P0-	USB Port 0 Differential Pair-
95	USB_P1+	USB Port 1 Differential Pair+	96	USB_P0+	USB Port 0 Differential Pair+
97	GND	Power Ground	98	GND	Power Ground
99	eDP0_TX0+ / LVDS_A0+	eDP Primary Channel 0+ LVDS Primary channel 0+	100	eDP1_TX0+ / LVDS_B0+	eDP Secondary channel 0+ LVDS Secondary channel 0+
101	eDP0_TX0- / LVDS_A0-	eDP Primary channel 0- LVDS Primary channel 0-	102	eDP1_TX0- / LVDS_B0-	eDP Secondary channel 0- LVDS Secondary channel 0-
103	eDP0_TX1+ / LVDS_A1+	eDP Primary channel 1+ LVDS Primary channel 1+	104	eDP1_TX1+ / LVDS_B1+	eDP Secondary channel 1+ LVDS Secondary channel 1+
105	eDP0_TX1- / LVDS_A1-	eDP Primary channel 1- LVDS Primary channel 1-	106	eDP1_TX1- / LVDS_B1-	eDP Secondary channel 1- LVDS Secondary channel 1-
107	eDP0_TX2+ / LVDS_A2+	eDP Primary channel 2+ LVDS Primary channel 2+	108	eDP1_TX2+ / LVDS_B2+	eDP Secondary channel 2+ LVDS Secondary channel 2+
109	eDP0_TX2- / LVDS_A2-	eDP Primary channel 2- LVDS Primary channel 2-	110	eDP1_TX2- / LVDS_B2-	eDP Secondary channel 2- LVDS Secondary channel 2-
111	LVDS_PPEN	LVDS Power enable	112	LVDS_BLEN	LVDS Backlight enable
113	eDP0_TX3+ / LVDS_A3+	eDP Primary channel 3+ LVDS Primary channel 3+	114	eDP1_TX3+ / LVDS_B3+	eDP Secondary channel 3+ LVDS Secondary channel 3+
115	eDP0_TX3- / LVDS_A3-	eDP Primary channel 3- LVDS Primary channel 3-	116	eDP1_TX3- / LVDS_B3-	eDP Secondary channel 3- LVDS Secondary channel 3-
117	GND	Power Ground	118	GND	Power Ground
119	eDP0_AUX+ / LVDS_A_CLK+	eDP Primary Auxilliary channel+ LVDS Primary channel CLK+	120	eDP1_AUX+ / LVDS_B_CLK+	eDP Secondary Auxiliary channel CLK+ LVDS Secondary channel CLK+

Pin	Signal	Description	Pin	Signal	Description
121	eDP0_AUX- / LVDS_A_CLK-	eDP Primary Auxilliary channel- LVDS Primary channel CLK-	122	eDP1_AUX- / LVDS_B_CLK-	eDP Secondary Auxiliary channel CLK- LVDS Secondary channel CLK-
123	LVDS_BLT_CTRL / GP_PWM_OUT0	PWM Backlight brightness General Purpose PWM Output	124	GP_1-Wire_Bus (*)	General Purpose 1-wire bus interface
125	LVDS_DID_DAT / GP_I2C_DAT	DDC Display ID Data line General Purpose I2C Data line	126	eDP0_HPD# / LVDS_BLC_DAT	SSC clock chip data line. Can be used as eDP primary hotplug detect
127	LVDS_DID_CLK / GP_I2C_CLK	DDC Display ID Clock line General Purpose I2C Clock line	128	eDP1_HPD# / LVDS_BLC_CLK (*)	SSC clock chip clock line. Can be used as eDP secondary hotplug detect
129	CAN0_TX (*)	CAN TX Output for CAN Bus Channel 0	130	CAN0_RX (*)	CAN RX Input for CAN Bus Channel 0
131	DP_LANE3+ / TMDS_CLK+	DisplayPort differential pair line lane 3. Multiplexed with TMDS differential pair clock+	132	RSVD (Differential)	Reserved
133	DP_LANE3- / TMDS_CLK-	DisplayPort differential pair line lane 3. Multiplexed with TMDS differential pair clock-	134	RSVD (Differential)	Reserved
135	GND	Power Ground	136	GND	Power Ground
137	DP_LANE1+ / TMDS_LANE1+	DisplayPort differential pair line lane 1 Multiplexed with TMDS differential pair lane1	138	DP_AUX+	DisplayPort auxiliary channel
139	DP_LANE1- / TMDS_LANE1-	DisplayPort differential pair line lane 1 Multiplexed with TMDS differential pair lane1	140	DP_AUX-	DisplayPort auxiliary channel
141	GND	Power Ground	142	GND	Power Ground
143	DP_LANE2+ / TMDS_LANE0+	DisplayPort differential pair line lane 2	144	RSVD (Differential Pair)	Reserved
145	DP_LANE2- / TMDS_LANE0-	DisplayPort differential pair line lane 2	146	RSVD (Differential Pair)	Reserved
147	GND	Power Ground	148	GND	Power Ground
149	DP_LANE0+ / TMDS_LANE2+	DisplayPort differential pair line lane 0 Multiplexed with TMDS differential pair lane2	150	HDMI_CTRL_DAT	DDC based control signal (data) for HDMI/ DVI device.
151	DP_LANE0- / TMDS_LANE2-	DisplayPort differential pair line lane 0 Multiplexed with TMDS differential pair lane2	152	HDMI_CTRL_CLK	DDC based control signal (clock) for HDMI/ DVI device.
153	DP_HDMI_HPD#	Hot plug detection for HDMI	154	DP_HPD#	Hot plug detection for DP
155	PCIE_CLK_REF+	PCI Express Reference Clock+	156	PCIE_WAKE#	PCI Express Wake event
157	PCIE_CLK_REF-	PCI Express Reference Clock-	158	PCIE_RST#	Reset Signal for external devices
159	GND	Power Ground	160	GND	Power Ground
161	PCIE3_TX+	PCI Express Channel 3 Output+	162	PCIE3_RX+	PCI Express Channel 3 Input+
163	PCIE3_TX-	PCI Express Channel 3 Output-	164	PCIE3_RX-	PCI Express Channel 3 Input-
165	GND	Power Ground	166	GND	Power Ground
167	PCIE2_TX+	PCI Express Channel 2 Output+	168	PCIE2_RX+	PCI Express Channel 2 Input+
169	PCIE2_TX-	PCI Express Channel 2 Output-	170	PCIE2_RX-	PCI Express Channel 2 Input-
171	UART0_TX	Serial Data Transmitter	172	UART0_RTS#	Handshake signal, ready to receive data
173	PCIE1_TX+	PCI Express Channel 1 Output+	174	PCIE1_RX+	PCI Express Channel 1 Input+
175	PCIE1_TX-	PCI Express Channel 1 Output-	176	PCIE1_RX-	PCI Express Channel 1 Input-
177	UART0_RX	Serial Data Receiver	178	UART0_CTS#	Handshake signal, ready to send data
179	PCIE0_TX+	PCI Express Channel 0 Output+	180	PCIE0_RX+	PCI Express Channel 0 Input+
181	PCIE0_TX-	PCI Express Channel 0 Output-	182	PCIE0_RX-	PCI Express Channel 0 Input-
183	GND	Power Ground	184	GND	Power Ground

Pin	Signal	Description	Pin	Signal	Description
185	LPC_AD0 / GPIO0	LPC Interface Address Data 0 General Purpose input/output 0	186	LPC_AD1 / GPIO1	LPC Interface Address Data 1 General Purpose input/output 1
187	LPC_AD2 / GPIO2	LPC Interface Address Data 2 General Purpose input/output 2	188	LPC_AD3 / GPIO3	LPC Interface Address Data 3 General Purpose input/output 3
189	LPC_CLK /GPIO4	LPC Interface Clock General Purpose input/output 4	190	LPC_FRAME# /GPIO5	LPC frame indicator General Purpose input/output 5
191	SERIRQ /GPIO6	Serialized interrupt General Purpose input/output 6	192	LPC_LDRQ# /GPIO7 (*)	LPC DMA request
193	VCC_RTC	3V backup cell input	194	SPKR /GP_PWM_OUT2	Output for audio enunciator General Purpose PWM Output
195	FAN_TACHOIN /GP_TIMER_IN	Fan tachometer input General Purpose Timer In	196	FAN_PWMOUT /GP_PWM_OUT1	Fan speed control (PWM) General Purpose PWM Output
197	GND	Power Ground	198	GND	Power Ground
199	SPI_MOSI	SPI Master serial output/Slave serial input	200	SPI_CS0#	SPI Chip Select 0 Output
201	SPI_MISO	SPI Master serial input/Slave serial output signal	202	SPI_CS1#	SPI Chip Select 1 Output
203	SPI_SCK	SPI Clock Output	204	MFG_NC4	Do not connect on carrier board
205	VCC_5V_SB	Standby power supply +5VDC, ±5%	206	VCC_5V_SB	Standby power supply +5VDC, ±5%
207	MFG_NC0	Do not connect on carrier board	208	MFG_NC2	Do not connect on carrier board
209	MFG_NC1	Do not connect on carrier board	210	MFG_NC3	Do not connect on carrier board
211	VCC	Power supply +5VDC ±5%	212	VCC	Power supply +5VDC ±5%
213	VCC	Power supply +5VDC ±5%	214	VCC	Power supply +5VDC ±5%
215	VCC	Power supply +5VDC ±5%	216	VCC	Power supply +5VDC ±5%
217	VCC	Power supply +5VDC ±5%	218	VCC	Power supply +5VDC ±5%
219	VCC	Power supply +5VDC ±5%	220	VCC	Power supply +5VDC ±5%
221	VCC	Power supply +5VDC ±5%	222	VCC	Power supply +5VDC ±5%
223	VCC	Power supply +5VDC ±5%	224	VCC	Power supply +5VDC ±5%
225	VCC	Power supply +5VDC ±5%	226	VCC	Power supply +5VDC ±5%
227	VCC	Power supply +5VDC ±5%	228	VCC	Power supply +5VDC ±5%
229	VCC	Power supply +5VDC ±5%	230	VCC	Power supply +5VDC ±5%

Note

The signals in the previous table marked with an asterisk symbol (*) are not supported on the conga-QG.

Table 5 PCI Express Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE0_RX+ PCIE0_RX-	180 182	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE0_TX+ PCIE0_TX-	179 181	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE1_RX+ PCIE1_RX-	174 176	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0.
PCIE1_TX+ PCIE1_TX-	173 175	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE2_RX+ PCIE2_RX-	168 170	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE2_TX+ PCIE2_TX-	167 169	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE3_RX+ PCIE3_RX-	162 164	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0.
PCIE3_TX+ PCIE3_TX-	161 163	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCI Express Reference Clock for Lanes 0 to 3.	O PCIE		
PCIE_WAKE#	156	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I 3.3VSB	PU 10k 3.3VSB	
PCIE_RST#	158	Reset Signal for external devices.	O 3.3V		

Table 6 UART Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
UART0_TX	171	Serial Data Transmitter	O 3.3V		
UART0_RX	177	Serial Data Reciever	I 3.3V	PU 100k 3.3V	
UART0_CTS#	178	Handshake signal, ready to send data	I 3.3V	PU 100k 3.3V	
UART0_RTS#	172	Handshake signal, ready to receive data	O 3.3V		

Table 7 Ethernet Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GBE_MDI0+ GBE_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI1+ GBE_MDI1-	11 9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI2+ GBE_MDI2-	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI3+ GBE_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_CTREF	15	Reference voltage for carrier board Ethernet magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		Not connected
GBE_LINK#	13	Ethernet controller 0 link indicator, active low.	O 3.3VSB PP		see note below
GBE_LINK100#	7	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB PP		see note below
GBE_LINK1000#	8	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB PP		see note below
GBE_ACT#	14	Ethernet controller 0 activity indicator, active low.	O 3.3VSB	PU 3.3VSB	see note below

Note

The GbE Controller used on the conga-QG supports only three LEDs outputs:

GBE_LINK100# 100Mb/s link indicator

GBE_LINK1000# 1000Mb/s link indicator

GBE_LINK#/ACT Combined all speed link with the link activity that is connected to GBE_LINK# pin on Qseven connector.

Additionally, the conga-QG can drive gigabit ethernet LEDs directly with up to 10mA.

Table 8 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA_ACT#	33	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V		up to 10mA

Table 9 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_P0+ USB_P0-	96 94	Universal Serial Bus Port 0 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Can be used to form a USB 3.0 Port together with USB_SSRX0, USB_SSTX0 signals.
USB_P1+ USB_P1-	95 93	Universal Serial Bus Port 1 differential pair. This port may be optionally used as USB client port.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1. USB Client is not supported.
USB_P2+ USB_P2-	90 88	Universal Serial Bus Port 2 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P3+ USB_P3-	89 87	Universal Serial Bus Port 3 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P4+ USB_P4- USB_SSRX1+ USB_SSRX1-	84 82	Universal Serial Bus Port 4 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path.	I/O I USBSS		USB 2.0 compliant. Backwards compatible to USB 1.1 Only USB_P4 is supported
USB_P5+ USB_P5- USB_SSTX1+ USB_SSTX1-	83 81	Universal Serial Bus Port 5 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path	I/O O USBSS		USB 2.0 compliant. Backwards compatible to USB 1.1. Only USB_P5 is supported
USB_P6+ USB_P6- USB_SSRX0+ USB_SSRX0-	78 76	Universal Serial Bus Port 6 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path	I USBSS		AC coupled on module Only USB_SSRX0 is supported. USB 3.0 Rev. 1.0 ompliant.
USB_P7+ USB_P7- USB_SSTX0+ USB_SSTX0-	77 75	Universal Serial Bus Port 7 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path	O USBSS		AC coupled on module Only USB_SSRX0 is supported. USB 3.0 Rev. 1.0 compliant.

USB_0_1_OC#	86	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	85	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	80	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	79	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_ID	92	USB Port 1 ID pin. Configures the mode of the USB Port 1. If the signal is detected as being 'high active' the BIOS will automatically configure USB Port 1 as USB Client and enable USB Client support. This signal should be driven as OC signal by external circuitry.	I 3.3VSB		Not connected
USB_VBUS	91	USB Client Connect pin. If USB Port 1 is configured for client mode then an externally connected USB host should set this signal to high-active in order to properly make the connection with the module's internal USB client controller. If the external USB host is disconnected, this signal should be set to low-active in order to inform the USB client controller that the external host has been disconnected. A level shifter/protection circuitry should be implemented on the carrier board for this signal.	I 5VSB		Not connected
USB_DRIVE_VBUS	56	USB Power enable pin for USB Port 1. Enables the Power for the USB-OTG port on the carrier board.	O 3.3VSB		Not connected

Note

The conga-QG supports one USB 3.0 and five USB 2.0 ports by default assembly option. The USB Client and USB-OTG ports are not supported

Table 10 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	43	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I/O 3.3V	PU 40k 3.3V	
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	O 3.3V		
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O 3.3V OD/PP	PU 40k 3.3V	
SDIO_LED	44	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	O 3.3V		Up to 1mA
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I/O 3.3V	PU 40k 3.3V	
SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/ MMC card device.	OD 3.3V	PU 10k 3.3V	
SDIO_DAT0 SDIO_DAT1 SDIO_DAT2 SDIO_DAT3 SDIO_DAT4 SDIO_DAT5 SDIO_DAT6 SDIO_DAT7	49 48 51 50 53 52 55 54	SDIO Data lines. These signals operate in push-pull mode.	I/O 3.3V PP	PU 40k 3.3V	Only SDIO_DAT0..3 are supported. SDIO_DAT4..7 are not connected.

Table 11 HDA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST# I2S_RST#	61	HD Audio Codec Reset. Multiplexed with I2S Codec Reset.	O 3.3V		Only HDA interface is supported.
HDA_SYNC I2S_WS	59	HD Audio Serial Bus Synchronization. Multiplexed with I2S Word Select from Codec.	O 3.3V		Only HDA interface is supported.
HDA_BITCLK I2S_CLK	63	HD Audio 24 MHz Serial Bit Clock from Codec. Multiplexed with I2S Serial Data Clock from Codec.	O 3.3V		Only HDA interface is supported.
HDA_SDO I2S_SDO	67	HD Audio Serial Data Output to Codec. Multiplexed with I2S Serial Data Output from Codec.	O 3.3V		Only HDA interface is supported.
HDA_SDI I2S_SDI	65	HD Audio Serial Data Input from Codec. Multiplexed with I2S Serial Data Input from Codec.	I/O 3.3VSB	PD 47k	Only HDA interface is supported.

Table 12 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_PPEN	111	Controls panel power enable.	O 3.3V	PD 10k	
LVDS_BLEN	112	Controls panel Backlight enable.	O 3.3V	PD 10k	
LVDS_BLT_CTRL /GP_PWM_OUT0	123	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
LVDS_A0+ LVDS_A0- eDP0_TX0+ eDP0_TX0-	99 101	LVDS primary channel differential pair 0. Display Port primary channel differential pair 0.	O LVDS		Only LVDS interface is supported by default assembly option.
LVDS_A1+ LVDS_A1- eDP0_TX1+ eDP0_TX1-	103 105	LVDS primary channel differential pair 1. Display Port primary channel differential pair 1.	O LVDS		Only LVDS interface is supported by default assembly option.
LVDS_A2+ LVDS_A2- eDP0_TX2+ eDP0_TX2-	107 109	LVDS primary channel differential pair 2. Display Port primary channel differential pair 2.	O LVDS		Only LVDS interface is supported by default assembly option.
LVDS_A3+ LVDS_A3- eDP0_TX3+ eDP0_TX3-	113 115	LVDS primary channel differential pair 3. Display Port primary channel differential pair 3.	O LVDS		Only LVDS interface is supported by default assembly option.
LVDS_A_CLK+ LVDS_A_CLK- eDP0_AUX+ eDP0_AUX-	119 121	LVDS primary channel differential pair clock lines. Display Port primary auxiliary channel.	O LVDS		Only LVDS interface is supported by default assembly option.
LVDS_B0+ LVDS_B0- eDP1_TX0+ eDP1_TX0-	100 102	LVDS secondary channel differential pair 0. Display Port secondary channel differential pair 0.	O LVDS		Only LVDS interface is supported by default assembly option.
LVDS_B1+ LVDS_B1- eDP1_TX1+ eDP1_TX1-	104 106	LVDS secondary channel differential pair 1. Display Port secondary channel differential pair 1.	O LVDS		Only LVDS interface is supported by default assembly option.
LVDS_B2+ LVDS_B2- eDP1_TX2+ eDP1_TX2-	108 110	LVDS secondary channel differential pair 2. Display Port secondary channel differential pair 2.	O LVDS		Only LVDS interface is supported by default assembly option.
LVDS_B3+ LVDS_B3- eDP1_TX3+ eDP1_TX3-	114 116	LVDS secondary channel differential pair 3. Display Port secondary channel differential pair 3.	O LVDS		Only LVDS interface is supported by default assembly option.

LVDS_B_CLK+ LVDS_B_CLK- eDP1_AUX+ eDP1_AUX-	120 122	LVDS secondary channel differential pair clock lines. Display Port secondary auxiliary channel.	O LVDS		Only LVDS interface is supported by default assembly option.
LVDS_DID_CLK /GP2_I2C_CLK	127	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus clock line.	I/O 3.3V OD	PU 2.2k 3.3V	
LVDS_DID_DAT /GP2_I2C_DAT	125	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus data line.	I/O 3.3V OD	PU 2.2k 3.3V	
LVDS_BLC_CLK eDP1_HPD#	128	Control clock signal for external SSC clock chip. If the primary functionality is not used, it can be used as an embedded DisplayPort secondary Hotplug detection.	I/O 3.3V OD	PU 10k 3.3V	Not supported
LVDS_BLC_DAT eDP0_HPD#	126	Control data signal for external SSC clock chip. If the primary functionality is not used, it can be used as an embedded DisplayPort primary Hotplug detection.	I/O 3.3V OD	PU 10k 3.3V	Not supported

Table 13 DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP_LANE3+ DP_LANE3-	131 133	DisplayPort differential pair lines lane 3 (Shared with TMDS_CLK+ and TMDS_CLK-)	O DP		AC coupled on module.
DP_LANE2+ DP_LANE2-	143 145	DisplayPort differential pair lines lane 2 (Shared with TMDS_LANE0+ and TMDS_LANE0-)	O DP		AC coupled on module.
DP_LANE1+ DP_LANE1-	137 139	DisplayPort differential pair lines lane 1 (Shared with TMDS_LANE1+ and TMDS_LANE1-)	O DP		AC coupled on module.
DP_LANE0+ DP_LANE0-	149 151	DisplayPort differential pair lines lane 0 (Shared with TMDS_LANE2+ and TMDS_LANE2-)	O DP		AC coupled on module.
DP_AUX+ DP_AUX-	138 140	Auxiliary channel used for link management and device control. Differential pair lines.	I/O DP		AC coupled off module.
DP_HPD#	154	DisplayPort Hot plug detection signal that serves as an interrupt request.	I 3.3V	PU 10k 3.3V	HDMI is selected if both DP_HPD# and DP_HDMI_HPD# signals are active.

Note

To implement DisplayPort++, convert HPD and CAD signals to Qseven DP_HPD# and DP_HDMI_HPD# signals according to the table below:

DisplayPort++		Qseven	
Pin 18	Pin 13	Pin 153	Pin 154
HPD	CAD	DP_HDMI_HPD#	DP_HPD#
0	0	1	1
0	1	1	1
1	0	1	0
1	1	0	1

Table 14 HDMI/DVI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS_CLK+ TMDS_CLK-	131 133	TMDS differential pair clock lines. (Shared with DP_LANE3- and DP_LANE3+)	O TMDS		TMDS is supported by an external level shifter. AC coupled on module.
TMDS_LANE0+ TMDS_LANE0-	143 145	TMDS differential pair lines lane 0. (Shared with DP_LANE2- and DP_LANE2+)	O TMDS		TMDS is supported by an external level shifter. AC coupled on module.
TMDS_LANE1+ TMDS_LANE1-	137 139	TMDS differential pair lines lane 1. (Shared with DP_LANE1- and DP_LANE1+)	O TMDS		TMDS is supported by an external level shifter. AC coupled on module.
TMDS_LANE2+ TMDS_LANE2-	149 151	TMDS differential pair lines lane 2. (Shared with DP_LANE0- and DP_LANE0+)	O TMDS		TMDS is supported by an external level shifter. AC coupled on module.
HDMI_CTRL_CLK	152	DDC based control signal (clock) for HDMI/DVI device.	I/O 3.3V OD	PU 4.7k 3.3V	Level shifter FET and 2.2k PU to 5V shall be placed between module and HDMI/DVI connector.
HDMI_CTRL_DAT	150	DDC based control signal (data) for HDMI device.	I/O 3.3V OD	PU 4.7k 3.3V	Level shifter FET and 2.2k PU to 5V shall be placed between module and HDMI/DVI connector.
DP_HDMI_HPD#	153	HDMI Hot plug active low detection signal that serves as an interrupt request.	I 3.3V	PU 10k 3.3V	If both DP_HPD# and DP_HDMI_HPD# are active then HDMI is selected.

Note

The TMDS interface is supported by an external DP to TMDS level shifter e.g PTN3360D or a passive level shifter with PD 499R.

Table 15 LPC/GPIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD0 GPIO0 LPC_AD1 GPIO1 LPC_AD2 GPIO2 LPC_AD3 GPIO3	185 186 187 188	Multiplexed Command, Address and Data (LPC_AD[0..3]) shared with General Purpose Input/Output [0..3]	I/O 3.3V	PU 47k 3.3V	Only LPC interface is supported.
LPC_FRAME# GPIO5	190	LPC frame indicates the start of a new cycle or the termination of a broken cycle. Shared with General Purpose Input/Output 5.	I/O 3.3V		Only LPC interface is supported.
LPC_LDRQ# GPIO7	192	LPC DMA request. General Purpose Input/Output 7	I/O 3.3V	PU 47k 3.3V	Only LPC interface is supported.
LPC_CLK GPIO4	189	LPC clock shared with General Purpose Input/Output 4	I/O 3.3V		Only LPC interface is supported.
SERIRQ GPIO6	191	Serialized Interrupt. General Purpose Input/Output 6	I/O 3.3V	PU 47k 3.3V	Only LPC interface is supported.

Table 16 SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_MOSI	199	Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device.	O 3.3VSB		
SPI_MISO	201	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module.	I 3.3VSB	PD 47k	
SPI_SCK	203	SPI clock output.	O 3.3VSB		
SPI_CS0#	200	SPI chip select 0 output.	O 3.3VSB	PU 10k 3.3VSB	
SPI_CS1#	202	SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.	O 3.3VSB	PU 10k 3.3VSB	

Note

The conga-QG supports only the BIOS SPI Flash memory on the SPI Bus

Table 17 CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN0_TX	129	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	O 3.3V		Not connected
CAN0_RX	130	RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	I 3.3V		Not connected

Table 18 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	211-230	Power Supply +5VDC ±5%.	P		
VCC_5V_SB	205-206	Standby Power Supply +5VDC ±5%.	P		
VCC_RTC	193	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.5 - 3.3 V).	P		

GND	1, 2, 23-25, 34, 39-40, 57-58, 73-74, 97-98, 117-118, 135-136, 141-142, 147-148, 159-160, 165-166, 183-184, 197-198	Power Ground.	P		

Table 19 Power Control Signal Descriptions

Signal	Pin #	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	26	High active input for the Qseven® module indicates that power from the power supply is ready.	I 5V	PU 10k 3.3V	
PWRBTN#	20	Power Button: Low active power button input. This signal is triggered on the falling edge.	I 3.3VSB	PU 10k 3.3VSB	

Table 20 Power Management Signal Descriptions

Signal	Pin #	Description of Power Management signals	I/O	PU/PD	Comment
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module.	I 3.3VSB	PU 10k 3.3VSB	
BATLOW#	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	I 3.3VSB	PU 10k 3.3VSB	
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	I 3.3VSB	PU 10k 3.3VSB	
SUS_STAT#	19	Suspend Status: indicates that the system will be entering a low power state soon.	O 3.3VSB		
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	O 3.3VSB		
SUS_S5#	16	S5 State: This signal indicates S4 or S5 (Soft Off) state.	O 3.3VSB		
SLP_BTN#	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	I 3.3VSB	PU 10k 3.3VSB	
LID_BTN#	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again.	I 3.3VSB	PU 10k 3.3VSB	

Table 21 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse.	I 3.3V	PU 10k 3.3V	
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	O 3.3V	PD 10k	
GP0_I2C_CLK	66	Clock line of I²C bus.	I/O 3.3VSB OD	PU 2.2k 3.3VSB	
GP0_I2C_DAT	68	Data line of I²C bus.	I/O 3.3VSB OD	PU 2.2k 3.3VSB	
GP1_SMB_CLK	60	Clock line of System Management Bus.	I/O 3.3VSB OD	PU 2.2k 3.3VSB	
GP1_SMB_DAT	62	Data line of System Management Bus.	I/O 3.3VSB OD	PU 2.2k 3.3VSB	
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	I/O 3.3VSB OD	PU 10k 3.3VSB	
SPKR /GP_PWM_OUT2	194	Primary functionality is output for audio enunciator, the “speaker” in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V	PD 10k	
BIOS_DISABLE# /BOOT_ALT#	41	Module BIOS disable input signal. Pull low to disable module’s onboard BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a bootloader.	I 3.3VSB	PU 10k 3.3VSB	Carrier shall pull to GND or left as no-connect.
RSVD	132,134,144, 146	Do not connect	NC		
GP_1-Wire_Bus	124	General Purpose 1-Wire bus interface. Can be used for consumer electronics control bus (CEC) of HDMI.	I/O 3.3V		Not connected

Table 22 Manufacturing Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
MFG_NC0	207	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TCK signal for boundary scan purposes during production or as a vendor specific control signal. When used as a vendor specific control signal the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC1	209	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDO signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_TX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC2	208	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDI signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_RX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	

MFG_NC3	210	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TMS signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific BOOT signal for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC4	204	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TRST# signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 (JTAG / UART). When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes.	NA	NA	
RSVD	124	Do not connect.	NA	NA	

Note

The MFG_NC0..4 pins are reserved for manufacturing and debugging purposes. It's recommended to route the signals to a connector on the carrier board.

The carrier board must not drive the MFG_NC-pins or have pull-up or pull-down resistors implemented for these signals. MFG_NC0...4 are defined to have a voltage level of 3.3V. It must be ensured that the carrier board has the correct voltage levels for JTAG/UART signals originating from the module. For this reason, a level shifting device may be required on the carrier board to guarantee that these voltage levels are correct in order to prevent damage to the module.

More information about implementing a carrier board multiplexer can be found in the Qseven® Design Guide.

Table 23 Thermal Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	69	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	I 3.3V	PU 10k 3.3V	
THRMTRIP#	71	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off).	O 3.3V	PU 10k 3.3V	Not supported

Table 24 Fan Control Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT /GP_PWM_OUT1	196	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V OC	PU 10k 3.3V	
FAN_TACHOIN /GP_TIMER_IN	195	Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input.	I 3.3V	PU 10k 3.3V	

Table 25 Boot Strap Signal Descriptions

Signal	Pin #	Description of Boot Strap Signal	I/O	PU/PD	Comment
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V	PU 10K 3.3V	
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V	PU 10K 3.3V	

Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either COM Express™ internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM Express™ module to malfunction and/or cause irreparable damage to the module.

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-QG module is functionally identical with a standard PC/AT.

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.1.1 LPC Bus

On the conga-QG, the PCI Express Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Express Bus. Only specified I/O ranges are forwarded to the LPC Bus. In the congatec Embedded BIOS, the following I/O address ranges are sent to the LPC Bus:

2Eh-2Fh	4Eh-4Fh	60h, 64h
220h-227h	228h-22Fh	230h-233h
238h-23Fh	240h-253h	260h-273h
278h-27Fh	280h-293h	2E8h-2EFh
2F8h-2FFh	338h-33Fh	378h-37Fh
3BCh-3BFh	3E8h-3EFh	3F8h-3FFh
678h-67Fh	778h-77Fh	7BCh-7BFh
A00h-BFFh	E00h-FFFh	

Some of these ranges are not available for customer use if a Super I/O is present and enabled on the carrier board or on the module. The I/O range E38h to EBFh is always used by on module LPC devices.

If you require additional LPC Bus resources other than those mentioned above or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 26 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Root Complex
00h	01h	00h	Internal	Integrated Graphics Controller (VGA)
00h	01h	01h	Internal	HDMI / DisplayPort HDA Controller (for HDMI/DisplayPort integrated audio only)
00h	02h	00h	N.A.	Host Bridge
00h (see Note 1)	02h	01h	Internal	PCIExpress Root Bridge 0
00h (see Note 1)	02h	02h	Internal	PCIExpress Root Bridge 1
00h (see Note 1)	02h	03h	Internal	PCIExpress Root Bridge 2
00h (see Note 1)	02h	04h	Internal	PCIExpress Root Bridge 3
00h (see Note 1)	02h	05h	Internal	PCIExpress Root Bridge 4
00h	10h	00h	Internal	XHCI Host Controller
00h	11h	00h	Internal	Serial ATA Controller
00h	12h	00h	Internal	OHCI Host Controller 0
00h	12h	02h	Internal	EHCI Host Controller 0
00h	13h	00h	Internal	OHCI Host Controller 1
00h	13h	02h	Internal	EHCI Host Controller 1
00h	14h	00h	N.A.	SMBus Host Controller
00h	14h	02h	Internal	High Definition Audio Controller
00h	14h	03h	N.A.	PCI to LPC Bridge
00h	14h	07h	Internal	SD Controller
00h	16h	00h	Internal	OHCI Host Controller 2
00h	16h	02h	Internal	EHCI Host Controller 2
00h	18h	00h	N.A.	Chipset Configuration Registers
00h	18h	01h	N.A.	Chipset Configuration Registers
00h	18h	02h	N.A.	Chipset Configuration Registers
00h	18h	03h	N.A.	Chipset Configuration Registers
00h	18h	04h	N.A.	Chipset Configuration Registers
00h	18h	05h	N.A.	Chipset Configuration Registers
01h (see Note 2)	00h	00h	Internal	Onboard Gigabit LAN Controller
02h (see Note 2)	00h	00h	Internal	PCI Express Port 0
03h (see Note 2)	00h	00h	Internal	PCI Express Port 1
04h (see Note 2)	00h	00h	Internal	PCI Express Port 2
05h (see Note 2)	00h	00h	Internal	PCI Express Port 3

Note

1. *The PCI Express ports are visible only if the PCI Express port is set to "Enabled" in the BIOS setup program and a device is attached to the corresponding PCI Express port on the carrier board.*

2. *The above table represents a case when a single function PCI Express device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*

9.3 PCI Interrupt Routing Map

Table 27 PCI Interrupt Routing Map

PIRQ	VGA	HDA (HDMI/DP)	XHCI0	OHCI0	EHCI 0	OHCI1	EHCI 1	OHCI2	EHCI 2	SM Bus	SATA	HDA (Main)
A												20
B					17		17		17			
C			18	18		18		18				
D											19	
E	44											
F		45										
G												
H												

PIRQ	PCI-EX Root Bridge 0	PCI-EX Root Bridge 1	PCI-EX Root Bridge 2	PCI-EX Root Bridge 3	PCI-EX Root Bridge 4	LAN	PCI-EX Port 0	PCI-EX Port 1	PCI-EX Port 2	PCI-EX Port 3
A	24		32		40	24		32		40
B								33		41
C								34		42
D								35		43
E		28		36			28		36	
F							29		37	
G							30		38	
H							31		39	

Note

The given numbers specify the APIC interrupt numbers assigned to the respective devices.

9.4 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.5 SM Bus

System Management (SM) bus signals are connected to the AMD Chipset and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

10 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

10.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <F2> key during POST.

10.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used, a selection will be displayed immediately after POST allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

10.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

Main	Advanced	Chipset	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold print indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

10.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
Main BIOS Version	no option	Displays the main BIOS version.
OEM BIOS Version	no option	Displays the additional OEM BIOS version.
Build Date	no option	Displays the date the BIOS was built.
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
Running Time	no option	Displays the time the board is running [in hours max. 65535].
Memory Information	no option	
Total Memory	no option	Displays the total amount of installed memory.
System Date	Day of the week, month/day/year	Specifies the current system date. *Note: The date is in month/day/year format.*
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24 hour format.*

10.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Graphics				
	Watchdog				
	Hardware Health Monitoring				
	Module Serial Ports				
	PCI & PCI Express				
	RTC Wake				
	ACPI				
	Trusted Computing				
	CPU				
	SATA				
	SDIO				
	USB				
	SMART Settings				
	Super I/O				
	Serial Port Console Redirection				
	UEFI Network Stack				
	Intel® I210 Gigabit Network Connection				

10.4.1 Graphics Submenu

Feature	Options	Description
Primary Graphics Device	IGD **PCI/PCIe**	Select primary graphics adapter to be used during boot up. IGD: Internal Graphics Device PCI/PCIe: Try to use external PCI Express or PCI Graphics Device. If not present, IGD is used.
Integrated Graphics Device	**Auto** Disabled Manual Configuration	Deactivate IGD or select frame buffer configuration mode. In auto mode, the frame buffer size will be defined based on the amount of physical memory present.
IGD Framebuffer Size	32M 64M 128M **256M** 512M 1G	Only visible if IGD is set to manual configuration. Set fixed graphics frame buffer size for IGD. The graphics driver may allocate additional memory.
CRT Interface	Disabled **Enabled**	Enable or disable the CRT interface.

Feature	Options	Description
Digital Display Interface	Disabled Auto Selection **Force HDMI/DVI**	Configure the digital display interface. Display Port or HDMI/DVI supported and automatically detected and configured.
LFP Interface	Disabled **Enabled**	Enable or disable the local flat panel (LFP) interface.
Always Try Auto Panel Detect	No **Yes**	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel output. If no external EDID data set is found, the data set selected under 'Local Flat Panel Type' will be used as fallback data set.
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x800 1x18 (01Eh) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. *Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.*
Backlight Inverter Type	**None** PWM I2C	Select the type of backlight inverter used. PWM = Use module's PWM output signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.
PWM Inverter Frequency (Hz)	**200**-40000	Only visible if Backlight Inverter Type is set to PWM. Set the PWM inverter frequency in Hertz.
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100%**	Actual backlight value in percent of the maximum setting.
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Setting	**No** Yes	Allow to invert backlight control values if required for the actual I2C type backlight hardware controller.
LVDS SSC	**Disabled, 0.5%,** 1.0%, 1.5%, 2.0%, 2.5%	Configure LVDS spread spectrum clock modulation depth. Using center spreading and a fixed modulation frequency of 32.9kHz.

10.4.2 Watchdog Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One time Trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to '*One time Trigger'* the watchdog will be disabled after the first trigger. If set to *'Single Event'*, every stage will be executed only once, then the watchdog will be disabled. If set to *'Repeated Event'* the last stage will be executed repeatedly until a reset occurs.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	ACPI Event **Reset** Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about *'ACPI Event'* see note below.
Event 2	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached. For more information about *'ACPI Event'* see note below.
Event 3	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached. For more information about *'ACPI Event'* see note below.
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.

Feature	Options	Description
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

Note

In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason, the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

10.4.3 Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	no option	Current CPU temperature.
Board Temperature	no option	Current board temperature.
12V Standard	no option	Current 12V input reading.
5V Standby	no option	Current 5V standby input reading.
Input Current	no option	CPU module input current reading.
CPU Fan Speed	no option	Current CPU fan speed reading.

10.4.4 Module Serial Ports Submenu

Feature	Options	Description
Serial Port 0	**Disabled** Enabled	Enable or disable module serial port 0.
I/O Base Address	3F8h, 2F8h, 220h, 228h, 238h, 2E8h, 338h, **3E8h**	Set serial port base address.
Interrupt	None, IRQ3, IRQ4, IRQ5, IRQ6, **IRQ10**, IRQ11, IRQ14, IRQ15	Set serial port interrupt.
PNP ID	None PNP0501 **CGT0501**	Set serial port ACPI ID.

Feature	Options	Description
Baudrate	**2400**, 4800, 9600, 19200, 38400, 57600, 115200	Set serial port initial baudrate.

10.4.5 PCI &PCI Express Submenu

Feature	Options	Description
PCI Settings		
PCI Latency Timer	**32,** 64, 96, 128, 160, 192, 224, 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
VGA Palette Snoop	**Disabled** Enabled	Enable or disable VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate PERR#.
SERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate SERR#.
Generate EXCD0/1_PERST#	Disabled 1ms 5ms **10ms** 50ms 100ms 150ms 200ms 250ms	Select whether and how long the COM Express EXCD0_PERST# and EXCD1_ PERST# pins should be driven low during POST.
►PCI Express Settings	submenu	PCI Express device and link settings.
►PCI Express Port Configuration	submenu	Configure PCI Express and PEG ports.
►PIRQ Routing & IRQ Reservation	submenu	Manual PIRQ routing and interrupt reservation for legacy devices.

10.4.5.1 PCI Express Settings Submenu

Feature	Options	Description
Relaxed Ordering	**Disabled** Enabled	Enable or disable PCI Express device relaxed ordering.
Extended Tag	**Disabled** Enabled	If enabled a device may use an 8-bit tag filed as a requester.
No Snoop	Disabled **Enabled**	Enable or disable PCI Express device 'No Snoop' option.
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum payload of PCI Express devices or allow system BIOS to select the value.
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum read request size of PCI Express devices or allow system BIOS to select the value.
Extended Synch	**Disabled** Enabled	If enabled, the generation of extended PCI Express synchronization patterns is allowed.
Extended Synch	**Disabled** Enabled	If enabled the generation of extended synchronization patterns is allowed.
Link Training Retry	Disabled 2 3 **5**	Defines numer of retry attempts software will take to retrain the link if the previous training attempt was unsuccessful.
Link Training Timeout (us)	10-10000 **(100)**	Defines number of microseconds software will wait before polling the link training bit in the link status register. Value ranges from 10us to 10000us.
Restore PCIE Registers	Enabled **Disabled**	On non-PCI Express aware operating systems some devices may not be re-initialized correctly after S3. Setting this node to Enabled restores PCI Express configuration on S3 resume. Warning: Enabling this may cause issues with other hardware after S3 resume.
PSPP Policy	Disabled **Performance** Balanced-High Balanced-Low Power Saving	Define PCI Express link speed selection policy.

10.4.5.2 PCI Express Port Configuration Submenu

Feature	Options	Description
Onboard LAN Controller	Disabled **Enabled**	Enable or disable the on module Ethernet controller.
PCI Express Port 0	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the 'Always Enable Port' support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
ASPM Support	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Configure PCI Express root port ASPM support.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 1	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the 'Always Enable Port' support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
ASPM Support	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Configure PCI Express root port ASPM support.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 2	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the 'Always Enable Port' support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
ASPM Support	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Configure PCI Express root port ASPM support.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 3	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the 'Always Enable Port' support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
ASPM Support	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Configure PCI Express root port ASPM support.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.

10.4.5.3 PIRQ Routing & IRQ Reservation Submenu

Feature	Options	Description
PIRQA	**Auto,** IRQ3, IRQ4, IRQ10, IRQ11, IRQ14, IRQ15	Set interrupt for selected PIRQ. Please refer to the board's resource list for a detailed list of devices connected to the respective PIRQ. **NOTE:** These settings will only be effective while operating in PIC (non-IOAPIC) interrupt mode.
PIRQB	same as PIRQA	same as PIRQA
PIRQC	same as PIRQA	same as PIRQA
PIRQD	same as PIRQA	same as PIRQA
PIRQE	same as PIRQA	same as PIRQA
PIRQF	same as PIRQA	same as PIRQA
PIRQG	same as PIRQA	same as PIRQA
PIRQH	same as PIRQA	same as PIRQA
Reserve Legacy Interrupt 1	**None,** IRQ3, IRQ4, IRQ10, IRQ11, IRQ14, IRQ15	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.
Reserve Legacy Interrupt 2	same as Reserve Legacy Interrupt 1	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.

10.4.6 RTC Wake Submenu

Feature	Options	Description
Wake System At Fixed Time	**Disabled** Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour		Specify wake up hour.
Wake up minute		Specify wake up minute.
Wake up second		Specify wake up second.

10.4.7 ACPI Submenu

Feature	Options	Description
Hibernation Support	Disabled **Enabled**	Enable or disable system ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.
Enable Hibernation	Disabled **Enabled**	Enable or disable system ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system sleep/suspend.
Critical Trip Point	**Disabled**, 70, 80, 90, 95, 100, 105, 110, 115°C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Active Trip Point	**Disabled**, 20, 30, 40, 50, 60, 70, 80, 90, 95°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.

Feature	Options	Description
Passive Trip Point	**Disabled**, 60, 70, 80, 90, 95°C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.
Lid Support	**Disabled** Enabled	Configure COM Express LID# signal to act as ACPI lid.
Sleep Button Support	**Disabled** Enabled	Configure COM Express SLEEP# signal to act as ACPI sleep button.

10.4.8 Trusted Computing Submenu

Feature	Options	Description
Security Device Support	**Disable** Enable	Enable or disable BIOS support for security device.
TPM State	**Disabled** Enabled	Enable or disable TPM chip. Note: System might restart several times during POST to acquire target state.
Pending operation	**None**, Enable Take Ownership, Disable Take Ownership, TPM Clear	Perform selected TPM chip operation. Note: System might restart several times during POST to perform selected operation.

10.4.9 CPU Submenu

Feature	Options	Description
AMD PowerNow! Support	Disabled **Enabled**	Enable or disable support for AMD PowerNow! technology. Allows operating systems to control CPU performance states.
Maximum Power Up P-State	**P-State 0** P-State 1 P-State 2 P-State 3 P-State 4 P-State 5 P-State 6 P-State 7	Select the maximum CPU performance state to be set at power up. Higher numbers mean lower performance. P-state 0 is the highest performance state.
Maximum OS P-State	**P-State 0** P-State 1 P-State 2 P-State 3 P-State 4 P-State 5 P-State 6 P-State 7	Select the maximum CPU performance state the operating system should support. Higher numbers mean lower performance. P-state 0 is the highest performance state.

Feature	Options	Description
NX Mode	Disabled **Enabled**	Enable or disable the 'no-execute' page protection function.
Virtualization Technology	Disabled **Enabled**	When enabled, a Virtual Machine Manager (VMM) can utilize the integrated hardware virtualization support.
C6 Support	**Disabled** Enabled	Enable or disable CPU C6 low power state support.
Core Performance Boost	Auto **Disabled**	Control usage of boosted P-States, i.e. P-States above the standard CPU P-State limit. Availability depends on CPU revision and type, actual usage on total CPU/GPU chip power consumption.
Core Leveling Support	**Automatic Mode**, Three cores per processor, Two cores per processor, One core per processor	Change/limit the number of active CPU cores.

10.4.10 SATA Submenu

Feature	Options	Description
SATA Controller	Disabled **Enabled**	Enable or disable the onboard SATA controller.
SATA Mode Selection	Native IDE **AHCI** Legacy IDE AHCI as ID 7804	Select onboard SATA controller mode.
SATA Gen2 Limit	**Disabled** Enabled	Limit all SATA ports to max. Gen2 speed.
SATA Port 0	**Enabled** Disabled	Enable or disable selected port.
Port Speed	**Auto** Gen1 Gen2	Select max. SATA speed generation for the selected port. Auto = up to Gen3
eSATA Support	**Disabled** Enabled	Enabled or disable eSATA and hotplug (only in AHCI mode) support.
SATA Port 1	**Enabled** Disabled	Enable or disable selected port.
Port Speed	**Auto** Gen1 Gen2	Select max. SATA speed generation for the selected port. Auto = up to Gen3
eSATA Support	**Disabled** Enabled	Enabled or disable eSATA and hotplug (only in AHCI mode) support.
SATA Port 0	no option	SATA drive 0 information.
SATA Port 1	no option	SATA drive 1 information.

10.4.11 SDIO Submenu

Feature	Options	Description
SDIO Access Mode	**Auto** DMA PIO	Select BIOS SD device access and boot mode. Auto = Access SD device in DMA mode if controller supports it, otherwise use PIO mode. DMA = Access SD device in DMA mode. PIO = Access SD device in PIO mode.
►SD Controller	submenu	Configure SD controller

10.4.11.1 SD Controller Submenu

Feature	Options	Description
SD Controller Mode	Disabled, **Advanced DMA**, DMA, PIO	Enable or disable the onboard SD controller and select its operating mode.
SD Clock Control	**50MHz/25MHz** 40MHz/20MHz 25MHz/12.5MHz	Select actual SD clocks for high and low speed transfer modes.
SD Speed Mode	Low Speed **High Speed**	Select SD transfer speed mode.
SD System Address Support	32Bit **64Bit**	Select 32bit or 64bit system address support for SD controller.
SD Host Controller Version	**SD 2.0** SD 3.0	Select SD host controller version.

10.4.12 USB Submenu

Feature	Options	Description
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
USB3.0 BIOS Support	**Enabled** Disabled	USB 3.0 operating mode support on USB ports 0-3 in BIOS run and pre-OS time. Enabled = USB ports are enabled to operate in USB 3.0 mode. Effective only when the XHCI controllers are enabled. Disabled = USB ports will operate in USB2.0 mode only.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI OS driver.
EHCI Hand-off	**Disabled** Enabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable or disable USB mass storage BIOS support.

Feature	Options	Description
USB Transfer Timeout	1 sec 5sec 10 sec **20 sec**	Timeout value for legacy USB control, bulk and interrupt transfers.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device start unit command timeout.
Device Power-Up Delay Selection	**Auto** Manual	Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.
Device Power-Up Delay Value	**5** 1-40	Actual power-up delay value in seconds.
USB Mass Storage Device Name *(Auto detected USB mass storage devices are listed here dynamically)*	**Auto** Floppy Forced FDD Hard Disk CD-ROM	Every USB mass storage device that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. *Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.* Select *AUTO* to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. *Forced FDD* allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. *Hard Disk* allows the device to be emulated as hard disk. *CDROM* assumes the CD.ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.
►USB Port & Controller Configuration	submenu	Configure USB ports and controllers.

10.4.12.1 USB Port & Controller Configuration Submenu

Feature	Options	Description
XHCI 0 (Port 0-1)	Disabled **Enabled**	Enable or disable the XHCI (USB 3.0) host controller.
OHCI 0 (Port 2-5)	Disabled **Enabled**	Enable or disable the OHCI host controller.
EHCI 0 (Port 2-5)	Disabled **Enabled**	Enable or disable the EHCI (USB 2.0) host controller.
OHCI 2 (Port 0-1)	Disabled **Enabled**	Enable or disable the OHCI host controller. Only visible if XHCI 0 is set to ‘Disabled’.
EHCI 2 (Port 0-1)	Disabled **Enabled**	Enable or disable the EHCI (USB 2.0) host controller. Only visible if XHCI 0 is set to ‘Disabled’
USB Port 0 (XHCI Mode) (USB Port 0)	Disabled **Enabled**	Enable or disable the respective USB port. Alternative port control if XHCI controller is disabled.

Feature	Options	Description
USB Port 1 (XHCI Mode) (USB Port 1)	Disabled **Enabled**	Enable or disable the respective USB port. Alternative port control if XHCI controller is disabled.
USB Port 2	Disabled **Enabled**	Enable or disable the respective USB port.
USB Port 3	Disabled **Enabled**	Enable or disable the respective USB port.
USB Port 4	Disabled **Enabled**	Enable or disable the respective USB port.
USB Port 5	Disabled **Enabled**	Enable or disable the respective USB port.

10.4.13 SMART Settings Submenu

Feature	Options	Description
SMART Self Test	**Disabled** Enabled	Run SMART Self Test on all harddisks during POST.

10.4.14 Super I/O Submenu

Feature	Options	Description
PS/2 Keyboard/Mouse Support	**Disabled** Enabled	Enable or disable PS/2 Keyboard/Mouse controller support.
Serial Port 0	Disabled **Enabled**	Enable or disable serial port 0.
Device Settings	IO=3F8h; IRQ=4;	Fixed configuration of serial port 0 if enabled.
Serial Port 1	Disabled **Enabled**	Enable or disable serial port 1.
Device Settings	IO=2F8h; IRQ=3;	Fixed configuration of serial port 1 if enabled.
Parallel Port	Disabled **Enabled**	Enable or disable parallel port.
Device Settings	IO=378h; IRQ=7;	Fixed configuration of the parallel port if enabled.
Device Mode	**Standard Parallel Mode** EPP Mode ECP Mode EPP Mode & ECP Mode	Set the parallel port mode.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

10.4.15 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
►Console Redirection Settings	submenu	Opens console redirection configuration submenu.
COM1 Console Redirection	**Disabled** Enabled	Enable or disable serial port 1 console redirection.
►Console Redirection Settings	submenu	Opens console redirection configuration submenu.

10.4.15.1 Console Redirection Settings Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select terminal type.
Baudrate	9600, 19200, 38400, 57600, **115200**	Select baudrate.
Data Bits	7, **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution.
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.

Feature	Options	Description
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Enabled** Disabled	Select whether serial redirection should be continued after POST.

10.4.16 UEFI Network Stack Submenu

Feature	Options	Description
UEFI Network Stack	Disabled Enabled	Enable or disable the UEFI network stack.
IPv4 PXE Support	Disabled Enabled	Enable IPv4 PXE boot support. If disabled IPv4 PXE boot option will not be created.
IPv6 PXE Support	Disabled Enabled	Enable IPv6 PXE boot support. If disabled IPv6 PXE boot option will not be created.
PXE Boot Wait Time	**1** 0 - 5	Time in seconds waiting for ESC keypress to abort the PXE boot.

10.4.17 Intel® I210 Gigabit Network Connection Submenu

Feature	Options	Description
► NIC Configuration	submenu	Opens the NIC Configuration submenu.
Blink LEDs	0-15 Default : 0	The Ethernet activity LEDs will blink as many seconds as entered.
UEFI Driver	no option	Displays the UEFI Driver version.
Adapter PBA	no option	Displays the Adapter PBA.
Chip Type	no option	Displays the type of Ethernet chip.
PCI Device ID	no option	Displays the PCI Device ID of the Ethernet controller.
Bus:Device:Function	no option	Displays the PCI Bus:Device:Function number of the Ethernet controller.
Link Status	no option	Displays the Link Status.
MAC Address	no option	Displays the MAC Address.
Virtual MAC Address	no option	Displays the programmatically assignable MAC Address.

10.4.18 NIC Configuration Submenu

Feature	Options	Description
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Specifies the port speed used for the selected boot protocol.
Wake On LAN	Disabled **Enabled**	Enables the server to be powered on using an in-band magic packet.

10.5 Chipset Setup

Select the Chipset tab from the setup menu to enter the Chipset setup screen

10.5.1 Chipset Settings Configuration

Feature	Options	Description
HDMI/DP Audio Support	Disabled **Enabled**	Enable or disable HDMI/DisplayPort integrated audio support.
HDA Controller	**Auto** Disabled Enabled	Control activation of the High Definition Audio controller device. Disabled = HDA controller will be unconditionally disabled Enabled = HDA controller will be unconditionally enabled Auto = HDA controller will be enabled if HDA codec present, disabled otherwise.
Isolate SMBus Segments	Never During POST **Always**	Allows to isolate the off-module/external SMBus segment from the on-module SMBus segment. This can be a workaround for non specification conform external SMBus devices.
Adaptive S4 Control	**Disabled** Enabled	E.nable or disable adaptive S4 control
SB Clock Spread Spectrum	Disabled **Enabled**	Enable or disable clock spreading for I/O components like USB (3.0) and SATA.
SB Clock Spread Spectrum Option	-0.362%, **-0.375%,** -0.400%, -0.425%, -0,450%, -0.475%	I/O clock spreading value.
Native PCI Express Support	Disabled **Enabled**	Enable or disable native PCI Express OS support.
USB MSI Option	**Disabled** Enabled	Enable or disable MSI (Message Signaled Interrupt) support for USB controllers.
HD Audio MSI Option	**Disabled** Enabled	Enable or disable MSI (Message Signaled Interrupt) support for the HDA controller.

Feature	Options	Description
LPC MSI Option	**Disabled** Enabled	Enable or disable MSI (Message Signaled Interrupt) support for the LPC bridge.
► Memory Configuration	Submenu	Opens the Memory Configuration submenu.

10.5.2 Memory Configuration Submenu

Feature	Options	Description
Memory Bus Clock	**Auto** 400MHz (DDR3-800) 533MHz (DDR3-1066) 667MHz (DDR3-1333) 800MHz (DDR3-1600)	Select or limit memory frequency.
Memory Hole Remapping	Disabled **Enabled**	Enable or disable memory hole remapping.
Bank Interleaving	**Disabled** Enabled	Enable or disable memory bank interleaving.
Memory Hole 15MB-16MB	**Disabled** Enabled	Create a memory hole in the range between 15MB and 16MB for some LPC/ISA expansion cards.

10.6 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.6.1 Boot Settings Configuration

Feature	Options	Description
Quiet Boot	**Disabled** Enabled	*Disabled* displays normal POST diagnostic messages. *Enabled* displays OEM logo instead of POST messages. Note: The default OEM logo is a dark screen.
Setup Prompt Timeout	**1** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot (not recommended), 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. *Remain Off* keeps the power off until the power button is pressed. *Turn On* restores power to the computer. *Last State* restores the previous power state before power loss occurred. *Note: Only works with an ATX type power supply.*
AT Shutdown Mode	System Reboot **Hot S5**	Determines the behavior of an AT-powered system after a shutdown.
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
Enter Setup If No Boot Device	No **Yes**	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The “Device Based” boot priority list allows you to select from a list of currently detected devices only. The “Type Based” boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the “Device Based” boot priority list might change dynamically in cases when devices are physically removed or added to the system. The “Type Based” boot menu is static and can only be changed by the user.
1st, 2nd, 3rd, ... Boot Device (Up to 12 boot devices can be prioritized if device based priority list control is selected. If “Type Based” priority list control is enabled only 8 boot devices can be prioritized.)	Disabled SATA 0 Drive SATA 1 Drive SATA 2 Drive SATA 3 Drive USB Floppy USB Harddisk USB CDROM Onboard LAN External LAN Other BEV Device	This view is only available when in the default “Type Based” mode. When in “Device Based” mode you will only see the devices that are currently connected to the system.

Feature	Options	Description
►CSM & Option ROM Control	submenu	Opens submenu which controls the execution of UEFI and legacy option ROMs.
UEFI Fast Boot	**Disabled** Enabled	Enable or disable boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS / legacy boot options.
SATA Support	**Last Boot HDD Only** All SATA Devices	Select which SATA device to be initialized in fast boot mode.
VGA Support	Auto **UEFI Driver**	If set to Auto, the legacy video option ROM will be installed for legacy OS boot; boot logo will NOT be shown during POST. For UEFI OS boot the UEFI GOP driver will be installed.
USB Support	Disabled **Full Init** Partial Init	If set to Disabled, no USB device will be available before OS boot. If set to Partial Init, specific USB ports/devices will NOT be available before OS boot. If set to Enabled, all USB devices will be available during POST and after OS boot.
PS/2 Device Support	Disabled **Enabled**	If set to Disabled, PS/2 devices will be skipped.
Network Stack Driver Support	**Disabled** Enabled	If set to Disabled, the UEFI network stack driver installation will be skipped.

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

10.6.1.1 CSM & Option ROM Control Submenu

Feature	Options	Description
Launch CSM	**Enabled** Disabled	Controls the execution of the CSM module. Only disable for pure UEFI operating system support.
Boot Option Filter	UEFI and Legacy **Legacy Only** UEFI Only	Controls which devices / boot loaders the system should boot to.
PXE Option ROM Launch Policy	**Do Not Launch** UEFI ROM Only Legacy ROM Only	Controls the execution of UEFI and legacy PXE option ROMs
Storage Option ROM Launch Policy	**Do Not Launch** UEFI ROM Only Legacy ROM Only	Controls the execution of UEFI and legacy mass storage device option ROMs
Video Option ROM Launch Policy	Do Not Launch UEFI ROM Only **Legacy ROM Only**	Controls the execution of UEFI and legacy video option ROMs
Other Option ROM Launch Policy	**UEFI ROM Only** Legacy ROM Only	Controls the execution of option ROMs for PCI / PCI Express devices other than network, mass storage or video.
GateA20 Active	**Upon Request** Always	Gate A20 control. Upon Request: Gate A20 can be disabled using BIOS services. Always: Do not allow disabling Gate A20 This option is useful when any runtime code is executed above 1MB.
Option ROM Messages	**Force BIOS** Keep Current	Set display mode for option ROMs.
INT19 Trap Response	**Immediate** Postponed	BIOS reaction on INT19 trapping by Option ROM Immediate: Execute the trap right away. Postponed: Execute the trap during legacy boot.

10.7 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

10.7.1 Security Settings

Feature	Options	Description
Administrator Password	Enter password	Specifies the setup administrator password.
HDD Security Configuration *List of all detected hard disks supporting the security feature set.*	Select device to open device security configuration submenu	

10.7.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

10.7.3 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen. You can display a Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options
► **Boot Override** *List of all boot devices currently detected.*	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to “Device Based”.

11 Additional BIOS Features

The conga-QG uses a congatec/AMI AptioEFI firmware that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as QFT3R1xx, where QFT3 is the congatec internal BIOS project name for conga-QG, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

The conga-QG BIOS binary size is approximately 8MB.

11.1 Supported Flash Devices

The conga-QG supports the following flash devices:

- Spansion S25FL064K0SMFI01 (8 MB)
- Winbond W25Q64CVSSIG (8 MB)
- Winbond W25Q64FVSSIG (8 MB)

The flash devices listed above can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.

11.2 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” refer to the user’s guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

11.3 BIOS Security Features

The BIOS provides a setup administrator password that limits access to the BIOS setup menu.

11.4 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to ‘lock’ and ‘unlock’ drives using the security password. A ‘locked’ drive will be detected by the system, but no data can be accessed. Accessing data on a ‘locked’ drive requires the proper password to ‘unlock’ the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within five attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

12 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Qseven® Specification	http://www.qseven-standard.org/
Qseven® Design Guide	http://www.qseven-standard.org/
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications