# TQMa6x
# User's Manual

TQMa6x UM 0100
15.03.2015

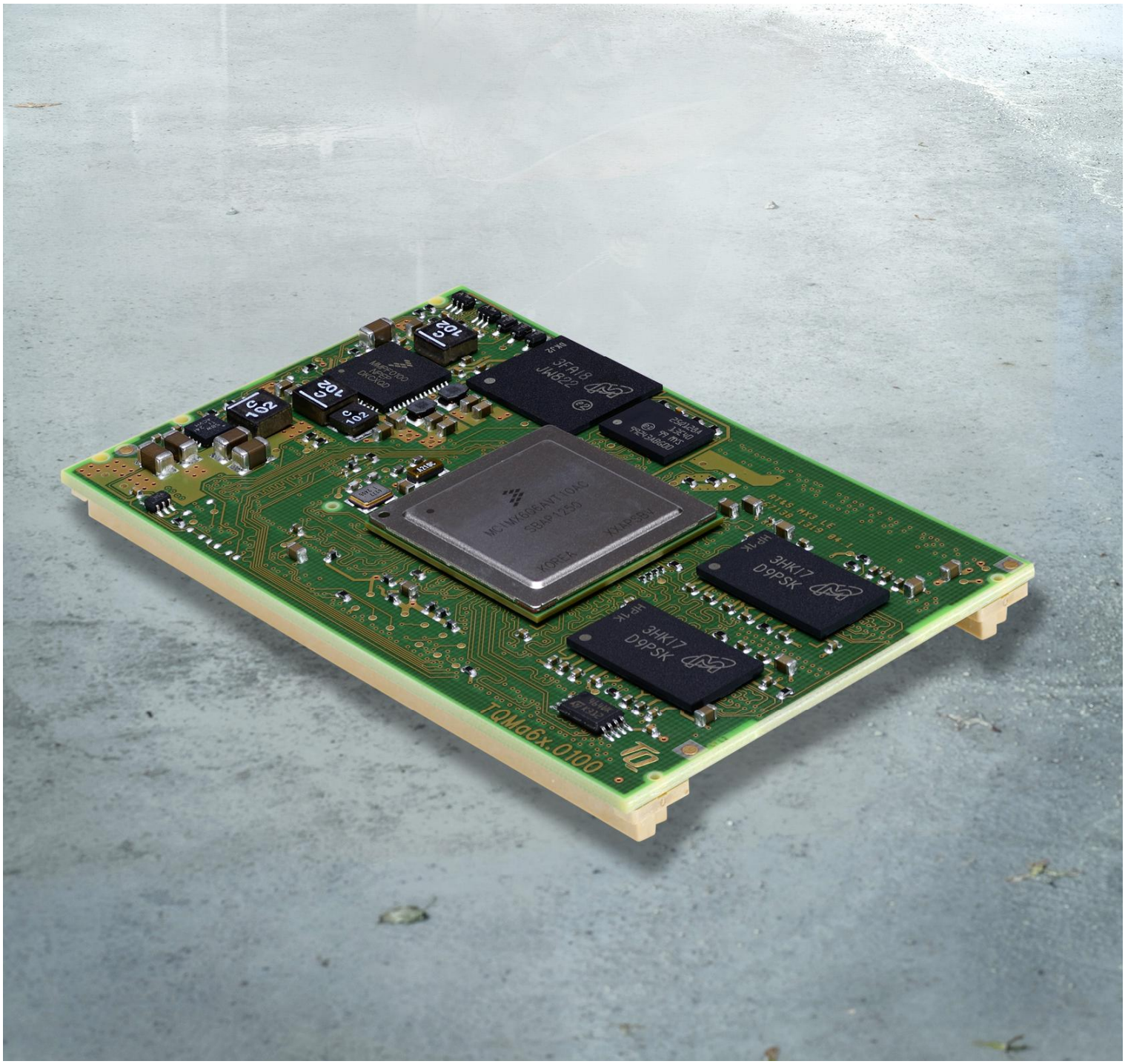


TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

TABLE DIRECTORY

ILLUSTRATION DIRECTORY

REVISION HISTORY

| Rev. | Date | Name | Pos. | Modification |
|---|---|---|---|---|
| 0001 | 04.07.2013 | Petz | | Document created |
| 0100 | 15.03.2015 | Petz | All | Complete rework |

# 1. ABOUT THIS MANUAL

## 1.1 Copyright and licence expenses



This User's Manual may not be copied, reproduced, translated, changed or distributed, completely or partially in electronic, machine readable, or in any other form without the written consent of TQ-Systems GmbH.

The drivers and utilities for the used components as well as the BIOS are subject to the copyrights of the respective manufacturers. The licence conditions of the respective manufacturer are to be adhered to.

Bootloader-licence expenses are paid by TQ-Systems GmbH and are included in the price.

Licence expenses for the operating system and applications are not taken into consideration and must be separately calculated / declared.

## 1.2 Registered trademarks

TQ-Systems GmbH aims to adhere to the copyrights of all the graphics and texts used in all publications, and strives to use original or license-free graphics and texts.

All the brand names and trademarks mentioned in the publication, including those protected by a third party, unless specified otherwise in writing, are subjected to the specifications of the current copyright laws and the proprietary laws of the present registered proprietor without any limitation. One should conclude that brand and trademarks are rightly protected by of a third party.

## 1.3 Disclaimer

TQ-Systems GmbH does not guarantee that the information in this User's Manual is up-to-date, correct, complete or of good quality. Nor does TQ-Systems GmbH assume guarantee for further usage of the information. Liability claims against TQ-Systems GmbH, referring to material or non-material related damages caused, due to usage or non-usage of the information given in the User's Manual, or due to usage of erroneous or incomplete information, are exempted, as long as there is no proven intentional or negligent fault of TQ-Systems GmbH.

TQ-Systems GmbH explicitly reserves the rights to change or add to the contents of this User's Manual or parts of it without special notification.

## 1.4 Imprint

TQ-Systems GmbH
Gut Delling, Mühlstraße 2
82229 Seefeld
Tel: +49 (0) 8153 9308–0
Fax: +49 (0) 8153 9308–134
Email: info@tq-group.com
Web: http://www.tq-group.com/

## 1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

## 1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

| Symbol | Meaning |
|---|---|
|  | This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V. |
|  | This symbol indicates the possible use of voltages higher than 24 V.<br>Please note the relevant statutory regulations in this regard.<br>Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component. |
|  | This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used. |
|  | This symbol represents important details or aspects for working with TQ-products. |
| `Command` | A font with fixed-width is used to denote commands, contents, file names, or menu items. |

## 1.7 Handling and ESD tips

General handling of your TQ-products

| | |
|---|---|
|  | The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.<br>A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off.<br>Violation of this guideline may result in damage / destruction of the TQMa6x and be dangerous to your health.<br>Improper handling of your TQ-product would render the guarantee invalid. |

Proper ESD handling

| | |
|---|---|
|  | The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD).<br>Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices. |

## 1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

## 1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the used modules:**
  These documents describe the service, functionality and special characteristics of the used module (incl. BIOS).
- **Specifications of the used components:**
  The manufacturer's specifications of the used components, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- Circuit diagram MBa6x
- CPU Reference Manual IMX6DQRM
- User's Manual STK-MBa6x
- Documentation of boot loader U-Boot (http://www.denx.de/wiki/U-Boot/Documentation)
- Documentation of PTXdist (http://www.ptxdist.de)

# 2. BRIEF DESCRIPTION

This User's Manual describes the TQMa6x Rev ≤0105, and refers to some software settings.
A certain derivative of the TQMa6x does not necessarily provide all features described in this User's Manual.
This User's Manual does also not replace the Freescale Reference Manuals of the CPU (3), (4).
The TQMa6x is a universal Minimodule based on the Freescale ARM CPU MCIMX6x (i.MX6x).
The Cortex A9 core of this CPU works with up to 800 MHz.
The TQMa6x extends the TQC product range and offers an outstanding computing performance.
A suitable CPU derivative (Single, Dual, Quad core) can be selected for each requirement.

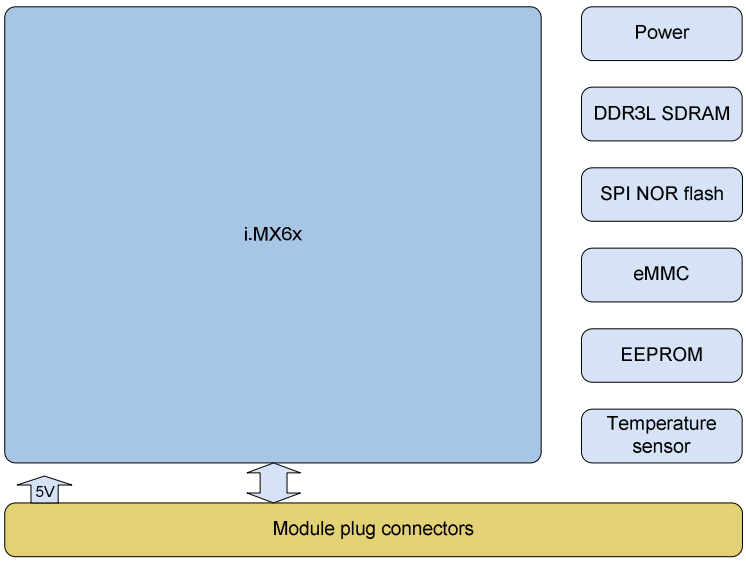



Illustration 1: Block diagram TQMa6x (simplified)

The TQMa6x provides the following key functions and characteristics:

## 2.1 Key functions and characteristics

- Freescale i.MX6 CPU ("Solo", "DualLite", "Dual", "Quad")
- Up to 2 GByte DDR3L SDRAM, 64 bit interface (except "Solo")
- Up to 8 GByte eMMC NAND flash
- Up to 128 Mbyte SPI NOR flash
- 64 kBit EEPROM
- Temperature sensor
- Freescale Power Management Integrated Circuit
- Extended temperature range
- Single 5 V power supply

All essential CPU pins are routed to the connectors.
There are therefore no restrictions for customers using the TQMa6x with respect to an integrated customised design.

# 3. ELECTRONICS SPECIFICATION

The information in this User's Manual is only valid in connection with the boot loader adapted for the TQMa6x, which is preinstalled on every TQMa6x (see also section 5) and the BSP provided by TQ-Systems GmbH.

## 3.1 System overview

### 3.1.1 System architecture / block diagram

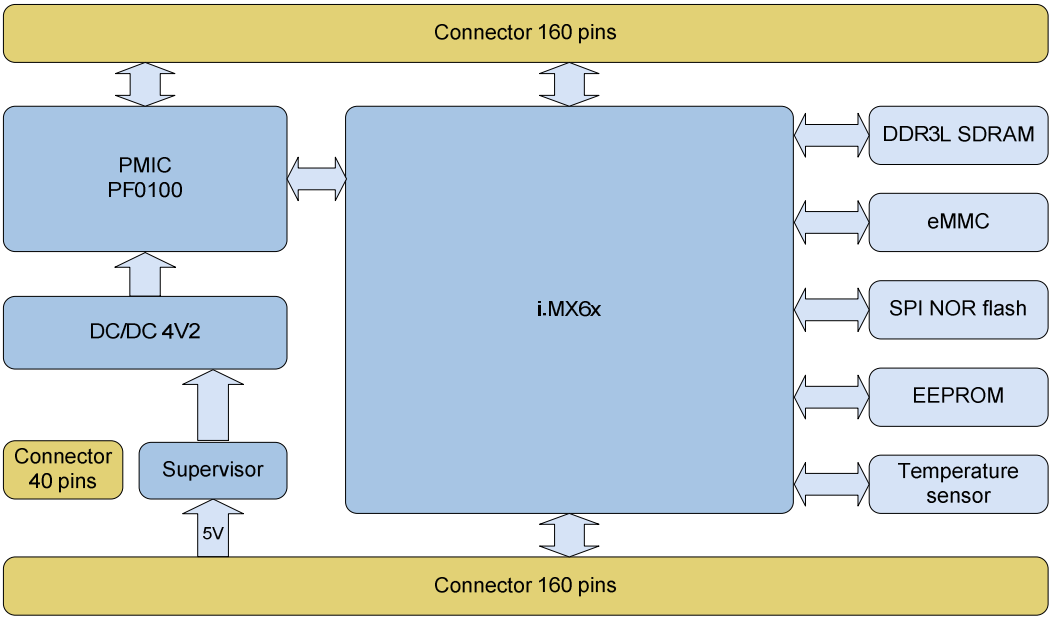



Illustration 2: Block diagram TQMa6x

### 3.1.2 Functionality

The following key functions are implemented on the TQMa6x:

- i.MX6 CPU
- DDR3L SDRAM
- eMMC NAND flash
- SPI NOR flash
- EEPROM
- Temperature sensor
- Supervisor
- PMIC / DC/DC converter

The following interfaces are provided at the connectors of the TQMa6x:[1]

- 1 × Ethernet 10/100/1000 RGMII
- 1 × HDMI 1.4
- 1 × $I^2S$
- 1 × JTAG
- 1 × MIPI CSI
- 1 × MIPI DSI
- 1 × MLB
- 1 × Parallel display RGB 24 bit
- 1 × PCIe 2.0 (1 Lane)
- 1 × SATA 3.0
- 1 × SD 8 Bit (SDIO / MMC / SD card)
- 1 × SPDIF
- 2 × CAN
- 2 × General Purpose Clocks
- 2 × $I^2C$
- 2 × LVDS display
- 2 × SPI
- 2 × USB 2.0 Hi-Speed (1 of it is OTG)
- 40 × GPIO
- 4 × PWM
- 4 × UART (with Handshake)

By adapting the pin configuration further interfaces of the i.MX6 are also available as an alternative to the mentioned factory configuration. These are amongst other:

- Camera Serial Interfaces
- EIM bus
- Enhanced Periodic Interrupt Timer
- Enhanced Serial Audio Interface
- Ethernet 10/100 RMII
- General Purpose Media Interface
- General Purpose Timer
- Keypad port
- MIPI HSI Host Controller
- More audio interfaces
- More $I^2C$ interfaces
- More SPI interfaces
- More UARTs
- One additional parallel display

1: Number depends on the i.MX6 derivative.

## 3.2 System components

### 3.2.1 i.MX6 processor

The following illustration shows the block diagram of the i.MX6 processor family:

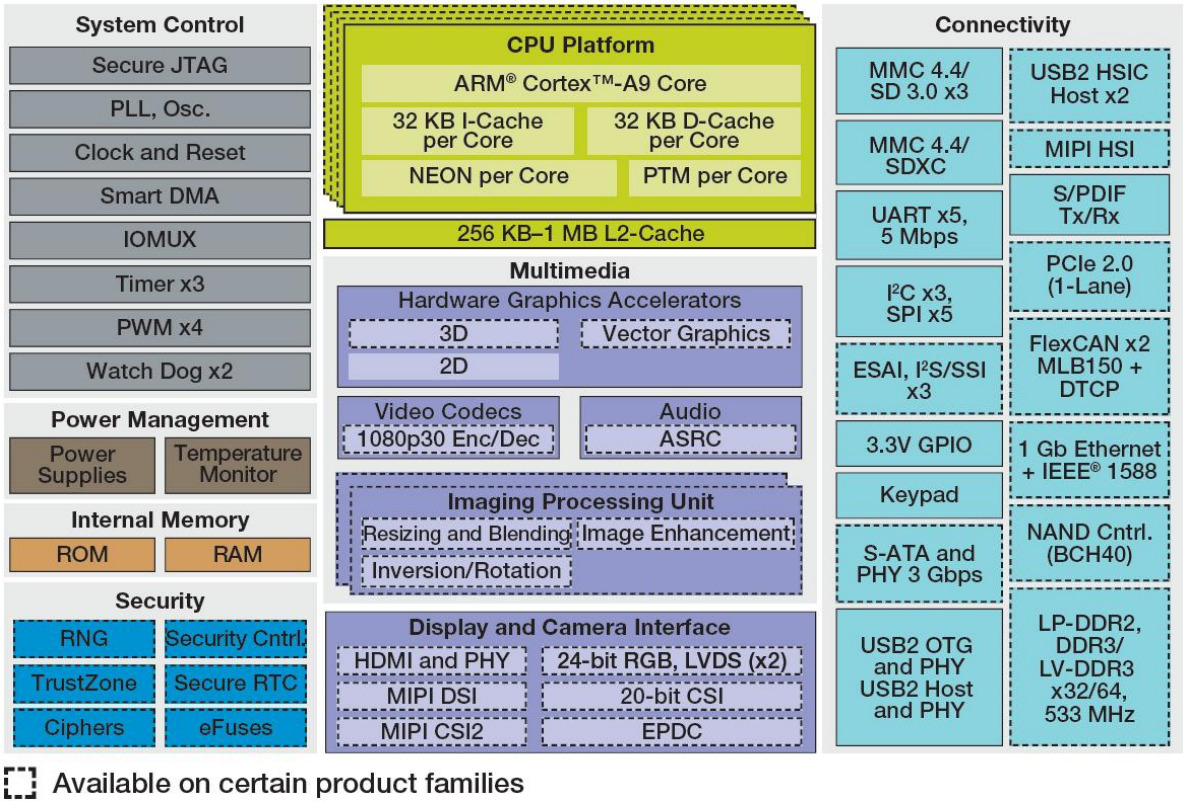



Illustration 3: Block diagram i.MX6
(Source: Freescale)

#### 3.2.1.1 i.MX6 processor derivatives

Depending on the derivative of the TQMa6x one of the following derivatives of the CPU is assembled:

Table 2: Processor derivatives

| Description | | Clock | Temperature | BSP support |
|---|---|---|---|---|
| i.MX6S | Solo | 800 MHz | –40 °C … +105 °C | Yes |
| i.MX6U | DualLite | 800 MHz | –40 °C … +105 °C | Yes |
| i.MX6D | Dual Industrial | 800 MHz | –40 °C … +105 °C | Yes |
| i.MX6Q | Quad Industrial | 800 MHz | –40 °C … +105 °C | Yes |

| **Attention: Malfunction** | |
|---|---|
|  | Please take note of the current errata of the i.MX6 (5), (6). |

#### 3.2.1.2 Boot modes

The i.MX6 contains a ROM with integrated boot loader.
After the start the boot code initializes the hardware and then loads the program image from the selected boot device.
The eMMC or the SPI NOR flash integrated on the TQMa6x can for example be selected as the standard boot device.
As an alternative to booting from the integrated eMMC or the SPI NOR flash it is also possible to boot from SD card or SATA, see 3.2.1.2.2. More information about boot interfaces and its configuration is to be taken from the CPU's data sheets (1), (7), and the Reference Manuals (3), (4).
The boot device and its configuration, as well as different CPU settings have to be set via different boot mode registers.
Therefore the i.MX6 provides two possibilities:

- Burning internal eFuses and / or
- Reading dedicated GPIO pins

The exact behaviour during booting depends on the value of the register BT_FUSE_SEL (Default = 0).
The following table shows the behaviour of the bit BT_FUSE_SEL in dependence of the selected boot mode.

Table 3: Boot modes and BT_FUSE_SEL

| BOOT_MODE[1:0] | Boot type | Setting BT_FUSE_SEL | Recommended for |
|---|---|---|---|
| 00 (default) | Boot From Fuses | 0 = Boot using Serial Loader (Default)<br>1 = Boot mode configuration is taken from fuses. | Series production |
| 01 | Serial Downloader | n/a | Development / production |
| 10 | Internal Boot | 0 = Boot mode configuration is taken from GPIOs. (Default)<br>1 = Boot mode configuration is taken from fuses. | Development |
| 11 | Reserved | n/a | n/a |

| Note: Malfunction | |
|---|---|
|  | Burning an eFuse is irreversible!<br>TQ-Systems GmbH takes no responsibility for the correct operation of the module, if eFuses are burnt by the user.<br>Burning eFuses has to be coordinated with TQ-Systems GmbH, since the module then no longer complies with the factory default after burning the eFuses (altered hardware). |

#### 3.2.1.2.1 Boot configuration

| Note: Boot configuration | |
|---|---|
|  | No boot device is set when the TQMa6x is delivered. |

Some general settings are done with some eFuses independent from the boot device.

Table 4: General boot settings

| Signal / eFuse | Pin name | Ball | Setting | Default | TQMa6x[2] |
|---|---|---|---|---|---|
| BOOT_CFG1[7:0] | – | – | **Boot configuration 1:**<br>Specific to selected boot mode | – | – |
| BOOT_CFG2[7:0] | – | – | **Boot configuration 2:**<br>Specific to selected boot mode | – | – |
| BOOT_CFG3[7] | EIM_A23 | J21 | **L1 I-Cache DISABLE:**<br>**0 = Enabled**<br>1 = Disabled | 0 | 0 |
| BOOT_CFG3[6] | EIM_A22 | F24 | **BT_MMU_DISABLE:**<br>**0 = MMU / L1 D Cache / PL310 enabled**<br>1 = MMU / L1 D Cache / PL310 disabled | 0 | 0 |
| BOOT_CFG3[5] | EIM_A21 | H23 | **DDR Memory Map Config:**<br>**00 = Single DDR channel**<br>01 = 2 × 32 Map<br>10 = 4 KB interleaving<br>11 = Reserved | 0 | 0 |
| BOOT_CFG3[4] | EIM_A20 | H22 | | 0 | 0 |
| BOOT_CFG3[3] | – | – | **Reserved** | – | – |
| BOOT_CFG3[2] | EIM_A18 | J22 | **Boot Frequencies ARM / DDR / AXI:**<br>**Solo / DualLite:**<br>**0 = 792 / 396 / 264 MHz**<br>1 = 396 / 306.6 / 176 MHz<br>**Dual / Quad:**<br>**0 = 792 / 528 / 264 MHz**<br>1 = 396 / 352 / 176 MHz | 0 | 0 |
| BOOT_CFG3[1] | – | – | **Reserved** | – | – |
| BOOT_CFG3[0] | EIM_A16 | – | **Disable SDMMC Manufacture Mode:[3]**<br>**0 = Enable**<br>1 = Disable | 0 | 0 |
| BOOT_CFG4[7] | EIM_EB3 | F23 | **Debug loop:**<br>**0 = Loop disabled**<br>1 = Loop enabled | 0 | 0 |
| BOOT_CFG4[6:0] | – | – | **Boot configuration 4:**<br>Specific to selected boot mode | – | – |

2: Recommended settings.
3: Only for “Solo” and “DualLite”, reserved for “Dual” and “Quad”.

#### 3.2.1.2.2 Boot interfaces

The configuration of the following boot devices is described in the next sections:

- eMMC
- SPI NOR flash
- SD card
- SATA

#### 3.2.1.2.3 Boot device eMMC

Table 5: Boot configuration eMMC at uSDHC3

| Signal / eFuse | Pin name | Ball | Setting | Default | TQMa6x |
|---|---|---|---|---|---|
| BOOT_CFG1[7] | EIM_DA7 | L25 | **Boot Device Selection:**<br>**01 = Boot from uSDHC Interfaces** | 0 | 0 |
| BOOT_CFG1[6] | EIM_DA6 | K25 | | 0 | 1 |
| BOOT_CFG1[5] | EIM_DA5 | L23 | **SD / MMC-Selection:**<br>0 = SD / eSD / SDXC<br>**1 = MMC / eMMC** | 0 | 1 |
| BOOT_CFG1[4] | EIM_DA4 | L22 | **Fast Boot Support:**<br>**0 = Regular**<br>1 = Fast Boot | 0 | 0 |
| BOOT_CFG1[3] | EIM_DA3 | K24 | **MMC Speed Mode:**<br>**0x = High Speed Mode**<br>1x = Normal Speed Mode | 0 | 0 |
| BOOT_CFG1[2] | EIM_DA2 | L21 | | 0 | 0 |
| BOOT_CFG1[1] | EIM_DA1 | J25 | **eMMC Reset Enable:**<br>0 = eMMC-Reset disabled<br>**1 = eMMC-Reset enabled** | 0 | 1 |
| BOOT_CFG2[7] | EIM_DA15 | N24 | **eMMC Bus Width:**<br>000 = 1 bit<br>001 = 4 bit<br>**010 = 8 bit**<br>101 = 4 bit DDR (MMC 4.4)<br>110 = 8 bit DDR (MMC 4.4) | 0 | 0 |
| BOOT_CFG2[6] | EIM_DA14 | N23 | | 0 | 1 |
| BOOT_CFG2[5] | EIM_DA13 | M23 | | 0 | 0 |
| BOOT_CFG2[4] | EIM_DA12 | M24 | **Port Select:**<br>00 = uSDHC1<br>01 = uSDHC2<br>**10 = uSDHC3**<br>11 = uSDHC4 | 0 | 1 |
| BOOT_CFG2[3] | EIM_DA11 | M20 | | 0 | 0 |
| BOOT_CFG2[2] | EIM_DA10 | M22 | **DLL Override:**<br>**0 = Boot ROM**<br>1 = Apply value per fuse field MMC_DLL_DLY[6:0] | 0 | 0 |
| BOOT_CFG2[1] | EIM_DA9 | M21 | **Boot Acknowledge:**<br>**0 = Boot Acknowledge enable**<br>1 = Boot Acknowledge disable | 0 | 0 |
| BOOT_CFG2[0] | EIM_DA8 | L24 | **Override Pad Settings:**<br>**0 = default values**<br>1 = Use PAD_SETTINGS values | 0 | 0 |

In addition to the mode listed above the following eMMC modes are supported at port uSDHC3:

Table 6: uSDHC3 eMMC modes

| eMMC mode | 1 Bit | 4 Bit | 8 Bit | Fast Boot | DDR |
|---|---|---|---|---|---|
| Normal Speed | × | × | × | –[4] | –[4] |
| High Speed | × | × | × | –[4] | –[4] |

4: Not yet supported by software.

#### 3.2.1.2.4 Boot device SPI NOR flash

Table 7: Boot configuration SPI NOR flash at eCSPI1

| Signal / eFuse | Pin name | Ball | Setting | Default | TQMa6x[5] |
|---|---|---|---|---|---|
| BOOT_CFG1[7] | EIM_DA7 | L25 | **Boot Device Selection:**<br>**0011 = Boot from Serial ROM** | 0 | 0 |
| BOOT_CFG1[6] | EIM_DA6 | K25 | | 0 | 0 |
| BOOT_CFG1[5] | EIM_DA5 | L23 | | 0 | 1 |
| BOOT_CFG1[4] | EIM_DA4 | L22 | | 0 | 1 |
| BOOT_CFG4[6] | EIM_EB2 | E22 | **EEPROM Recovery:**[6]<br>**0 = disabled**<br>1 = enabled | 0 | 0 |
| BOOT_CFG4[5] | EIM_RW | K20 | **CS select (SPI only):**<br>00 = CS#0<br>**01 = CS#1**<br>10 = CS#2<br>11 = CS#3 | 0 | 0 |
| BOOT_CFG4[4] | EIM_EB1 | K23 | | 0 | 1 |
| BOOT_CFG4[3] | EIM_EB0 | K21 | **SPI Addressing (SPI only)**<br>0 = 2-bytes (16-bit) (3,75 MHz Clock)<br>**1 = 3 Bytes (24-bit) (15 MHz Clock)** | 0 | 1 |
| BOOT_CFG4[2] | EIM_LBA | K22 | **Port Select:**<br>**000 = ECSPI-1**<br>001 = ECSPI-2<br>010 = ECSPI-3<br>001 = ECSPI-4<br>100 = ECSPI-5<br>101 = I2C-1<br>110 = I2C-2<br>111 = I2C-3 | 0 | 0 |
| BOOT_CFG4[1] | EIM_WAIT | M25 | | 0 | 0 |
| BOOT_CFG4[0] | EIM_A24 | F25 | | 0 | 0 |

5: Recommended settings.
6: The i.MX6 supports recovery devices. If this bit is set, the SPI NOR flash serves as recovery boot device.

#### 3.2.1.2.5 Boot device SD card

Table 8: Boot configuration SD card at uSDHC2

| Signal / eFuse | Pin name | Ball | Setting | Default | TQMa6x[7] |
|---|---|---|---|---|---|
| BOOT_CFG1[7] | EIM_DA7 | L25 | **Boot Device Selection:** | 0 | 0 |
| BOOT_CFG1[6] | EIM_DA6 | K25 | **01 = Boot from uSDHC Interfaces** | 0 | 1 |
| BOOT_CFG1[5] | EIM_DA5 | L23 | **SD / MMC-Selection:**<br>**0 = SD / eSD / SDXC**<br>1 = MMC / eMMC | 0 | 0 |
| BOOT_CFG1[4] | EIM_DA4 | L22 | **Fast Boot:**<br>0 = Regular<br>**1 = Fast Boot** | 0 | 1 |
| BOOT_CFG1[3] | EIM_DA3 | K24 | **SD Speed Mode:**<br>**00 = Normal / SDR12**<br>01 = High / SDR25<br>10 = SDR50 (on uSDHC3 and uSDHC4 only)<br>11 = SDR104 (on uSDHC3 and uSDHC4 only) | 0 | 0 |
| BOOT_CFG1[2] | EIM_DA2 | L21 | | 0 | 0 |
| BOOT_CFG1[1] | EIM_DA1 | J25 | **SD Power Cycle Enable:**<br>**0 = No Power Cycle**<br>1 = Power cycle enabled via SD_RST pad<br>(on uSDHC3 and uSDHC4 only) | 0 | 0 |
| BOOT_CFG1[0] | EIM_DA0 | L20 | **SD Loopback Clock Source Sel (for SDR50 and SDR104 only)**<br>**0 = through SD pad**<br>1 = direct | 0 | 0 |
| BOOT_CFG2[7] | EIM_DA15 | N24 | **SD Calibration Step:**<br>**00 = 1 delay cell**<br>01 = 1 delay cell<br>10 = 2 delay cell<br>11 = 3 delay cell | 0 | 0 |
| BOOT_CFG2[6] | EIM_DA14 | N23 | | 0 | 0 |
| BOOT_CFG2[5] | EIM_DA13 | M23 | **Bus Width:**<br>0 = 1 bit<br>**1 = 4 bit** | 0 | 1 |
| BOOT_CFG2[4] | EIM_DA12 | M24 | **Port:**<br>00 = uSDHC1<br>**01 = uSDHC2**<br>10 = uSDHC3<br>11 = uSDHC4 | 0 | 0 |
| BOOT_CFG2[3] | EIM_DA11 | M20 | | 0 | 1 |
| BOOT_CFG2[1] | EIM_DA9 | M21 | **Pull-Down during SD Power Cycle:**<br>**0 = Use default SD pad settings during power cycle**<br>1 = Set pull-down on SD pads during power cycle<br>(used only if "SD Power Cycle Enable" enabled) | 0 | 0 |
| BOOT_CFG2[0] | EIM_DA8 | L24 | **Override Pad Settings:**<br>**0 = Use default values**<br>1 = Use PAD_SETTINGS values | 0 | 0 |

In addition to the mode listed above the following SD card modes are supported at port uSDHC2:

Table 9: uSDHC2 SD card modes

| SD mode | 1 Bit | 4 Bit | Fast Boot |
|---|---|---|---|
| SDR12 | × | × | × |
| SDR25 | × | × | × |
| SDR50 | – | – | – |
| SDR104 | – | – | – |

7: Recommended settings.

#### 3.2.1.2.6 Boot device SATA

Table 10: Boot configuration SATA

| Signal / eFuse | Pin name | Ball | Setting | Default | TQMa6x[8] |
|---|---|---|---|---|---|
| BOOT_CFG1[7] | EIM_DA7 | L25 | **Boot Device Select:**<br>**0010 = Boot from Hard Disk** | 0 | 0 |
| BOOT_CFG1[6] | EIM_DA6 | K25 | | 0 | 0 |
| BOOT_CFG1[5] | EIM_DA5 | L23 | | 0 | 1 |
| BOOT_CFG1[4] | EIM_DA4 | L22 | | 0 | 0 |
| BOOT_CFG2[4] | EIM_DA12 | M24 | **Tx Spread Spectrum:**<br>**0 = Disabled**<br>1 = Enabled | 0 | 0 |
| BOOT_CFG2[3] | EIM_DA11 | M20 | **Rx Spread Spectrum:**<br>**0 = Enabled**<br>1 = Disabled | 0 | 0 |
| BOOT_CFG2[2] | EIM_DA10 | M22 | **SATA Speed:**<br>**0 = GEN2 (3.0 Gbps)**<br>1 = GEN1 (1.5 Gbps) | 0 | 0 |
| BOOT_CFG2[1] | EIM_DA9 | M21 | **SATA Type:**<br>**00 = i (Cable length 1 m)**<br>01 = m (Short Backplane Application)<br>10 = x (Long Backplane Application)<br>11 = Reserved | 0 | 0 |
| BOOT_CFG2[0] | EIM_DA8 | L24 | | 0 | 0 |

8: Not tested.

### 3.2.2 Memory

#### 3.2.2.1 DDR3L SDRAM

Depending on the CPU derivate up to four DDR3L SDRAM chips are assembled on the TQMa6x.
All chips have one common chip select. The chips are connected to the CPU with a bus width of 64 bit.
(Exception: The i.MX6 "Solo" is connected with a bus width of 32bit.)
The following block diagram shows how the DDR3L SDRAM is connected to the processor.

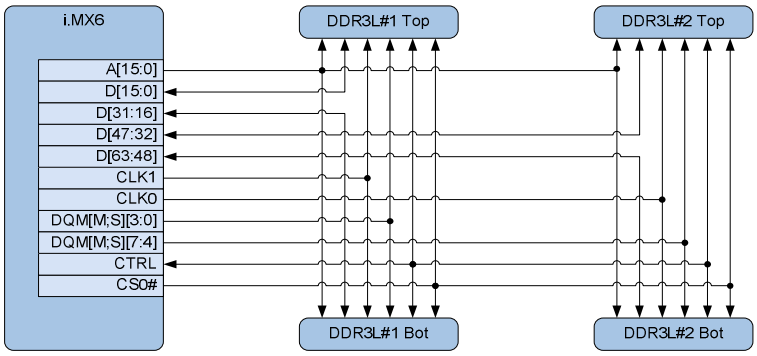



Illustration 4: Block diagram DDR3L SDRAM connection

The characteristics of the memory interface depend on the CPU derivate.
The following table shows the different possibilities:

Table 11: i.MX6 SDRAM interface according to CPU derivate

| CPU derivative | Bus width max. | Frequency max. | No. of SDRAM chips | Support in BSP |
|---|---|---|---|---|
| i.MX6 Solo | × 32 | 400 MHz | 2 | Yes |
| i.MX6 DualLite | × 64 | 400 MHz | 4 | Yes |
| i.MX6 Dual | × 64 | 533 MHz | 4 | Yes |
| i.MX6 Quad | × 64 | 533 MHz | 4 | Yes |

The assembly options of DDR3L SDRAM on the TQMa6x are listed in the following table.

Table 12: Options of memory size DDR3L SDRAM

| Assembly option | Size |
|---|---|
| 2 × DDR3L 128M16 / ×32 | 512 Mbyte |
| 2 × DDR3L 256M16 / ×32 | 1 Gbyte[9] |
| 4 × DDR3L 128M16 / ×64 | 1 Gbyte |
| 4 × DDR3L 256M16 / ×64 | 2 Gbyte[9] |

The following address range is reserved for the DDR controller in *mode X32 / X64 fixed*:

Table 13: DDR3L SDRAM address range

| Start address | Size | Chip Select | Remark |
|---|---|---|---|
| 0x1000_0000 | 0xFFFF_FFFF | CS0# | 3840 Mbyte |

9: Not yet qualified.

#### 3.2.2.2 eMMC NAND flash

An eMMC NAND flash is provided for the boot loader and the application software.
The following block diagram shows how the eMMC flash is connected to the processor.

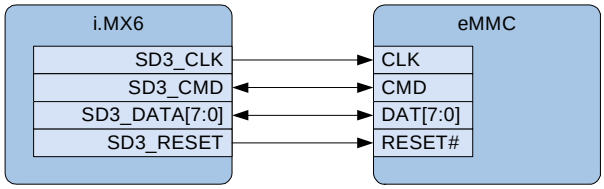



Illustration 5: Block diagram eMMC flash connection

#### 3.2.2.3 SPI NOR flash

An SPI NOR flash is also available. It can, e.g., be used as a recovery device.
The following block diagram shows how the SPI NOR flash is connected to the processor.

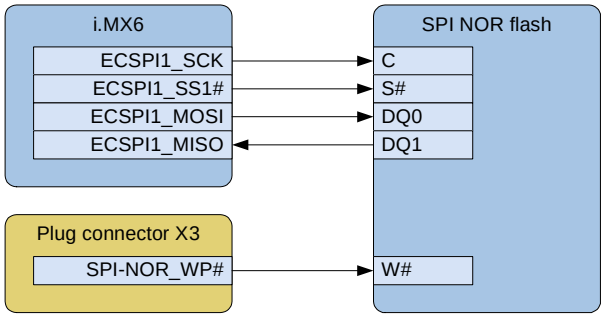



Illustration 6: Block diagram SPI NOR flash connection

The write protection pin of the memory is available on the connector.

The assembly options of SPI NOR flash on the TQMa6x are listed in the following table.

Table 14: SPI NOR flash assembly options

| Manufacturer | Capacity | Temp. range |
|---|---|---|
| Micron | 16 Mbyte | –40 °C … +85 °C |
| Micron | 32 Mbyte[10] | –40 °C … +85 °C |
| Micron | 64 Mbyte[10] | –40 °C … +85 °C |
| Micron | 128 Mbyte[10] | –40 °C … +85 °C |

10: Not yet qualified.

#### 3.2.2.4 EEPROM

A serial EEPROM is available for permanent storage of e.g. module characteristics or customers parameters.
The EEPROM is controlled via the I2C3 bus of the processor.
The following block diagram shows how the EEPROM is connected to the processor.

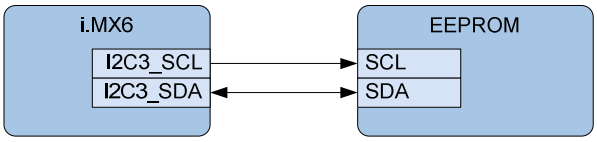



Illustration 7: Block diagram EEPROM connection

The following table shows the EEPROM used.

Table 15: EEPROM

| Manufacturer | Part number | Size | Temp. range |
|---|---|---|---|
| STM | M24C64-WDW6TP | 64 kbit | –45 °C … +85 °C |

- The $I^2C$ address of the EEPROM is `0x50 / 0b1010000`

In the EEPROM module-specific data is stored. It is, however, not essential for the correct operation of the TQMa6x.
The data can be deleted or altered by the user.

In the following table the parameters stored in the EEPROM are shown.

Table 16: EEPROM module specific data

| Offset | Payload (byte) | Padding (byte) | Size (byte) | Type | Remark |
|---|---|---|---|---|---|
| `0x00` | Variable | Variable | $32_{(10)}$ | Binary | Hard Reset Configuration Word (HRCW), (optional) |
| `0x20` | $6_{(10)}$ | $10_{(10)}$ | $16_{(10)}$ | Binary | MAC address |
| `0x30` | $8_{(10)}$ | $8_{(10)}$ | $16_{(10)}$ | ASCII | Serial number |
| `0x40` | Variable | Variable | $64_{(10)}$ | ASCII | Order code |
| `0x80` | – | – | $8{,}064_{(10)}$ | – | (Unused) |

### 3.2.3 RTC

The i.MX6 provides an RTC, which has its own power domain (SNVS).
The accuracy of the RTC is mainly determined by the characteristics of the quartz used.
The type FC-135 used on the TQMa6x has a standard frequency tolerance of ±20 ppm at 25 °C.
(Parabolic coefficient: max. $-0.04 \times 10^{-6}$ / °C$^2$).
The following block diagram shows the implementation on the TQMa6x.

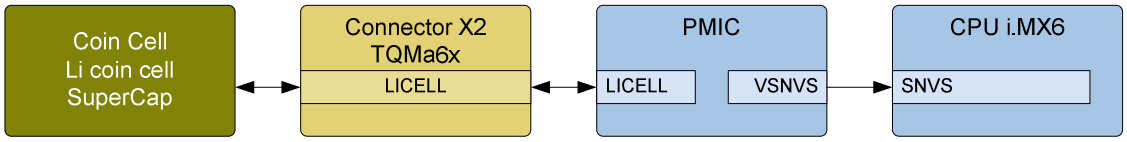



Illustration 8: Block diagram RTC

The RTC power domain SNVS of the CPU is supplied by the PMIC via the internal regulator VSNVS. The internal regulator VSNVS is either supplied by VIN (VDD4V2) or by LICELL. LICELL supports simple coin cells, but also Lithium coin cells or SuperCaps, which can also be charged by the PMIC. Charging methods and electrical characteristics of the pin LICELL are to be taken from the data sheet of the PMIC (2).
A coin cell is not suitable for long term bridging on account of the high current consumption. A Li coin cell or a SuperCap might be an option depending on the use case. It is to be taken note of that the typical charging current is only 60 µA.
For long term bridging an external RTC connected at the I²C bus on the carrier board is recommended.

Table 17: Current consumption RTC at pin LICELL

| Voltage coin cell | Typical current consumption PF0100 | Typical current consumption PF0100A |
|---|---|---|
| 2,4 V | 135 µA | 85 µA |
| 2,7 V | 165 µA | 100 µA |
| 3.0 V | 200 µA | 115 µA |
| 3.3 V | 230 µA | 130 µA |

### 3.2.4 Temperature sensor

A temperature sensor for supervision of the module temperature is provided on the TQMa6x.
It is placed on the bottom side of the TQMa6x, (D2 in Illustration 20).
The temperature sensor is connected to the I2C3 bus of the processor.
The following block diagram shows how the temperature sensor is connected to the processor.

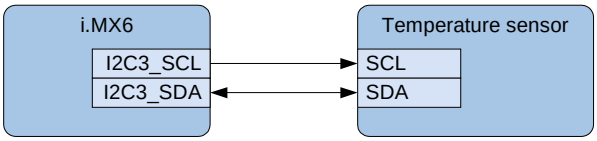



Illustration 9: Block diagram temperature sensor connection

The "OS"-output (over-temperature shutdown) of the sensor is not connected.

The following table shows the temperature sensor used.

Table 18: Temperature sensor

| Manufacturer | Part number | Resolution | Error | Temp. range |
|---|---|---|---|---|
| NXP | LM75ADP | 11 bit ADC | Max. ±3 °C | –55 °C … +125 °C |

➢ The I²C address of the temperature sensor is `0x48 / 0b1001000`

### 3.2.5 Interfaces

#### 3.2.5.1 Overview

The TQMa6x provides interfaces with primary functions. They can all be used simultaneously independent of their configuration. Some of the primary functions cannot be used if a secondary function (e.g. the EIM bus) is used.

Table 19: Internal interfaces

| Interface | Number | Function | Section | Remark |
|---|---|---|---|---|
| uSDHC3 | 1 | Primary | 3.2.2.2 | eMMC, 8 bit |
| ECSPI | 1 | Primary | 3.2.2.3 | ECSPI1 / SPI NOR flash |

Table 20: External interfaces

| Interface | Number | Function | Section | Remark |
|---|---|---|---|---|
| AUDMUX | 1 | Primary | 3.2.5.2 | AUD3 / I2S |
| | 3 | Secondary | | AUD4 / AUD5 / AUD6 \| Multiplexing has to be adapted |
| CCM | 2 | Primary | 3.2.5.3 | General Purpose Clocks |
| ECSPI | 2 | Primary | 3.2.5.4 | ECSPI1 / ECSPI5 |
| | 3 | Secondary | | ECSPI2 / ECSPI3 / ECSPI4 \| Multiplexing has to be adapted |
| EIM | 1 | Secondary | | Multiplexing has to be adapted |
| ENET | 1 | Primary | 3.2.5.5 | RGMII (GbE) |
| | 1 | Secondary | | ENET (10/100) / 1588 \| Multiplexing has to be adapted |
| EPIT | 2 | Secondary | | EPIT1 / EPIT2 \| Multiplexing has to be adapted |
| ESAI | 1 | Secondary | | Multiplexing has to be adapted |
| FLEXCAN | 2 | Primary | 3.2.5.6 | FLEXCAN1 / FLEXCAN2 |
| GPIO | 40 | Primary | 3.2.5.7 | – |
| GPMI | 1 | Secondary | | Multiplexing has to be adapted |
| GPT | 1 | Secondary | | Multiplexing has to be adapted |
| HDMI | 1 | Primary | 3.2.5.8 | – |
| I2C | 2 | Primary | 3.2.5.9 | I2C1 / I2C3 |
| | 1 | Secondary | | I2C2 \| Multiplexing has to be adapted |
| IPU | 1 | Primary | 3.2.5.10 | DISP0 (RGB) |
| | 4 | Secondary | | CSI0 / CSI1 / DISP0 / DISP1 \| Multiplexing has to be adapted |
| KPP | 1 | Secondary | | Multiplexing has to be adapted |
| LDB | 2 | Primary | 0 | LVDS0 / LVDS1 |
| MIPI_CSI | 1 | Primary | 3.2.5.12 | – |
| MIPI_DSI | 1 | Primary | 3.2.5.13 | – |
| MIPI_HSI | 1 | Secondary | | Multiplexing has to be adapted |
| MLB | 1 | Primary | 3.2.5.14 | – |
| PCIe | 1 | Primary | 3.2.5.15 | – |
| PWM | 4 | Primary | 3.2.5.16 | PWM1 / PWM3 / PWM4 |
| | 1 | Secondary | | PWM2 \| Multiplexing has to be adapted |
| SATA | 1 | Primary | 3.2.5.17 | – |
| SJC | 1 | Primary | 3.2.5.18 | JTAG |
| SPDIF | 1 | Primary | 3.2.5.19 | – |
| TAMPER | 1 | Primary | 3.2.5.20 | – |
| UART | 4 | Primary | 3.2.5.21 | UART2 / UART3 / UART4 / UART5 |
| | 1 | Secondary | | UART1 \| Multiplexing has to be adapted |
| USB | 2 | Primary | 3.2.5.22 | USB_H1 / USB_OTG |
| uSDHC | 1 | Primary | 3.2.5.23 | uSDHC2 / SD card / 1/4/ 8 Bit |
| | 2 | Secondary | | uSDHC1 / uSDHC4 \| Multiplexing has to be adapted |
| WDOG | 1 | Primary | 3.2.5.24 | WDOG1 |
| | 1 | Secondary | | WDOG2 \| Multiplexing has to be adapted |
| XTAL | 2 | Primary | 3.2.5.25 | XTALOSC1 / XTALOSC1 |

In the following sections only the external primary interfaces are described.

#### 3.2.5.2 AUDMUX

The signals of the digital audio multiplexer 3 (AUD3) are available via SSI on the connectors.
An audio-codec can be connected via e.g. I2S.
The following table shows the signals used by the AUD3 interface:

Table 21: Signals AUD3

| Signal name | Direction | Signals I2S | Pin |
|---|---|---|---|
| AUD3_RXC | I | – | X1–99 |
| AUD3_RXD | I | I2S_DOUT | X1–103 |
| AUD3_RXFS | I | – | X1–101 |
| AUD3_TXC | O | I2S_SCLK | X1–100 |
| AUD3_TXD | O | I2S_DIN | X1–104 |
| AUD3_TXFS | O | I2S_LRCLK | X1–102 |

- The signal CCM_CLKO1 is used as I2C_MCLK in the Linux-BSP provided by TQ-Systems GmbH.

Besides I2S, the SSI interface supports more synchronous modes. Details are to be taken from the Freescale Reference Manual (4).

#### 3.2.5.3 CCM

The CPU uses the clock controller module to provide two programmable clocks.
The following table shows the signals of the CCM:

Table 22: Signals CCM

| Signal name | Direction | Pin | Remark |
|---|---|---|---|
| CCM_CLKO1 | O | X1–78 | TQ-BSP: I2S_MCLK |
| CCM_CLKO2 | O | X2–82 | – |

#### 3.2.5.4 ECSPI

The i.MX6 provides five ECSPI interfaces (Enhanced Configurable SPI). Primarily ECSPI1 and ECSPI5 are available on the connectors. The CPU derivatives “Solo” and “DualLite” do not provide ECSPI5.
The following table shows the signals used by the ECSPI1 interface:

Table 23: Signals ECSPI1

| Signal name | Direction | Pin | Remark |
|---|---|---|---|
| ECSPI1_SCLK | O | X2–64 | – |
| ECSPI1_MOSI | O | X2–66 | – |
| ECSPI1_MISO | I | X2–63 | – |
| ECSPI1_SS1# | O | X2–65 | Used for optional SPI NOR flash on the TQMa6x |
| ECSPI1_SS2# | O | X2–72 | – |
| ECSPI1_SS3# | O | X2–71 | – |

The following table shows the signals used by the ECSP5 interface:

Table 24: Signals ECSPI5

| Signal name | Direction | Pin | Remark |
|---|---|---|---|
| ECSPI5_SCLK | O | X1–114 | – |
| ECSPI5_MOSI | O | X1–110 | – |
| ECSPI5_MISO | I | X1–108 | – |
| ECSPI5_SS0# | O | X1–112 | – |

#### 3.2.5.5 ENET

The i.MX6 provides a 10/100/1000 MAC core, which supports MII, RMII and RGMII.
Die RGMII signals are available as primary function at the connectors.
The following table shows the signals used by the RGMII interface.

Table 25: Signals RGMII

| Signal name | Direction | Pin | Power group |
|---|---|---|---|
| ENET_MDC | O | X2–49 | NVCC_ENET (2.5 V / 3.3 V) |
| ENET_MDIO | I/O | X2–51 | NVCC_ENET (2.5 V / 3.3 V) |
| ENET_REFCLK | I | X2–50 | NVCC_ENET (2.5 V / 3.3 V) |
| RGMII_RD[3:0] | I | X2 pins 43, 41, 39, 37 | NVCC_RGMII (2.5 V) |
| RGMII_RX_CTL | I | X2–45 | NVCC_RGMII (2.5 V) |
| RGMII_RXC | I | X2–33 | NVCC_RGMII (2.5 V) |
| RGMII_TD[3:0] | O | X2 pins 44, 42, 40, 38 | NVCC_RGMII (2.5 V) |
| RGMII_TX_CTL | O | X2–46 | NVCC_RGMII (2.5 V) |
| RGMII_TXC | O | X2–34 | NVCC_RGMII (2.5 V) |

| **Attention:** | |
|---|---|
|  | NVCC_ENET has to be connected externally! |

The RGMII interface of the i.MX6 works with an I/O voltage of 2.5 V. In order to use the interface, additional signals of the signal group ENET are required. The accompanying power supply pin is routed to the connector to operate these signals on the same I/O voltage, if RGMII is used.

- If RGMII is used, NVCC_ENET has to be connected to VCC2V5_RGMII_OUT.
  It is important that all 10 signals of the signal group ENET are then also set to 2.5 V.
- If RGMII is not required, NVCC_ENET has to be connected to VCC3V3_REF_OUT.

By adapting the multiplexing it is possible to use MII or RMII. Details are to be taken from the Freescale Reference Manuals (3), (4).
The module voltage VCC2V5_RGMII_OUT can be used to supply an RGMII-PHY to save an additional I/O voltage power supply on the carrier board. VCC2V5_RGMII_OUT provides a maximum of 200 mA, from which the TQMa6x requires approximately 80 mA.

#### 3.2.5.6 FLEXCAN

The i.MX6 provides two integrated CAN controllers. Both pairs of signals are available at the connectors.
The required drivers have to be implemented on the carrier board.
The following table shows the signals used by the CAN interface.

Table 26: Signals FLEXCAN

| Signal name | Direction | Pin |
|---|---|---|
| CAN1_TX | O | X1–96 |
| CAN1_RX | I | X1–94 |
| CAN2_TX | O | X1–92 |
| CAN2_RX | I | X1–90 |

#### 3.2.5.7 GPIO

Beside their interface function most of the pins of the i.MX6 can also be used as GPIO.
All these GPIOs can trigger an interrupt.
Details are to be taken from the Freescale Reference Manuals (3), (4).
In addition, different pins are already marked as GPIO and are available on the connectors.
The following table shows the GPIO signals used.

Table 27: Signals GPIO

| Signal name | Direction | Pin |
|---|---|---|
| GPIO1_IO[30:28] | I/O | X1 pins 149, 151, 153 |
| GPIO1_IO[26:25] | I/O | X1 pins 154, 155 |
| GPIO1_IO21 | I/O | X1–106 |
| GPIO1_IO[08:07] | I/O | X1 pins 157, 152 |
| GPIO2_IO[25:23] | I/O | X2 pins 81, 83, 84 |
| GPIO2_IO11 | I/O | X1–23 |
| GPIO2_IO08 | I/O | X1–21 |
| GPIO2_IO[03:00] | I/O | X1 pins 19, 17, 15, 13 |
| GPIO3_IO[29:26] | I/O | X2 pins 77, 78, 75, 76 |
| GPIO3_IO23 | I/O | X2–69 |
| GPIO3_IO20 | I/O | X2–68 |
| GPIO4_IO[09:05] | I/O | X2 pins 58, 57, 55 + X1 pins 74, 113 |
| GPIO5_IO[21:20] | I/O | X1 pins 84, 111 |
| GPIO5_IO18 | I/O | X1–82 |
| GPIO6_IO31 | I/O | X2–126 |
| GPIO6_IO16 | I/O | X2–94 |
| GPIO6_IO14 | I/O | X1–31 |
| GPIO6_IO11 | I/O | X1–29 |
| GPIO6_IO[08:07] | I/O | X1 pins 27, 25 |
| GPIO7_IO[13:11] | I/O | X1 pins 148, 72, 150 |

The electrical characteristics of the GPIOs are to be taken from the Freescale data sheets (1), (7).

#### 3.2.5.8 HDMI

The i.MX6 provides an integrated HDMI transmitter.
The following table shows the signals used by the HDMI interface:

Table 28: Signals HDMI

| Signal name | Direction | Pin |
|---|---|---|
| HDMI_CLKN | O | X1–38 |
| HDMI_CLKP | O | X1–40 |
| HDMI_D[2:0]N | O | X1 pins 56, 50, 44 |
| HDMI_D[2:0]P | O | X1 pins 58, 52, 46 |
| HDMI_DDC_SCL | O | X1–62 |
| HDMI_DDC_SDA | I/O | X1–64 |
| HDMI_HPD | I | X1–66 |

#### 3.2.5.9 I2C

The i.MX6 derivatives “Solo” and “DualLite” provide four, the i.MX6 derivatives “Dual” and “Quad” provide three $I^2C$ interfaces.
On every TQMa6x I2C1 and I2C3 are available at the connectors as primary function.
The following table shows the signals used by the I2C interface:

Table 29: Signals I2C

| Signal name | Direction | Pin | Remark |
|---|---|---|---|
| I2C1_SCL | O | X1–107 | – |
| I2C1_SDA | I/O | X1–109 | – |
| I2C3_SCL | $O_{PU}$ | X1–86 | Pull-Up 4.7 kΩ to 3.3 V on TQMa6x |
| I2C3_SDA | $I/O_{PU}$ | X1–88 | Pull-Up 4.7 kΩ to 3.3 V on TQMa6x |

The I2C3 bus is used for devices on the TQMa6x.
On the TQMa6x the following devices are connected to the I2C3 bus:

Table 30: I2C3 address assignment

| Component | Address |
|---|---|
| EEPROM (M24C64) | `0x50 / 0b1010000` |
| Temperature sensor (LM75A) | `0x48 / 0b1001000` |
| PMIC (MMPF0100) | `0x08 / 0b0001000` |

If more devices are connected to the I2C3 bus on the carrier board, the maximum capacitive bus load according to the $I^2C$ standard has to be taken note of. If necessary, additional Pull-Ups at the bus should be provided on the carrier board.

#### 3.2.5.10 IPU

The i.MX6 provides two parallel display interfaces (max. 4,096 × 2,048 pixel). One of them, DISP0, is routed to the connectors as primary function. Information with respect to the supported types of displays and formats are to be taken from the Freescale Reference Manuals (3), (4).
The following table shows the signals used by the display interface DISP0.

Table 31: Signals parallel display

| Signal name | Direction | Pin | Remark |
|---|---|---|---|
| DISP0_DAT[23:0] | O | X2 [158:147], [144:133] | Display Output RGB-Data / i.MX6 signal: IPU1_DISP0_DATA[23:0] |
| DISP0_HSYNC | O | X2–128 | Display Output Horizontal Sync / i.MX6 signal: IPU1_DI0_PIN2 |
| DISP0_VSYNC | O | X2–130 | Display Output Vertical Sync / i.MX6 signal: IPU1_DI0_PIN3 |
| DISP0_CLK | O | X2–125 | Display Output Clock / i.MX6 signal: IPU1_DI0_DISP_CLK |
| DISP0_DRDY | O | X2–127 | Display Output Data Enable / i.MX6 signal: IPU1_DI0_PIN15 |
| DISP0_CONTRAST | O | X2–129 | Display Backlight PWM / i.MX6 signal: IPU1_DI0_PIN4[11] |

#### 3.2.5.11 LDB

The i.MX6 provides two integrated LVDS display-bridges, which are routed to the connectors.
The following table shows the signals used by the LVDS0 interface:

Table 32: Signals LVDS0

| Signal name | Direction | Pin |
|---|---|---|
| LVDS0_CLK_N | O | X1–136 |
| LVDS0_CLK_P | O | X1–138 |
| LVDS0_TX[3:0]_N | O | X1 pins 142, 130, 124, 118 |
| LVDS0_TX[3:0]_P | O | X1 pins 144, 132, 126, 120 |

The following table shows the signals used by the LVDS1 interface.

Table 33: Signals LVDS1

| Signal name | Direction | Pin |
|---|---|---|
| LVDS1_CLK_N | O | X1–135 |
| LVDS1_CLK_P | O | X1–137 |
| LVDS1_TX[3:0]_N | O | X1 pins 141, 129, 123, 117 |
| LVDS1_TX[3:0]_P | O | X1 pins 143, 131, 125, 119 |

11: Currently not supported; use PWM1 instead.

#### 3.2.5.12 MIPI_CSI

The i.MX6 provides a MIPI Camera Serial Interface (CSI), which is routed to the connectors.
The following table shows the signals used by the MIPI_CSI interface:

Table 34: Signals MIPI_CSI

| Signal name | Direction | Pin |
|---|---|---|
| CSI_CLK0M | I | X3–3 |
| CSI_CLK0P | I | X3–5 |
| CSI_D[3:0]M | I | X3 pins 27, 21, 15, 9 |
| CSI_D[3:0]P | I | X3 pins 29, 23, 17, 11 |

#### 3.2.5.13 MIPI_DSI

The i.MX6 provides a MIPI_DSI interface, which is routed to the connectors.
The following table shows the signals used by the MIPI_DSI interface:

Table 35: Signals MIPI_DSI

| Signal name | Direction | Pin |
|---|---|---|
| DSI_CLK0M | O | X3–22 |
| DSI_CLK0P | O | X3–24 |
| DSI_D[1:0]M | O | X3 pins 34, 28 |
| DSI_D[1:0]P | O | X3 pins 36, 30 |

#### 3.2.5.14 MLB[12]

Depending on the derivate the i.MX6 provides a Media-Local-Bus interface (MLB), which is routed to the connectors.
The following table shows the signals used by the MLB interface:

Table 36: Signals MLB

| Signal name | Direction | Pin |
|---|---|---|
| MLB_CN | I | X3–4 |
| MLB_CP | I | X3–6 |
| MLB_SN | I/O | X3–16 |
| MLB_SP | I/O | X3–18 |
| MLB_DN | I/O | X3–10 |
| MLB_DP | I/O | X3–12 |

12: Currently not supported.

#### 3.2.5.15 PCIe

The i.MX6 provides a PCIe interface, which is routed to the connectors.
The following table shows the signals used by the PCIe interface:

Table 37: Signals PCIe

| Signal name | Direction | Pin |
|---|---|---|
| PCIE_TXM | O | X1–14 |
| PCIE_TXP | O | X1–16 |
| PCIE_RXM | I | X1–20 |
| PCIE_RXP | I | X1–22 |

CLK1 of the module XTAL can be used as a differential clock (see 3.2.5.25).

#### 3.2.5.16 PWM

The i.MX6 provides several PWMs, which are routed to the connectors.
The following table shows the available PWM signals:

Table 38: Signals PWM

| Signal name | Direction | Pin | Remark |
|---|---|---|---|
| PWM[4:3] | O | X1 pins 105, 33 | – |
| PWM1 | O | X1–147 | TQ-Linux-BSP: BACKLIGHT_PWM (DISP0_CONTRAST) |

#### 3.2.5.17 SATA

The i.MX6 provides a SATA controller with integrated PHY.
The following table shows the signals used by the SATA interface:

Table 39: Signals SATA

| Signal name | Direction | Pin |
|---|---|---|
| SATA_TXM | O | X1–61 |
| SATA_TXP | O | X1–63 |
| SATA_RXM | I | X1–55 |
| SATA_RXP | I | X1–57 |

#### 3.2.5.18 SJC

The i.MX6 can operate in two different JTAG modes. The pin JTAG_MOD defines the mode.
The following table shows the existing modes as well as the mode set on the TQMa6x.

Table 40: JTAG-Modes

| JTAG_MOD | Default | Name | Remark |
|---|---|---|---|
| 0 | X | Daisy Chain All | For common SW debug (High speed and series production) |
| 1 | | SJC only | IEEE 1149.1 JTAG compliant mode |

The following table shows the signals used by the JTAG interface:

Table 41: Signals JTAG

| Signal name | Direction | Pin | Remark |
|---|---|---|---|
| JTAG_TCK | I | X1–77 | i.MX6-internal Pull-Up 47 kΩ |
| JTAG_TMS | I | X1–69 | i.MX6-internal Pull-Up 47 kΩ |
| JTAG_TDI | I | X1–71 | i.MX6-internal Pull-Up 47 kΩ |
| JTAG_TDO | O | X1–73 | i.MX6-internal keeper |
| JTAG_TRST# | I | X1–67 | i.MX6-internal Pull-Up 47 kΩ |
| JTAG_MOD | I | X1–75 | Pull-Down 4.7 kΩ on TQMa6x + i.MX6-internal Pull-Up 100 kΩ |

#### 3.2.5.19 SPDIF

The i.MX6 provides an SPDIF interface with transmit and receive functionality.
The following table shows the signals used by the SPDIF interface:

Table 42: Signals SPDIF

| Signal name | Direction | Pin |
|---|---|---|
| SPDIF_IN | I | X1–158 |
| SPDIF_OUT | O | X1–156 |

#### 3.2.5.20 Tamper

The i.MX6 provides protection against unauthorised opening or manipulation of the device by tamper detection.
The pin TAMPER is available at the connectors for this purpose.
The following table shows the signal used:

Table 43: Signal TAMPER

| Signal name | Direction | Pin |
|---|---|---|
| TAMPER | I | X3–39 |

Details about the behaviour and how to connect the TAMPER pin are to be taken from the Freescale Reference Manuals (3), (4).

#### 3.2.5.21 UART

The i.MX6 provides five UART interfaces. UART2 to UART5 also offer handshake signals and are available at the connectors as primary function.

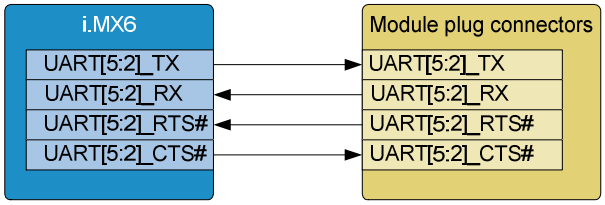



Illustration 10: Block diagram UART[5:2] interfaces

The following table shows the signals used by the UART interface.

Table 44: Signals UART

| Signal name | Direction | Pin |
|---|---|---|
| UART5_TXD | O | X1–91 |
| UART5_RXD | I | X1–89 |
| UART5_CTS# | O | X1–95 |
| UART5_RTS# | I | X1–93 |
| UART4_TXD | O | X1–83 |
| UART4_RXD | I | X1–81 |
| UART4_CTS# | O | X1–87 |
| UART4_RTS# | I | X1–85 |
| UART3_TXD | O | X2–61 |
| UART3_RXD | I | X2–59 |
| UART3_CTS# | O | X2–80 |
| UART3_RTS# | I | X2–79 |
| UART2_TXD | O | X2–29 |
| UART2_RXD | I | X2–27 |
| UART2_CTS# | O | X2–30 |
| UART2_RTS# | I | X2–28 |

#### 3.2.5.22 USB

The i.MX6 provides three USB Host controllers and one USB OTG controller. The USB HOST1 controller and the USB OTG controller provide an integrated High-Speed PHY. They are available at the connectors as primary function.
The following table shows the signals used by the USB_H1 interface:

Table 45: Signals USB_H1

| Signal name | Direction | Pin | Remark |
|---|---|---|---|
| USB_H1_DN | I/O | X1–34 | – |
| USB_H1_DP | I/O | X1–32 | – |
| USB_H1_PWR | O | X1–39 | – |
| USB_H1_OC | I | X1–41 | – |
| USB_H1_VBUS | P | X1–37 | Should be directly connected to a 5 V supply. |

The following table shows the signals used by the USB_OTG interface:

Table 46: Signals USB_OTG

| Signal name | Direction | Pin | Remark |
|---|---|---|---|
| USB_OTG_DN | I/O | X1–51 | – |
| USB_OTG_DP | I/O | X1–49 | – |
| USB_OTG_ID | I | X1–45 | Device Mode: connect to Micro-USB connector<br>Host Mode : connect to Micro-USB connector and to ground |
| USB_OTG_PWR | O | X2–70 | – |
| USB_OTG_OC | I | X2–67 | – |
| USB_OTG_VBUS | P | X1–43 | – |

#### 3.2.5.23 uSDHC

The uSDHC2 port of the i.MX6 is routed to the connectors to connect an MMC, SD or SDIO card.
The following table shows the signals used by the uSDHC interface.

Table 47: Signals uSDHC2

| Signal name | Direction | Pin |
|---|---|---|
| SD2_DAT[7:0] | I/O | X2[10:3] |
| SD2_CLK | O | X2–13 |
| SD2_CMD | I/O | X2–12 |
| SD2_CD# | I | X2–14 |
| SD2_WP | O | X2–11 |

#### 3.2.5.24 Watchdog

The i.MX6 provides a watchdog timer.
The following table shows the signal used by the watchdog timer.

Table 48: Signal WDOG

| Signal name | Direction | Pin |
|---|---|---|
| WDOG1# | O | X2–60 |

The watchdog of the i.MX6 has two functions:

- Power-down counter
  After the CPU is reset a power-down counter is started automatically. If it is not deactivated within 16 seconds, the signal WDOG1# will be activated. More information is to be taken from the Freescale Reference Manuals (3), (4).

- Watchdog timer
  If the watchdog timer is activated but not reset within the configured time, the signal WDOG1# will be activated. At the same time the internal signal WDOG_RST# triggers the system reset controller of the i.MX6 and triggers a warm reset. The signal WDOG1# remains on low level, or Hi-Z up to the next power-on reset.
  More information is to be taken from the Freescale Reference Manuals (3), (4).

#### 3.2.5.25 XTAL

The i.MX6 provides two differential clock outputs, which are routed to the connectors.
The following table shows the signals used:

Table 49: Signals XTAL

| Signal name | Direction | Pin |
|---|---|---|
| CLK2_N | O | X3–33 |
| CLK2_P | O | X3–35 |
| CLK1_N | O | X1–26 |
| CLK1_P | O | X1–28 |

### 3.2.6 Reset

Reset inputs or outputs are available at the connectors of the TQMa6x.
The following block diagram shows the wiring of the reset signals.

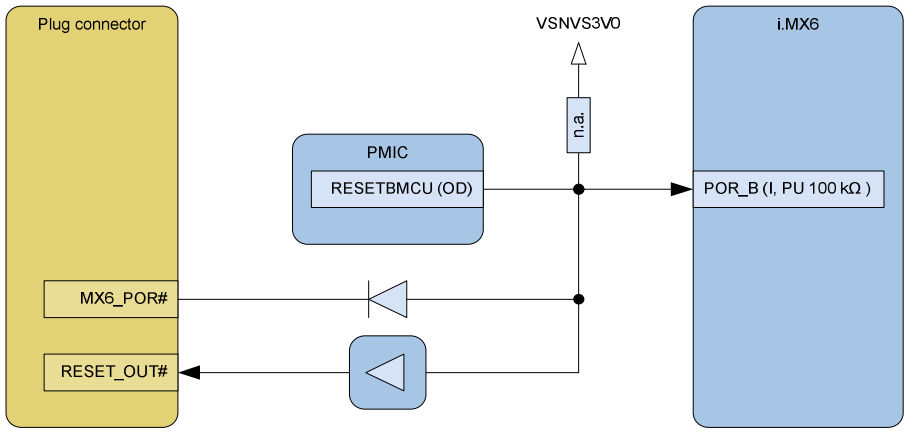



Illustration 11: Block diagram Reset

The following table describes the reset signals available at the connectors.

Table 50: Reset signals

| Signal name / pin | Direction | Remark |
|---|---|---|
| MX6_POR# / X2–23 | $I_{PU\_100\ k\Omega}$ | • Reset input POR_B (Power-On Reset) of the i.MX6<br>• Generates COLD-Reset of the CPU<br>• Low-active signal |
| RESET_OUT# / X2–25 | $O_{OD}$ | • Reset output RESETBMCU of the PMIC<br>• Can be used for reset inputs of external periphery<br>• Open Drain, requires Pull-Up on the carrier board (max. 3.3 V) |

### 3.2.7 Power supply

In addition to the required PMIC another voltage converter is used on the TQMa6x to provide the input voltage of 4.2 V for the PMIC. The input voltage for the TQMa6x is set to 5.00 V ±5 %. This results in an input voltage range of 4.75 V to 5.25 V.

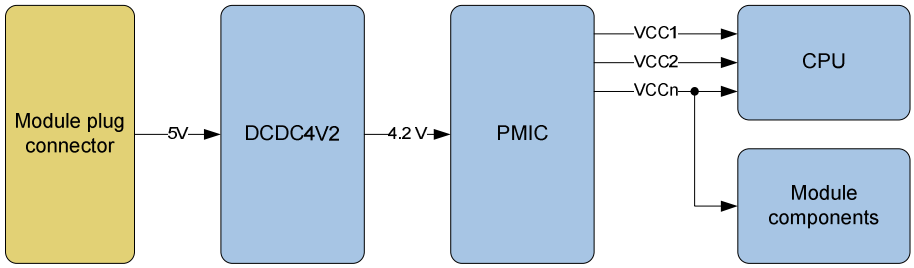



Illustration 12: Block diagram power supply

The characteristics and functions of the single pins and signals are to be taken from the data sheet of the PMIC (2) or the Reference Manual of the CPU (3), (4).

Die following illustration shows the block diagram of the PMIC signals:

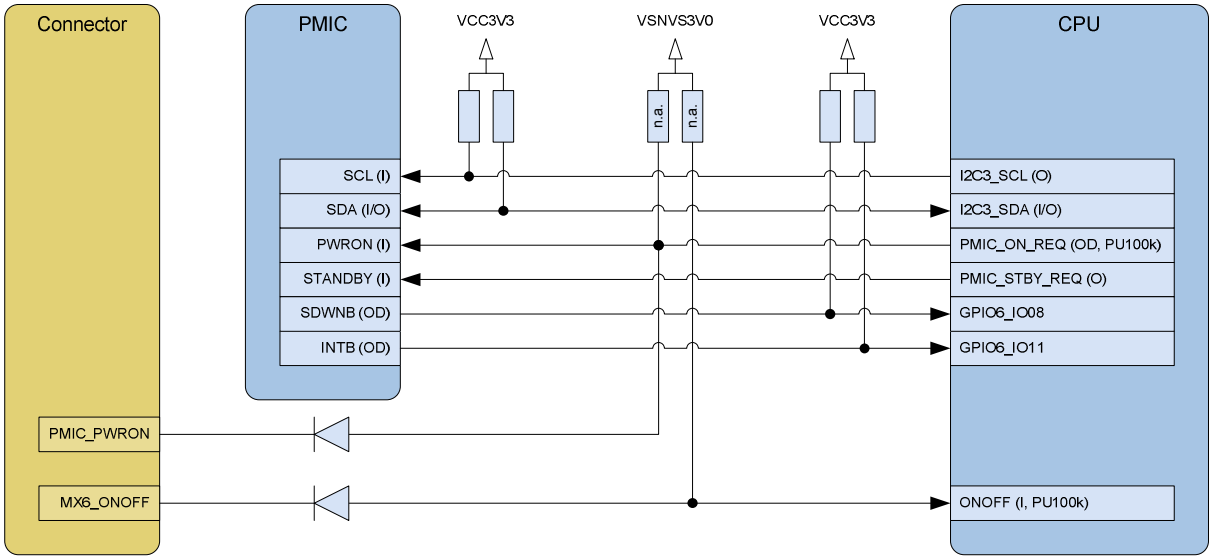



Illustration 13: Block diagram PMIC signals

#### 3.2.7.1 Power-Up sequence TQMa6x / carrier board

The TQMa6x operates with 5 V, but the 3.3 V I/O voltages of the CPU signals are generated on the TQMa6x.

This leads to requirements for the carrier board design concerning the chronological characteristics of the voltages generated on the carrier board. To ensure a correct Power-Up, the following sequence must be met on the carrier board:

The supply voltage of 5 V for the TQMa6x is present and the carrier board supply of 3.3 V is activated by the module pin VCC3V3_REF_OUT (X2–56).

The following illustration shows how VCC3V3_REF_OUT controls the voltage regulator on a carrier board.

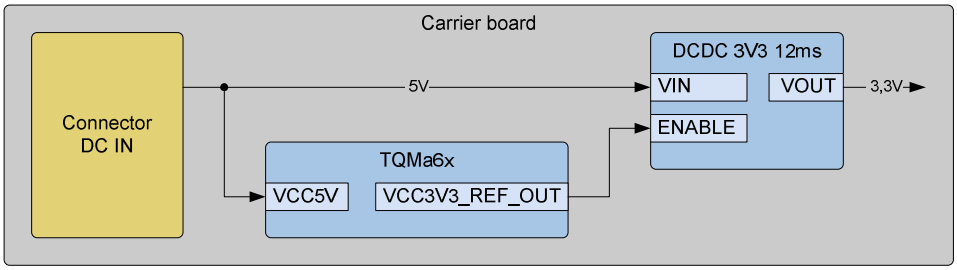



Illustration 14: Block diagram power supply carrier board

| Attention: Power-Up sequence | |
|---|---|
|  | No I/O pins of external components may be driven during the boot-process to avoid cross-supply and errors in the power-up sequence. |

#### 3.2.7.2 Power consumption

The given current consumption has to be seen as an approximate value.

The power consumption of the TQMa6x strongly depends on the application, the mode of operation and the operating system.

The following table shows technical parameters of the module supply and power consumption.

Table 51: Parameter module supply

| Module | Current @ 5 V ±5 % | Power consumption | Remark |
|---|---|---|---|
| TQMa6S | 1591 mA | ~ 7.96 W | Theoretical worst case |
| | 146 mA | ~ 0.73 W | U-Boot prompt |
| | 184 mA | ~ 0.92 W | Linux-prompt |
| | 365 mA | ~ 1.83 W | Full load (Linux stress-test application) |
| TQMa6DL | 2251 mA | ~ 11.26 W | Theoretical worst case |
| | – | – | (Not measured) |
| | – | – | (Not measured) |
| | – | – | (Not measured) |
| TQMa6D | 2221 mA | ~ 11.11 W | Theoretical worst case |
| | – | – | (Not measured) |
| | – | – | (Not measured) |
| | – | – | (Not measured) |
| TQMa6Q | 2489 mA | ~ 12.45 W | Theoretical worst case |
| | 200 mA | ~ 1.00 W | U-Boot prompt |
| | 245 mA | ~ 1.23 W | Linux-prompt |
| | 783 mA | ~ 3.92 W | Full load (Linux stress-test application) |

## 3.3 Module interface

### 3.3.1 Pin multiplexing

When using the processor signals the multiple pin configurations by different processor-internal function units must be taken note of. The pins assignment listed in Table 52, Table 53 and Table 54 refer to the corresponding standard BSP of TQ-Systems GmbH in combination with the Starterkit STK-MBa6x.

The electrical and pin characteristics are to be taken from the data sheets of CPU, (1), (3), (4) and the PMIC (2).

| Attention: Destruction or malfunction | |
|---|---|
|  | Depending on the configuration many of the CPU pins can provide several different functions.<br>Please take note of the information concerning the configuration of these pins in the<br>i.MX6 Reference Manuals (3), (4) before integration or start-up of your carrier board / Starterkit. |

### 3.3.2 Pinout connector X1

Table 52: Pinout connector X1

| Ball | I/O | Level | Group | Signal | Pin | | Pin | Signal | Group | Level | I/O | Ball |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| – | P | 5 V | POWER | VCC5V | 1 | | 2 | VCC5V | POWER | 5 V | P | – |
| – | P | 5 V | POWER | VCC5V | 3 | | 4 | VCC5V | POWER | 5 V | P | – |
| – | P | 5 V | POWER | VCC5V | 5 | | 6 | VCC5V | POWER | 5 V | P | – |
| – | P | 0 V | POWER | DGND | 7 | | 8 | DGND | POWER | 0 V | P | – |
| – | P | 0 V | POWER | DGND | 9 | | 10 | DGND | POWER | 0 V | P | – |
| – | P | 0 V | POWER | DGND | 11 | | 12 | DGND | POWER | 0 V | P | – |
| A18 | I/O | 3.3 V | GPIO | GPIO2_IO00 | 13 | | 14 | PCIE_TXM | PCIE | –[13] | O | A03 |
| C17 | I/O | 3.3 V | GPIO | GPIO2_IO01 | 15 | | 16 | PCIE_TXP | PCIE | –[13] | O | B03 |
| F16 | I/O | 3.3 V | GPIO | GPIO2_IO02 | 17 | | 18 | DGND | POWER | 0 V | P | – |
| D17 | I/O | 3.3 V | GPIO | GPIO2_IO03 | 19 | | 20 | PCIE_RXM | PCIE | –[13] | I | B01 |
| D18 | I/O | 3.3 V | GPIO | GPIO2_IO08 | 21 | | 22 | PCIE_RXP | PCIE | –[13] | I | B02 |
| A20 | I/O | 3.3 V | GPIO | GPIO2_IO11 | 23 | | 24 | DGND | POWER | 0 V | P | – |
| C15 | I/O | 3.3 V | GPIO | GPIO6_IO07 | 25 | | 26 | CLK1_N | XTAL | 2.5 V | O | C07 |
| A16 | I/O | 3.3 V | GPIO | GPIO6_IO08 | 27 | | 28 | CLK1_P | XTAL | 2.5 V | O | D07 |
| F15 | I/O | 3.3 V | GPIO | GPIO6_IO11 | 29 | | 30 | DGND | POWER | 0 V | P | – |
| C16 | I/O | 3.3 V | GPIO | GPIO6_IO14 | 31 | | 32 | USB_H1_DP | USB | –[14] | I/O | E10 |
| B19 | O | 3.3 V | PWM | PWM3 | 33 | | 34 | USB_H1_DN | USB | –[14] | I/O | F10 |
| – | P | 0 V | POWER | DGND | 35 | | 36 | DGND | POWER | 0 V | P | – |
| D10 | P | 5 V | POWER | USB_H1_VBUS | 37 | | 38 | HDMI_CLKM | HDMI | –[15] | O | J05 |
| T05 | O | 3.3 V | USB | USB_H1_PWR | 39 | | 40 | HDMI_CLKP | HDMI | –[15] | O | J06 |
| R07 | I | 3.3 V | USB | USB_H1_OC | 41 | | 42 | DGND | POWER | 0 V | P | – |
| E09 | P | 5 V | POWER | USB_OTG_VBUS | 43 | | 44 | HDMI_D0M | HDMI | –[15] | O | K05 |
| T04 | I | 3.3 V | USB | USB_OTG_ID | 45 | | 46 | HDMI_D0P | HDMI | –[15] | O | K06 |
| – | P | 0 V | POWER | DGND | 47 | | 48 | DGND | POWER | 0 V | P | – |
| A06 | I/O | –[14] | USB | USB_OTG_DP | 49 | | 50 | HDMI_D1M | HDMI | –[15] | O | J03 |
| B06 | I/O | –[14] | USB | USB_OTG_DN | 51 | | 52 | HDMI_D1P | HDMI | –[15] | O | J04 |
| – | P | 0 V | POWER | DGND | 53 | | 54 | DGND | POWER | 0 V | P | – |
| A14 | I | –[16] | SATA | SATA_RXM | 55 | | 56 | HDMI_D2M | HDMI | –[15] | O | K03 |
| B14 | I | –[16] | SATA | SATA_RXP | 57 | | 58 | HDMI_D2P | HDMI | –[15] | O | K04 |
| – | P | 0 V | POWER | DGND | 59 | | 60 | DGND | POWER | 0 V | P | – |
| B12 | O | –[16] | SATA | SATA_TXM | 61 | | 62 | HDMI_DDC_SCL | HDMI | –[15] | O | U05 |
| A12 | O | –[16] | SATA | SATA_TXP | 63 | | 64 | HDMI_DDC_SDA | HDMI | –[15] | I/O | T07 |
| – | P | 0 V | POWER | DGND | 65 | | 66 | HDMI_HPD | HDMI | –[15] | I | K01 |
| C02 | I | 3.3 V | JTAG | JTAG_TRST# | 67 | | 68 | BOOT_MODE0 | CONFIG | 3.0 V[17] | $I_{iPD}$ | C12 |
| C03 | I | 3.3 V | JTAG | JTAG_TMS | 69 | | 70 | BOOT_MODE1 | CONFIG | 3.0 V[17] | $I_{iPD}$ | F12 |
| G05 | I | 3.3 V | JTAG | JTAG_TDI | 71 | | 72 | GPIO7_IO12 | GPIO | 3.3 V | I/O | R01 |
| G06 | O | 3.3 V | JTAG | JTAG_TDO | 73 | | 74 | GPIO4_IO06 | GPIO | 3.3 V | I/O | W05 |
| H06 | $I_{PD}$ | 3.3 V | JTAG | JTAG_MOD | 75 | | 76 | VSNVS_REF_OUT | POWER | 3.0 V | P | – |
| H05 | I | 3.3 V | JTAG | JTAG_TCK | 77 | | 78 | CCM_CLKO1 | CLKO | 3.3 V | O | P04 |
| – | P | 0 V | POWER | DGND | 79 | | 80 | DGND | POWER | 0 V | P | – |

13: See PCIe 1.1/2.0 Specification.
14: See USB 2.0 Specification.
15: See HDMI 1.4 Specification.
16: See Serial ATA 3.0 Specification.
17: Use VSNVS_REF_OUT as reference voltage.

Table 43: Pinout connector X1 (continued)

| Ball | I/O | Level | Group | Signal | Pin | | Pin | Signal | Group | Level | I/O | Ball |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L01 | I | 3.3 V | UART | UART4_RX | 81 | | 82 | GPIO5_IO18 | GPIO | 3.3 V | I/O | P01 |
| M02 | O | 3.3 V | UART | UART4_TX | 83 | | 84 | GPIO5_IO21 | GPIO | 3.3 V | I/O | N02 |
| L04 | I | 3.3 V | UART | UART4_RTS# | 85 | | 86 | I2C3_SCL | I2C | 3.3 V | $O_{PU}$ | R04 |
| L03 | O | 3.3 V | UART | UART4_CTS# | 87 | | 88 | I2C3_SDA | I2C | 3.3 V | $I/O_{PU}$ | T03 |
| M05 | I | 3.3 V | UART | UART5_RX | 89 | | 90 | CAN2_RX | CAN | 3.3 V | I | V05 |
| M04 | O | 3.3 V | UART | UART5_TX | 91 | | 92 | CAN2_TX | CAN | 3.3 V | O | T06 |
| M06 | I | 3.3 V | UART | UART5_RTS# | 93 | | 94 | CAN1_RX | CAN | 3.3 V | I | W04 |
| L06 | O | 3.3 V | UART | UART5_CTS# | 95 | | 96 | CAN1_TX | CAN | 3.3 V | O | W06 |
| – | P | 0 V | POWER | DGND | 97 | | 98 | DGND | POWER | 0 V | P | – |
| M01 | I | 3.3 V | AUDIO | AUD3_RXC | 99 | | 100 | AUD3_TXC | AUDIO | 3.3 V | O | N01 |
| M03 | I | 3.3 V | AUDIO | AUD3_RXFS | 101 | | 102 | AUD3_TXFS | AUDIO | 3.3 V | O | N04 |
| N03 | I | 3.3 V | AUDIO | AUD3_RXD | 103 | | 104 | AUD3_TXD | AUDIO | 3.3 V | O | P02 |
| F17 | O | 3.3 V | PWM | PWM4 | 105 | | 106 | GPIO1_IO21 | GPIO | 3.3 V | I/O | F18 |
| N05 | O | 3.3 V | I2C | I2C1_SCL | 107 | | 108 | SPI5_MISO | SPI | 3.3 V | I | A21 |
| N06 | I/O | 3.3 V | I2C | I2C1_SDA | 109 | | 110 | SPI5_MOSI | SPI | 3.3 V | O | B21 |
| P03 | I/O | 3.3 V | GPIO | GPIO5_IO20 | 111 | | 112 | SPI5_SS0# | SPI | 3.3 V | O | C20 |
| P05 | I/O | 3.3 V | GPIO | GPIO4_IO05 | 113 | | 114 | SPI5_SCK | SPI | 3.3 V | O | D20 |
| – | P | 0 V | POWER | DGND | 115 | | 116 | DGND | POWER | 0 V | P | – |
| Y01 | O | –[18] | LVDS | LVDS1_TX0_N | 117 | | 118 | LVDS0_TX0_N | LVDS | –[18] | O | U02 |
| Y02 | O | –[18] | LVDS | LVDS1_TX0_P | 119 | | 120 | LVDS0_TX0_P | LVDS | –[18] | O | U01 |
| – | P | 0 V | POWER | DGND | 121 | | 122 | DGND | POWER | 0 V | P | – |
| AA02 | O | –[18] | LVDS | LVDS1_TX1_N | 123 | | 124 | LVDS0_TX1_N | LVDS | –[18] | O | U04 |
| AA01 | O | –[18] | LVDS | LVDS1_TX1_P | 125 | | 126 | LVDS0_TX1_P | LVDS | –[18] | O | U03 |
| – | P | 0 V | POWER | DGND | 127 | | 128 | DGND | POWER | 0 V | P | – |
| AB01 | O | –[18] | LVDS | LVDS1_TX2_N | 129 | | 130 | LVDS0_TX2_N | LVDS | –[18] | O | V02 |
| AB02 | O | –[18] | LVDS | LVDS1_TX2_P | 131 | | 132 | LVDS0_TX2_P | LVDS | –[18] | O | V01 |
| – | P | 0 V | POWER | DGND | 133 | | 134 | DGND | POWER | 0 V | P | – |
| Y03 | O | –[18] | LVDS | LVDS1_CLK_N | 135 | | 136 | LVDS0_CLK_N | LVDS | –[18] | O | V04 |
| Y04 | O | –[18] | LVDS | LVDS1_CLK_P | 137 | | 138 | LVDS0_CLK_P | LVDS | –[18] | O | V03 |
| – | P | 0 V | POWER | DGND | 139 | | 140 | DGND | POWER | 0 V | P | – |
| AA03 | O | –[18] | LVDS | LVDS1_TX3_N | 141 | | 142 | LVDS0_TX3_N | LVDS | –[18] | O | W02 |
| AA04 | O | –[18] | LVDS | LVDS1_TX3_P | 143 | | 144 | LVDS0_TX3_P | LVDS | –[18] | O | W01 |
| – | P | 0 V | POWER | DGND | 145 | | 146 | DGND | POWER | 0 V | P | – |
| T02 | O | 3.3 V | PWM | PWM1 | 147 | | 148 | GPIO7_IO13 | GPIO | 3.3 V | I/O | P06 |
| U20 | I/O | ENET[19] | GPIO | GPIO1_IO30 | 149 | | 150 | GPIO7_IO11 | GPIO | 3.3 V | I/O | R02 |
| W20 | I/O | ENET[19] | GPIO | GPIO1_IO29 | 151 | | 152 | GPIO1_IO07 | GPIO | 3.3 V | I/O | R03 |
| V21 | I/O | ENET[19] | GPIO | GPIO1_IO28 | 153 | | 154 | GPIO1_IO26 | GPIO | ENET[19] | I/O | W22 |
| U21 | I/O | ENET[19] | GPIO | GPIO1_IO25 | 155 | | 156 | SPDIF_OUT | AUDIO | ENET[19] | O | W21 |
| R05 | I/O | 3.3 V | GPIO | GPIO1_IO08 | 157 | | 158 | SPDIF_IN | AUDIO | ENET[19] | I | W23 |
| – | P | 0 V | POWER | DGND | 159 | | 160 | DGND | POWER | 0 V | P | – |

18: See LVDS Specification (ANSI EIA-644-A).
19: 2.5 V if NVCC_ENET is connected to VCC2V5_RGMII_OUT. 3.3 V if NVCC_ENET is connected to VCC3V3_REF_OUT.

### 3.3.3 Pinout connector X2

Table 53: Pinout connector X2

| Ball | I/O | Level | Group | Signal | Pin | | Signal | Group | Level | I/O | Ball |
|---|---|---|---|---|---|---|---|---|---|---|---|
| – | P | 0 V | POWER | DGND | 1 | 2 | DGND | POWER | 0 V | P | – |
| A22 | I/O | 3.3 V | SD | SD2_DAT0 | 3 | 4 | SD2_DAT1 | SD | 3.3 V | I/O | E20 |
| A23 | I/O | 3.3 V | SD | SD2_DAT2 | 5 | 6 | SD2_DAT3 | SD | 3.3 V | I/O | B22 |
| A19 | I/O | 3.3 V | SD | SD2_DAT4 | 7 | 8 | SD2_DAT5 | SD | 3.3 V | I/O | B18 |
| E17 | I/O | 3.3 V | SD | SD2_DAT6 | 9 | 10 | SD2_DAT7 | SD | 3.3 V | I/O | C18 |
| T01 | I | 3.3 V | SD | SD2_WP | 11 | 12 | SD2_CMD | SD | 3.3 V | I/O | F19 |
| C21 | O | 3.3 V | SD | SD2_CLK | 13 | 14 | SD2_CD# | SD | 3.3 V | I | R06 |
| – | P | 0 V | POWER | DGND | 15 | 16 | DGND | POWER | 0 V | P | – |
| – | P | 3.3 V | POWER | LICELL | 17 | 18 | VCC8V25_OTP | CONFIG | 8.25 V | P | – |
| – | $I_{PU}$ | 3.3 V | CONFIG | PMIC_PWRON | 19 | 20 | VCC3V3_OTP | CONFIG | 3.3 V | P | – |
| D12 | $I_{PU}$ | 3.3 V | CONFIG | MX6_ONOFF | 21 | 22 | OTP_SCL | CONFIG | 3.3 V | I | – |
| C11 | $I_{PU}$ | 3.3 V | CONFIG | MX6_POR# | 23 | 24 | OTP_SDA | CONFIG | 3.3 V | I/O | – |
| – | $O_{OD}$ | 3.3 V | CONFIG | RESET_OUT# | 25 | 26 | RFU1 | RFU | – | I | – |
| E18 | I | 3.3 V | UART | UART2_RX | 27 | 28 | UART2_RTS# | UART | 3.3 V | I | C19 |
| D19 | O | 3.3 V | UART | UART2_TX | 29 | 30 | UART2_CTS# | UART | 3.3 V | O | B20 |
| – | P | 0 V | POWER | DGND | 31 | 32 | DGND | POWER | 0 V | P | – |
| B25 | I | 2.5 V | RGMII | RGMII_RXC | 33 | 34 | RGMII_TXC | RGMII | 2.5 V | O | D21 |
| – | P | 0 V | POWER | DGND | 35 | 36 | DGND | POWER | 0 V | P | – |
| C24 | I | 2.5 V | RGMII | RGMII_RD0 | 37 | 38 | RGMII_TD0 | RGMII | 2.5 V | O | C22 |
| B23 | I | 2.5 V | RGMII | RGMII_RD1 | 39 | 40 | RGMII_TD1 | RGMII | 2.5 V | O | F20 |
| B24 | I | 2.5 V | RGMII | RGMII_RD2 | 41 | 42 | RGMII_TD2 | RGMII | 2.5 V | O | E21 |
| D23 | I | 2.5 V | RGMII | RGMII_RD3 | 43 | 44 | RGMII_TD3 | RGMII | 2.5 V | O | A24 |
| D22 | I | 2.5 V | RGMII | RGMII_RX_CTL | 45 | 46 | RGMII_TX_CTL | RGMII | 2.5 V | O | C23 |
| – | P | 0 V | POWER | DGND | 47 | 48 | DGND | POWER | 0 V | P | – |
| V20 | O | ENET[20] | MII | ENET_MDC | 49 | 50 | ENET_REFCLK | RGMII | ENET[20] | I | V22 |
| V23 | I/O | ENET[20] | MII | ENET_MDIO | 51 | 52 | DGND | POWER | 0 V | P | – |
| R19 | P | ENET[21] | POWER | NVCC_ENET | 53 | 54 | VCC2V5_RGMII_OUT | POWER | 2.5 V | P | – |
| V06 | I/O | 3.3 V | GPIO | GPIO4_IO07 | 55 | 56 | VCC3V3_REF_OUT | POWER | 3.3 V | P | – |
| U07 | I/O | 3.3 V | GPIO | GPIO4_IO08 | 57 | 58 | GPIO4_IO09 | GPIO | 3.3 V | I/O | U06 |
| E16 | I | 3.3 V | UART | UART3_RX | 59 | 60 | WDOG1# | WDOG | 3.3 V | O | E19 |
| B17 | O | 3.3 V | UART | UART3_TX | 61 | 62 | DGND | POWER | 0 V | P | – |
| F21 | I | 3.3 V | SPI | SPI1_MISO | 63 | 64 | SPI1_SCK | SPI | 3.3 V | O | C25 |
| G21 | O | 3.3 V | SPI | (SPI1_SS1#)/DNC[22] | 65 | 66 | SPI1_MOSI | SPI | 3.3 V | O | D24 |
| H20 | I | 3.3 V | USB | USB_OTG_OC | 67 | 68 | GPIO3_IO20 | GPIO | 3.3 V | I/O | G20 |
| D25 | I/O | 3.3 V | GPIO | GPIO3_IO23 | 69 | 70 | USB_OTG_PWR | USB | 3.3 V | O | E23 |
| G22 | O | 3.3 V | SPI | SPI1_SS3# | 71 | 72 | SPI1_SS2# | SPI | 3.3 V | O | F22 |
| – | P | 0 V | POWER | DGND | 73 | 74 | DGND | POWER | 0 V | P | – |
| E25 | I/O | 3.3 V | GPIO | GPIO3_IO27 | 75 | 76 | GPIO3_IO26 | GPIO | 3.3 V | I/O | E24 |
| J19 | I/O | 3.3 V | GPIO | GPIO3_IO29 | 77 | 78 | GPIO3_IO28 | GPIO | 3.3 V | I/O | G23 |
| H21 | I | 3.3 V | UART | UART3_RTS# | 79 | 80 | UART3_CTS# | UART | 3.3 V | O | J20 |

20: 2.5 V if NVCC_ENET is connected to VCC2V5_RGMII_OUT. 3.3 V if NVCC_ENET is connected to VCC3V3_REF_OUT.
21: 2.5 V if connected to VCC2V5_RGMII_OUT on carrier board. 3.3 V if connected to VCC3V3_REF_OUT on carrier board.
22: DNC if SPI NOR flash is assembled.

Table 44: Pinout connector X2 (continued)

| Ball | I/O | Level | Group | Signal | Pin | | Pin | Signal | Group | Level | I/O | Ball |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| J24 | I/O | 3.3 V | GPIO | GPIO2_IO25 | 81 | | 82 | CCM_CLKO2 | CCM | 3.3 V | O | A17 |
| J23 | I/O | 3.3 V | GPIO | GPIO2_IO24 | 83 | | 84 | GPIO2_IO23 | GPIO | 3.3 V | I/O | H24 |
| F23 | I | 3.3 V[23] | BOOT | BOOT_CFG4_7 | 85 | | 86 | BOOT_CFG4_6 | BOOT | 3.3 V[23] | I | E22 |
| – | P | 0 V | POWER | DGND | 87 | | 88 | DGND | POWER | 0 V | P | – |
| K20 | I | 3.3 V[23] | BOOT | BOOT_CFG4_5 | 89 | | 90 | BOOT_CFG4_4 | BOOT | 3.3 V[23] | I | K23 |
| K21 | I | 3.3 V[23] | BOOT | BOOT_CFG4_3 | 91 | | 92 | BOOT_CFG4_2 | BOOT | 3.3 V[23] | I | K22 |
| M25 | I | 3.3 V[23] | BOOT | BOOT_CFG4_1 | 93 | | 94 | GPIO6_IO16 | GPIO | 3.3 V | I/O | D16 |
| H19 | I/O | 3.3 V | HDMI | HDMI_CEC_LINE | 95 | | 96 | BOOT_CFG4_0 | BOOT | 3.3 V[23] | I | F25 |
| J21 | I | 3.3 V[23] | BOOT | BOOT_CFG3_7 | 97 | | 98 | BOOT_CFG3_6 | BOOT | 3.3 V[23] | I | F24 |
| H23 | I | 3.3 V[23] | BOOT | BOOT_CFG3_5 | 99 | | 100 | BOOT_CFG3_4 | BOOT | 3.3 V[23] | I | H22 |
| G25 | I | 3.3 V[23] | BOOT | BOOT_CFG3_3 | 101 | | 102 | BOOT_CFG3_2 | BOOT | 3.3 V[23] | I | J22 |
| G24 | I | 3.3 V[23] | BOOT | BOOT_CFG3_1 | 103 | | 104 | BOOT_CFG3_0 | BOOT | 3.3 V[23] | I | H25 |
| – | P | 0 V | POWER | DGND | 105 | | 106 | DGND | POWER | 0 V | P | – |
| N24 | I | 3.3 V[23] | BOOT | BOOT_CFG2_7 | 107 | | 108 | BOOT_CFG2_6 | BOOT | 3.3 V[23] | I | N23 |
| M23 | I | 3.3 V[23] | BOOT | BOOT_CFG2_5 | 109 | | 110 | BOOT_CFG2_4 | BOOT | 3.3 V[23] | I | M24 |
| M20 | I | 3.3 V[23] | BOOT | BOOT_CFG2_3 | 111 | | 112 | BOOT_CFG2_2 | BOOT | 3.3 V[23] | I | M22 |
| M21 | I | 3.3 V[23] | BOOT | BOOT_CFG2_1 | 113 | | 114 | BOOT_CFG2_0 | BOOT | 3.3 V[23] | I | L24 |
| L25 | I | 3.3 V[23] | BOOT | BOOT_CFG1_7 | 115 | | 116 | BOOT_CFG1_6 | BOOT | 3.3 V[23] | I | K25 |
| L23 | I | 3.3 V[23] | BOOT | BOOT_CFG1_5 | 117 | | 118 | BOOT_CFG1_4 | BOOT | 3.3 V[23] | I | L22 |
| K24 | I | 3.3 V[23] | BOOT | BOOT_CFG1_3 | 119 | | 120 | BOOT_CFG1_2 | BOOT | 3.3 V[23] | I | L21 |
| J25 | I | 3.3 V[23] | BOOT | BOOT_CFG1_1 | 121 | | 122 | BOOT_CFG1_0 | BOOT | 3.3 V[23] | I | L20 |
| – | P | 0 V | POWER | DGND | 123 | | 124 | DGND | POWER | 0 V | P | – |
| N19 | O | 3.3 V | DISP | DISP0_CLK | 125 | | 126 | GPIO6_IO31 | GPIO | 3.3 V | I/O | N22 |
| N21 | O | 3.3 V | DISP | DISP0_DRDY | 127 | | 128 | DISP0_HSYNC | DISP | 3.3 V | O | N25 |
| P25 | O | 3.3 V | DISP | DISP0_CONTRAST | 129 | | 130 | DISP0_VSYNC | DISP | 3.3 V | O | N20 |
| – | P | 0 V | POWER | DGND | 131 | | 132 | DGND | POWER | 0 V | P | – |
| P24 | O | 3.3 V | DISP | DISP0_DAT0 | 133 | | 134 | DISP0_DAT1 | DISP | 3.3 V | O | P22 |
| P23 | O | 3.3 V | DISP | DISP0_DAT2 | 135 | | 136 | DISP0_DAT3 | DISP | 3.3 V | O | P21 |
| P20 | O | 3.3 V | DISP | DISP0_DAT4 | 137 | | 138 | DISP0_DAT5 | DISP | 3.3 V | O | R25 |
| R23 | O | 3.3 V | DISP | DISP0_DAT6 | 139 | | 140 | DISP0_DAT7 | DISP | 3.3 V | O | R24 |
| R22 | O | 3.3 V | DISP | DISP0_DAT8 | 141 | | 142 | DISP0_DAT9 | DISP | 3.3 V | O | T25 |
| R21 | O | 3.3 V | DISP | DISP0_DAT10 | 143 | | 144 | DISP0_DAT11 | DISP | 3.3 V | O | T23 |
| – | P | 0 V | POWER | DGND | 145 | | 146 | DGND | POWER | 0 V | P | – |
| T24 | O | 3.3 V | DISP | DISP0_DAT12 | 147 | | 148 | DISP0_DAT13 | DISP | 3.3 V | O | R20 |
| U25 | O | 3.3 V | DISP | DISP0_DAT14 | 149 | | 150 | DISP0_DAT15 | DISP | 3.3 V | O | T22 |
| T21 | O | 3.3 V | DISP | DISP0_DAT16 | 151 | | 152 | DISP0_DAT17 | DISP | 3.3 V | O | U24 |
| V25 | O | 3.3 V | DISP | DISP0_DAT18 | 153 | | 154 | DISP0_DAT19 | DISP | 3.3 V | O | U23 |
| U22 | O | 3.3 V | DISP | DISP0_DAT20 | 155 | | 156 | DISP0_DAT21 | DISP | 3.3 V | O | T20 |
| V24 | O | 3.3 V | DISP | DISP0_DAT22 | 157 | | 158 | DISP0_DAT23 | DISP | 3.3 V | O | W24 |
| – | P | 0 V | POWER | DGND | 159 | | 160 | DGND | POWER | 0 V | P | – |

23: Use VCC3V3_REF_OUT as reference voltage for BOOT-CFG resistors.

### 3.3.4 Pinout connector X3

Table 54: Pinout connector X3

| Ball | I/O | Level | Group | Signal | Pin | | Signal | Group | Level | I/O | Ball |
|---|---|---|---|---|---|---|---|---|---|---|---|
| – | P | 0 V | POWER | DGND | 1 | 2 | DGND | POWER | 0 V | P | – |
| F04 | I | –[24] | MIPI-CSI | CSI_CLK0M | 3 | 4 | MLB_CN | MLB | –[24] | O | A11 |
| F03 | I | –[24] | MIPI-CSI | CSI_CLK0P | 5 | 6 | MLB_CP | MLB | –[24] | O | B11 |
| – | P | 0 V | POWER | DGND | 7 | 8 | DGND | POWER | 0 V | P | – |
| E04 | I | –[24] | MIPI-CSI | CSI_D0M | 9 | 10 | MLB_DN | MLB | –[24] | I/O | B10 |
| E03 | I | –[24] | MIPI-CSI | CSI_D0P | 11 | 12 | MLB_DP | MLB | –[24] | I/O | A10 |
| – | P | 0 V | POWER | DGND | 13 | 14 | DGND | POWER | 0 V | P | – |
| D01 | I | –[24] | MIPI-CSI | CSI_D1M | 15 | 16 | MLB_SN | MLB | –[24] | I/O | A09 |
| D02 | I | –[24] | MIPI-CSI | CSI_D1P | 17 | 18 | MLB_SP | MLB | –[24] | I/O | B09 |
| – | P | 0 V | POWER | DGND | 19 | 20 | DGND | POWER | 0 V | P | – |
| E01 | I | –[24] | MIPI-CSI | CSI_D2M | 21 | 22 | DSI_CLK0M | MIPI-DSI | –[24] | O | H03 |
| E02 | I | –[24] | MIPI-CSI | CSI_D2P | 23 | 24 | DSI_CLK0P | MIPI-DSI | –[24] | O | H04 |
| – | P | 0 V | POWER | DGND | 25 | 26 | DGND | POWER | 0 V | P | – |
| F02 | I | –[24] | MIPI-CSI | CSI_D3M | 27 | 28 | DSI_D0M | MIPI-DSI | –[24] | O | G02 |
| F01 | I | –[24] | MIPI-CSI | CSI_D3P | 29 | 30 | DSI_D0P | MIPI-DSI | –[24] | O | G01 |
| – | P | 0 V | POWER | DGND | 31 | 32 | DGND | POWER | 0 V | P | – |
| C05 | O | 2.5 V | XTAL | CLK2_N | 33 | 34 | DSI_D1M | MIPI-DSI | –[24] | I | H02 |
| D05 | O | 2.5 V | XTAL | CLK2_P | 35 | 36 | DSI_D1P | MIPI-DSI | –[24] | I | H01 |
| – | P | 0 V | POWER | DGND | 37 | 38 | DGND | POWER | 0 V | P | – |
| E11 | I | 3.0 V[25] | CONFIG | TAMPER | 39 | 40 | SPI NOR_WP# | CONFIG | 3.3 V | I | – |

24: See datasheets of i.MX6 (3), (4).
25: Use VSNVS_REF_OUT as reference voltage.

# 4. MECHANICS

## 4.1 Connectors

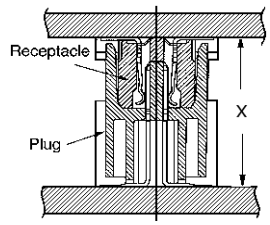
The TQMa6x is connected to the carrier board with 360 pins on three connectors.
The following table shows details of the plug connector used.

Table 55: Plug connectors on the TQMa6x

| Manufacturer | Part number | Remark |
|---|---|---|
| TE connectivity | 160-pin: 5177985-8 | • 0.8 mm pitch<br>• Plating: Gold 0.2 µm<br>• –40 °C to 125 °C |
| TE connectivity | 40-pin: 5177985-1 | • 0.8 mm pitch<br>• Plating: Gold 0.2 µm<br>• –40 °C to 125 °C |

The TQMa6x is held in the plug connectors with a considerable retention force.
To avoid damaging the plug connectors of the TQMa6x as well as the carrier board plug connectors while removing the TQMa6x the use of an extraction tool is strongly recommended. See section 4.8 for further information.
The following table shows some suitable mating plug connectors for the carrier board.

Table 56: Suitable carrier board mating plug connectors

| Manufacturer | Part number | Stack height (X) | |
|---|---|---|---|
| TE connectivity | 40-pin: 5177986-1<br>160-pin: 5177986-8 | 5 mm |  |
| TE connectivity | 40-pin: 1-5177986-1<br>160-pin: 2-5179230-8 | 6 mm | |
| TE connectivity | 40-pin: 2-5177986-1<br>160-pin: 5179030-8 | 7 mm | |
| TE connectivity | 40-pin: 3-5177986-1<br>160-pin: 3-5177986-8 | 8 mm | |

## 4.2 Dimensions

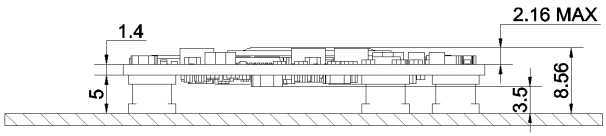



Illustration 15: Height of TQMa6x Rev. 0100 … Rev. 0104

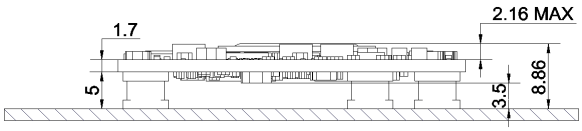



Illustration 16: Height of TQMa6x Rev. 0105

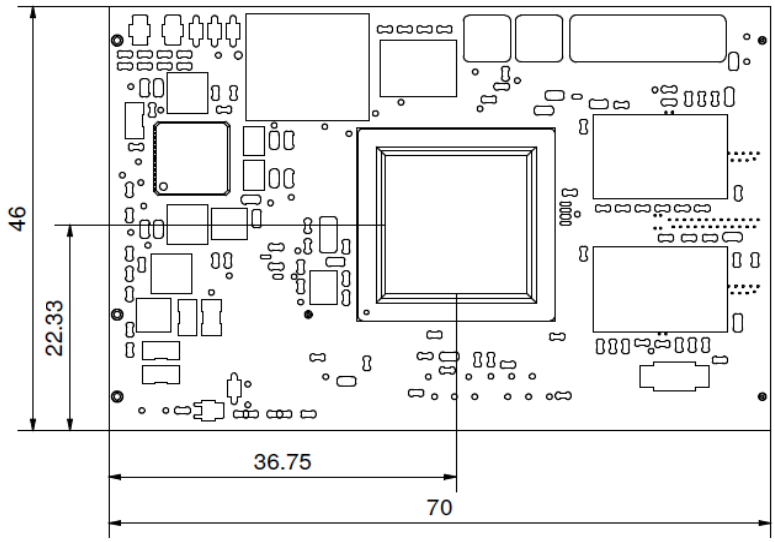



Illustration 17: Overall dimensions (top view)

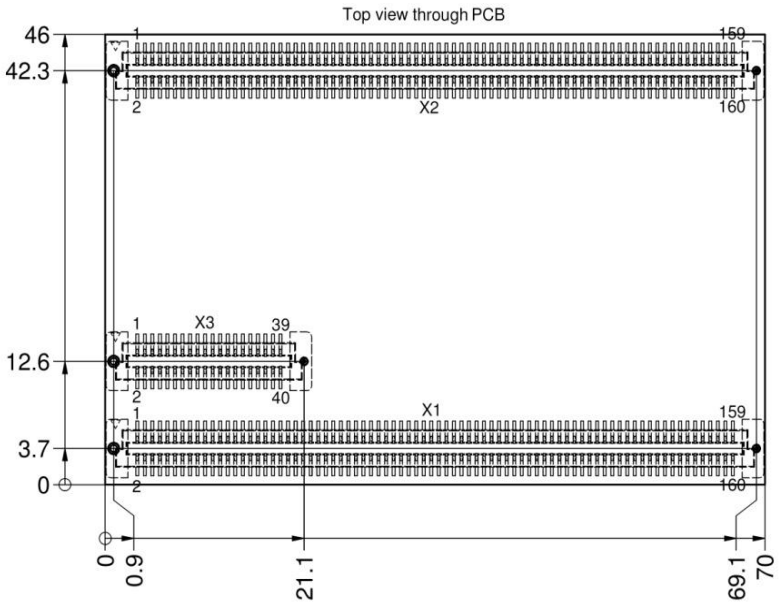



Illustration 18: Top view through PCB

## 4.3 Component placement

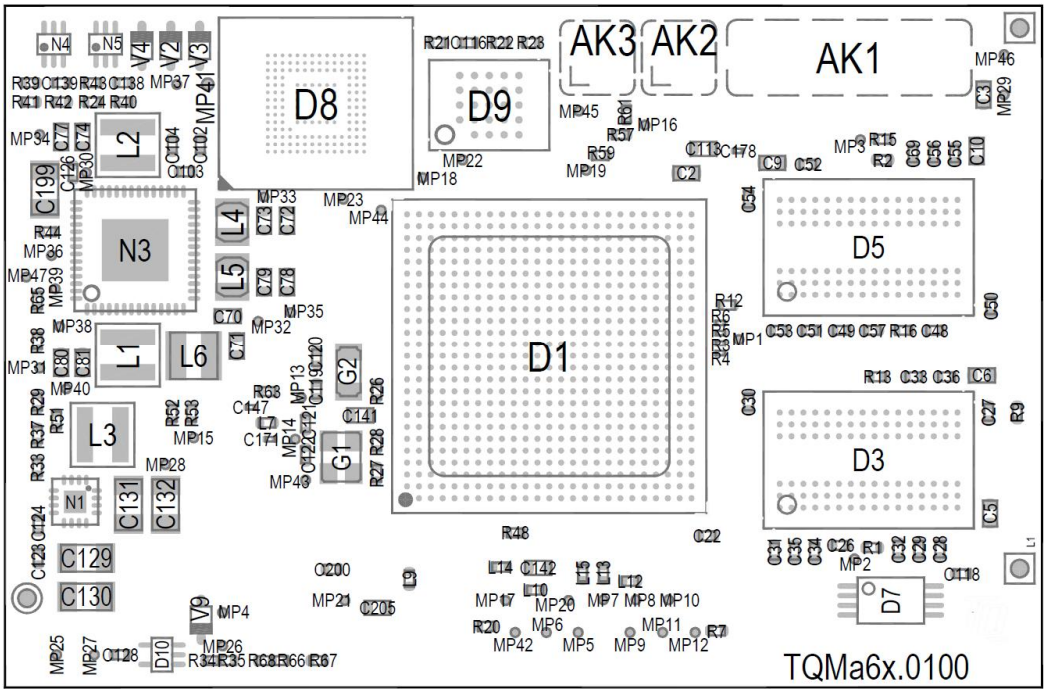



Illustration 19: Component placement top

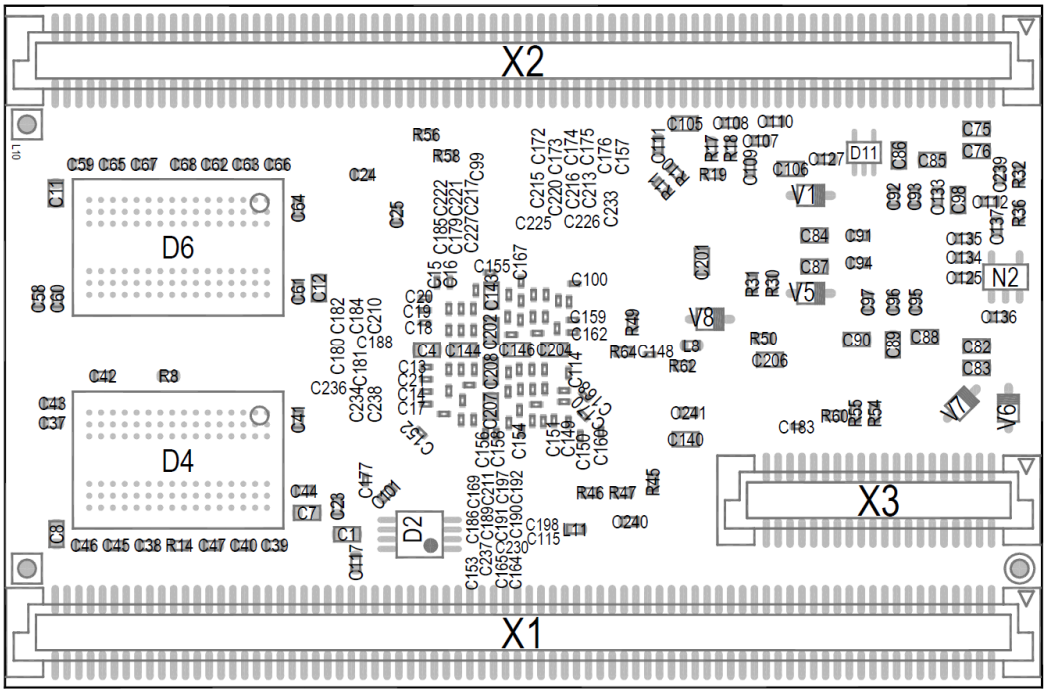



Illustration 20: Component placement bottom

### 4.4 Adaptation to the environment

The overall dimensions (length × width × height) of the TQMa6x are 70 × 46 × 7.1 mm³.
The maximum height of the TQMa6x above the carrier board is approximately 8.5 mm.

### 4.5 Protection against external effects

As an embedded module the TQMa6x is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

### 4.6 Thermal management

To cool the TQMa6x, a maximum of approximately 12.5 W have to be dissipated, see also section 3.2.7.2.
The power dissipation originates primarily in the processor, the DDR3L SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See Freescale Application Notes (8) / (9) / (10) for further information.

| Attention: Destruction or malfunction | |
|---|---|
|  | The CPU belongs to a performance category in which a cooling system may be essential in certain applications. It is the responsibility of the customer to define a suitable cooling method depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). |

### 4.7 Structural requirements

The TQMa6x is held in the mating plug connectors by the retention force of the pins (a total of 360). For high requirements with respect to vibration and shock firmness an additional holder has to be provided in the final product to hold the TQMa6x in its position. For this purpose TQ-Systems GmbH can provide a suitable solution. As no heavy and big components are used, no further requirements are given.

### 4.8 Notes of treatment

To avoid damage caused by mechanical stress, the TQMa6x may only be extracted from the carrier board by using the extraction tool MOZI8XXL that can also be obtained separately.

| Attention: Note with respect to the component placement of the carrier board | |
|---|---|
|  | 2.5 mm should be kept free on the carrier board, along the longitudinal edges on both sides of the TQMa6x for the extraction tool. |

## 5. SOFTWARE

The TQMa6x is delivered with a preinstalled boot loader and a BSP which is configured for the Starterkit STK-MBa6x.
The boot loader provides module-specific as well as board-specific settings, e.g.:

- CPU configuration
- PMIC configuration
- RAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

More information can be found in the Support Wiki for the TQMa6x.

# 6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

## 6.1 EMC

The TQMa6x was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short;
  avoid interference of other signals by distance and / or shielding besides,
  take note of not only the frequency, but also the signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

Because the TQMa6x is used on an application-specific carrier board, EMC or ESD tests only make sense for the whole device.
The TQMa6x it designed to pass the following test:

- EMC-Interference radiation:
  Measurement of the electrically radiated emission for standard, residential, commercial and light industrial environments in the range of 30 MHz to 6 GHz according to DIN EN 55022 A1:2007.

## 6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa6x.
Following measures are recommended for a carrier board:

- Generally applicable: Shielding of the inputs
  (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, perhaps Zener diode(s)
- Fast signal lines: Integrated protective devices (e.g., suppressor diode arrays)

## 6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety haven't been carried out.

## 6.4 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection), hence, no fixed value can be given for the whole assembly.

In general, a reliable operation is given when following conditions are met:

Table 57: Climate and operational conditions extended temperature range –25 … 85 °C

| Parameter | Range | Remark |
|---|---|---|
| Chip temperature CPU i.MX6x | –40 … 105 °C | Typ. max 90 °C |
| Environment temperature CPU i.MX6x | –40 … 85 °C | – |
| Chip temperature PMIC | –40 … 125 °C | – |
| Environment temperature PMIC | –40 … 85 °C | – |
| Package temperature DDR3L-RAM | –40 … 85 °C | – |
| Package temperature other ICs | –25 … 85 °C | – |
| Permitted storage temperature TQMa6x | –40 … 85 °C | – |
| Relative humidity (operating / storage) | 10 … 90 % | Not condensing |

Table 58: Climate and operational conditions industrial temperature range –40 … 85 °C

| Parameter | Range | Remark |
|---|---|---|
| Chip temperature CPU i.MX6x | –40 °C … 105 °C | Typ. max 90 °C |
| Environment temperature CPU i.MX6x | –40 °C … 85 °C | – |
| Chip temperature PMIC | –40 °C … 125 °C | – |
| Environment temperature PMIC | –40 °C … 85 °C | – |
| Package temperature DDR3L-RAM | –40 °C … 85 °C | – |
| Package temperature other ICs | –40 °C … 85 °C | – |
| Permitted storage temperature TQMa6x | –40 °C … 85 °C | – |
| Relative humidity (operating / storage) | 10 % … 90 % | Not condensing |

Detailed information concerning the thermal characteristics of the CPU is to be taken from the Freescale data sheets (3) and (4).

## 6.5 Reliability and service life

No detailed MTBF calculation has been done for the TQMa6x.

The TQMa6x is designed to be insensitive to vibration and impact.

Middle grade connectors, which guarantee at least 100 mating cycles, were used for the TQMa6x.

Detailed information concerning the service life of the CPU under different operational conditions is to be taken from the Freescale Application Notes (11) and (12).

## 6.6 Environment protection

### 6.6.1 RoHS compliance

The TQMa6x is manufactured RoHS compliant.

- All used components and assemblies are RoHS compliant
- RoHS compliant soldering processes are used

### 6.6.2 WEEE regulation

The company placing the product on the market is responsible for the observance of the WEEE regulation.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

## 6.7 Batteries

No batteries are used on the TQMa6x.

## 6.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.

The energy consumption of this subassembly is minimised by suitable measures.

Printed PC-boards are delivered in reusable packaging.

Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.

Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

# 7. APPENDIX

## 7.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 59: Acronyms

| Acronym | Meaning |
|---|---|
| ADC | Analog/Digital Converter |
| ARM® | Advanced RISC Machine |
| ASCII | American Standard Code for Information Interchange |
| ATA | Advanced Technology Attachment |
| BIOS | Basic Input/Output System |
| BSP | Board Support Package |
| CAN | Controller Area Network |
| CCM | Clock Control Module |
| CPU | Central Processing Unit |
| CSI | Camera Serial Interface |
| CSPI | Configurable SPI |
| DDR | Double Data Rate |
| DDR3L | DDR3 Low Voltage |
| DIN | Deutsche Industrie Norm |
| DNC | Do Not Connect |
| DSI | Display Serial Interface |
| ECSPI | Enhanced Configurable SPI |
| EEPROM | Electrically Erasable Programmable Read-only Memory |
| EIM | External Interface Module |
| EMC | Electro-Magnetic Compatibility |
| eMMC | embedded Multi-Media Card |
| EN | Europäische Norm |
| EPIT | Enhanced Periodic Interrupt Timer |
| ESAI | Enhanced Serial Audio Interface |
| ESD | Electro-Static Discharge |
| FR4 | Flame Retardant-4 |
| GbE | Gigabit Ethernet |
| Gbps | Gigabit per second |
| GPIO | General Purpose Input/Output |
| GPMI | General Purpose Media Interface |
| GPT | General Purpose Timer |
| HDMI | High Definition Multimedia Interface |
| HRCW | Hard Reset Configuration Word |
| HSI | High-Speed Interface |
| I/O | Input Output |
| IEEE® | Institute of Electrical and Electronics Engineers |
| IP | Ingress Protection |
| IPD | Internal Pull-Down |
| IPU | Internal Pull-Up |
| $I^2C$ | Inter-Integrated Circuit |
| $I^2S$ | Inter-Integrated Sound |
| JTAG | Joint Test Action Group |
| LDB | LVDS Display Bridge |
| LICELL | Lithium Cell |
| LVDS | Low Voltage Differential Signal |

Table 48: Acronyms (continued)

| Acronym | Meaning |
|---|---|
| MAC | Media Access Control |
| MII | Media Independent Interface |
| MIPI | Mobile Industry Processor Interface |
| MISO | Master In Slave Out |
| MLB | Media-Local-Bus |
| MMC | Multimedia Card |
| MMU | Memory Management Unit |
| MOSI | Master Out Slave In |
| MOZI | Module extractor (Modulzieher) |
| MTBF | Mean operating Time Between Failures |
| NAND | Not-And |
| NOR | Not-Or |
| OD | Open-Drain |
| OTG | On-The-Go |
| OTP | One-Time Programmable |
| PCB | Printed Circuit Board |
| PCIE | Peripheral Component Interconnect express |
| PCMCIA | People Cant Memorize Computer Industries Acronyms |
| PD | Pull-Down |
| PMIC | Power Management Integrated Circuit |
| PU | Pull-Up |
| PWM | Pulse-Width Modulation |
| RAM | Random Access Memory |
| RF | Radio Frequency |
| RFU | Reserved for Future Use |
| RGB | Red, Green, Blue |
| RGMII | Reduced Gigabit Media Independent Interface |
| RMII | Reduced Media Independent Interface |
| RoHS | Restriction of (the use of certain) Hazardous Substances |
| ROM | Read-Only Memory |
| RTC | Real-Time Clock |
| SATA | Serial ATA |
| SD | Secure Digital |
| SDIO | Secure Digital Input/Output |
| SDRAM | Synchronous Dynamic Random Access Memory |
| SDXC | SD eXtended Capacity |
| SJC | System JTAG Controller |
| SNVS | Secure Non-Volatile Storage |
| SPDIF | Sony-Philips Digital Interface Format |
| SPI | Serial Peripheral Interface |
| SSI | Synchronous Serial Interface |
| SW | Software |
| UART | Universal Asynchronous Receiver Transmitter |
| UM | User's Manual |
| USB | Universal Serial Bus |
| uSDHC | Ultra Secured Digital Host Controller |
| VSNVS | Voltage (for) Secure Non-Volatile Storage |
| WDOG | Watchdog |
| WEEE® | Waste Electrical and Electronic Equipment |

## 7.2 References

Table 60: Further applicable documents

| No. | Name | Rev. / Date | Company |
|---|---|---|---|
| (1) | IMX6DQIEC, i.MX Dual / Quad Applications Processors for Industrial Products | Rev. 3, 03/2014 | Freescale |
| (2) | MMPF0100, 14 Channel Configurable Power Management Integrated Circuit | Rev. 9, 07/2014 | Freescale |
| (3) | IMX6DQRM, i.MX6 Dual / Quad Applications Processor Reference Manual | Rev. 2, 06/2014 | Freescale |
| (4) | IMX6SDLRM i.MX6 Solo / DualLite Applications Processor Reference Manual | Rev. 1, 04/2013 | Freescale |
| (5) | IMX6DQCE, Chip Errata for the i.MX6 Dual / Quad | Rev. 4, 07/2014 | Freescale |
| (6) | IMX6SDLCE, Chip Errata for the i.MX6Solo / DualLite | Rev. 5, 12/2014 | Freescale |
| (7) | IMX6SDLIEC, Data Sheet i.MX6Solo / DualLite Applications Processors for Industrial Products | Rev. 4, 12/2014 | Freescale |
| (8) | AN4509, i.MX6Dual / Quad Power Consumption Measurement | Rev. 0, 09/2012 | Freescale |
| (9) | AN4576, i.MX6 DualLite Power Consumption Measurement | Rev. 1, 03/2013 | Freescale |
| (10) | AN4579, i.MX6 Series Thermal Management Guidelines | Rev. 0, 11/2012 | Freescale |
| (11) | AN4724, Application Note i.MX6 Dual / Quad Product Usage Lifetime Estimates | Rev. 2, 07/2014 | Freescale |
| (12) | AN4725, Application Note i.MX6Solo / DualLite Product Usage Lifetime Estimates | Rev. 1, 12/2014 | Freescale |

**TQ-Systems GmbH**
Mühlstraße 2 I Gut Delling I 82229 Seefeld
info@tq-group.com I www.tq-group.com

Technology in Quality