COM Express™ conga-TM67/TS67

2nd Generation Intel® Core™ i7, i5, i3 or Celeron® processor with an Intel® 6 Series QM67 or HM65 chipset

User's Guide

Revision 1.2

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2012.07.13	AEM	• Preliminary release
1.0	2012.12.07	AEM	• Corrected and updated the power consumption tables in section 1.6 “Power Consumption”. • Changed maximum torque rating for heatspreader screws in section 3.1 “Heatspreader Dimensions” and added a caution statement. • Updated section 4.1.12 “Power Control”. • Added statement about the optionally use of the PEG interface for connecting a x1, x2, x4, or x8 non-graphic PCI Express device in section 4.2.2 “PCI Express Graphics(PEG)”. • Deleted the note in section 4.2.4 “HDMI”, section 4.2.5 “DisplayPort” and section 7.5 “Boot Strap Signals” which made reference to the application note AN17_HDMI_DP_Implementation.pdf because the referred application note applies to COM Express Type 2 designs only. • Added note about Watchdog NMI mode not being supported to sections 5.3 “Watchdog” and 9.4.2 “Watchdog Configuration Submenu”. • Added note to “Gigabit Ethernet Signal Descriptions” table in section 7. • Corrected the note in section 8.5 “PCI Interrupt Routing Map“. • Deleted the menu bar chipset column and the F7 key option in section 9.2 “Setup Menu and Navigation“. • Deleted the power column in section 9.4 “Advanced Setup“. • Changed the BIOS Save Options feature in section 9.6.3 “Save & Exit Menu” from “Load CMOS Defaults“ to “Restore Defaults“. • Official release
1.1	2013.01.07	AEM	• Added Microsoft Windows 8 support in section 1.2 “Supported Operating System“ • Corrected the peak power consumption of the Intel® 2610UE processor from 90W to 30W in section 1.6.6. • Added the Intel® Celeron® B810E processor to conga-TS67 variants in “Options Information” and in section 1.6 “Power Consumption”.
1.2	2013.05.07	AEM	• Added section 1 “Introduction”. Moved COM Express™ Concept and “Options Information” to section 1 “Introduction”. • Added section 5 “Onboard Sensors”. • Updated section 6.2.2 “PCI Express Graphics (PEG)”. • Deleted the comment “Connect to CB_RESET#” for express card reset signals in table 7. • Deleted the wake event signal “PME#” from section 8.5 “ACPI Suspend Modes and Resume Events” because this signal is not supported in COM Express type 6 specification. • Updated section 11 “BIOS Setup Description”. Added section 12.1 “Supported Flash Devices”.

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-TM67/TS67. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide

COM Express™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHz	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PEG	PCI Express Graphics
PCH	Platform Controller Hub
PATA	Parallel ATA
T.O.M.	Top of memory = max. DRAM installed
HDA	High Definition Audio
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

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1 INTRODUCTION

COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation provides the ability to make a smooth transition from legacy interfaces to the newest technologies available today. COM Express™ modules are available in following form factors:

- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x 110mm

The COM Express™ specification 2.0 defines seven different pinout types.

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports
Type 1	A-B	Up to 6			1
Type 2	A-B C-D	Up to 22	32 bit	1	1
Type 3	A-B C-D	Up to 22	32 bit		3
Type 4	A-B C-D	Up to 32		1	1
Type 5	A-B C-D	Up to 32			3
Type 6	A-B C-D	Up to 24			1
Type 10	A-B	Up to 4			1

conga-TM67/TS67 modules utilize the Type 6 pinout definition. They are equipped with two high performance connectors that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are a legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 6 pinout provides the ability to offer PCI Express, Serial ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

conga-TM67/TS67 Options Information

The conga-TM67 is available in four variants and the conga-TS67 is available in seven variants. This user's guide describes all of these variants. The tables below show the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

conga-TM67

Part-No.	046301	046302	046303	046304
Processor	Intel® Core™ i7-2710QE 2.1 GHz	Intel® Core™ i5-2510E 2.5 GHz	Intel® Core™ i3-2330E 2.2 GHz	Intel® Celeron® B810 1.6 GHz 2 Core™
Intel® Smart Cache	6 MByte	3 MByte	3 MByte	2 MByte
PEG	Yes	Yes	Yes	Yes
SDVO	1 Port	1 Port	1 Port	1 Port
DisplayPort (DP)	Yes	Yes	Yes	Yes
HDMI	Yes	Yes	Yes	Yes
Processor TDP	45 W	35 W	35 W	35 W

conga-TS67

Part-No.	046401	046402	046403	046404	046405	046406
Processor	Intel® Core™ i7-2655LE 2.2 GHz	Intel® Core™ i7-2610UE 1.5 GHz	Intel® Core™ i3-2340UE 1.3 GHz	Intel® Celeron® 847E 1.1 GHz 2 Core™	Intel® Celeron® 827E 1.4 GHz 1 Core™	Intel® Celeron® 807UE 1.0 GHz 1 Core™
Intel® Smart Cache	4 MByte	4 MByte	3 MByte	2 MByte	1.5 MByte	1.0 MByte
PEG	Yes	Yes	Yes	Yes	Yes	No
SDVO	1 Port	1 Port	1 Port	1 Port	1 Port	1 Port
DisplayPort (DP)	Yes	Yes	Yes	Yes	Yes	Yes
HDMI	Yes	Yes	Yes	Yes	Yes	Yes
Processor TDP	25 W	17 W	17 W	17 W	17 W	10 W

Part-No.	046407
Processor	Intel® Celeron® B810E 1.6 GHz 2 Core™
Intel® Smart Cache	2 MByte
PEG	Yes
SDVO	1 Port
DisplayPort (DP)	Yes
HDMI	Yes
Processor TDP	35W

2 Specifications

2.1 Feature List

Table 1 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 6 (Basic size 95 x 125mm)
Processor	**conga-TM67:** Intel® Core™ i7-2710QE 2.1 GHz with 6-MByte Intel® Smart Cache (Socketed rPGA989) **conga-TM67:** Intel® Core™ i5-2510E 2.5 GHz 3-MByte Intel® Smart Cache (Socketed rPGA989) **conga-TM67:** Intel® Core™ i3-2330E 2.2 GHz 3-MByte Intel® Smart Cache (Socketed rPGA989) **conga-TM67:** Intel® Celeron® B810 1.6 GHz 2 Core™ with 2-MByte Intel® Smart Cache (Socketed rPGA989) **conga-TS67:** Intel® Core™ i7-2655LE 2.2 GHz with 4-MByte Intel® Smart Cache **conga-TS67:** Intel® Core™ i7-2610UE 1.5 GHz with 4-MByte Intel® Smart Cache **conga-TS67:** Intel® Core™ i3-2340UE 1.3 GHz with 3-MByte Intel® Smart Cache **conga-TS67:** Intel® Celeron® 847E 1.1 GHz 2 Core™ with 2-MByte Intel® Smart Cache **conga-TS67:** Intel® Celeron® 827E 1.4 GHz 1 Core™ with 1.5-MByte Intel® Smart Cache **conga-TS67:** Intel® Celeron® 807UE 1.0 GHz 1 Core™ with 1-MByte Intel® Smart Cache **conga-TS67:** Intel® Celeron® B810E 1.6 GHz 2 Core™ with 2-MByte Intel® Smart Cache
Memory	2 sockets: SO-DIMM DDR3 1333MHz up to 16-GByte. Sockets located top and bottom side of module.
Chipset	Intel® 6 Series Chipset: Intel® BD82QM67 PCH (BD82HM65 for Celeron® equipped modules)
Audio	HDA (High Definition Audio)/digital audio interface with support for multiple codecs
Ethernet	Gigabit Ethernet: Integrated within the Intel® QM67 (HM65) + Intel® 82579LM Phy.
Graphics Options	Intel® Flexible Display Interface (FDI), Intel® Dynamic Video Memory Technology (Intel® DVMT) OpenGL 3.0 and DirectX10.1 support. Two independent pipelines for full dual view support.

	• CRT Interface 340.4 MHz RAMDAC. Resolutions up to 2048x1536 @ 75Hz (QXGA)
	• Flat panel Interface (integrated) with 25-112MHz single/dual-channel LVDS Transmitter. Supports:
	  • Single-channel LVDS interface: 1 x 18 bpp or 1 x 24 bpp.
	  • Dual channel LVDS interface: 2 x 18 bpp or 2 x 24 bpp panel.
	  • VESA LVDS color mappings.
	  • Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3).
	  • Resolutions 640x480 up to 1900x1200 (WUXGA).
	• x16 PEG (PCI Express Graphics) support.
	• HDMI: 3x HDMI ports on digital ports B, C and D. Multiplexed with DisplayPort (DP).
	• 3x DDI (Digital Display Interface) with support for
	  • 3x DisplayPort 1.1 on digital ports B, C and D. Multiplexed with HDMI/DVI ports. Supports Hot-Plug detect.
	  • 3x DVI ports on digital ports B, C and D. Multiplexed with HDMI/DP ports. Supports Hot-Plug detect.
	  • 1x Intel® compliant SDVO port (200MPixel/sec) on digital port B and multiplexed with HDMI/DP/DVI ports on DDI1. Only supports the connection of external DVI transmitters.

Peripheral Interfaces	• 4x Serial ATA®, with RAID support 0/1/5/10. • 7 PCI Express® Lanes. Support for full 5 Gb/s bandwidth in each direction per x1 links (can be configured via BIOS firmware to support one x1s and one x4 link. A special BIOS is required for one x4 link). • LPC Bus • I²C Bus, Fast Mode, multimaster • SM Bus • 8x USB 2.0 (EHCI)
BIOS	AMI Aptio® UEFI 2.x firmware, 8MByte serial SPI with congatec Embedded BIOS features
Power Management	ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 11 of this user's guide to determine what options are available on your particular module.

2.2 Supported Operating Systems

The conga-TM67/TS67 supports the following operating systems.

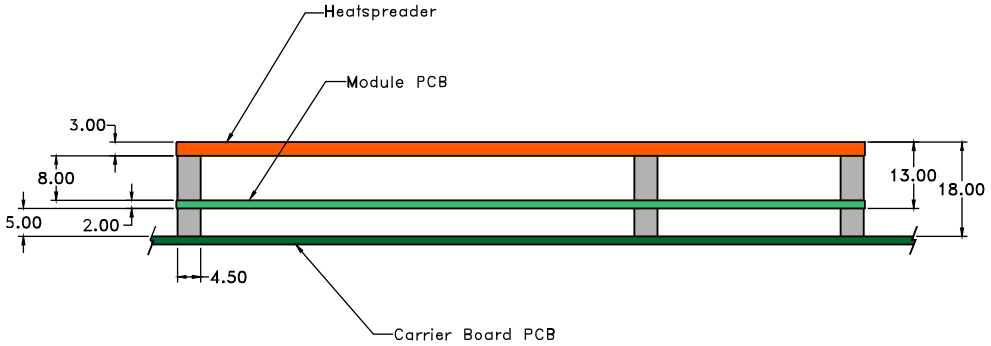
- Microsoft® Windows® 8
- Microsoft® Windows® 7
- Microsoft® Windows® XP
- Microsoft® Windows® Embedded Standard
- Linux

Note

A warning message may display after installing Microsoft® Windows® 8 (32 and 64 bit). To get rid of this message, install cougme.inf .

2.3 Mechanical Dimensions

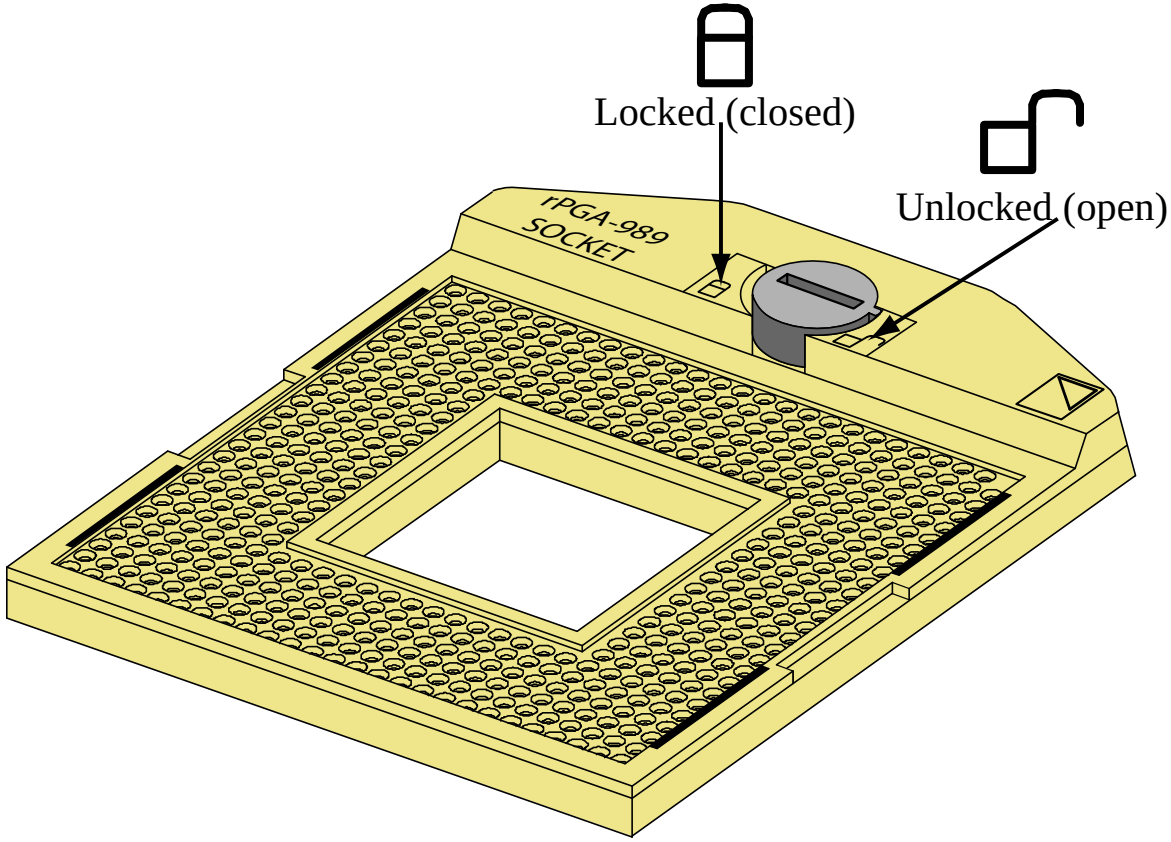
- 95.0 mm x 125.0 mm (3.74" x 4.92")
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm.



2.4 Socketed Variant of conga-TM67

The conga-TM67 is equipped with a PGA socket. This socket has 988 contacts and mates with a rPGA package that has a maximum of 988 pins. The insertion and extraction forces are zero when the socket is not engaged (in the “open” position).

There are clear indicator marks located on the actuation mechanism that identify the lock (closed) and unlock (open) positions of the cover as well as the actuation direction (see picture below). These marks remain visible after the processor is inserted into the socket.



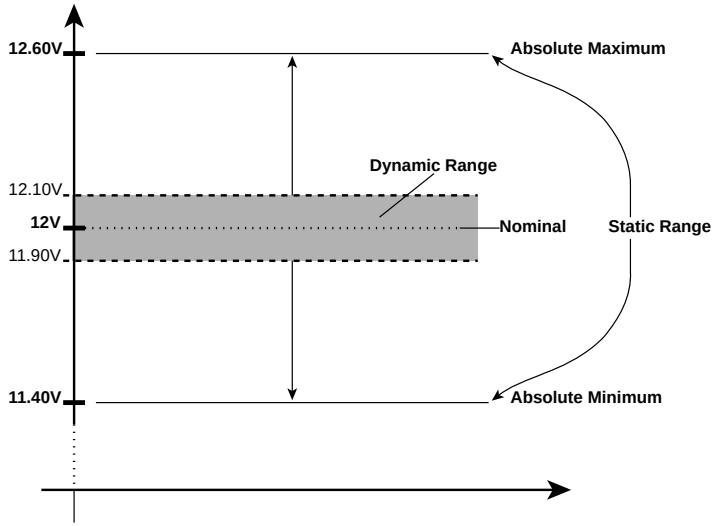
Electrostatic Sensitive Device

The conga-TM67 is an electrostatic sensitive device. Do not handle the conga-TM67, or processor, except at an electrostatic-free workstation. Failure to do so may cause damage to the module and/or processor and void the manufacturer’s warranty.

2.5 Supply Voltage Standard Power

- 12V DC ± 5%

The dynamic range shall not exceed the static range.



2.5.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.5.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

2.6 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used for testing includes a conga-TM67/TS67 module, conga-Cdebug carrier board, CRT monitor, SATA drive, and USB keyboard. The conga-Cdebug is modified so that the 12V input is only routed to the module and all other circuity on the carrier itself is powered by the 5V input. The SATA drive was powered externally by an ATX power supply so that it does not influence the power consumption value that is measured for the module. The USB keyboard was detached once the module was configured within the OS. All recorded values were averaged over a 30 second time period. Cooling of the module was done by the module specific heatpipe heatspreader and a fan cooled heatsink to measure the power consumption under normal thermal conditions.

The conga-Cdebug originally does not provide 5V standby power. Therefore, an extra 5V_SB connection without any external loads was made. Using this setup, the power consumption of the module in S3 (Standby) mode was measured directly.

Each module was measured while running Windows 7 Professional 64Bit, Hyper Threading enabled, Speed Step enabled, CPU Turbo Mode enabled and Power Plan set to “Power Saver”. This setting ensures that Core™ processors run in LFM (lowest frequency mode) with minimal core voltage during desktop idle. Each module was tested while using two 1GB memory modules. Using different sizes of RAM, as well as one or two memory modules, will cause slight variances in the measured results.

To measure the worst case power consumption the cooling solution was removed and the CPU core temperature was allowed to run up to between 95° and 100°C while running 100% workload with the Power Plan set to “Balanced”. The peak current value was then recorded. This value should be taken into consideration when designing the system’s power supply to ensure that the power supply is sufficient during worst case scenarios.

Power consumption values were recorded during the following stages:

Windows 7 (64 bit)

- Desktop Idle (power plan = Power Saver)
- 100% CPU workload (see note below, power plan = Power Saver)
- 100% CPU workload at approximately 100°C peak power consumption (power plan = Balanced)
- Suspend to RAM. Supply power for S3 mode is 5V.

Note

A software tool was used to stress the CPU to Max Turbo Frequency.

Processor Information

In the following power tables there is some additional information about the processors. Intel® offers processors that are considered to be low power consuming. These processors can be identified by their voltage status and Intel® uses specific terms to describe the voltage status. For example with the i7-2610UE, the U represents ultra low voltage. For more information about these naming conventions visit the Intel® website.

Intel® also describes the type of manufacturing process used for each processor. The following term is used:

nm=nanometer

The manufacturing process description is included in the power tables as well. See example below. For information about the manufacturing process visit Intel®'s website.

Intel® Core™ i7-2710QE 2.1 GHz 6MB Intel® Smart Cache

32nm

2.6.1 conga-TM67 Intel® Core™ i7-2710QE 2.1 GHz 6MB Cache

conga-TM67 Art. No. 046301	Intel® Core™ i7-2710QE 2.1 GHz 6MB Intel® Smart Cache 32nm Layout Rev. TM67LX0 /BIOS Rev. TM67R000			
Max Turbo Frequency	3.0 GHz			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	**Desktop Idle**	**100% workload**	**100% workload approx. 100°C CPU temp (peak)**	**Suspend to Ram (S3) 5V Input Power**
Power consumption (measured in Amperes/Watts)	**0.76 A/9.1 W (12V)**	**3.51 A/42.1 W (12V)**	**5.59 A/67.1 W (12V)**	**0.10 A/0.5 W (5V)**

2.6.2 conga-TM67 Intel® Core™ i5-2510E 2.5 GHz 3MB Cache

conga-TM67 Art. No. 046302	Intel® Core™ i5-2510E 2.5 GHz 3MB Intel® Smart Cache 32nm Layout Rev. TM67LX0 /BIOS Rev. TM67R000			
Max Turbo Frequency	3.1 GHz			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	**Desktop Idle**	**100% workload**	**100% workload approx. 100°C CPU temp (peak)**	**Suspend to Ram (S3) 5V Input Power**
Power consumption (measured in Amperes/Watts)	**0.62 A/7.4 W (12V)**	**3.28 A/39.4 W (12V)**	**4.44 A/53.3 W (12V)**	**0.10 A/0.5 W (5V)**

2.6.3 conga-TM67 Intel® Core™ i3-2330E 2.13 GHz 3MB Cache

conga-TM67 Art. No. 046303	Intel® i3-2330E 2.13 GHz 3MB Intel® Smart Cache 32nm Layout Rev. TM67LX0 /BIOS Rev. TM67R000			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.63 A/7.6 W (12V)**	**2.83 A/33.9 W (12V)**	**4.16 A/49.9 W (12V)**	**0.10 A/0.5 W (5V)**

2.6.4 conga-TM67 Intel® Celeron® B810 1.6 GHz 4MB Cache

conga-TS67 Art. No. 046304	Intel® Celeron® B810 1.6 GHz 2 Core™ 2MB Intel® Smart Cache 32nm Layout Rev. TS67LX0 /BIOS Rev. TM67R000			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.67 A/8.1 W (12V)**	**2.05 A/24.6 W (12V)**	**2.98 A/35.8 W (12V)**	**0.10 A/0.5 W (5V)**

2.6.5 conga-TS67 Intel® Core™ i7-2655LE 2.2 GHz 4MB Cache

conga-TS67 Art. No. 046401	Intel® Core™ i7-2655LE 2.2 GHz 4MB Intel® Smart Cache 32nm Layout Rev. TS67LX0 /BIOS Rev. TM67R000			
Max Turbo Frequency	2.9 GHz			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.62 A/7.4 W (12V)**	**2.26 A/27.1 W (12V)**	**3.29 A/39.5 W (12V)**	**0.10 A/0.5 W (5V)**

2.6.6 conga-TS67 Intel® Core™ i7-2610UE 1.5 GHz 3MB Cache

conga-TS67 Art. No. 046402	Intel® Core™ i7-2610UE 1.5 GHz 3MB Intel® Smart Cache 32nm Layout Rev. TS67LX0 /BIOS Rev. TM67R000			
Max Turbo Frequency	2.4 GHz			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.67 A/8.1 W (12V)**	**1.58 A/18.9 W (12V)**	**7.50 A/30.0 W (12V)**	**0.10 A/0.5 W (5V)**

2.6.7 conga-TS67 Intel® Core™ i3-2340UE 1.3 GHz 3MB Cache

conga-TS67 Art. No. 046403	Intel® Core™ i3-2340UE 1.3 GHz 3MB Intel® Smart Cache 32nm Layout Rev. TS67LX0 /BIOS Rev. TM67R000			
Max Turbo Frequency	N.A.			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.63 A/7.6 W (12V)**	**1.41 A/16.9 W (12V)**	**2.23 A/26.8 W (12V)**	**0.10 A/0.5 W (5V)**

2.6.8 conga-TS67 Intel® Celeron® 847E 1.1 GHz 2 Core™ 2MB Cache

conga-TS67 Art. No. 046404	Intel® Celeron® 847E 1.1 GHz 2 Core™ 2MB Intel® Smart Cache 32nm Layout Rev. TS67LX0 /BIOS Rev. TM67R000			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.58 A/6.9 W (12V)**	**1.3 A/15.6 W (12V)**	**1.39 A/16.7 W (12V)**	**0.10 A/0.5 W (5V)**

2.6.9 conga-TS67 Intel® Celeron® 827E 1.4 GHz 1 Core™ 1.5MB Cache

conga-TS67 Art. No. 046405	Intel® Celeron® 827E 1.4 GHz 1 Core™ 1.5MB Intel® Smart Cache 32nm Layout Rev. TS67LX0 /BIOS Rev. TM67R000			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.58** A/6.9 W (12V)	**1.08** A/12.9 W (12V)	**2.19** A/26.3 W (12V)	**0.10** A/0.5 W (5V)

2.6.10 conga-TS67 Intel® Celeron® 807UE 1.0 GHz 1 Core™ 1MB Cache

conga-TS67 Art. No. 046406	Intel® Celeron® 807UE 1.0 GHz 1 Core™ 1.0MB Intel® Smart Cache 32nm Layout Rev. TS67LX0 /BIOS Rev. TM67R000			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.53** A/6.4 W (12V)	**0.79** A/9.5 W (12V)	**1.53** A/18.4 W (12V)	**0.10** A/0.5 W (5V)

2.6.11 conga-TS67 Intel® Celeron® B810E 1.6 GHz 2 Core™ 2MB Cache

conga-TS67 Art. No. 046407	Intel® Celeron® B810E 1.6 GHz 2 Core™ 2MB L3 Intel® Smart Cache 32nm Layout Rev. TS67LX0 /BIOS Rev. TM67R000			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	**Desktop Idle**	**100% workload**	**100% workload approx. 100°C CPU temp (peak)**	**Suspend to Ram (S3) 5V Input Power**
Power consumption (measured in Amperes/Watts)	**TBD A/W (12V)**	**TBD A/ W (12V)**	**TBD A/ W (12V)**	**TBD A/ W (5V)**

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Supply power for S3 mode is 5V while all other measured modes are supplied with 12V power. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

2.7 Supply Voltage Battery Power

- 2.0V-3.5V DC
- Typical 3V DC

2.7.1 CMOS Battery Power Consumption

RTC @ 20°C	Voltage	Current
Integrated in the Intel® BD82QM67 or BD82HM65 PCH	3V DC	2.45 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

2.8 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

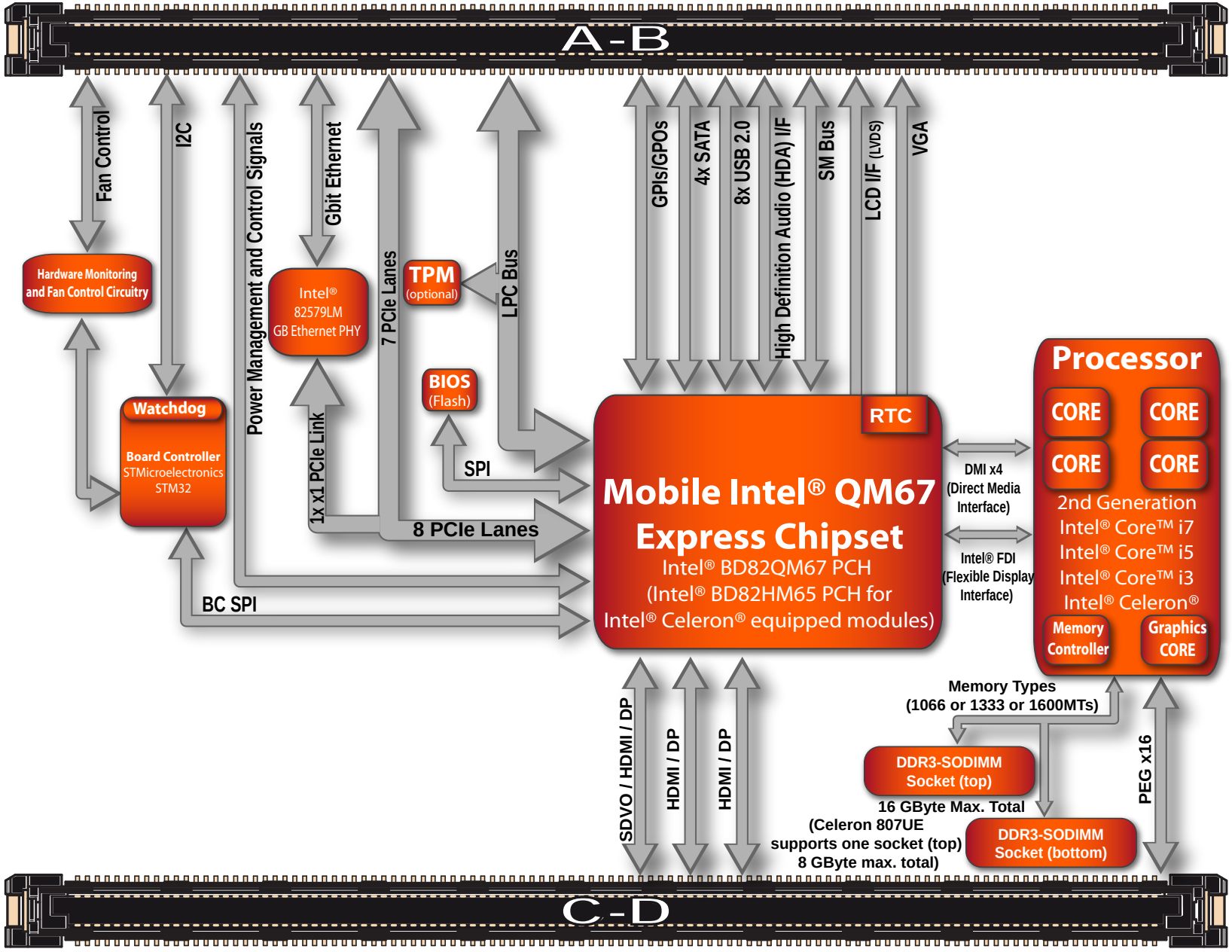
congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.

If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

For more information about operating a congatec module without heatspreader contact congatec technical support.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



4 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module and its aluminum plate is 3mm thick. The heatspreader is thermally coupled to the CPU and other heat generating components via a heat pipe.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis thereby using the whole chassis as a heat dissipater.

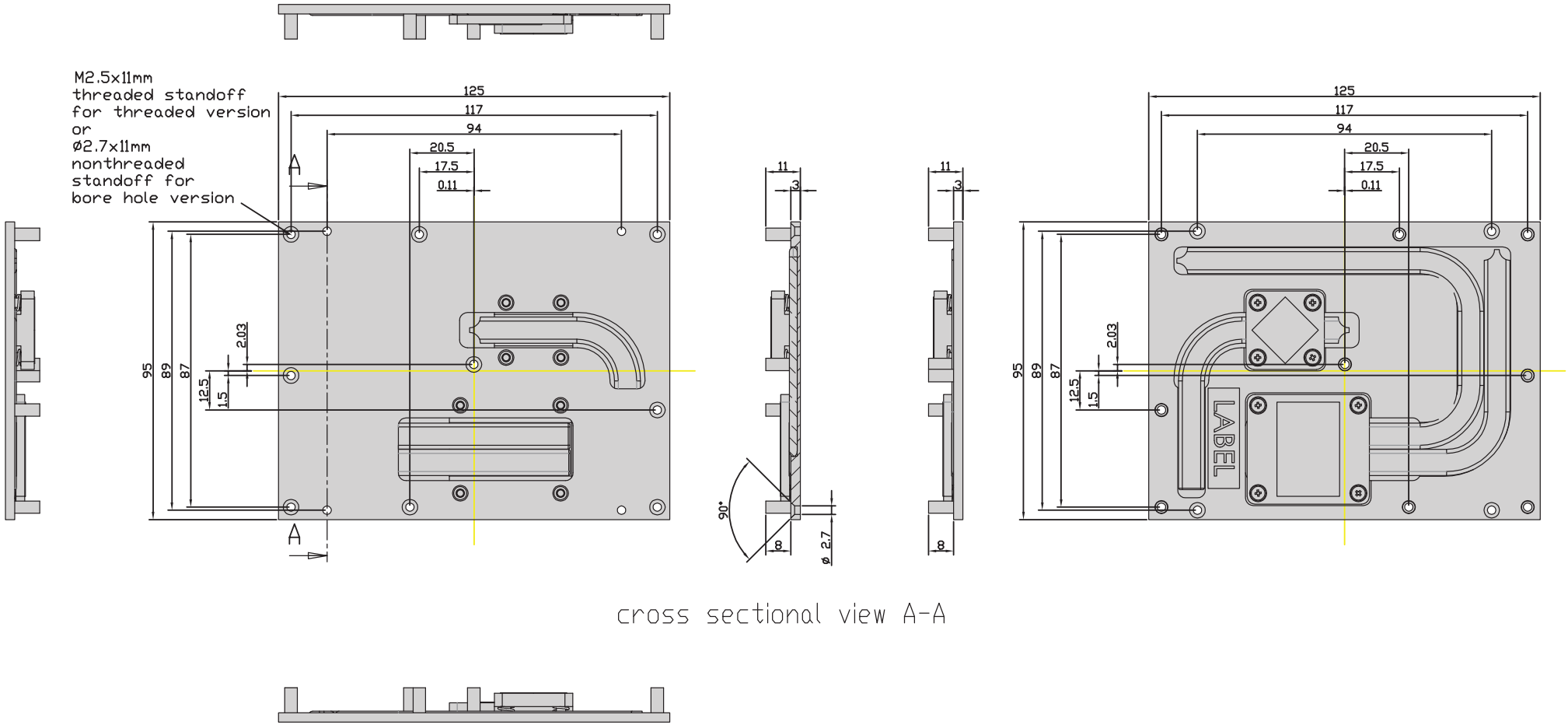
For additional information about the conga-TM67/TS67 heatspreader, refer to section 4.2 of this document.

Caution

There are mounting holes on the heatspreader designed to attach the heatspreader to the module. These mounting holes must be used to ensure that all components that are required to make contact with heatspreader do so. Failure to utilize these mounting holes will result in improper contact between these components and heatspreader thereby reducing heat dissipation efficiency.

Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

4.1 Heatspreader Dimensions



cross sectional view A-A

Note

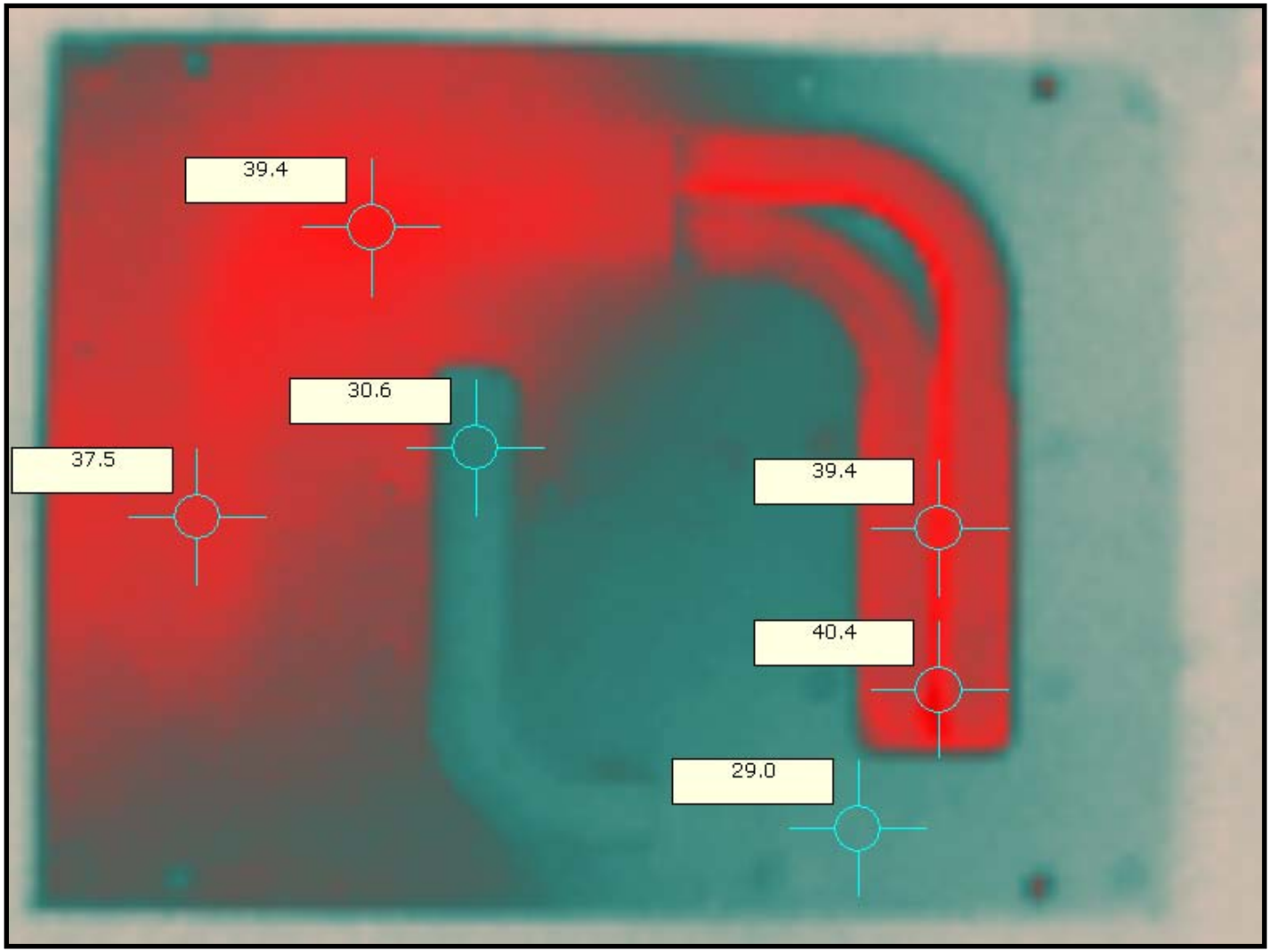
All measurements are in millimeters. Torque specification for heatspreader screws is 0.3 Nm. Mechanical system assembly mounting shall follow the valid DIN/IS0 specifications.

Caution

When using the heatspreader in a high shock and/or vibration environment, congatec recommends the use of a thread-locking fluid on the heatspreader screws to ensure the above mentioned torque specification is maintained.

4.2 Heatspreader Thermal Imagery

The conga-TM67/TS67 heatspreader solution features heat pipes. A heat pipe is a simple device that can quickly transfer heat from one point to another. They are often referred to as the “superconductors” of heat as they possess an extra ordinary heat transfer capacity and rate with almost no heat loss. The thermal image below provides a reference to where the heat is being transferred to on the heatspreader surface area when using the conga-BM57, which is similar to conga-TM67/TS67. All surface temperatures shown in the thermal image are in centigrade. System designers must ensure that the system’s cooling solution is designed to dissipate the heat from the hottest surface spots of the heatspreader.

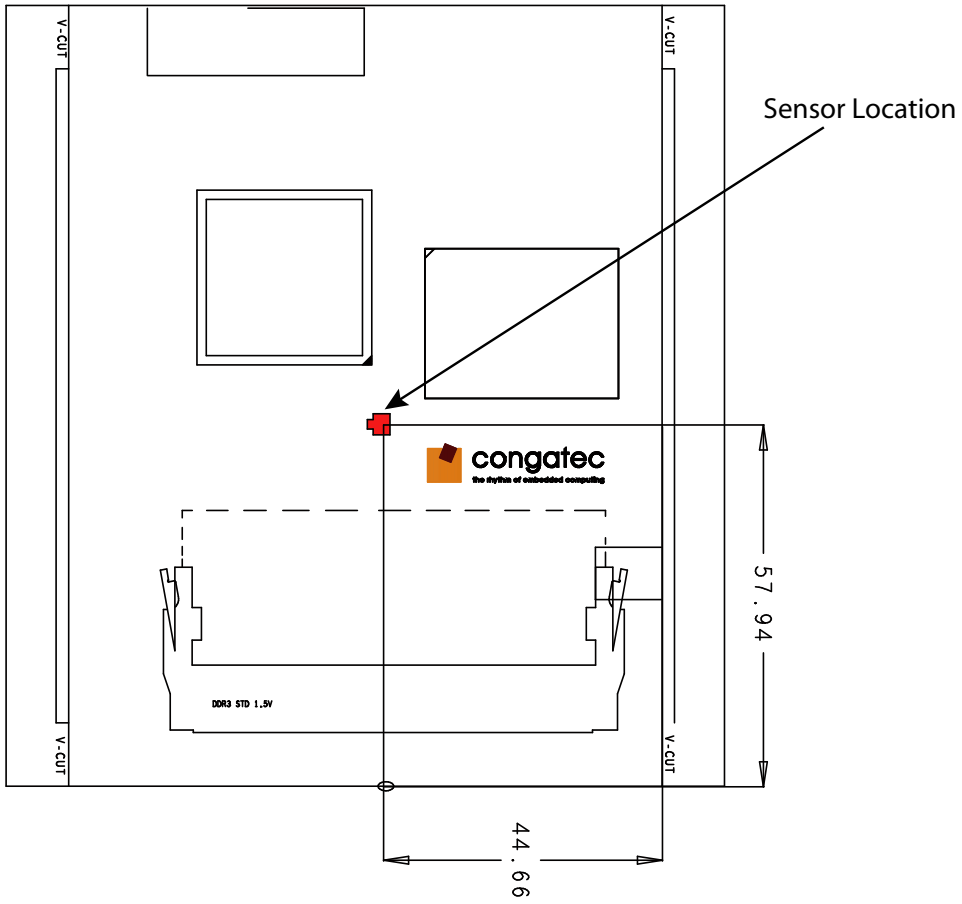


5 Onboard Temperature Sensors

Onboard the conga-TM67/TS67 are two sensors - the board temperature sensor and the system environment temperature sensor. These sensors are defined in the CGOS API as CGOS_TEMP_BOARD and CGOS_TEMP_ENV.

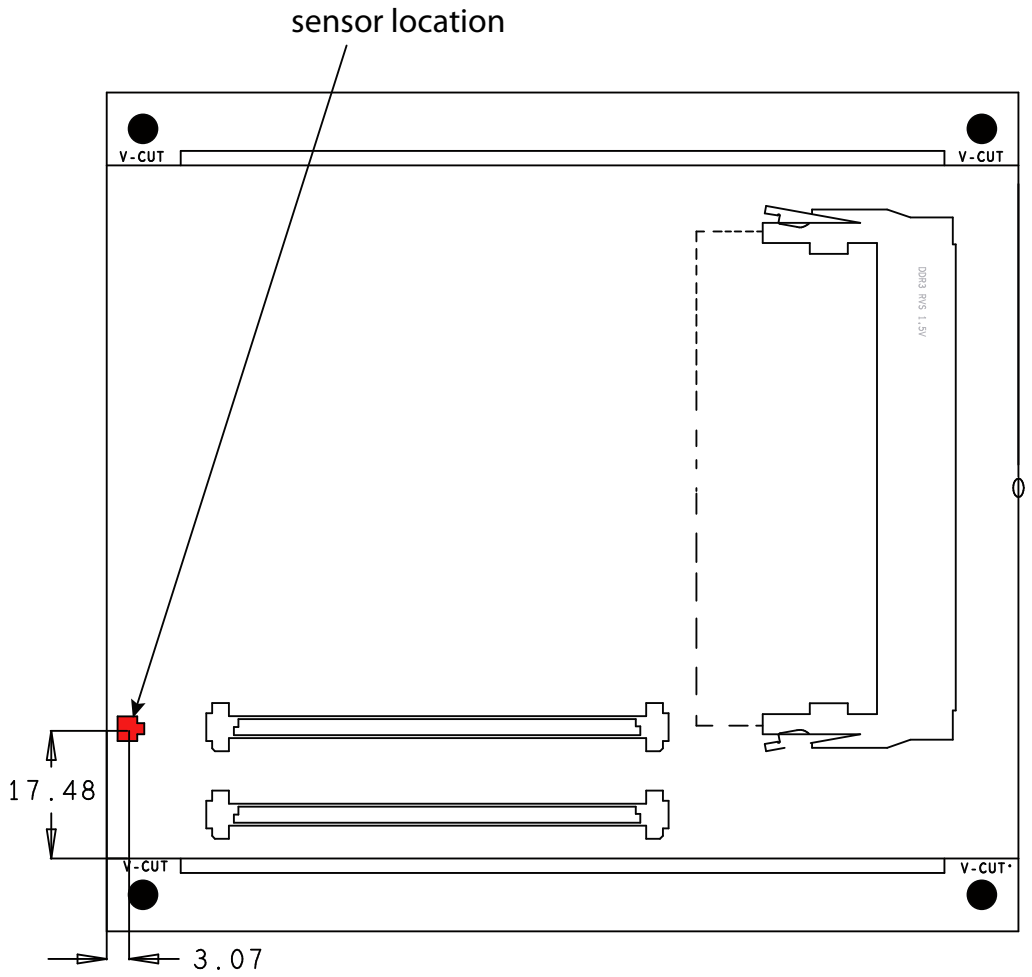
Board Temperature Sensor:

The board sensor is located at the top of the conga-TM67/TS67. This sensor measures the board temperature and is defined in CGOS API as CGOS_TEMP_BOARD. It is located on the module as shown below:



System Environment Temperature Sensor:

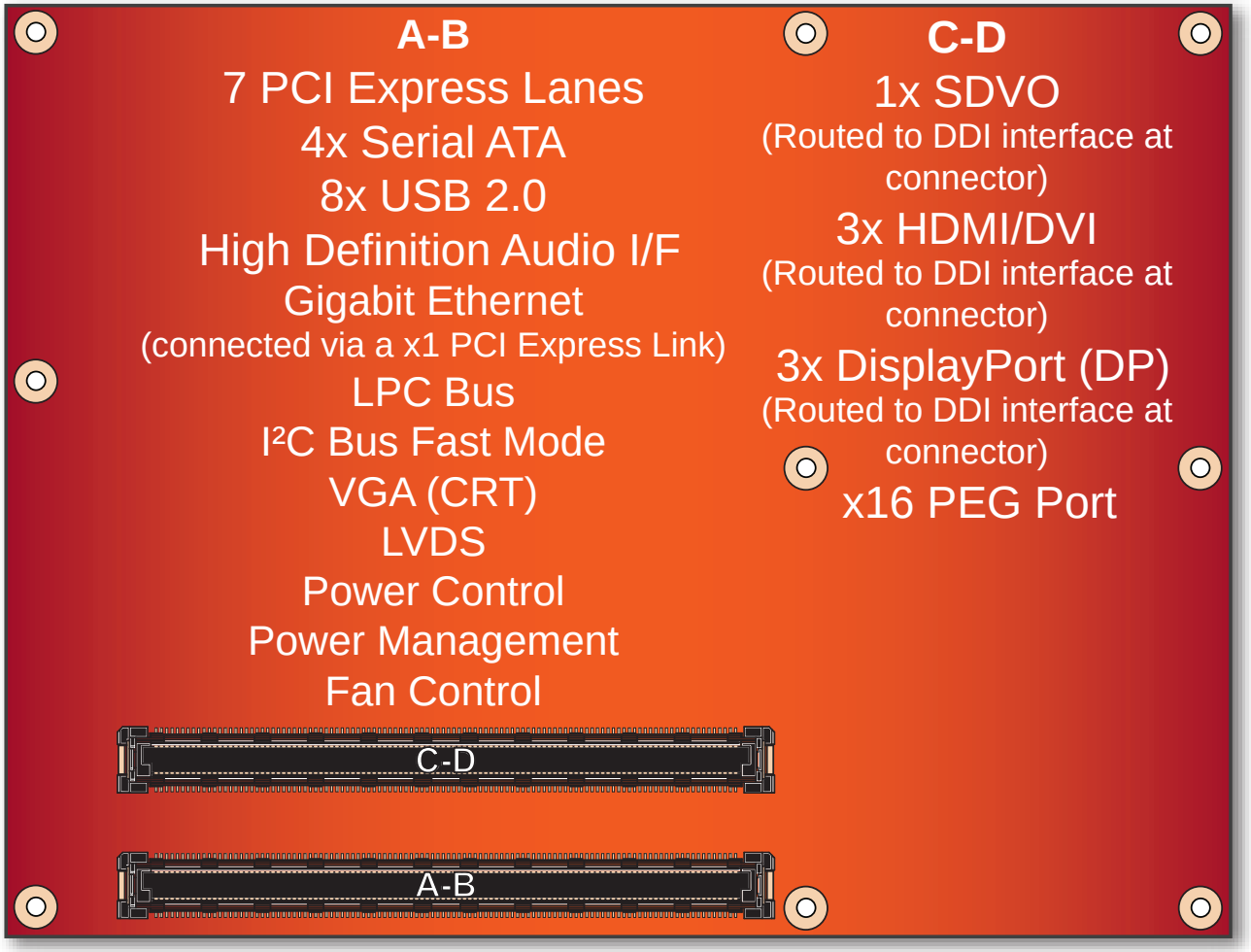
The system environment sensor is located at the bottom of the conga-TM67/TS67. This sensor measures the system environment temperature and is defined in CGOS API as CGOS_TEMP_ENV. It is located on the module as shown below:



6 Connector Subsystems Rows A, B, C, D

The conga-TM67/TS67 is connected to the carrier board via two 220-pin connectors (COM Express Type 6 pinout) for a total of 440 pins connectivity. These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.

In this view the connectors are seen “through” the module.



top view

6.1 Primary Connector Rows A and B

The following subsystems can be found on the primary connector rows A and B.

6.1.1 Serial ATA™ (SATA)

Six Serial ATA connections are provided via the Intel® BD82QM67 or BD82HM65 (QM67 or HM65) PCH. Two of these SATA ports (SATA 0 and 1) are capable of up to 6.0 Gb/s transfer rate. The SATA ports 2 and 3 are Gen 2, supporting transfer rates up to 3Gb/s. The conga-TM67/TS67 provides 4 SATA ports (SATA 0-3) externally.

6.1.2 USB 2.0

The conga-TM67/TS67 offers two EHCI USB host controllers provided by the Intel® BD82QM67 or BD82HM65 (QM67 or HM65) PCH. These controllers comply with USB standard 1.1 and 2.0 and offer a total of 8 USB ports via connector rows A and B. Each port is capable of supporting USB 1.1 and 2.0 compliant devices. For more information about how the USB host controllers are routed see section 8.6.

6.1.3 High Definition Audio (HDA) Interface

The conga-TM67/TS67 provides an interface that supports the connection of HDA audio codecs.

6.1.4 Gigabit Ethernet

The conga-TM67/TS67 is equipped with a Gigabit Ethernet Controller that is integrated within the Intel® BD82QM67 or BD82HM65 (QM67 or HM65) PCH. This controller is combined with an Intel® 82579LM Phy that is implemented through the use of the seventh PCI Express lane. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

Note

The GBE0_LINK# output is only active during a 100Mbit or 1Gbit connection, it is not active during a 10Mbit connection. This is a limitation of Ethernet controller since it only has 3 LED outputs, ACT#, LINK100# and LINK1000#. The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TM67/TS67 module.

6.1.5 LPC Bus

conga-TM67/TS67 offers the LPC (Low Pin Count) bus through the use of the Intel® BD82QM67 or BD82HM65 (QM67 or HM65) PCH. There are many devices available for this Intel® defined bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific baseboard using this bus. See section 10.2.1 for more information about the LPC Bus.

6.1.6 I²C Bus Fast mode

The I²C bus is implemented through the congatec board controller (STMicroelectronics STM32). It provides a Fast Mode multi-master I²C Bus that has maximum I²C bandwidth.

6.1.7 PCI Express™

The conga-TM67/TS67 offers 8 PCI Express™ lanes via the Intel® BD82QM67 or BD82HM65 (QM67 or HM65) PCH. The Gen2 PCI Express™ interface offers support for full 5 Gb/s bandwidth in each direction per x1 link.

One of the eight PCI Express lanes is utilized by the onboard Gigabit Ethernet interface. Six PCI Express lanes are available on the A,B connector row. Default configuration for these 6 lanes is 6x x1 link. A 1x x4 and 2x x1 link configuration is also possible but requires a special/ customized BIOS firmware. Contact congatec technical support for more information about this subject.

The PCI Express interface is based on the PCI Express Specification 2.0 both Gen 1 (2.5Gb/s) and Gen 2 (5 Gb/s) speed.

6.1.8 ExpressCard™

The conga-TM67/TS67 supports the implementation of ExpressCards, which requires the dedication of one USB port and a x1 PCI Express link for each ExpressCard used.

6.1.9 Graphics Output (VGA/CRT)

The conga-TM67/TS67 graphics are driven by a Mobile Intel® 6 Series HD graphics engine, which is incorporated within the processor found on the conga-TM67/TS67. This graphic engine offers significantly higher performance than previous Intel® graphics engines found on previous Intel® chipsets.

6.1.10 LCD

The Intel® BD82QM67 or BD82HM65 (QM67 or HM65) PCH, found on the conga-TM67/TS67, offers an integrated dual channel LVDS interface. There are two LVDS transmitter channels (Channel A and Channel B) in the LVDS interface. Channel A and Channel B consist of 4-data pairs and a clock pair each.

6.1.11 General Purpose Serial Interface

Two TTL compatible two wire ports are available on Type 6 COM Express modules. These pins are designated SER0_TX, SER0_RX, SER1_TX and SER1_RX. Data out of the module is on the _TX pins. Hardware handshaking and hardware flow control are not supported. The module asynchronous serial ports are intended for general purpose use and for use with debugging software that make use of the “console redirect” features available in many operating systems.

Note

The General Purpose Serial Interface is not supported on the conga-TM67/TS67 module.

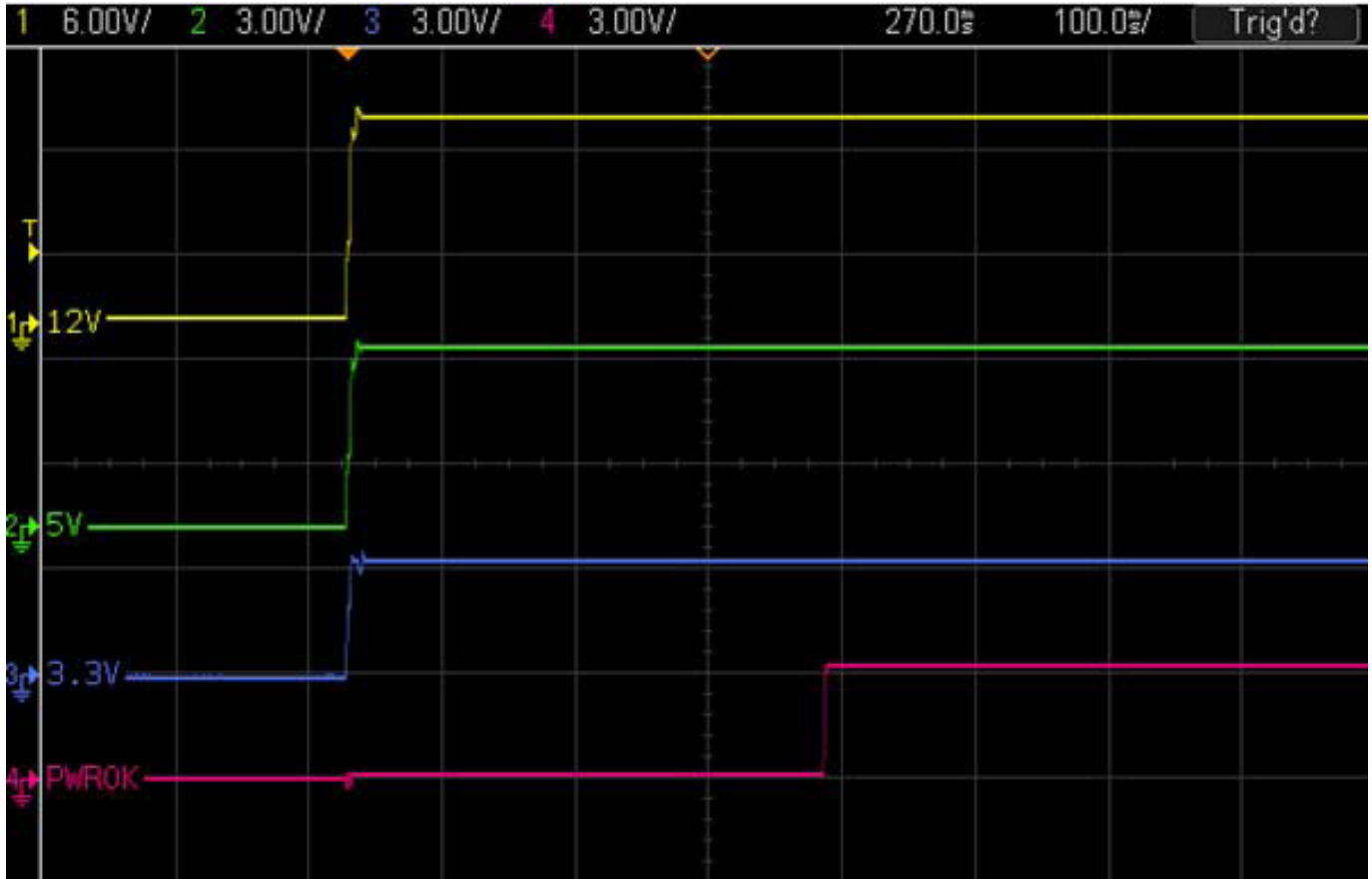
6.1.12 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system.

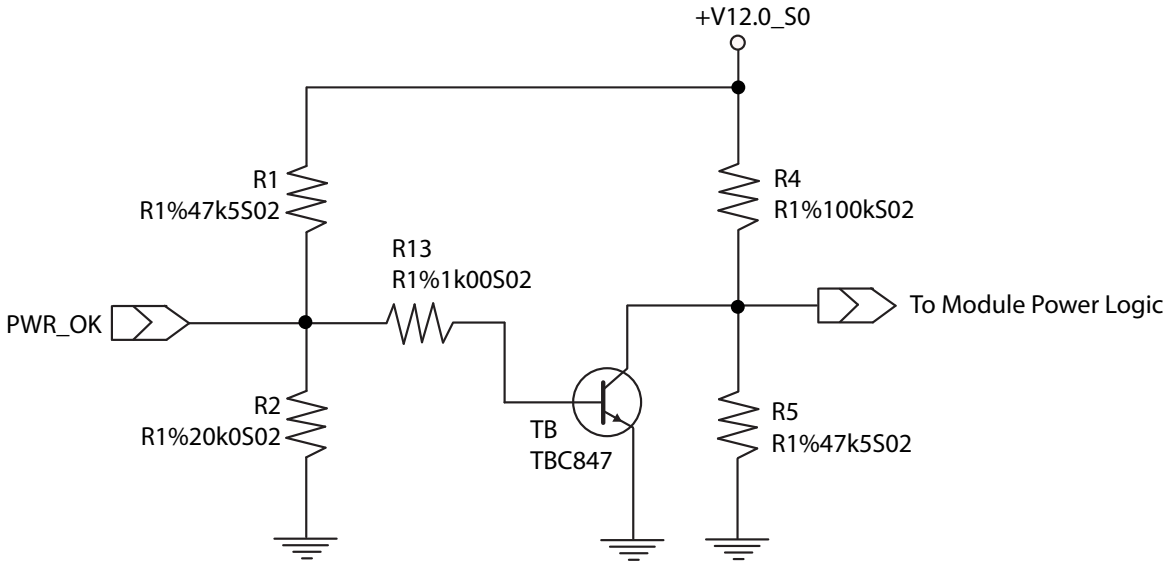
A sample screenshot is shown below:



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The conga-TM67/TS67 PWR_OK input circuitry is implemented as shown below:



The voltage divider ensures that the input complies with 3.3V CMOS characteristic and also allows for carrier board designs that are not driving PWR_OK. Although the PWR_OK input is not mandatory for the onboard power-up sequencing, it is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

When considering the above shown voltage divider circuitry and the transistor stage, the voltage measured at the PWR_OK input pin may be only around 0.8V when the 12V is applied to the module. Actively driving PWR_OK high is compliant to the COM Express specification but this can cause back driving. Therefore, congatec recommends driving the PWR_OK low to keep the module in reset and tri-state PWR_OK when the carrier board hardware is ready to boot.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the “power good” signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, it must be ensured that by the time the 3.3V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-TM67/TS67 provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-TM67/TS67's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

12 volt input power is the sole operational power source for the conga-TM67/TS67. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-TM67/TS67 application:

- It has also been noticed that on some occasions, problems occur when using a 12V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

6.1.13 Power Management

ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

6.2 Secondary Connector Rows C and D

The following subsystems can be found on the secondary connector rows C and D.

6.2.1 PCI Express™

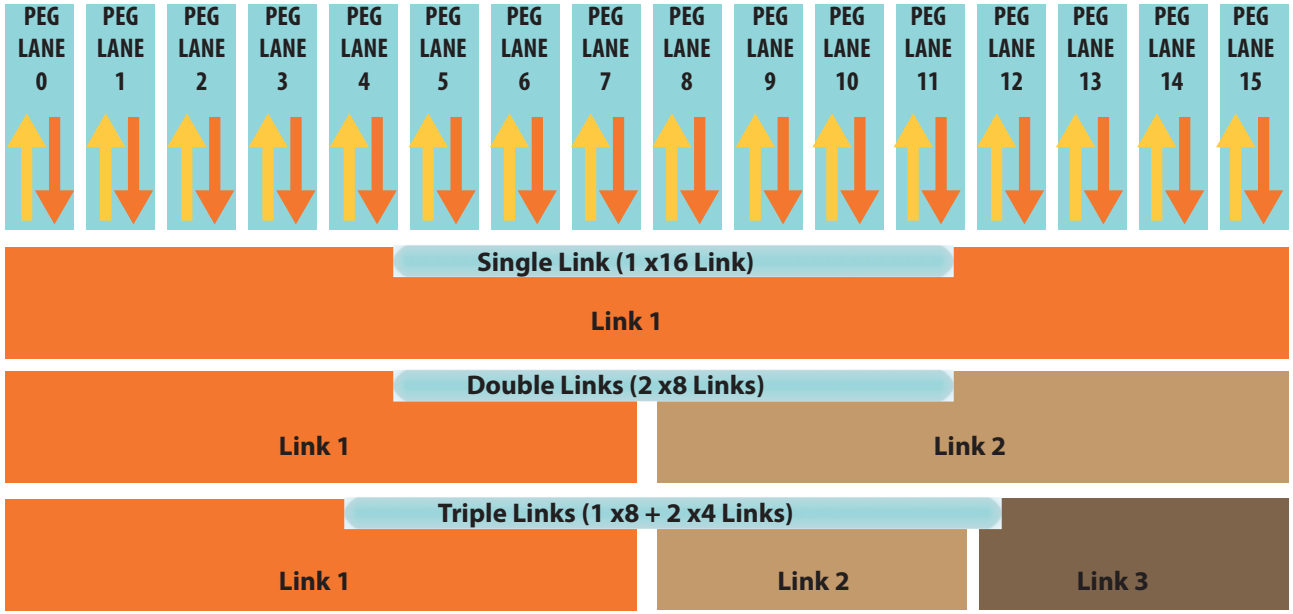
The conga-TM67/TS67 offers 8 PCI Express™ lanes via the Intel® BD82QM67 or BD82HM65 (QM67 or HM65) PCH. The Gen2 PCI Express™ interface offers support for full 5 Gb/s bandwidth in each direction per x1 link. One of these PCI Express lanes (PCIe lane 7) is available on the C,D connector row.

The PCI Express interface is based on the PCI Express Specification 2.0 both Gen 1 (2.5Gb/s) and Gen 2 (5 Gb/s) speed.

6.2.2 PCI Express Graphics (PEG)

The PCI Express graphics interface is supported on conga-TM67/TS67. The PEG lanes are same as PCI Express lanes 16-31.

It is possible to optionally use the PEG interface for connecting a x1, x2, x4, or x8 non-graphic PCI Express device instead of using the x16 link for a PCI Express graphics device. This will increase the available PCI Express links on top of those explained in section 6.1.7. These additional links cannot be linked together with each other or with the other PCI Express links found on the conga-TM67/TS67.



The 16 PCIe lanes of the PEG port are controlled by three controllers. The possible configurations as shown in the diagram above are:

- 1 x16 link (default PEG)
- 2 x8 links
- 1 x8 + 2 x4 links

Each controller can automatically operate on a lower link width allowing up to three simultaneous operating devices on the PEG interface. The PEG root port configuration can be selected in the BIOS setup program. This feature is only available on conga-TM67 variants with hardware revision B.x or later and on conga-TS67 variants with hardware revision A.x or later.

6.2.3 SDVO

The Serial Digital Video Output (SDVO) is multiplexed with HDMI and DisplayPort on the Digital Display Interface channel 1 (DDI1) of the COM Express connector. It may be used for a third party SDVO compliant device connected to DDI1. See section 9.5 of this document for more information about enabling SDVO peripherals.

Note

The SDVO interface only supports the connection of DVI transmitters. The connection of other transmitters such as TV or LVDS is not supported.

6.2.4 HDMI

The Intel® BD82QM67 or BD82HM65 (QM67 or HM65) PCH on the conga-TM67/TS67 supports integrated HDMI, which is multiplexed onto the Digital Display Interface (DDI) of the COM Express connector. The Intel® QM67 or HM65 provides three ports capable of supporting HDMI. See section 9.5 of this document for more information about enabling HDMI peripherals.

6.2.5 DisplayPort (DP)

The conga-TM67/TS67 offers three DP ports, each capable of supporting link-speeds of 1.62 Gbps and 2.7 Gbps on 1, 2 or 4 data lanes. The DP is multiplexed onto the PCI Express Graphics (PEG) interface of the COM Express connector. The DisplayPort specification is a VESA standard aimed at consolidating internal and external connection methods to reduce device complexity, supporting key cross industry applications, and providing performance scalability to enable the next generation of displays. The Intel® BD82QM67 or BD82HM65 (QM67 or HM65) PCH can support a maximum of 2 DP ports simultaneously. See section 9.5 of this document for more information about enabling DisplayPort peripherals.

7 Additional Features

7.1 congatec Board Controller (cBC)

The conga-TM67/TS67 is equipped with a STMicroelectronics STM32 microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

7.2 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

7.3 Watchdog

The conga-TM67/TS67 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-TM67/TS67 does not support external hardware triggering. For more information about the Watchdog feature see the BIOS setup description section 11.4.2 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

Note

The conga-TM67/TS67 modules do not support the watchdog NMI mode. COM Express type 6 modules do not support the PCI bus and therefore the PCI_SERR# signal is not available. There is no way to drive a NMI to the processor without the presence of the PCI_SERR# PCI bus signal.

7.4 I²C Bus

The conga-TM67/TS67 offers support for the frequently used I²C bus. Thanks to the I²C host controller in the cBC the I²C bus is multimaster capable and runs at fast mode.

7.5 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behaviour of the system after a AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

7.6 Embedded BIOS

The conga-TM67/TS67 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. These are the most important embedded PC features:

7.6.1 CMOS Backup in Non Volatile Memory

A copy of the CMOS memory (SRAM) is stored in the BIOS flash device. This prevents the system from not booting up with the correct system configuration if the backup battery (RTC battery) has failed. Additionally, it provides the ability to create systems that do not require a CMOS backup battery.

7.6.2 OEM CMOS Default Settings and OEM BIOS Logo

This feature allows system designers to create and store their own CMOS default configuration and BIOS logo (splash screen) within the BIOS flash device. Customized BIOS development by congatec for these changes is no longer necessary because customers can easily do these changes by themselves using the congatec system utility CGUITL.

7.6.3 OEM BIOS Code

With the congatec embedded BIOS it is even possible for system designers to add their own code to the BIOS POST process. Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table, verb tables for HDA codecs, rare graphic modes and Super I/O controllers.

For more information about customizing the congatec embedded BIOS refer to the congatec System Utility user’s guide, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com or contact congatec technical support.

7.6.4 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-TM67/TS67 BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

7.6.5 API Support (CGOS/EAPI)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

Other COM (Computer on Modules) vendors offer similar driver solutions for these kind of embedded PC features, which are by nature proprietary. All the API solutions that can be found on the market are not compatible to each other. As a result, writing application software that can run on more than one vendor's COM is not so easy. Customers have to change their application software when switching to another COM vendor. EAPI (Embedded Application Programming Interface) is a programming interface defined by the PICMG that addresses this problem. With this unified API, it is now possible to run the same application on all vendor's COMs that offer EAPI driver support. Contact congatec technical support for more information about EAPI.

7.7 Security Features

The conga-TM67/TS67 can be equipped optionally with a “Trusted Platform Module“ (TPM 1.2). This TPM 1.2 includes coprocessors to calculate efficient hash and RSA algorithms with key lengths up to 2,048 bits as well as a real random number generator. Security sensitive applications like gaming and e-commerce will benefit also with improved authentication, integrity and confidence levels.

7.8 Suspend to Ram

The Suspend to RAM feature is available on the conga-TM67/TS67.

8 conga Tech Notes

The conga-TM67/TS67 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

8.1 Intel Turbo Boost 2

Intel® Turbo Boost 2 Technology allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits. Intel® Turbo Boost 2 Technology is activated when the Operating System (OS) requests the highest processor performance state. The maximum frequency of Intel® Turbo Boost 2 Technology is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost 2 Technology state depends on the workload and operating environment. Any of the following can set the upper limit of Intel® Turbo Boost 2 Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase by 100 MHz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached. For more information about Intel® Turbo Boost 2 Technology visit the Intel® website.

Note

Only conga-TM67/TS67 module variants that feature the Core™ i7 and i5 processors support Intel® Turbo Boost 2 Technology. Refer to the power consumption tables in section 2.6 of this document for information about the max. turbo frequency available for each variant of the conga-TM67/TS67.

8.2 Intel® Matrix Storage Technology

The Intel® BD82QM67 or BD82HM65 (QM67 or HM65) PCH provides support for Intel® Matrix Storage Technology, allowing AHCI functionality.

8.2.1 AHCI

The QM67 or HM65 PCH provides hardware support for Advanced Host Controller Interface (AHCI), a new programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

8.2.2 RAID

The industry-leading RAID capability provides high performance RAID 0, 1, 5, and 10 functionality on the 4 SATA ports of Intel® BD82QM67 (QM67) PCH. Software components include an Option ROM for pre-boot configuration and boot functionality, a Microsoft* Windows* compatible driver, and a user interface for configuration and management of the RAID capability of the Intel® BD82QM67 (QM67) PCH.

Note

RAID support is not available on conga-TM67/TS67 variants that feature the Intel® BD82HM65 (HM65) chipset.

8.3 Intel® Processor Features

8.3.1 Thermal Monitor and Catastrophic Thermal Protection

Intel® Core™ i7/i5/i3 and Celeron® processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature, that the Intel® Thermal Monitor uses to activate the TCC, cannot be configured by the user nor is it software visible.

The Thermal Monitor can control the processor temperature through the use of two different methods defined as TM1 and TM2. TM1 method consists of the modulation (starting and stopping) of the processor clocks at a 50% duty cycle. The TM2 method initiates an Enhanced Intel Speedstep transition to the lowest performance state once the processor silicon reaches the maximum operating temperature.

Note

The maximum operating temperature for Intel® Core™ i7/i5/i3 and Celeron® processors is 100°C. TM2 mode is used for Intel® Core™ i7/i5/i3

and the latest generation of Celeron® processors.

Two modes are supported by the Thermal Monitor to activate the TCC. They are called Automatic and On-Demand. No additional hardware, software, or handling routines are necessary when using Automatic Mode.

Note

To ensure that the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Core™ i7/i5/i3 and Celeron® processor's respective datasheet can provide you with more information about this subject.

THERMTRIP# signal is used by Intel®'s Core™ i7/i5/i3 and Celeron® processors for catastrophic thermal protection. If the processor's silicon reaches a temperature of approximately 125°C then the processor signal THERMTRIP# will go active and the system will automatically shut down to prevent any damage to the processor as a result of overheating. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

Note

In order for THERMTRIP# to be able to automatically switch off the system it is necessary to use an ATX style power supply.

8.3.2 Processor Performance Control

Intel® Core™ i7/i5/i3 and Celeron® processors found on the conga-TM67/TS67 run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it's not being fully utilized. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that your power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

8.3.3 Intel® 64

The formerly known Intel® Extended Memory 64 Technology is an enhancement to Intel®'s IA-32 architecture. Intel® 64 is only available on Intel® Core™ i7/i5/i3 and Celeron® processors and is designed to run with newly written 64-bit code and access more than 4GB of memory. Processors with Intel® 64 architecture support 64-bit-capable operating systems from Microsoft, Red Hat and SuSE. Processors running in legacy mode remain fully compatible with today's existing 32-bit applications and operating systems

Platforms with Intel® 64 can be run in three basic ways :

1. **Legacy Mode:** 32-bit operating system and 32-bit applications. In this mode no software changes are required, however the benefits of Intel® 64 are not utilized.

2. **Compatibility Mode:** 64-bit operating system and 32-bit applications. This mode requires all device drivers to be 64-bit. The operating system will see the 64-bit extensions but the 32-bit application will not. Existing 32-bit applications do not need to be recompiled and may or may not benefit from the 64-bit extensions. The application will likely need to be re-certified by the vendor to run on the new 64-bit extended operating system.

3. **64-bit Mode:** 64-bit operating system and 64-bit applications. This usage requires 64-bit device drivers. It also requires applications to be modified for 64-bit operation and then recompiled and validated.

Intel® 64 provides support for:

- 64-bit flat virtual address space
- 64-bit pointers
- 64-bit wide general purpose registers
- 64-bit integer support
- Up to one Terabyte (TB) of platform address space

You can find more information about Intel® 64 Technology at: http://developer.intel.com/technology/intel64/index.htm

8.3.4 Intel® Virtualization Technology

Virtualization solutions enhanced by Intel® VT will allow a Core™ i7/i5/i3 platform to run multiple operating systems and applications in independent partitions. When using virtualization capabilities, one computer system can function as multiple “virtual” systems. With processor and I/O enhancements to Intel®’s various platforms, Intel® Virtualization Technology can improve the performance and robustness of today’s software-only virtual machine solutions.

Intel® VT is a multi-generational series of extensions to Intel® processor and platform architecture that provides a new hardware foundation for virtualization, establishing a common infrastructure for all classes of Intel® based systems. The broad availability of Intel® VT makes it possible to create entirely new applications for virtualization in servers, clients as well as embedded systems thus providing new ways to improve system reliability, manageability, security, and real-time quality of service.

The success of any new hardware architecture is highly dependent on the system software that puts its new features to use. In the case of virtualization technology, that support comes from the virtual machine monitor (VMM), a layer of software that controls the underlying physical platform resources sharing them between multiple “guest” operating systems. Intel® VT is already incorporated into most commercial and open-

source VMMs including those from VMware, Microsoft, XenSource, Parallels, Virtual Iron, Jaluna and TenAsys.

You can find more information about Intel Virtualization Technology at: http://developer.intel.com/technology/virtualization/index.htm

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

8.4 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-TM67/TS67 ACPI thermal solution offers three different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the "active cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (4°C hysteresis).

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the

appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled according to the formula below.

$$\Delta P[\%] = TC1(T_n - T_{n-1}) + TC2(T_n - T_t)$$

- *ΔP is the performance delta*
- *T_t is the target temperature = critical trip point*
- *The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants. These constants are set to fixed values for the conga-TM67/TS67:*
- *TC1= 1*
- *TC2= 5*
- *TSP= 5 seconds*

See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

8.5 ACPI Suspend Modes and Resume Events

conga-TM67/TS67 supports S3 (STR= Suspend to RAM). For more information about S3 wake events see section 11.4.5 “ACPI Configuration Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

- Windows 7, Windows Vista, Linux, Windows XP and Windows 2K

This table lists the “Wake Events” that resume the system from S3 unless otherwise stated in the “Conditions/Remarks” column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
SMBALERT#	Wakes unconditionally from S3-S5.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
USB Mouse/Keyboard Event	When Standby mode is set to S3, the following must be done for a USB Mouse/Keyboard Event to be used as a Wake Event. USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). Under Windows XP add following registry entries: Add this key: HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\usb Under this key add the following value: “USBBIOSx“=DWORD:00000000 *Note that Windows XP disables USB wakeup from S3, so this entry has to be added to re-enable it.* Configure USB keyboard/mouse to be able to wake up the system: In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check ‘Allow this device to bring the computer out of standby’. *Note: When the standby state is set to S3 in the ACPI setup menu, the power management tab for USB keyboard /mouse devices only becomes available after adding the above registry entry and rebooting to allow the registry changes to take affect.*
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

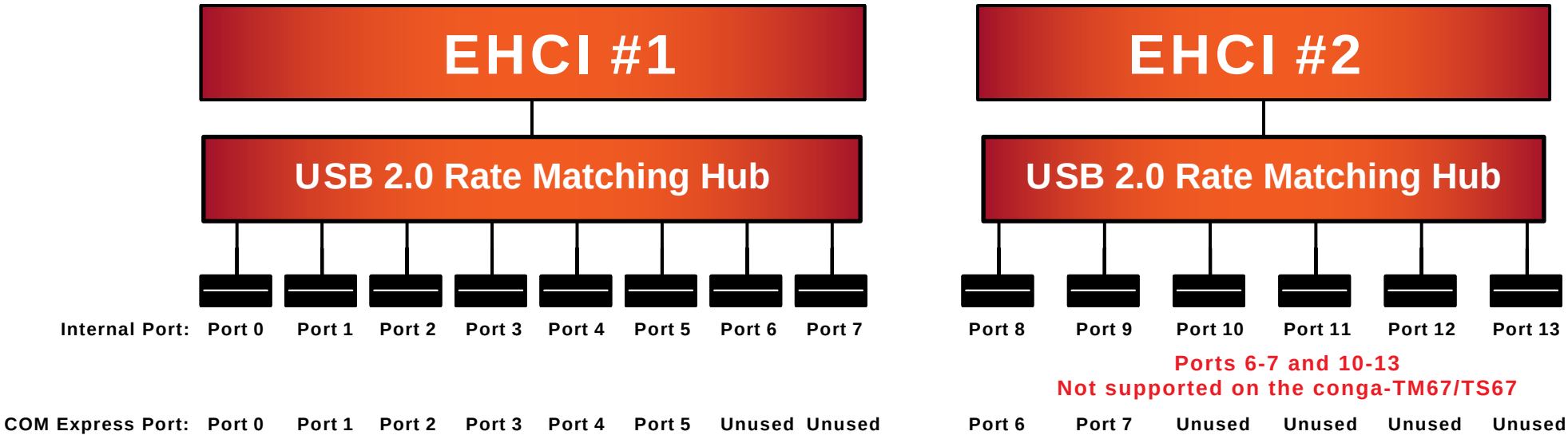
Note

The above list has been verified using a Windows XP SP3 ACPI enabled installation.

8.6 USB 2.0 EHCI Host Controller Support

The 8 available USB ports are provided by two USB 2.0 Rate Matching Hubs (RMH) integrated within the Intel® BD82QM67 or BD82HM65 (QM67 or HM65) PCH. Each EHCI controller has one hub connected to it as shown below. The Hubs convert low and full-speed traffic into high-speed traffic. When the RMHs are enabled, they will appear to software like an external hub is connected to Port 0 of each EHCI controller. In addition, port 1 of each of the RMHs is muxed with Port 1 of the EHCI controllers and is able to bypass the RMH for use as the Debug Port. The hub operates like any USB 2.0 Discrete Hub and will consume one tier of hubs allowed by the USB 2.0 Spec. A maximum of four additional non-root hubs can be supported on any of the PCH USB Ports. The RMH will report the following Vendor ID = 8087h and Product ID = 0024h.

Routing Diagram



9 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type 6 connectors used for congatec AG modules. The pinout of the modules complies with COM Express Type 6 Rev. 2.1.

Table 2 describes the terminology used in this section for the signal description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used; if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip’s datasheet.

Table 2 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0
PEG	PCI Express Graphics
SATA	In compliance with Serial ATA specification, Revision 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

9.1 A-B Connector Signal Descriptions

Table 3 Intel® High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC/HDA_RST#	A30	**Intel® High Definition Audio Reset:** This signal is the master hardware reset to external codec(s).	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SYNC	A29	**Intel® High Definition Audio Sync:** This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3VSB	PU 1K 3.3VSB	AC'97 codecs are not supported. AC/HDA_SYNC is a boot strap signal (see note below)
AC/HDA_BITCLK	A32	**Intel® High Definition Audio Bit Clock Output:** This signal is a 24.000MHz serial data clock generated by the Intel® High Definition Audio controller.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SDOUT	A33	**Intel® High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3VSB	PU 1K 3.3VSB	AC'97 codecs are not supported. AC/HDA_SDOUT is a boot strap signal (see note below)
AC/HDA_SDIN[2:0]	B28-B30	**Intel® High Definition Audio Serial Data In [0]:** These signals are serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.	I 3.3VSB		AC'97 codecs are not supported.

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module.

For more information refer to section 9.5 of this user's guide.

Table 4 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 / 100 / 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.			Not connected

Note

The GBE0_LINK# output is only active during a 100Mbit or 1Gbit connection, it is not active during a 10Mbit connection. This is a limitation of Ethernet controller since it only has 3 LED outputs, ACT#, LINK100# and LINK1000#. The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TM67/TS67 module.

Table 5 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	I/O 3.3v		

Table 6 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 7 ExpressCard Support Pins Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request.	I 3.3V	PU 10k 3.3V	
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset	O 3.3V	PU 10k 3.3V	

Table 8 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V		
LPC_SERIRQ	A50	LPC serial interrupt	I/O OD 3.3V	PU 10k 3.3V	
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V		

Table 9 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+	A37	USB Port 6, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6-	A36	USB Port 6, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+	B37	USB Port 7, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7-	B36	USB Port 7, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

Table 10 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/O OD 5V	PU 2k2 3.3V	
VGA_I2C_DAT	B96	DDC data line.	I/O OD 5V	PU 2k2 3.3V	

Table 11 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10k	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10k	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	LVDS_I2C_DAT is a boot strap signal (see note below).

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 9.5 of this user's guide.

Table 12 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB		Carrier shall pull to SPI_POWER when external SPI provided but not used.
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	+ 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or leave no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or leave no-connect

Table 13 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O 3.3V	PU 2K2 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O 3.3V	PU 2K2 3.3VSB	
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		SPEAKER is a boot strap signal (see note below)
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V		
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM.	O OD 3.3V	PU 10K 3.3V	
FAN_TACHIN	B102	Fan tachometer input.	I OD	PU 10K 3.3V	Requires a fan with a two pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V		Trusted Platform Module chip is optional.

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 9.5 of this user’s guide.

Table 14 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins. Shared with SD_CLK. Output from COM Express, input to SD	O 3.3V		SDIO interface is not supported on the conga-TM67/TS67
GPO1	B54	General purpose output pins. Shared with SD_CMD. Output from COM Express, input to SD	O 3.3V		SDIO interface is not supported on the conga-TM67/TS67
GPO2	B57	General purpose output pins. Shared with SD_WP. Output from COM Express, input to SD	O 3.3V		SDIO interface is not supported on the conga-TM67/TS67
GPO3	B63	General purpose output pins. Shared with SD_CD. Output from COM Express, input to SD	O 3.3V		SDIO interface is not supported on the conga-TM67/TS67
GPI0	A54	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal	I 3.3V	PU 10K 3.3V	SDIO interface is not supported on the conga-TM67/TS67
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3V	PU 10K 3.3V	SDIO interface is not supported on the conga-TM67/TS67
GPI2	A67	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal	I 3.3V	PU 10K 3.3V	SDIO interface is not supported on the conga-TM67/TS67
GPI3	A85	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3V	PU 10K 3.3V	SDIO interface is not supported on the conga-TM67/TS67

Table 15 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on rising edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V	PD 100k	
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V		Set by resistor divider to accept 3.3V.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB	PU 10k 3.3VSB	
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as “PS_ON”) may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		Not supported
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10k 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10k 3.3VSB	

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 10k 3.3V	
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 10k 3.3V	
SMB_CK	B13	System Management Bus bidirectional clock line.	I/O 3.3VSB	PU 2k2 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line.	I/O OD 3.3VSB	PU 2k2 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3VSB	PU 10k 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch.	I OD 3.3V	PU 10k 3.3VSB	
SLEEP	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3V	PU 10k 3.3VSB	

Table 16 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O 3.3V		Not supported
SER1_TX	A101	General purpose serial port transmitter	O 3.3V		Not supported
SER0_RX	A99	General purpose serial port receiver	I 3.3V		Not supported
SER1_RX	A102	General purpose serial port receiver	I 3.3V		Not supported

Table 17 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

9.2 A-B Connector Pinout

Table 18 Connector A-B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#	A73	LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+	B22	SATA3_TX+	A77	LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX-	B23	SATA3_TX-	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	SATA2_RX+	B25	SATA3_RX+	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX-	B26	SATA3_RX-	A81	LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	AC/HDA_BITCLK	B32	SPKR	A87	RSVD	B87	VCC_5V_SBY
A33	AC/HDA_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX (*)	B98	RSVD
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX (*)	B99	RSVD
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX (*)	B101	FAN_PWMOUT
A47	VCC_RTC	B47	EXCD1_PERST#	A102	SER1_RX (*)	B102	FAN_TACHIN
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga TM67/TS67.

9.3 C-D Connector Signal Descriptions

Table 19 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		Not supported

Table 20 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I		Not supported
USB_SSRX0-	C3		I		Not supported
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not supported
USB_SSTX0-	D3		O		Not supported
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I		Not supported
USB_SSRX1-	C6		I		Not supported
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not supported
USB_SSTX1-	D6		O		Not supported
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I		Not supported
USB_SSRX2-	C9		I		Not supported
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not supported
USB_SSTX2-	D9		O		Not supported
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I		Not supported
USB_SSRX3-	C12		I		Not supported
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not supported
USB_SSTX3-	D12		O		Not supported

Note

The conga-TM67/TS67 modules do not support USB 3.0.

Table 21 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs. *Note: Can also be used as PCI Express Receive Input differential pairs 16 through 31 known as PCIE_RX[16-31] + and -.*	I PCIE		
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_TX0+	D52	PCI Express Graphics Transmit Output differential pairs. *Note: Can also be used as PCI Express Transmit Output differential pairs 16 through 31 known as PCIE_TX[16-31] + and -.*	O PCIE		
PEG_TX0-	D53				
PEG_TX1+	D55				
PEG_TX1-	D56				
PEG_TX2+	D58				
PEG_TX2-	D59				
PEG_TX3+	D61				
PEG_TX3-	D62				
PEG_TX4+	D65				
PEG_TX4-	D66				
PEG_TX5+	D68				
PEG_TX5-	D69				
PEG_TX6+	D71				
PEG_TX6-	D72				
PEG_TX7+	D74				
PEG_TX7-	D75				
PEG_TX8+	D78				
PEG_TX8-	D79				
PEG_TX9+	D81				
PEG_TX9-	D82				
PEG_TX10+	D85				
PEG_TX10-	D86				
PEG_TX11+	D88				
PEG_TX11-	D89				
PEG_TX12+	D91				
PEG_TX12-	D92				
PEG_TX13+	D94				
PEG_TX13-	D95				
PEG_TX14+	D98				
PEG_TX14-	D99				
PEG_TX15+	D101				
PEG_TX15-	D102				
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I	PU 10k 3.3V	PEG_LAN_RV# is a boot strap signal (see note below)

Note

Dedicated PEG Channels are provided in Type 6. SDVO is no longer multiplexed on the PEG port.

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 9.5 of this user's guide.

Table 22 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with SDVO1_RED+, DP1_LANE0+ and TMDS1_DATA2+. Multiplexed with SDVO1_RED-, DP1_LANE0- and TMDS1_DATA2-.	O PCIE		
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with SDVO1_GRN+, DP1_LANE1+ and TMDS1_DATA1+. Multiplexed with SDVO1_GRN-, DP1_LANE1- and TMDS1_DATA1-.	O PCIE		
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with SDVO1_BLU+, DP1_LANE2+ and TMDS1_DATA0+. Multiplexed with SDVO1_BLU-, DP1_LANE2- and TMDS1_DATA0-.	O PCIE		
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with SDVO1_CK+, DP1_LANE3+ and TMDS1_CLK+. Multiplexed with SDVO1_CK-, DP1_LANE3- and TMDS1_CLK-.	O PCIE		
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	Multiplexed with SDVO1_INT+. Multiplexed with SDVO1_INT-.			
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	Multiplexed with SDVO1_TVCLKIN+. Multiplexed with SDVO1_TVCLKIN-.			
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	Multiplexed with SDVO1_FLDSTALL+. Multiplexed with SDVO1_FLDSTALL-.			
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD.	I 3.3V	PD 1M	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with SDVO1_CTRLCLK, DP1_AUX+ and HMDI1_CTRLCLK. DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	 I/O PCIE I/O OD 3.3V	PD100k	
DDI1_CTRLDATA_AUX-	D16	Multiplexed with SDVO1_CTRLDATA, DP1_AUX- and HDMI1_CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	 I/O PCIE I/O OD 3.3V	PU 100k 3.3V	DDI1_CTRLDATA_AUX- is a boot strap signal (see not below). DDI enable strap already populated.
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1M	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+ and TMDS2_DATA2+. Multiplexed with DP2_LANE0- and TMDS2_DATA2-.	O PCIE		
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+ and TMDS2_DATA1+. Multiplexed with DP2_LANE1- and TMDS2_DATA1-.	O PCIE		
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+ and TMDS2_DATA0+. Multiplexed with DP2_LANE2- and TMDS2_DATA0-.	O PCIE		
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+ and TMDS2_CLK+. Multiplexed with DP2_LANE3- and TMDS2_CLK-.	O PCIE		
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD.	I 3.3V	PD 1M	
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+ and HDMI2_CTRLCLK. DP AUX+ function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	 I/O PCIE I/O OD 3.3V	PD 100k	
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA. DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	 I/O PCIE I/O OD 3.3V	PU 100k 3.3V	DDI2_CTRLCLK_AUX- is a boot strap signal (see note below). DDI enable strap already populated.

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V		
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+. Multiplexed with DP3_LANE0- and TMDS3_DATA2-.	O PCIE		
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+. Multiplexed with DP3_LANE1- and TMDS3_DATA1-.	O PCIE		
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+. Multiplexed with DP3_LANE2- and TMDS3_DATA0-.	O PCIE		
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+. Multiplexed with DP3_LANE3- and TMDS3_CLK-.	O PCIE		
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3_HPD.	I 3.3V	PD 1M	
DDI3_CTRLCLK_AUX+	C36	Multiplexed with DP3_AUX+ and HDMI3_CTRLCLK. DP AUX+ function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high	 I/O PCIE I/O OD 3.3V	PD 100k	
DDI3_CTRLDATA_AUX-	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA. DP AUX- function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high.	 I/O PCIE I/O OD 3.3V	PU 100k	DDI3_CTRLDATA_AUX- is a boot strap signal (see note below). DDI enable strap already populated.
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V	PD 1M	

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 9.5 of this user's guide.

The Digital Display Interface (DDI) signals are multiplexed with HDMI, DisplayPort (DP) and SDVO. The signals for these interfaces are routed to the DDI interface of the COM Express connector. Refer to the SDVO, HDMI and DisplayPort signal description tables in this section for information about the signals routed to the DDI interface of the COM Express connector.

Table 23 SDVO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDVO1_RED+ SDVO1_RED-	D26 D27	Serial Digital Video red output differential pair. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0- pair.	O PCIE		
SDVO1_GRN+ SDVO1_GRN-	D29 D30	Serial Digital Video green output differential pair. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-.	O PCIE		
SDVO1_BLU+ SDVO1_BLU-	D32 D33	Serial Digital Video blue output differential pair. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
SDVO1_CK+ SDVO1_CK-	D36 D37	Serial Digital Video clock output differential pair. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
SDVO1_INT+ SDVO1_INT-	C25 C26	Serial Digital Video Interrupt input differential pair. .Multiplexed with DDI1_PAIR4+ and DDI1_PAIR4-.	I PCIE		
SDVO1_TVCLKIN+ SDVO1_TVCLKIN-	C29 C30	Serial Digital Video TVOUT synchronization clock pair. Multiplexed with DDI1_PAIR5+ and DDI1_PAIR5-.	I PCIE		
SDVO1_FLDSTALL+ SDVO1_FLDSTALL-	C15 C16	Serial Digital Video Field Stall input differential pair. Multiplexed with DDI1_PAIR6+ and DDI1_PAIR6-.	I PCIE		
SDVO1_CTRLCLK	D15	SDVO I²C clock line - to set up SDVO peripherals. Multiplexed with DDI1_CTRLCLK_AUX+.	I/O OD 3.3V	PD 100k	
SDVO1_CTRLDATA	D16	SDVO I²C data line - to set up SDVO peripherals. Multiplexed with DDI1_CTRLDATA_AUX-.	I/O OD 3.3V	PU 100k 3.3V	SDVO1_CTRLDATA is a boot strap signal (see note below). SDVO enable strap already populated.

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 9.5 of this user's guide.

Table 24 HDMI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS1_CLK + TMDS1_CLK -	D36 D37	HDMI/DVI TMDS Clock output differential pair. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
TMDS1_DATA0+ TMDS1_DATA0-	D32 D33	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
TMDS1_DATA1+ TMDS1_DATA1-	D29 D30	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-..	O PCIE		
TMDS1_DATA2+ TMDS1_DATA2-	D26 D27	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
HDMI1_HPD	C24	HDMI/DVI Hot-plug detect. Multiplexed with DDI1_HPD.	I PCIE	PD 1M	
HDMI1_CTRLCLK	D15	HDMI/DVI I²C Control Clock Multiplexed with DDI1_CTRLCLK_AUX+	I/O OD 3.3V	PD 100k	
HDMI1_CTRLDATA	D16	HDMI/DVI I²C Control Data Multiplexed with DDI1_CTRLDATA_AUX-	I/O OD 3.3V	PU 100k 3.3V	HDMI1_CTRLDATA is a boot strap signal (see note below). HDMI enable strap already populated
TMDS2_CLK + TMDS2_CLK -	D49 D50	HDMI/DVI TMDS Clock output differential pair.. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-.	O PCIE		
TMDS2_DATA0+ TMDS2_DATA0-	D46 D47	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-.	O PCIE		
TMDS2_DATA1+ TMDS2_DATA1-	D42 D43	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-.	O PCIE		
TMDS2_DATA2+ TMDS2_DATA2-	D39 D40	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-..	O PCIE		
HDMI2_HPD	D44	HDMI/DVI Hot-plug detect. Multiplexed with DDI2_HPD	I PCIE	PD 1M	
HDMI2_CTRLCLK	C32	HDMI/DVI I²C Control Clock Multiplexed with DDI2_CTRLCLK_AUX+	I/O OD 3.3V	PD 100k	
HDM12_CTRLDATA	C33	HDMI/DVI I²C Control Data Multiplexed with DDI2_CTRLDATA_AUX-	I/O OD 3.3V	PU 100k 3.3V	HDMI2_CTRLDATA is a boot strap signal (see note below). HDMI enable strap is already populated.
TMDS3_CLK + TMDS3_CLK -	C49 C50	HDMI/DVI TMDS Clock output differential pair.. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		
TMDS3_DATA0+ TMDS3_DATA0-	C46 C47	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		
TMDS3_DATA1+ TMDS3_DATA1-	C42 C43	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-..	O PCIE		
TMDS3_DATA2+ TMDS3_DATA2-	C39 C40	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		
HDMI3_HPD	C44	HDMI/DVI Hot-plug detect. Multiplexed with DDI3_HPD.	I PCIE	PD 1M	
HDMI3_CTRLCLK	C36	HDMI/DVI I²C Control Clock Multiplexed with DDI3_CTRLCLK_AUX+	I/O OD 3.3V	PD 100k	

Signal	Pin #	Description	I/O	PU/PD	Comment
HDMI3_CTRLDATA	C37	HDMI/DVI I²C Control Data Multiplexed with DDI3_CTRLDATA_AUX-	I/O OD 3.3V	PU 100k 3.3V	HDMI3_CTRLDATA is a boot strap signal (see note below). HDMI enable strap is already populated.

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 9.5 of this user's guide.

Table 25 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP1_LANE3+ DP1_LANE3-	D36 D37	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
DP1_LANE2+ DP1_LANE2-	D32 D33	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
DP1_LANE1+ DP1_LANE1-	D29 D30	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-.	O PCIE		
DP1_LANE0+ DP1_LANE0-	D26 D27	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
DP1_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI1_HPD.	I 3.3V	PD 1M	
DP1_AUX+	D15	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP1_AUX-	D16	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	DP1_AUX- is a boot strap signal (see note below). DP enable strap is already populated.
DP2_LANE3+ DP2_LANE3-	D49 D50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O PCIE		
DP2_LANE2+ DP2_LANE2-	D46 D47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O PCIE		
DP2_LANE1+ DP2_LANE1-	D42 D43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O PCIE		
DP2_LANE0+ DP2_LANE0-	D39 D40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR0+ and DDI1_PAIR0-	O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
DP2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI2_HPD.	I 3.3V	PD 1M	
DP2_AUX+	C32	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP2_AUX-	C33	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	DP2_AUX- is a boot strap signal (see note below). DP enable strap already populated.
DP3_LANE3+ DP3_LANE3-	C49 C50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		
DP3_LANE2+ DP3_LANE2-	C46 C47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		
DP3_LANE1+ DP3_LANE1-	C42 C43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-.	O PCIE		
DP3_LANE0+ DP3_LANE0-	C39 C40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		
DP3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI3_HPD.	I 3.3V	PD 1M	
DP3_AUX+	C36	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP3_AUX-	C37	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	DP3_AUX- is a boot strap signal (see note below). DP enable strap already populated.

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 9.5 of this user's guide.

Table 26 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# / TYPE1# / TYPE0# X / X / X — Pinout Type 1 NC / NC / NC — Pinout Type 2 NC / NC / GND — Pinout Type 3 (no IDE) NC / GND / NC — Pinout Type 4 (no PCI) NC / GND / GND — Pinout Type 5 (no IDE, no PCI) GND / NC / NC — Pinout Type 6 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.	PDS	TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard. The conga-TM67/TS67 is based on the COM Express Type 6 pinout therefore the pins 0 and 1 are not connected and pin 2 is connected to GND.
TYPE10#	A97	Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed. TYPE10# NC — Pinout R2.0 PD — Pinout Type 10 pull down to ground with 4.7k resistor 12V — Pinout R1.0 This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7k resistor.	PDS	Not connected to indicate "Pinout R2.0".

Table 27 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

9.4 C-D Connector Pinout

Table 28 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1-	D56	PEG_TX1-
C2	GND	D2	GND	C57	TYPE1#	D57	TYPE2#
C3	USB_SSRX0- (*)	D3	USB_SSTX0- (*)	C58	PEG_RX2+	D58	PEG_TX2+
C4	USB_SSRX0+ (*)	D4	USB_SSTX0+ (*)	C59	PEG_RX2-	D59	PEG_TX2-
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1- (*)	D6	USB_SSTX1- (*)	C61	PEG_RX3+	D61	PEG_TX3+
C7	USB_SSRX1+ (*)	D7	USB_SSTX1+ (*)	C62	PEG_RX3-	D62	PEG_TX3-
C8	GND	D8	GND	C63	RSVD	D63	DDPC_CTRLCLK
C9	USB_SSRX2- (*)	D9	USB_SSTX2- (*)	C64	RSVD	D64	DDPC_CTRLDATA
C10	USB_SSRX2+ (*)	D10	USB_SSTX2+ (*)	C65	PEG_RX4+	D65	PEG_TX4+
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4-	D66	PEG_TX4-
C12	USB_SSRX3- (*)	D12	USB_SSTX3- (*)	C67	RSVD	D67	GND
C13	USB_SSRX3+ (*)	D13	USB_SSTX3+ (*)	C68	PEG_RX5+	D68	PEG_TX5+
C14	GND	D14	GND	C69	PEG_RX5-	D69	PEG_TX5-
C15	DDI1_PAIR6+	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	DDI1_PAIR6-	D16	DDI1_CTRLDATA_AUX-	C71	PEG_RX6+	D71	PEG_TX6+
C17	RSVD	D17	RSVD	C72	PEG_RX6-	D72	PEG_TX6-
C18	RSVD	D18	RSVD	C73	GND	D73	GND
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	PEG_RX7+	D74	PEG_TX7+
C20	PCIE_RX6-	D20	PCIE_TX6-	C75	PEG_RX7-	D75	PEG_TX7-
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+ (*)	D22	PCIE_TX7+ (*)	C77	RSVD	D77	RSVD
C23	PCIE_RX7- (*)	D23	PCIE_TX7- (*)	C78	PEG_RX8+	D78	PEG_TX8+
C24	DDI1_HPD	D24	RSVD	C79	PEG_RX8-	D79	PEG_TX8-
C25	DDI1_PAIR4+	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)
C26	DDI1_PAIR4-	D26	DDI1_PAIR0+	C81	PEG_RX9+	D81	PEG_TX9+
C27	RSVD	D27	DDI1_PAIR0-	C82	PEG_RX9-	D82	PEG_TX9-
C28	RSVD	D28	RSVD	C83	RSVD	D83	RSVD
C29	DDI1_PAIR5+	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	DDI1_PAIR5-	D30	DDI1_PAIR1-	C85	PEG_RX10+	D85	PEG_TX10+
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10-	D86	PEG_TX10-
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+	C87	GND	D87	GND
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-	C88	PEG_RX11+	D88	PEG_TX11+
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11-	D89	PEG_TX11-
C35	RSVD	D35	RSVD	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+	C91	PEG_RX12+	D91	PEG_TX12+
C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-	C92	PEG_RX12-	D92	PEG_TX12-

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C38	DDI3_DDC_AUX_SEL	D38	RSVD	C93	GND	D93	GND
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+	C94	PEG_RX13+	D94	PEG_TX13+
C40	DDI3_PAIR0-	D40	DDI2_PAIR0-	C95	PEG_RX13-	D95	PEG_TX13-
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+	C97	RVSD	D97	RSVD
C43	DDI3_PAIR1-	D43	DDI2_PAIR1-	C98	PEG_RX14+	D98	PEG_TX14+
C44	DDI3_HPD	D44	DDI2_HPD	C99	PEG_RX14-	D99	PEG_TX14-
C45	RSVD	D45	RSVD	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+	C101	PEG_RX15+	D101	PEG_TX15+
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-	C102	PEG_RX15-	D102	PEG_TX15-
C48	RSVD	D48	RSVD	C103	GND	D103	GND
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3-	D50	DDI2_PAIR3-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+	D52	PEG_TX0+	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0-	D53	PEG_TX0-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV#	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+	D55	PEG_TX1+	C110	GND (FIXED)	D110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-TM67/TS67.

9.5 Boot Strap Signals

Table 29 Boot Strap Signal Descriptions

Signal	Pin #	Description of Boot Strap Signal	I/O	PU/PD	Comment
AC/HDA_SYNC	A29	**High Definition Audio Sync:** This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3VSB	PU 1K 3.3VSB	AC/HDA_SYNC is a boot strap signal (see caution statement below)
AC/HDA_SDOUT	A33	**High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for High Definition Audio.	O 3.3VSB	PU 1K 3.3VSB	AC/HDA_SDOUT is a boot strap signal (see caution statement below)
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	LVDS_I2C_DAT is a boot strap signal (see caution statement below).
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		SPKR is a boot strap signal (see caution statement below)
PEG_LAN_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order	I 3.3V	PU 10k 3.3V	PEG_LANE_RV# is a boot strap signal (see caution statement below).
DDI1_CTRLDATA_AUX-SDVO1_CTRLDATA DP1_AUX-HDMI_CTRLDATA	D16	Multiplexed with SDVO1_CTRLDATA, DP1_AUX- and HDMI1_CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3V	PU100k 3.3V	DDI1_CTRLDATA_AUX- is a boot strap signal (see caution statement below).
DDI2_CTRLDATA_AUX-DP2_AUX-HDM2_CTRLDATA	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA. DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3V	PU100k 3.3V	DDI2_CTRLDATA_AUX- is a boot strap signal (see caution statement below).
DDI3_CTRLDATA_AUX-DP3_AUX-HDM3_CTRLDATA	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA. DP AUX- function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PU100k 3.3V	DDI3_CTRLDATA_AUX- is a boot strap signal (see caution statement below).

Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either COM Express™ internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM Express™ module to malfunction and/or cause irreparable damage to the module.

10 System Resources

10.1 System Memory Map

Table 30 Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(TOM-xxxx) – TOM	N.A.	N.A.	ACPI reclaim, PCI memory range, Video, ….
1024kB – (TOM-xxxx)	100000 – N.A	N.A.	Extended memory
869kB – 1024kB	E0000 - FFFFF	128kB	Runtime BIOS
768kB – 896kB	C0000 - DFFFF		Expansion Area
640kB – 768kB	A0000 - BFFFF	128kB	Video memory and BIOS
639kB – 640kB	9FC00 - 9FFFF	1kB	Extended BIOS data
0 – 639kB	00000 - 9FC00	512kB	Conventional memory

Note

T.O.M. = Top of memory = max. DRAM installed

10.2 I/O Address Assignment

The I/O address assignment of the conga-TM67/TS67 module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed in the table below.

Table 31 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000 - 00FF	256 bytes	No	Motherboard resources
03B0 – 03DF	16 bytes	No	Video system
0400 - 047F	128 bytes	No	Motherboard resources
0500 - 057F	128 bytes	No	Motherboard resources
0CF8 - 0CFB	4 bytes	No	PCI configuration address register
0CFC - 0CFF	4 bytes	No	PCI configuration data register
0D00 – FFFF		See note	PCI / PCI Express bus

Note

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

10.2.1 LPC Bus

On the conga-TM67/TS67, the PCI Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Bus not the LPC Bus. Only specified I/O ranges are forwarded to the LPC Bus. In the congatec Embedded BIOS the following I/O address ranges are sent to the LPC Bus:

3F8 – 3FF
3E8 – 3EF
A00 - A0F

Parts of these ranges are not available if a Super I/O is used on the carrier board. If a Super I/O is not implemented on the carrier board, then these ranges are available for customer use. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

10.3 Interrupt Request (IRQ) Lines

Table 32 IRQ Lines in PIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		IRQ3 via SERIRQ or PCI BUS INTx
4	Yes		IRQ4 via SERIRQ or PCI BUS INTx
5	Yes		IRQ5 via SERIRQ or PCI BUS INTx
6	Yes		IRQ6 via SERIRQ or PCI BUS INTx
7	Yes		IRQ7 via SERIRQ or PCI BUS INTx
8	No	Real-time Clock	Not applicable
9	No	SCI	Not applicable
10	Yes		IRQ10 via SERIRQ or PCI BUS INTx
11	Yes		IRQ11 via SERIRQ or PCI BUS INTx
12	Yes		IRQ12 via SERIRQ or PCI BUS INTx
13	No	Math processor	Not applicable
14	Yes		PCI BUS INTx
15	Yes		PCI BUS INTx

Note

In PIC mode, the PCI bus interrupt lines can be routed to any free IRQ.

Table 33 IRQ Lines in APIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin / Function
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		IRQ3 via SERIRQ
4	Yes		IRQ4 via SERIRQ
5	Yes		IRQ5 via SERIRQ
6	Yes		IRQ6 via SERIRQ
7	Yes		IRQ7 via SERIRQ
8	No	Real-time Clock	Not applicable
9	No	SCI	SCI
10	Yes		IRQ10 via SERIRQ
11	Yes		IRQ11 via SERIRQ
12	Yes		IRQ12 via SERIRQ
13	No	Math processor	Not applicable
14	Yes		
15	Yes		
16	No		PIRQA, PCI Bus INTB, Integrated VGA Controller, PCI Express Root Port 0, PCI Express Root Port 4, EHCI Host Controller 2
17	No		PIRQB, PCI Bus INTC, PCI Express Root Port 1, PCI Express Root Port 5
18	No		PIRQC, PCI Bus INTD, PCI Express Root Port 2, SMBus Controller
19	No		PIRQD, PCI Bus INTA, PCI Express Root Port 3, Serial ATA Host Controller 1, Serial ATA Host Controller 2
20	Yes		PIRQE, onboard Gigabit LAN Controller
21	Yes		PIRQF
22	Yes		PIRQG, Intel High Definition Audio Controller
23	Yes		PIRQH, EHCI Host Controller 1

Note

In APIC mode, the PCI bus interrupt lines are connected with IRQ 16, 17, 18 and 19.

10.4 PCI Configuration Space Map

Table 34 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	02h	00h	Internal	VGA Graphics
00h	06h	00h	Internal	PCI Express Graphic (PEG) Port
00h(Note1)	16h	00h	Internal	Management Engine (ME) Interface 1
00h(Note1)	16h	01h	Internal	Intel ME Interface 2
00h(Note1)	16h	02h	Internal	ME IDE Redirection (IDE-R) Interface
00h(Note1)	16h	03h	Internal	ME KT (Remote Keyboard and Text)
00h	19h	00h	Internal	Onboard Gigabit LAN Controller
00h	1Ah	00h	Internal	EHCI Host Controller 2
00h	1Bh	00h	Internal	Intel High Definition Audio Controller
00h	1Ch	00h	Internal	PCI Express Root Port 0
00h(Note2)	1Ch	01h	Internal	PCI Express Root Port 1
00h (Note2)	1Ch	02h	Internal	PCI Express Root Port 2
00h (Note2)	1Ch	03h	Internal	PCI Express Root Port 3
00h (Note2)	1Ch	04h	Internal	PCI Express Root Port 4
00h (Note2)	1Ch	05h	Internal	PCI Express Root Port 5
00h	1Ch	07h	Internal	PCI Express Root Port 7
00h	1Dh	00h	Internal	EHCI Host Controller 1
00h	1Fh	00h	N.A.	PCI to LPC Bridge
00h	1Fh	02h	Internal	Serial ATA Controller 1
00h	1Fh	03h	Internal	SMBus Host Controller
00h	1Fh	05h	Internal	Serial ATA Controller 2
00h	1Fh	06h	Internal	Thermal Subsystem
01h (Note3)	00h	00h	Internal	PEG Port
02h (Note3)	00h	00h	Internal	PCI Express Port 0
03h (Note3)	00h	00h	Internal	PCI Express Port 1
04h (Note3)	00h	00h	Internal	PCI Express Port 2
05h (Note3)	00h	00h	Internal	PCI Express Port 3
06h (Note3)	00h	00h	Internal	PCI Express Port 4
07h (Note3)	00h	00h	Internal	PCI Express Port 5
08h (Note3)	00h	00h	Internal	PCI Express Port 6

Note

1. In the standard configuration the Intel Management Engine (ME) related devices are partially present or not present at all.

2. The PCI Express Ports are visible only if a device is attached behind them to the PCI Express Slot on the carrier board.

3. *The table represents a case when a single function PCI/PCIe device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*

10.5 PCI Interrupt Routing Map

Table 35 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line [1]	APIC Mode IRQ	VGA	HDA	EHCI 1	EHCI 2	SM Bus	LAN	SATA1	SATA2	PEG Root Port	PEG Port
A	INTA	16	x			x						x [2]
B	INTB	17										x [3]
C	INTC	18					x					x [4]
D	INTD	19							x	x	x	x [5]
E		20						x				
F		21										
G		22		x								
H		23			x							

PIRQ	PCI-EX Root Port 0	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Root Port 3	PCI-EX Root Port 4	PCI-EX Root Port 5	PCI-EX Root Port 7	PCI-EX Port 0	PCI-EX Port 1	PCI-EX Port 2	PCI-EX Port 3	PCI-EX Port 4	PCI-EX Port 5	PCI-EX Port 6
A	x				x			x [2]	x [5]	x [4]	x [3]	x [2]	x [5]	x [3]
B		x				x		x [3]	x [2]	x [5]	x [4]	x [3]	x [2]	x [4]
C			x					x [4]	x [3]	x [2]	x [5]	x [4]	x [3]	x [5]
D				x			x	x [5]	x [4]	x [3]	x [2]	x [5]	x [4]	x [2]
E														
F														
G														
H														

Note

[1] *These interrupt lines are virtual (message based)*

[2] *Interrupt used by single function PCI Express devices (INTA).*

[3] *Interrupt used by multifunction PCI Express devices (INTB).*

[4] *Interrupt used by multifunction PCI Express devices (INTC).*

[5] *Interrupt used by multifunction PCI Express devices (INTD).*

10.6 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

10.7 SM Bus

System Management (SM) bus signals are connected to the Intel® BD82QM67 or BD82HM65 (QM67 or HM65) PCH and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

11 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

11.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <F2> key during POST.

11.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used, a selection will be displayed immediately after POST allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

11.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

Main	Advanced	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

Note

Entries in the option column that are displayed in bold print indicate BIOS default values.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

11.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
Main BIOS Version	no option	Displays the main BOIS version.
OEM BIOS Version	no option	Displays the additional OEM BIOS version.
Build Date	no option	Displays the date the BIOS was built.
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
Running Time	no option	Displays the time the board is running [in hours max. 65535].
►Platform Information	submenu	Opens the platform information submenu.
System Date	Day of week, month/ day/year	Specifies the current system date *Note: The date is in month/day/year format.*
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24-hour format.*

11.3.1 Platform Information

The platform information submenu offers additional hardware and software information.

Feature	Options	Description
Processor Type	no option	Displays the processor ID string. The “Processor Type” text itself is not displayed just the ID string.
Processor Speed	no option	Displays the processor speed.
Processor Signature	no option	Displays the processor signature.
Microcode Revision	no option	Displays the processor microcode revision .
Processor Cores	no option	Displays the number of processor cores.
IGD VBIOS Version	no option	Displays the video BIOS version.
IGD HW Version	no option	Displays the version of the graphics controller.
Total Memory	no option	Displays the total amount of installed memory.
Memory Slot0	no option	Displays the amount of installed memory in the top memory slot.
Memory Slot2	no option	Displays the amount of installed memory in the bottom memory slot.
PCH Name	no option	Displays the name of the platform controller hub.
PCH Version	no option	Displays the version of the platform controller hub.

11.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features and only features described within this user’s guide are listed.

Main	Advanced	Boot	Security	Save & Exit
	Graphics Configuration			
	Watchdog Configuration			
	Hardware Health Monitoring			
	PCI & PCI Express Configuration			
	ACPI Settings			
	RTC Wake Settings			
	Trusted Computing Configuration (*)			
	CPU Configuration			
	Chipset Configuration			
	SATA Configuration			
	Intel TXT(LT) Configuration (*)			
	ME Firmware Configuration (*)			
	ME/AMT Configuration (*)			

Main	Advanced	Boot	Security	Save & Exit
	USB Configuration			
	Super IO Configuration			
	Serial Port Console Redirection			

Note

The features marked with an asterisk symbol are only available in BIOS version BQ67R6xx or BQ67R7xx.

11.4.1 Graphics Configuration Submenu

Feature	Options	Description
Primary Graphics Device	Auto **IGD** PEG PCI/PCIe	Select primary graphics adapter to be used during boot up. Auto: BIOS will select it automatically. IGD: Internal Graphics Device (IGD) located in Chipset. PEG: External PCI Express Graphics card attached to the x16 PEG port. PCI/PCIe: Standard PCI Express or PCI Graphics Device
IGD Pre-Allocated Graphics Memory	0M, 32M**, 64M**, 96M, 128M, 160M, 192M, 224M, 256M, 288M, 320M, 352M, 384M, 416M, 448M, 480M, 512M	Select amount of pre-allocated (fixed) graphics memory used by the Internal Graphics Device.
IGD Total Graphics Memory	128MB **256MB** MAX	Select amount of total graphics memory that maybe used by the Internal Graphics Device. Memory above the fixed graphics memory will be dynamically allocated by the graphics driver according to DVMT 5.0 specification. MAX = Use as much graphics memory as possible. Depends on total system memory installed and the operating system used (see DVMT 5.0 specification).
Primary IGD Boot Display Device	**Auto** CRT LFP EFP EFP2 EFP3	Select the Primary IGD display device(s) used for boot up. CRT selects Analog VGA display port. LFP (Local Flat Panel) selects a LVDS panel connected to the integrated LVDS port. EFPx (External Flat Panel) selects a HDMI/DVI or DisplayPort device connected to the display ports B, C or D. Examples for EFPx name assignment to port B, C, D: 1. If only IGD port C is enabled that the EFP name is assigned to port C. 2. If both port B and C is enabled than EFP is assigned to port B and EFP2 is assigned to port C.
Secondary IGD Boot Display Device	**Disabled** CRT LFP EFP EFP2 EFP3	Select the Secondary IGD display device(s) used for boot up. VGA modes will be supported only on Primary display. For other details see Primary IGD Boot Display Device.
Active LFP Configuration	No Local Flat Panel **Integrated LVDS**	Select the active local flat panel configuration.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel. When no external EDID data set can be found, then the data set selected under 'Local Flat Panel Type' will be used as a fallback data set.

Feature	Options	Description
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. *Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.*
Backlight Inverter Type	None **PWM** I2C	Select the type of backlight inverter used. PWM = Use IGD PWM signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.
PWM Inverter Polarity	**Normal** Inverted	Select PWM inverter polarity. Only visible if Backlight Inverter Type is set to PWM.
PWM Inverter Frequency	**200** - 40000	Set the PWM inverter frequency in Hz. Only visible if Backlight Inverter Type is set to PWM.
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100%**	Actual backlight value in percent of the maximum setting.
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Setting	**No** Yes	Allow to invert backlight control values if required for the actual I2C type backlight hardware controller.
Display Port B Interface	**Disabled** SDVO Display Port HDMI/DVI	Select the interface the physical display port should offer.
Select SDVO Device	**SDVO DVI**	Only SDVO DVI supported.
Display Port C Interface	**Disabled** Display Port HDMI/DVI	Select the interface the physical display port should offer.
Display Port D Interface	**Disabled** Display Port HDMI/DVI	Select the interface the physical display port should offer.
Display Mode Persistence	**Disabled** Enable	Display mode persistence means that previous display device configurations can be ‘remembered’ and restored by the system. E.g. a dual view DVI configuration will automatically be restored if both DVI monitors are connected again even if during an earlier boot only one DVI monitor had been connected and active.

11.4.2 Watchdog Configuration Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset..
Stop Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One-time Trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to '*One-time Trigger'* the watchdog will be disabled after the first trigger. If set to *'Single Event'*, every stage will be executed only once, then the watchdog will be disabled. If set to *'Repeated Event'* the last stage will be executed repeatedly until a reset occurs.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	ACPI Event **Reset** Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about ACPI Event, see note below.
Event 2	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Selects the timeout value for the first stage watchdog event.

Feature	Options	Description
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

Note

In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason, the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

Additionally, the conga-TM67/TS67 modules do not support the watchdog NMI mode. COM Express type 6 modules do not support the PCI bus and therefore the PCI_SERR# signal is not available. There is no way to drive a NMI to the processor without the presence of the PCI_SERR# PCI bus signal.

11.4.3 Hardware Health Monitoring

Feature	Options	Description
CPU Temperature	no option	Displays the actual CPU Temperature in °C.
Board Temperature 1	no option	Displays the actual Board Temperature 1 in °C.
Board Temperature 2	no option	Displays the actual Board Temperature 2 in °C.
Board Temperature 3	no option	Displays the actual Board Temperature 3 in °C.
12V Standard	no option	Displays the actual voltage of the 12V Standard power supply.
5V Standby	no option	Displays the actual voltage of the 5V Standby power supply.
CPU Fan Speed	no option	Displays the actual CPU Fan Speed in RPM.
Fan PWM Frequency Mode	**Low Frequency** High Frequency	Select fan PWM base frequency mode. Low frequency: 35.3Hz High frequency: 22.5kHz
Continuous Tacho Reading	Disabled **Enabled**	If enabled, the fan tacho pulses are measured continuously instead of once per second. Helps to avoid audible 'pulsing' of the fan as the speed would be set to 100% for a very short time during measurement.
Pulses Per Revolution	1, 2, 3, 4	Select number of pulses per revolution generated by the attached fan.
Automatic Fan Speed Control	Disabled **Enabled**	Enable hardware fan speed control. Independent from any operating system the fan will be turned on once a certain start temperature is reached and linearly ramped up to the defined maximum speed within the given temperature range.
Fan Control Temperature	**CPU Temperature** Board Temperature 1 Board Temperature 2 Board Temperature 3	Select which temperature input is used for the automatic fan speed control.

Feature	Options	Description
Start Temperature	30, 40, 50, **60**, 70, 80, 90, 100°C	At this temperature the fan will be turned on at the defined minimum fan speed.
Temperature Range	5, 10, 15, 20, 25, **30**, 40, 55, 80°C	Within this temperature range the fan will ramp up to the defined maximum fan speed.
Minimum Fan Speed	Fan Off, 10%, 15%, 20%, 25%, 30%, 35%, 40%, 45%, **50%**, 55%, 60%, 65%, 70%, 75%, 80%, 85%, 90%, 95%, 100%	Select minimum/start fan speed to be set when the start temperature of the control slope is reached.
Maximum Fan Speed	Fan Off, 10%, 15%, 20%, 25%, 30%, 35%, 40%, 45%, 50%, 55%, 60%, 65%, 70%, 75%, 80%, 85%, 90%, 95%, **100%**	Select maximum/end fan speed to be ramped up to until the end temperature of the control slope is reached.
Fan Always On At Minimum Speed	**Disabled** Enabled	If enabled, the fan will always run at least at the selected minimum speed, even if the control temperature is below the fan control start temperature. This is to ensure a minimum air flow all the time.

11.4.4 PCI & PCI Express Configuration Submenu

Feature	Options	Description
PCI ROM Priority	Legacy ROM **EFI Compatible ROM**	Specify which PCI option ROM to launch in case that multiple option ROMs (legacy and EFI compatible) are present.
Launch PXE Option ROM	**Disabled** Enabled	Enable or disable start of PXE option ROMs for legacy network devices.
Launch Storage Option ROM	Disabled **Enabled**	Enable or disable start of option ROMs for legacy mass storage devices.
PCI Settings		
PCI Latency Timer	**32**, 64, 96, 128, 160, 192, 224, 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
VGA Palette Snoop	**Disabled** Enabled	Enable or disable VGA palette registers snooping.
Generate EXCD0/1_PERST#	Disabled 1ms 5ms **10ms** 50ms 100ms 150ms 200ms 250ms	Select whether the COM Express EXCD0_PERST# and EXCD1_PERST# pins should be driven low during POST or how long if it will be, if enabled.
Early Initialization Delay	**Disabled** 200ms, 400ms, 1s, 2s, 5s, 10s, 20s, 30s, 40s, 50s	Add Additional boot delay at early POST before PCI/PCI Express initialization. Meant to grant slow external PCI Express devices additional time to power up.
PCI Express Device & Link Settings		
Relaxed Ordering	**Disabled** Enabled	Enable or disable PCI Express device relaxed ordering.
Extended Tag	**Disabled** Enabled	If enabled a device may use an 8-bit tag filed as a requester.
No Snoop	Disabled **Enabled**	Enable or disable PCI Express device 'No Snoop' option.
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum payload of PCI Express devices or allow system BIOS to select the value.

Feature	Options	Description
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum read request size of PCI Express devices or allow system BIOS to select the value.
Extended Synch	**Disabled** Enabled	If enabled, the generation of extended PCI Express synchronization patterns is allowed.
►PIRQ Routing & IRQ Reservation	submenu	Manual PIRQ routing and interrupt reservation for legacy devices.
►PCI Express Graphics (PEG) Port	submenu	PCI Express Graphics (PEG) port settings. PEG port is not supported on low end CPUs.
►PCI Express Port 0	submenu	Opens the PCI Express Port submenu
►PCI Express Port 1	submenu	Opens the PCI Express Port submenu
►PCI Express Port 2	submenu	Opens the PCI Express Port submenu
►PCI Express Port 3	submenu	Opens the PCI Express Port submenu
►PCI Express Port 4	submenu	Opens the PCI Express Port submenu
►PCI Express Port 5	submenu	Opens the PCI Express Port submenu
►PCI Express Port 6	submenu	Opens the PCI Express Port submenu

11.4.4.1 PIRQ Routing & IRQ Reservation Submenu

Feature	Options	Description
PIRQA	**Auto**, IRQ3, IRQ4, IRQ5, IRQ6, IRQ10, IRQ11, IRQ14, IRQ15	Set interrupt for selected PIRQ. Please refer to the board's resource list for a detailed list of devices connected to the respective PIRQ. NOTE: These settings will only be effective while operating in PIC (non-IOAPIC) interrupt mode.
PIRQB	Same as PIRQA	Same as PIRQA
PIRQC	Same as PIRQA	Same as PIRQA
PIRQD	Same as PIRQA	Same as PIRQA
PIRQE	Same as PIRQA	Same as PIRQA
PIRQF	Same as PIRQA	Same as PIRQA
PIRQG	Same as PIRQA	Same as PIRQA
PIRQH	Same as PIRQA	Same as PIRQA
Reserve Legacy Interrupt 1	None, IRQ3, IRQ4, IRQ5, IRQ6, IRQ10, IRQ11, IRQ14, IRQ15	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.
Reserve Legacy Interrupt 2	Same as Reserve Legacy Interrupt 1	same as Reserve Legacy Interrupt 1

11.4.4.2 PCI Express Graphics (PEG) Port Submenu

Feature	Options	Description
PEG	no option	Displays the width and the operation mode at which the attached device currently operates. Some Gen2 devices start up in Gen1 mode and just their OS driver sets them to Gen2 mode.
PEG -Gen X	**Auto** Gen1	PEG port (B0:D1:F0) operation mode. Auto = Gen1 (2.5GT/s) or Gen2 (5.0GT/s) Gen1 = 2.5GT/s operation mode Some older non-complaint PCI Express devices will function just if Gen1 is selected.
Always Enable PEG	Disabled **Enabled**	Disabled = Disable the internal PEG interface devices if no device is detected on PEG port. Enabled = Enable the internal PEG interface devices also if no device is detected on PEG port.
PEG ASPM	**Disabled** Auto ASPM L0s ASPM L0sL1	Control ASPM support for the PEG device. This has no effect if PEG is not the currently active device.
De-emphasis Control	-6 dB **-3.5 dB**	Configure the De-emphasis control on the PEG.

11.4.4.3 PCI Express Port Submenu

Feature	Options	Description
PCI Express Port x	Disabled **Enabled**	Enable or disable the respective PCI Express port x.
PME SCI	Disabled **Enabled**	Enable or disable PCI Express PME (power management event) SCI.
Always Enable Port	**Disabled** Enabled	Disabled = Disable the internal PCI Express interface device if no device is detected on the port. Enabled = Enable the internal PCI Express interface device also if no device is detected on the port.

11.4.5 ACPI Configuration Submenu

Feature	Options	Description
Hibernation Support	Disabled **Enabled**	Enable or disable system ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system sleep/suspend.
Critical Trip Point	100 /POR, 71, 79, 87, 95, 103, **111**, 119°C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Active Trip Point	**Disabled**, 15, 23, 31, 39, 47, **55**, 63, 71, 79, 87, 95, 103, 111, 119°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.

Feature	Options	Description
Passive Trip Point	Disabled, 15, 23, 31, 39, 47, 55, 63, 71, 79, 87, 95, 103, 111, **119**°C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling. This method of Passive cooling is not recommended. The preferred method of passive cooling is the setting of the TCC active offset in CPU Configuration menu.
LID Button Support	**Disabled** Enabled	Configure COM Express LID# Signal to act as ACPI LID button.
Sleep Button Support	**Disabled** Enabled	Configure COM Express SLEEP# Signal to act as ACPI Sleep button.

11.4.6 RTC Wake Settings Submenu

Feature	Options	Description
Wake System AT Fixed Time	**Disabled** Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour		Specify wake up hour
Wake up minute		Specify wake up minute
Wake up second		Specify wake up second

11.4.7 Trusted Computing Configuration Submenu

Feature	Options	Description
TPM Support	**Disabled** Enabled	Enable or disable TPM support. System reset is required after change.
TPM State	**Disabled** Enabled	Enable or disable TPM Chip Note: System might restart several times during POST to acquire target state.
Pending TPM Operation	None, Enable Take Ownership, Disable Take Ownership, TPM Clear	Perform selected TPM chip operation Note: System might restart several times during POST to perform selected operation.

Note

This menu is only available in BIOS version BQ67R6xx or BQ67R7xx.

11.4.8 CPU Configuration Submenu

Feature	Options	Description
Active Processor Cores	**All** 1 2 3	Set number of cores to be enabled.
Hyper-Threading	Disabled **Enabled**	Enable or disable Hyper-Threading support.
Execute Disable Bit	Disabled **Enabled**	Enable or disable the Execute Disable Bit (XD) of the processor. With the XD bit set to enabled certain classes of malicious buffer overflow attacks can be prevented when combined with a supporting OS.
Limit CPUID Maximum	**Disabled** Enabled	When **enabled**, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When **disabled**, the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Hardware Prefetcher	Disabled **Enabled**	Enable or disable the Mid Level Cache (MLC) streamer prefetcher.
Adjacent Cache Line Prefetch	Disabled **Enabled**	Enable or disable prefetching of adjacent cache lines.
Intel Virtualization Technology	Disabled **Enabled**	Enable or disable support for the Intel virtualization technology.
Memory Remap	Enabled **Disabled**	Enable or disable memory remap above 4GB.
Power Management		
Intel(R) SpeedStep(tm)	Disabled **Enabled**	Disabled: CPU speed is set to maximum and cannot be altered by the operating system. Enabled: CPU speed is controlled by the operating system.
CPU Turbo Mode	Disabled **Enabled**	Disabled: CPU speed cannot be altered by the intel software driver above the CPU nominal operating frequency. Enabled: CPU speed can be altered by the Intel software driver above the CPU nominal operating frequency.
TCC Active Offset	0-15 Default : **0**	Offset from the Intel factory Thermal Control Circuit (TCC) activation temperature. The TCC activation will lower both CPU core and graphics core frequency, voltage or both. The factory TCC activation temperature is normally 100C. So by entering 10 for TCC active offset the TCC will be normally activated at 90C.
CPU C3 Report	**Disabled** Enabled	Enable/Disable CPU C3(ACPI C2) report to OS
CPU C6 Report	**Disabled** Enabled	Enable/Disable CPU C6(ACPI C3) report to OS
CPU C7 Report	**Disabled** Enabled	Enable/Disable CPU C7(ACPI C3) report to OS

11.4.9 Chipset Configuration Submenu

Feature	Options	Description
PCH LAN Controller	**Enabled** Disabled	Enable or disable the onboard, PCH integrated Ethernet controller
Wake On LAN	**Enabled** Disabled	Enable or disable the wake on LAN capability of the onboard, PCH integrated ethernet controller.
HDA Controller	Disabled Enabled **Auto**	Control activation of the HDA controller device. Disabled = HDA controller will be unconditionally disabled Enabled = HDA controller will be unconditionally enabled Auto = HDA Controller will be enabled if HDA codec present, disabled otherwise.
HDA Controller internal HDMI Codec	**Disabled** Enabled	Enable or disable the internal HDMI codec for the HDA Controller.
HDMI codec for Display Port B	**Disabled** Enabled	Enable or disable the internal HDMI codec Port for relevant display port.
HDMI codec for Display Port C	**Disabled** Enabled	Enable or disable the internal HDMI codec Port for relevant display port.
HDMI codec for Display Port D	**Disabled** Enabled	Enable or disable the internal HDMI codec Port for relevant display port.
NB CRID	Enabled **Disabled**	Enable or disable northbridge compatible revision ID support.
SB CRID	**Disabled** Enabled	Enable or disable southbridge compatible revision ID support.
High Precision Timer	Disabled **Enabled**	Enable or disable the high precision event timer (HPET). This timer can be used for precise multimedia or real time application timing. Special software support is required.
PCI Express Clock Gating	**Disabled** Enabled	Enable or disable dynamic PCI Express clock gating for all root ports.
DMI Link ASPM Control	Disabled L0s **L0sL1**	Control active state power management of the DMI link between CPU/GMCH and PCH.

11.4.10 SATA Configuration Submenu

Feature	Options	Description
SATA Controller(s)	**Enabled** Disabled	Enable or disable the onboard SATA controllers.
SATA Mode Selection	**Native IDE** AHCI RAID	Select SATA controller mode. RAID Option is not supported on all chipsets.
SATA Test Mode	Enabled **Disabled**	Should be set to Disabled. Test Mode is used just for verification measurements.
Aggressive LPM Support	**Enabled** Disabled	Enable PCH to aggressively enter link power state.
Alternate ID	Enabled **Disabled**	Report alternate Device ID. Displayed just for RAID SATA Mode.
Serial ATA Port 0, 1, 2, 3	no option	Displays the name of the connected Hard Disk or DVDROM when the port is enabled. Empty is displayed when the port is enabled but nothing is connected to it.
Port 0 ,1, 2, 3	Disabled **Enabled**	Enable or disable the relevant SATA port. Not possible in Native IDE mode.
Hot Plug	**Disabled** Enabled	Select hot plug support for relevant SATA port. Not possible in Native IDE mode.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify if the relevant SATA port is connected to solid state drive or hard disk drive. Not possible in Native IDE mode.
Spin Up Device	**Disabled** Enabled	When enabled the controller runs an initialization sequence for the connected device during startup at relevant SATA port.Not possible in Native IDE mode.

11.4.11 Intel TXT(LT) Configuration Submenu

Feature	Options	Description
CPU Secure Mode Extension (SMX)	**Disabled** Enabled	Indicates support for Intel CPU secure mode extensions. Requires TPM chip.
Intel TXT(LT) Support	**Disabled** Enabled	Intel TXT support requires enabled CPU SMX support as well as active CPU and I/O virtualization technology support.

Note

This menu is only available in BIOS version BQ67R6xx or BQ67R7xx.

11.4.12 ME Firmware Configuration Submenu

Feature	Options	Description
ME FW Version	no option	Displays the Intel management engine firmware version.
ME Firmware Mode	no option	Displays the Intel management engine firmware operating mode.
ME Firmware Type	no option	Displays the Intel management engine firmware type.
ME Firmware SKU	no option	Displays the Intel management engine firmware SKU.

Note

This menu is only available in BIOS version BQ67R6xx or BQ67R7xx.

11.4.13 ME/AMT Configuration Submenu

Feature	Options	Description
Intel ME/AMT BIOS Extension	Disabled **Enabled**	Enable or disable the Intel management engine / active management technology BIOS extension (MEBX). Note: ME/AMT hardware is always enabled. This option only controls the BIOS extension execution.
Intel MEBX Setup Prompt	**Disabled** Enabled	Enable or disable the MEBX setup prompt.
MEBX Hotkey Pressed	**Disabled** Enabled	Enable or disable the MEBX setup hotkey pressed simulation in order to enter the MEBX setup automatically.
MEBX Selection Screen	**Disabled** Enabled	Enable or disable the MEBX submenu selection screen.
Clear ME/AMT Configuration	**Disabled** Enabled	Clear ME and AMT configuration without requiring the MEBX password.
USB Provisioning	Disabled **Enabled**	Enable or disable USB provisioning support.
AMT Wait Timer	**0** - 65535	Define time (in seconds) to wait before sending the ASF (Alert Standard Format) get boot options command for remote boot.
ASF	Disabled **Enabled**	Enable or disable the alert standard format support. It has to be enabled for remote boot support.
Watchdog	**Disabled** Enabled	Enable or disable the ASF watchdog timer.
OS Timer	**0** - 65535	Set OS watchdog timer in seconds.
BIOS Timer	**0** - 65535	Set BIOS watchdog timer in seconds.
CIRA Process	**Disabled** Enabled	Enable or disable the client initiated remote assistance (CIRA) process.
CIRA Timeout	**0** - 255	Define the time to wait for the remote assistance connection to be established. 0 - Use default timeout value of 60 seconds. 255 - MEBX waits until the connection is established.

Note

This menu is only available in BIOS version BQ67R6xx or BQ67R7xx.

11.4.14 USB Configuration Submenu

Feature	Options	Description
USB Devices	no option	Displays the detected USB devices.
EHCI1	Disabled **Enabled**	Enable or disable EHCI controller 1. One EHCI controller must always be enabled.
EHCI2	Disabled **Enabled**	Enable or disable EHCI controller 2. One EHCI controller must always be enabled.
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
►Per-Port Legacy USB Support Control	submenu	Opens the Per-Port Legacy USB Support Control submenu
EHCI Hand-off	Disabled **Enabled**	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device Start Unit command timeout.
USB Transfer Timeout	1 sec 5 sec 10 sec **20 sec**	The timeout value for control, bulk, and interrupt transfers.
Device Power -Up Delay Selection	**Auto** Manual	Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.
Device Power -Up Delay Value	0-40 Default : **5**	Actual power-up delay value in seconds.
USB Mass Storage Device Name (Auto detected USB mass storage devices are listed here dynamically)	**Auto** Floppy Forced FDD Hard Disk CD-ROM	Every USB mass storage device that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. *Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.* Select *AUTO* to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. *Forced FDD* allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. *Hard disk* allows the device to be emulated as hard disk. *CDROM* assumes the CD-ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

11.4.14.1 Per Port Legacy USB Support Control Submenu

Feature	Options	Description
USB0 Port Legacy Support	Disabled **Enabled**	Enable or disable legacy USB support for this port. Enabled is only effective if the port is not disabled with other setting in USB Configuration menu.
USB1 Port Legacy Support	Disabled **Enabled**	Same as USB0 Port Legacy Support
USB2 Port Legacy Support	Disabled **Enabled**	Same as USB0 Port Legacy Support
USB3 Port Legacy Support	Disabled **Enabled**	Same as USB0 Port Legacy Support
USB4 Port Legacy Support	Disabled **Enabled**	Same as USB0 Port Legacy Support
USB5 Port Legacy Support	Disabled **Enabled**	Same as USB0 Port Legacy Support
USB6 Port Legacy Support	Disabled **Enabled**	Same as USB0 Port Legacy Support
USB7 Port Legacy Support	Disabled **Enabled**	Same as USB0 Port Legacy Support

11.4.15 Super I/O Configuration Submenu

Feature	Options	Description
Serial Port 0	Disabled **Enabled**	Enable or disable serial port 0.
Device Settings	IO=3F8h; IRQ=4;	Fixed configuration of serial port 0 if enabled.
Serial Port 1	Disabled **Enabled**	Enable or disable serial port 1.
Device Settings	IO=2F8h; IRQ=3;	Fixed configuration of serial port 1 if enabled.
Parallel Port	**Disabled** Enabled	Enable or disable parallel port.
Device Settings	IO=378h; IRQ=7;	Fixed configuration of the parallel port if enabled.
Device Mode	**Standard Parallel Mode** EPP Mode ECP Mode EPP Mode & ECP Mode	Set the parallel port mode.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

11.4.16 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
►Console Redirection Settings	submenu	Opens console redirection configuration sub menu.
COM1 Console Redirection	**Disabled** Enabled	Enable or disable serial port 1 console redirection.
►Console Redirection Settings	submenu	Opens console redirection configuration sub menu.

11.4.16.1 Console Redirection Settings Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select terminal type.
Baud rate	9600, 19200, 38400, 57600, **115200**	Select baud rate.
Data Bits	7, **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution in UEFI environment.
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.

11.5 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

11.5.1 Boot Settings Configuration

Feature	Options	Description
Quiet Boot	**Disabled** Enabled	Disabled displays normal POST diagnostic messages. Enabled displays OEM logo instead of POST messages. *Note: The default OEM logo is a dark screen.*
Setup Prompt Timeout	**2** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot, 65535 means infinite wait.
POST/Setup VGA Support	**Disabled** Enabled	Select VGA mode for setup and POST screen. Enables setup and POST screen output support for VGA and WVGA display resolutions.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. *Note: Only works with an ATX type power supply.*
Enter Setup If No Boot Device	No **Yes**	*Select whether the setup menu should be started if no boot device is connected.*
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The “Device Based” boot priority list allows you to select from a list of currently detected devices only. The “Type Based” boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the “Device Based” boot priority list might change dynamically in cases when devices are physically removed or added to the system. The “Type Based” boot menu is static and can only be changed by the user.

Feature	Options	Description
1st, 2nd, 3rd, ... Boot Device (Up to 12 boot devices can be prioritized if device based priority list control is selected. If “Type Based” priority list control is enabled only 8 boot devices can be prioritized.)	Disabled SATA 0 Drive SATA 1 Drive SATA 2 Drive SATA 3 Drive PATA Drive USB Floppy USB Hard disk USB CDROM Onboard LAN External LAN Other BEV Device OEM BEV Device	This view is only available when in the default “Type Based” mode. When in “Device Based” mode you will only see the devices that are currently connected to the system.
►USB Boot Control	submenu	Enables or disables the OS boot from some USB port.
GateA20 Active	**Upon Request** Always	Gate A20 control. Upon Request = Gate A20 can be disabled using BIOS services. Always = Do not allow disabling Gate A20.
Option ROM Messages	**Force BIOS** Keep Current	Set display mode for option ROMs.
Interrupt 19 Capture	**Disabled** Enabled	Defines whether option ROMs may trap the INT19h legacy boot vector.

Note

1. *The term ‘AC power loss’ stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

3. *Unlike other module designs available in the embedded market, a CMOS battery is not required by congatec modules to support the ‘Power Loss Control’ feature.*

11.5.1.1 USB Boot Control Submenu

Feature	Options	Description
USB Port x Boot	Disabled **Enabled**	Enables or disables the OS boot from the relevant USB port.

11.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

11.6.1 Security Settings

Feature	Options	Description
Administrator Password	enter password	Specifies the setup administrator password.
HDD Security Configuration		
List of all detected hard disks supporting the security feature set	Select device to open device security configuration submenu	

11.6.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

11.6.3 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen.

You can display an Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.
► **Boot Override** *List of all boot devices currently detected.*	Select device to leave setup menu and boot from the selected device.

12 Additional BIOS Features

The conga-TM67/TS67 uses a congatec/AMI AptioEFI that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as BQ67R1xx or BH67R1xx where:

- BQ67 is the BIOS for modules with the QM67 chipset
- BH67 is the BIOS for modules with the HM65 chipset

R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number. The conga-TM67/TS67 BIOS binary size for both the QM67 and the HM65 variants is approximately 8MB.

12.1 Supported Flash Devices

The conga-TM67/TS67 supports the following flash devices:

- Spansion S25FL064K0SMFI01
- Winbond W25Q64CVSSIG

The flash devices listed above can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.

12.2 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” refer to the user’s guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

12.3 BIOS Security Features

The BIOS provides a setup administrator password that limits access to the BIOS setup menu.

12.4 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to ‘lock’ and ‘unlock’ drives using the security password. A ‘locked’ drive will be detected by the system, but no data can be accessed. Accessing data on a ‘locked’ drive requires the proper password to ‘unlock’ the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within four attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

13 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.3	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0	http://www.serialata.org
PICMG® COM Express Module™ Base Specification	http://www.picmg.org/
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications