



TQMa53 User's Manual

TQMa53 UM 400
12.02.2014





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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
100	05.09.2012	Petz		Document created
200	28.03.2013	Petz	All	Complete rework
400	12.02.2014	Petz	All	Complete rework



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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.


1.6 Symbols and typographic conventions

Table 1: Terms and Conventions


Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	<p>The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.</p> <p>A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off.</p> <p>Violation of this guideline may result in damage / destruction of the module and be dangerous to your health.</p> <p>Improper handling of your TQ-product would render the guarantee invalid.</p>
---	--

Proper ESD handling

	<p>The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD).</p> <p>Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.</p>
---	--



1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.

Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.

Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring. The identification of the individual functions follows the above conventions.

Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the used modules:**
These documents describe the service, functionality and special characteristics of the used module (incl. BIOS).
- **Specifications of the used components:**
The manufacturer's specifications of the used components, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of.
The manufacturer's advice should be followed.
- **Software behaviour:**
No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- Circuit diagram MBa53
- CPU Manual IMX53RM
- User's Manual STK-MBa53
- Documentation of boot loader U-Boot (<http://www.denx.de/wiki/U-Boot/Documentation>)
- Documentation of PTXdist (<http://www.ptxdist.de>)

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa53 revision 04xx.

The User's Manual describes the hardware of the TQMa53, and refers to some software settings. It does not replace the Reference Manual of the CPU. The TQMa53 is a universal Minimodule based on the Freescale ARM CPU MCIMX53 (i.MX53). The Cortex A8 core of this CPU works with up to 1.2 GHz. The TQMa53 extends the TQC product range and offers an outstanding computing performance combined with high-performance graphics power.

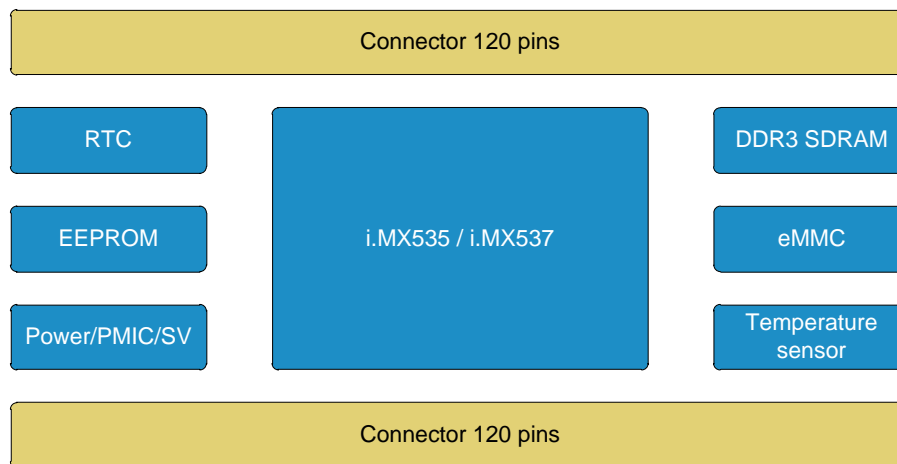


Illustration 1: Block diagram TQMa53 (simplified)

The TQMa53 provides the following key functions and characteristics:

2.1 Key functions and characteristics:

- Freescale CPU i.MX53 (i.MX537 or i.MX535)
- Up to 1 Gbyte DDR3 SDRAM
- Up to 16 Gbyte eMMC NAND flash
- 64 Kbit EEPROM
- Temperature sensor
- Real-time clock
- Freescale Power Management Integrated Circuit (PMIC)
- All essential CPU pins are routed to the module connectors
- Extended temperature range
- Single power supply 5 V

3. ELECTRONICS SPECIFICATION

3.1 System overview

3.1.1 System architecture / block diagram

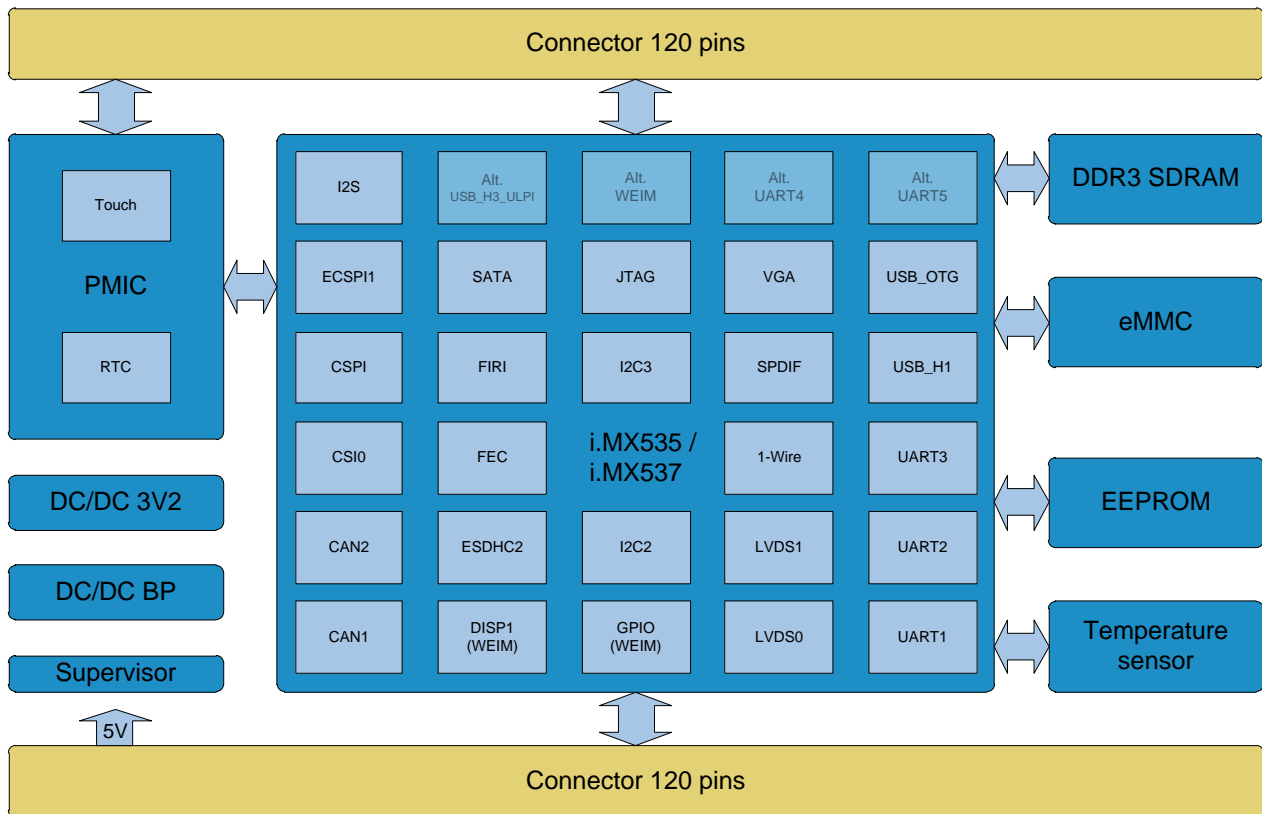


Illustration 2: Block diagram TQMa53



3.1.2 Functionality

The following key functions are implemented on the TQMa53:

- i.MX53 processor
- DDR3 SDRAM
- eMMC NAND flash
- EEPROM
- Temperature sensor
- PMIC / DC/DC converter / supervisor

The following interfaces are provided at the module connectors of the TQMa53:

- 2 × CAN
- 1 × Camera Sensor Interface
- 1 × CSPI (SPI)
- 1 × parallel display (DISP)
- 1 × ESDHC2 (SDIO/MMC/SD card)
- 1 × ECSPI (SPI)
- 1 × Ethernet 10/100 Mbit
- 1 × FIRI (Fast Infrared)
- 2 × I²C
- 1 × I²S
- 2 × LVDS display
- 1 × 1-Wire
- 1 × SATA
- 1 × SPDIF
- 3 × UART (1 × with handshake)
- 2 × USB 2.0 Hi-Speed
- 1 × VGA
- 1 × Touch
- GPIOs
- JTAG
- Boot mode

As an alternative to the factory configuration further interfaces of the i.MX53 can also be used:

- USB 2.0 Hi-Speed ULPI interface
- WEIM bus
- ESDHC1 (SDIO/MMC/SD card)
- General Purpose Timer
- PWM
- More UARTs

3.2 System components

3.2.1 i.MX53 processor details

The following illustration shows the block diagram of the i.MX53 derivative i.MX537.

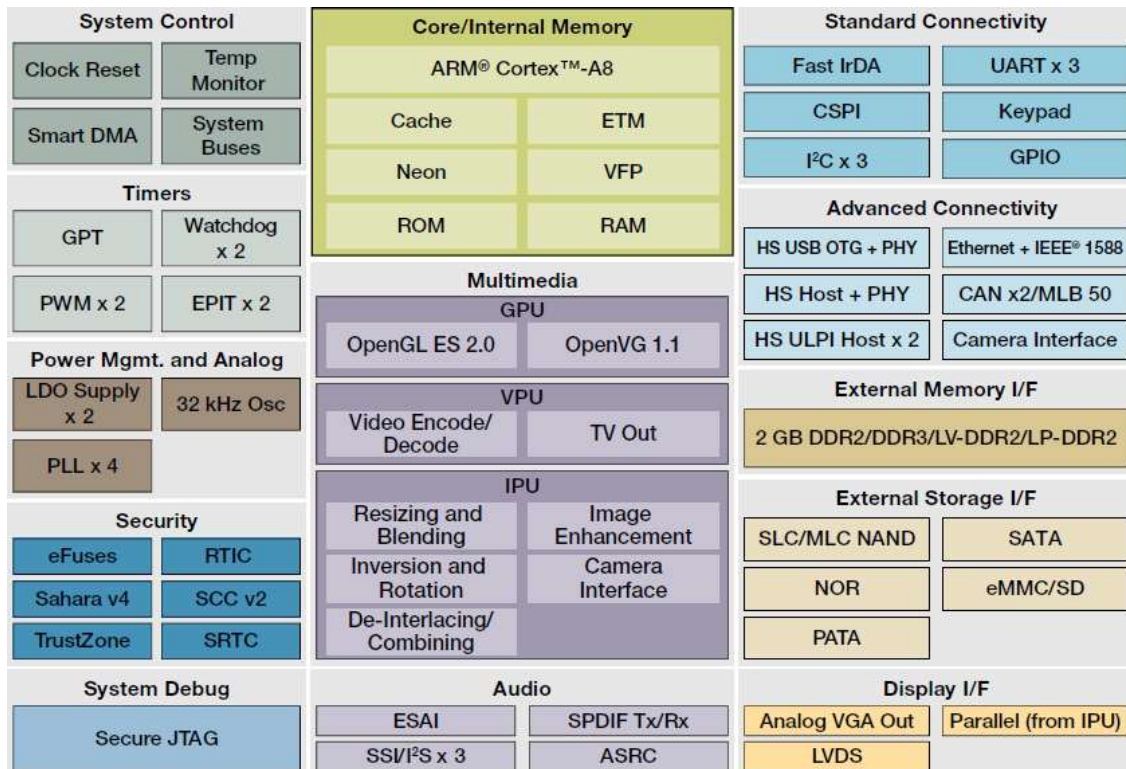


Illustration 3: Block diagram i.MX537
(Source: [Freescale](#))

3.2.1.1 i.MX53 processor versions

Depending on the version of the TQMa53 one of the following versions of the CPU is assembled:

Table 2: Processor versions

Manufacturer	Part number	Features	Mask Set	Temperature	Package
Freescale	MCIMX537CVV8C	800 MHz	N78C	–40 °C to +85 °C	19 × 19 mm² BGA
Freescale	MCIMX535DVV1C	1 GHz	N78C	–20 °C to +85 °C	19 × 19 mm² BGA
Freescale	MCIMX535DVV2C	1.2 GHz	N78C	–20 °C to +85 °C	19 × 19 mm² BGA

3.2.1.2 CPU errata

Attention: Malfunction



Please take note of the current errata of the Freescale CPU (4).

3.2.1.3 Boot mode

The boot mode of the i.MX53 is set with the pins BOOT_MODE0 and BOOT_MODE1.

The following table shows the supported boot modes, as well as the boot mode selected for the TQMa53.

Table 3: Boot modes i.MX53

BOOT_MODE[1:0]	Boot type	TQMa53	Remark
00	Internal Boot	–	Settings for boot configuration via GPIO pins
01	Reserved	–	–
10	Boot From Fuses	X	BOOT_MODE1 10 kΩ PU BOOT_MODE0 10 kΩ PD
11	Serial Downloader	–	Via USBOTG or UART2

Both signals BOOT_MODE[1:0] are additionally made available at the module connectors.

All possible boot modes can therefore be set by alternative placement of resistor combinations on the carrier board.

- To enable the reading of the boot configuration via the GPIO pins, BOOT_MODE[1:0] has to be set to 00. For that purpose the pin BOOT_MODE1 has to be pulled low on the carrier board.
- The reference voltage for BOOT_MODE[1:0] is VCC2V775, which is also available at the module connectors.

3.2.1.4 Boot configuration

A total of 21 GPIO pins are available for the boot configuration.

- Freescale recommends overriding the eFuses by GPIO pins only during development and to burn the necessary eFuses in the final product.

Note: Boot configuration



The TQMa53 is delivered with no preset boot configuration.

- On the TQMa53 none of the 21 boot-configuration pins are connected.
- Attention: in the initial state the voltage VDD_FUSE is deactivated on the TQMa53 to prevent eFuses from being burnt by mistake. Before the eFuses can be burnt the signal VDD_FUSE_EN# on GPIO2_GPIO4 must be pulled low.
- The bus signals have to be separated with resistors, because the GPIO pins to read the boot configuration are on these bus signals. (See Freescale System Development Users Guide (7)).
- See also section 3.2.14.4 for notes on the wiring of the configuration resistors.

The following table shows the pins of the boot configuration, or the corresponding eFuses.

To boot from the internal eMMC the recommended settings are blue highlighted in the right column.

The settings for other boot devices are to be taken from the Freescale Reference Manual of the processor (1).

3.2.1.5 Boot interfaces

The i.MX53 contains a ROM with integrated boot loader.

After the start the boot code initializes the hardware and then loads the program image from the selected boot device. The eMMC integrated on the TQMa53 can for example be selected as the standard boot-device. As an alternative to booting from the integrated eMMC it is also possible to boot from one of the following interfaces:

- ESDHC2 (e.g. SD card)
- ECSP11 (e.g. serial NOR flash)
- SATA
- WEIM (e.g. NOR flash)

The boot-device and its configuration, as well as different CPU settings have to be set via different boot mode registers. Therefore the i.MX53 provides two possibilities:

- To burn internal eFuses and/or
- To read dedicated GPIO pins

The exact behaviour during booting depends on the value of the register BT_FUSE_SEL (Default = 0):

- BT_FUSE_SEL = 0: The values in the eFuses are overwritten by GPIO pins.
- BT_FUSE_SEL = 1: All boot options are defined exclusively by the values the eFuses.

The following table shows the behaviour of the bit BT_FUSE_SEL in dependence of the chosen boot mode. (Boot modes see section 3.2.1.3).

Table 4: Boot-Mode register BT_FUSE_SEL

Boot-Mode	Setting BT_FUSE_SEL	Recommended for
00	0 = Boot mode configuration is taken from GPIOs. (Default) 1 = Boot mode configuration is taken from fuses.	Development
10	0 = Boot using Serial Loader (UART/USB) (Default) 1 = Boot mode configuration is taken from fuses.	Series production

3.2.1.6 Pin multiplexing

Depending on the configuration, the pin multiplexing permits the usage of different pins for different purposes. This document describes the configuration in the Standard-BSP of TQ-Systems GmbH.

Attention: Destruction or malfunction



Many of the CPU pins permit the usage of several different configurations. Please heed the notes in the i.MX53 Reference Manual (1) concerning the wiring of these pins before integration / start-up of your carrier board / Starterkit.

Table 5: Boot configuration

Pin name	Signal TQMa53	eFuse	Setting	Default	eMMC
EIM_A22	DISP1_DAT17	BOOT_CFG1[7]	0000 = NOR / OneNAND (EIM) 0001 = Reserved 0010 = Hard Disk (PATA / SATA) 0011 = Serial ROM (I ² C / SPI) 010x = SD / eSD 011x = MMC / eMMC 1xxx = NAND	0	0
EIM_A21	DISP1_DAT16	BOOT_CFG1[6]	Fast Boot Support 0 = Normal Boot 1 = Fast Boot	0	1
EIM_A20	DISP1_DAT15	BOOT_CFG1[5]	SD/MMC Speed Mode 0 = High Speed Mode 1 = Normal Speed Mode	0	1
EIM_A19	DISP1_DAT14	BOOT_CFG1[4]	Reserved	0	0
EIM_A18	DISP1_DAT13	BOOT_CFG1[3]	BT_FREQ 0 = ARM Frequency 800 MHz 1 = ARM Frequency 400 MHz	0	0
EIM_A17	DISP1_DAT12	BOOT_CFG1[2]	BT_MMU_ENABLE 0 = MMU/Cache is disabled by ROM during the boot 1 = MMU/Cache is enabled by ROM during the boot	0	0
EIM_A16	DISP1_CLK	BOOT_CFG1[1]	Bus Width SD/eSD: xx0 = 1 Bit xx1 = 4 Bit MMC/eMMC: 000 = 1 Bit 001 = 4 Bit 010 = 8 Bit 101 = 4 Bit DDR (MMC 4.4) 110 = 8 Bit DDR (MMC 4.4) Else – Reserved	0	0
EIM_LBA	GPIO2_GPIO27	BOOT_CFG1[0]	AXI / DDR Frequency 0 = 200 MHz AXI / 400 MHz DDR 1 = 166 MHz AXI / 333 MHz DDR	0	1
EIM_EB0	DISP1_DAT11	BOOT_CFG2[7]	OSC_FREQ_SEL 0 = 19.2; 24; 26; 27 MHz Auto Detection 1 = OSC Frequency 24 MHz	0	0
EIM_EB1	DISP1_DAT10	BOOT_CFG2[6]	Reserved	0	0
EIM_DA0	DISP1_DAT9	BOOT_CFG2[5]	Security Configuration 00 = Reserved 01 = Open 1x = Closed	0	0
EIM_DA1	DISP1_DAT8	BOOT_CFG2[4]	Reserved	1	1
EIM_DA2	DISP1_DAT7	BOOT_CFG2[3]	Reserved	0	0
EIM_DA3	DISP1_DAT6	BOOT_CFG2[2]	Port Select 00 = ESDHCV2-1 01 = ESDHCV2-2 10 = ESDHCV3-3 11 = ESDHCV2-4	0	0
n/a	n/a	BOOT_CFG2[1]	DLL Override 0 = Boot ROM default 1 = Apply value per fuse field MMC_DLL_DLY[3:0]	0	1
n/a	n/a	BOOT_CFG2[0]	Boot Acknowledge Disable 0 = Boot Acknowledge Enabled 1 = Boot Acknowledge Disabled	0	0
EIM_DA4	DISP1_DAT5	BOOT_CFG3[7]	Reserved	0	0
EIM_DA5	DISP1_DAT4	BOOT_CFG3[6]	Reserved	0	0
EIM_DA6	DISP1_DAT3	BOOT_CFG3[5]	Reserved	0	0
EIM_DA7	DISP1_DAT2	BOOT_CFG3[4]	Reserved	0	0
EIM_DA8	DISP1_DAT1	BOOT_CFG3[3]	Reserved	0	0
EIM_DA9	DISP1_DAT0	BOOT_CFG3[2]	Reserved	0	0
EIM_DA10	DISP1_DRDY_DE	BOOT_CFG3[1]	Reserved	0	0
n/a	n/a	BOOT_CFG3[0]	Direct External Memory Boot Disable 0 = Direct boot from external memory is allowed 1 = Direct boot from external memory is not allowed	0	0

3.2.2 Memory

3.2.2.1 DDR3 SDRAM

On the TQMa53 DDR3 SDRAM is used. Up to four DDR3 128M16 memory chips are assembled. Each pair of chips has one common chip select and is together connected to the CPU with a bus width of 32 bit. The DDR3 SDRAM on the TQMa53 is clocked with 400 MHz. The following block diagram shows how the DDR3 SDRAM is connected to the processor.

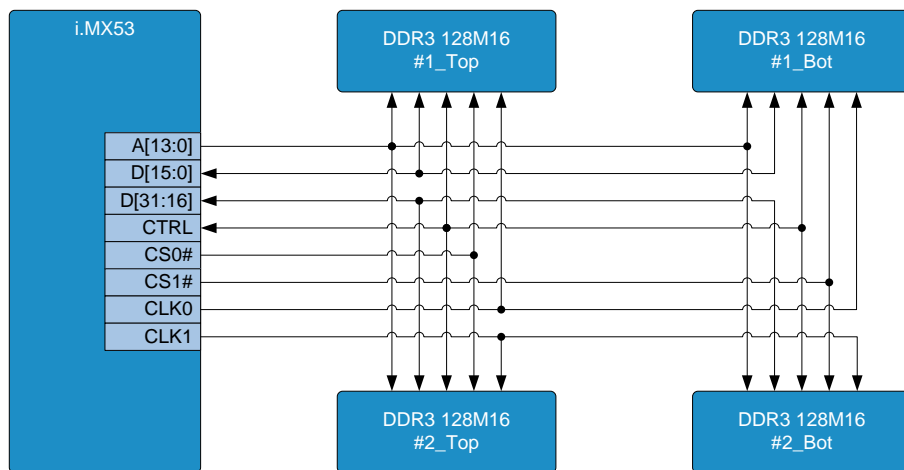


Illustration 4: Block diagram DDR3 SDRAM connection

In the following table the possible variations of the TQMa53 using different types of memory chips are shown:

Table 6: DDR3 SDRAM

Placement option	Capacity
2 × DDR3 128M16 (2 × TOP assembled)	512 Mbyte
4 × DDR3 128M16 (2 × TOP and 2 × BOTTOM assembled)	1 Gbyte

The SDRAM is mapped to the following address ranges:

Table 7: DDR3-SDRAM address range

Start address	Size	Chip Select	Remark
0x7000_0000	0x2000_0000	CS0#	DDR3 Top
0xB000_0000	0x2000_0000	CS1#	DDR3 Bottom

3.2.2.2 eMMC NAND flash

An eMMC NAND flash is provided to contain the boot loader and the application software. In the BSP provided by TQ-Systems GmbH a clock rate of 50 MHz is supported.

The following block diagram shows how the eMMC flash is connected to the processor.

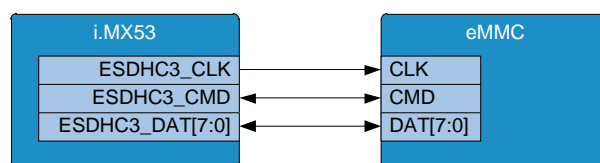


Illustration 5: Block diagram eMMC flash connection

3.2.2.3 EEPROM

A serial EEPROM is available for permanent storage of e.g. module characteristics or customers parameters. The EEPROM is controlled via I²C bus 2 of the processor. The write protection (WP) of the EEPROM is not available. The following block diagram shows how the EEPROM is connected to the processor.

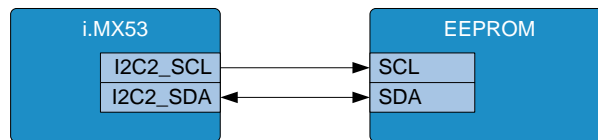


Illustration 6: Block diagram EEPROM connection

The following table shows the EEPROM used.

Table 8: EEPROM

Manufacturer	Part number	Capacity	Temperature range
STM	M24C64-WDW6TP	64 kbit	–40 °C to +85 °C

- The I²C address of the EEPROM is 0x50 / 0b1010000.

In the EEPROM module-specific data is stored. It is, however, not essential for the correct operation of the TQMa53. The data can be deleted or altered by the user.

In the following table the parameters stored in the EEPROM are shown.

Table 1: EEPROM module specific data

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
0x00	Variable	Variable	32 ₁₀	Binary	Hard Reset Configuration Word (HRCW), (optional)
0x20	6 ₁₀	10 ₁₀	16 ₁₀	Binary	MAC address
0x30	8 ₁₀	8 ₁₀	16 ₁₀	ASCII	Serial number
0x40	Variable	Variable	64 ₁₀	ASCII	Module name

3.2.3 Temperature sensor

A temperature sensor (LM75A from NXP) for supervision of the module temperature is provided on the TQMa53. The sensor is placed on the top side of the module (D8 in Illustration 16). The temperature sensor is connected to the I²C bus 2 of the processor. The overtemperature detection output of the sensor is not connected to the CPU. The following block diagram shows how the temperature sensor is connected to the processor.

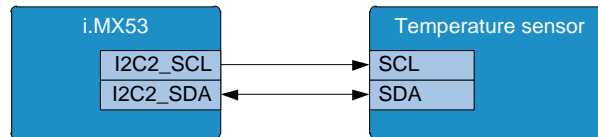


Illustration 7: Block diagram temperature sensor connection

The following table shows the temperature sensor used.

Table 9: Temperature sensor

Manufacturer	Part number	Remark	Error	Temperature range
NXP	LM75ADP	11 bit ADC	Max. $\pm 3^{\circ}\text{C}$	-55°C to $+125^{\circ}\text{C}$

- The I²C address of the temperature sensor is 0x48 / 0b1001000.

3.2.4 RTC

The i.MX53, as well as the PMIC MC34708 provide an RTC. Additionally the PMIC provides an SRTC support for the i.MX53. The choice of RTC used depends on the software implementation. More details are to be taken from the Freescale Reference Manual of the CPU and the PMIC. The accuracy the RTC is mainly determined by the characteristics of the quartz used. The type FC-135 used on the TQMa53 has a standard frequency tolerance of ± 20 ppm at 25°C . (Parabolic coefficient: max. $-0.04 \times 10^{-6} / ^{\circ}\text{C}^2$).

The manufacturer of the RTC provides the following values for the typical current consumption:

Table 10: Current consumption RTC

RTC	Typical current consumption	Remark
PMIC RTC	4.0 μA	Mode RTC / Power Cut
CPU SRTC	<10 μA	–

The PMIC provides the necessary supply voltage and a clock signal for the SRTC of the CPU. The following block diagram shows the implementation on the TQMa53.

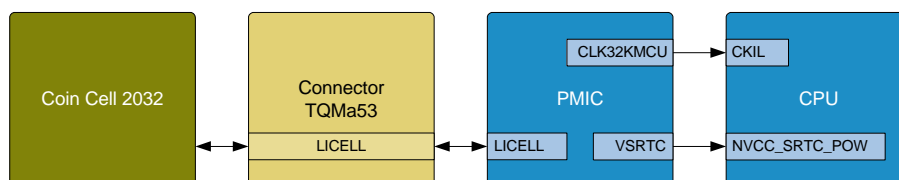


Illustration 8: Block diagram RTC

The RTC domain of the PMIC on the TQMa53 offers the possibility of a backup supply. It supports simple coin cells, but also Lithium coin cells or a SuperCap which can also be charged by the PMIC. Charging methods and electrical characteristics of the pin LICELL are to be taken from the data sheet of the PMIC MC34708 (5). It is to be taken note of that the typical charging current is only 60 μA . Concerning the RTC the errata sheet of the PMIC (6) contains two errata (number 5 and 23) which describe a failure of the RTC or the backup supply which can occur under certain circumstances. No workaround was provided with regard to these errata on the TQMa53. To avoid these errata on the target system, the use of an I²C-RTC on the carrier board is recommended.

3.2.5 Ethernet

The i.MX53 provides a 10/100 Mbit Fast Ethernet Controller (FEC) with RMII, whose signals are routed to the module connectors. The following table shows the signals used by the FEC.

Table 11: FEC signals

Signal name	TQMa53 pin	Direction	Remark
FEC_REF_CLK	X2-88	I	Ethernet Input Transmit Reference Clock
FEC_TX_EN	X2-79	O	Ethernet Output Transmit Enable
FEC_TXD[1:0]	X2-83:81	O	Ethernet Output Transmit Data
FEC_RX_DV	X2-84	I	Ethernet Input Receive Data Valid
FEC_RXD[1:0]	X2-82:80	I	Ethernet Input Receive Data
FEC_RX_ER	X2-87	I	Ethernet Input Receive Error
FEC_MDC	X2-85	O	Ethernet Output Management Data Clock
FEC_MDIO	X2-86	I/O _{PU}	Ethernet Management Data (PU 1.5 kΩ)
FEC_RST#	X2-78	O	Ethernet Output Reset (GPIO)
FEC_INT#	X2-77	I	Ethernet Input Interrupt (GPIO)

3.2.6 SD card

An SD card can be connected to the TQMa53. The Enhanced Secured Digital Host Controller 2 version 2 (ESDHCv2-2) is routed to the module connectors for this purpose.

The following table shows the signals used by the SD card interface.

Table 12: SD card signals

Signal name	TQMa53 pin	Direction	Remark
ESDHC2_CLK	X2-97	O	SD-Card Output Clock
ESDHC2_DAT[3:0]	X2-98:96:94:92	I/O	SD-Card Data
ESDHC2_CMD	X2-95	I/O	SD-Card Command
ESDHC2_WP	X2-91	I	SD-Card Write-Protect
ESDHC2_CD#	X2-93	I	SD-Card Card-Detect

The supported modes of operation, as well as MMC specifications are to be taken from the Freescale Reference Manual of the CPU (1).

- When required the port ESDHC2 can be configured as a boot device.

3.2.7 Touch

The PMIC used on the TQMa53 provides a touch interface which is routed to the module connectors.

A 4-wire touch can be connected here.

The following table shows the signals used by the touch interface.

Table 13: Touch signals

Signal name	TQMa53 pin	Direction	Remark
TSX1	X2-13	AI	Left
TSX2	X2-15	AI	Right
TSY1	X2-14	AI	Top
TSY2	X2-16	AI	Bottom

A wake-up by the touch is possible in principle. The practical implementation and the question in which power modes this is possible depends on the respective software implementation.

3.2.8 GPIO

Besides their interface function most of the pins of the i.MX53 can also be used as GPIOs. All these GPIOs are interrupt- and therefore wake-up capable. Details are to be taken from the Freescale Reference Manual of the CPU (1). Moreover several pins marked as GPIO are already available at the module connectors. The following table shows the signals which can be used as GPIOs.

Table 14: GPIO signals

Signal name	TQMa53 pin	Direction	Remark
GPIO1_GPIO3	X2-61	I/O	–
GPIO2_GPIO23	X1-38	I/O	–
GPIO2_GPIO25	X1-37	I/O	–
GPIO2_GPIO26	X1-35	I/O	–
GPIO2_GPIO27	X1-36	I/O	–
GPIO3_GPIO11	X1-38	I/O	–
GPIO3_GPIO12	X1-39	I/O	–
GPIO3_GPIO13	X1-40	I/O	–
GPIO3_GPIO14	X1-42	I/O	–
GPIO3_GPIO20	X1-30	I/O	–
GPIO3_GPIO21	X1-34	I/O	–
GPIO3_GPIO22	X1-33	I/O	–
GPIO3_GPIO28	X1-31	I/O	–
GPIO3_GPIO29	X1-32	I/O	–
GPIO5_GPIO0	X1-41	I/O	–

The electrical characteristics of the GPIOs are to be taken from the respective data sheet provided by Freescale (2) / (3).

3.2.9 JTAG

The i.MX53 provides two JTAG modes, which can be set with the signal at the pin JTAG_MOD.

The following table shows the available modes, as well as the mode set on the TQMa53.

With the assembly option R43 and R45 the mode can be changed.

Table 15: JTAG modes

Name	JTAG_MODE	Default	Remark
Daisy Chain All	0	X	For common SW debug (high speed and production)
SJC only	1	–	IEEE 1149.1 JTAG compliant mode

- The JTAG port works in the power domain 2.775 V.
The voltage VCC2V775 is routed to the plug connectors and can be used as a reference voltage for a JTAG adaptor.

The following table shows the signals used by the JTAG interface.

Table 16: JTAG signals

Signal name	TQMa53 pin	Direction	Remark
JTAG_TCK	X2-68	I _{PD}	PD 10 kΩ on TQMa53
JTAG_TMS	X2-65	I _{PU}	PU 10 kΩ to 2.775 V on TQMa53
JTAG_TDI	X2-66	I _{PU}	PU 10 kΩ to 2.775 V on TQMa53
JTAG_TDO	X2-63	O	–
JTAG_TRST#	X2-67	I _{PU}	PU 10 kΩ to 2.775 V on TQMa53

3.2.10 External Memory Bus

Address and data bus, as well as control signals of the external memory interface of the i.MX53 are available at the module connectors. The signals of the WEIM bus are mostly on the interfaces DISP1 and ECSP1. DISP1 and ECSP1 are not available if the WEIM bus is used. The chip-selects of the External Memory Bus are configurable. Information is to be taken from the Freescale Reference Manual of the CPU (1).

The following table shows the signals used, as well as their characteristics on the EMI interface.

Table 17: WEIM signals

Signal name	TQMa53 pin	Remark
WEIM_DA[15:0]		
EMI_NAND_WEIM_DA0	X1-61	Assigned to: DISP1_DAT9
EMI_NAND_WEIM_DA1	X1-74	Assigned to: DISP1_DAT8
EMI_NAND_WEIM_DA2	X1-59	Assigned to: DISP1_DAT7
EMI_NAND_WEIM_DA3	X1-72	Assigned to: DISP1_DAT6
EMI_NAND_WEIM_DA4	X1-57	Assigned to: DISP1_DAT5
EMI_NAND_WEIM_DA5	X1-70	Assigned to: DISP1_DAT4
EMI_NAND_WEIM_DA6	X1-55	Assigned to: DISP1_DAT3
EMI_NAND_WEIM_DA7	X1-68	Assigned to: DISP1_DAT2
EMI_NAND_WEIM_DA8	X1-53	Assigned to: DISP1_DAT1
EMI_NAND_WEIM_DA9	X1-66	Assigned to: DISP1_DAT0
EMI_NAND_WEIM_DA10	X1-51	Assigned to: DISP1_DRDY_DE
EMI_NAND_WEIM_DA11	X1-39	Assigned to: GPIO3_GPIO11
EMI_NAND_WEIM_DA12	X1-44	Assigned to: GPIO3_GPIO12
EMI_NAND_WEIM_DA13	X1-40	Assigned to: GPIO3_GPIO13
EMI_NAND_WEIM_DA14	X1-42	Assigned to: GPIO3_GPIO14
EMI_NAND_WEIM_DA15	X1-79	Assigned to: VGA_HSYNC
WEIM_D[31:16]		
EMI_WEIM_D16	X1-54	Assigned to: ESPI_SCLK
EMI_WEIM_D17	X1-43	Assigned to: ESPI_MISO
EMI_WEIM_D18	X1-45	Assigned to: ESPI_MOSI
EMI_WEIM_D19	X1-46	Assigned to: ESPI_SS1#
EMI_WEIM_D20	X1-30	Assigned to: GPIO3_GPIO20
EMI_WEIM_D21	X1-34	Assigned to: GPIO3_GPIO21
EMI_WEIM_D22	X1-33	Assigned to: GPIO3_GPIO22
EMI_WEIM_D23	X1-60	Assigned to: LCD_HSYNC
EMI_WEIM_D24	X1-47	Assigned to: ESPI_SS2#
EMI_WEIM_D25	X1-50	Assigned to: ESPI_SS3#
EMI_WEIM_D26	X1-88	Assigned to: DISP1_DAT22
EMI_WEIM_D27	X1-75	Assigned to: DISP1_DAT23
EMI_WEIM_D28	X1-31	Assigned to: GPIO3_GPIO28
EMI_WEIM_D29	X1-32	Assigned to: GPIO3_GPIO29
EMI_WEIM_D30	X1-73	Assigned to: DISP1_DAT21
EMI_WEIM_D31	X1-86	Assigned to: DISP1_DAT20
WEIM_CONTROL		
EMI_WEIM_CS0	X1-38	Assigned to: GPIO2_GPIO23
EMI_WEIM_CS1	X1-81	Assigned to: VGA_VSYNC
EMI_WEIM_OE	X1-37	Assigned to: GPIO2_GPIO25
EMI_WEIM_RW	X1-35	Assigned to: GPIO2_GPIO26
EMI_WEIM_EB2	X1-48	Assigned to: ESPI_SS0#
EMI_WEIM_EB3	X1-62	Assigned to: LCD_VSYNC
EMI_WEIM_LBA	X1-36	Assigned to: GPIO2_GPIO27
EMI_WEIM_WAIT	X1-41	Assigned to: GPIO5_GPIO0

3.2.11 Graphics interfaces

3.2.11.1 CSI

The i.MX53 has two Camera Sensor Interfaces (max. 8192 × 4096 pixel). CSI0 is routed to the module connectors. The following table shows the signals used by the Camera Sensor Interface (CSI0).

Table 18: Camera Sensor Interface signals

Signal name	TQMa53 pin	Direction	Remark
IPU_CSI0_PIXCLK	X1-4	I	Camera-Sensor Input Clock
IPU_CSI0_HSYNC	X1-3	I	Camera-Sensor Input Horizontal Sync
IPU_CSI0_VSYNC	X1-5	I	Camera-Sensor Input Vertical Sync
IPU_CSI0_[D19:4]	X1-24:9	I	Camera-Sensor Input Data
IPU_CSI0_DATA_EN	X1-8	I	Camera-Sensor Input Data Enable
CCM_CSI0_MCLK	X1-26	O	Camera-Sensor Output Master Clock
CSI0_PWDN	X1-25	O	Camera-Sensor Output Power Down (GPIO)
CSI0_RST#	X1-27	O	Camera-Sensor Output Reset (GPIO)

3.2.11.2 DISP

The i.MX53 has two parallel Display Interfaces (max. 4096 × 2048 pixel). DISP1 is routed to the module connectors. Information to different types of displays and supported formats can be taken from the Freescale Reference Manual (1). The following table shows the signals used by the DISP1 interface.

Table 19: Parallel display signals

Signal name	TQMa53 pin	Direction	Remark
DISP1_DAT[23:0]	X1	O	Display Output RGB Data
DISP1_HSYNC	X1-60	O	Display Output Horizontal Sync / i.MX53-Signal: IPU_DI1_PIN2
DISP1_VSYNC	X1-62	O	Display Output Vertical Sync / i.MX53-Signal: IPU_DI1_PIN3
DISP1_CLK	X1-56	O	Display Output Clock / i.MX53-Signal: IPU_DI1_DISP_CLK
DISP1_DRDY_DE	X1-51	O	Display Output Data Enable / i.MX53-Signal: IPU_DI1_PIN15

3.2.11.3 LCD control

The following additional signals are available at the module connectors for control of the displays. The following table shows the signals used.

Table 20: Display control signals

Signal name	TQMa53 pin	Direction	Remark
LCD_POWER_EN	X2-24	O	LCD Power Enable Output (GPIO)
LCD_RESET	X2-26	O	LCD Reset Output (GPIO)
LCD_BLT_EN	X2-23	O	LCD Backlight Enable (GPIO)
LCD_CONTRAST	X2-25	O	LCD Contrast Output (PWM)



3.2.11.4 LVDS

The i.MX53 has two integrated LVDS display bridges, which are routed to the module connectors. The following table shows the signals used by the LVDS0 interface.

Table 21: LVDS0 signals

Signal name	TQMa53 pin	Direction	Remark
LVDS0_CLK_P	X1-91	O	–
LVDS0_CLK_N	X1-93	O	–
LVDS0_TX[3:0]_P	X1-115-109-103-97	O	–
LVDS0_TX[3:0]_N	X1-117-111-105-99	O	–

The following table shows the signals used by the LVDS1 interface.

Table 22: LVDS1 signals

Signal name	TQMa53 pin	Direction	Remark
LVDS1_CLK_P	X1-92	O	–
LVDS1_CLK_N	X1-94	O	–
LVDS1_TX[3:0]_P	X1-116-110-104-98	O	–
LVDS1_TX[3:0]_N	X1-118-112-106-100	O	–

3.2.11.5 VGA

The i.MX53 has a VGA port, which is routed to the module connectors. The following table shows the signals used by the VGA interface.

Table 23: VGA signals

Signal name	TQMa53 pin	Direction	Remark
TVDAC_IOR	X1-87	AO	–
TVDAC_I0G	X1-85	AO	–
TVDAC_I0B	X1-83	AO	–
VGA_HSYNC	X1-79	O	i.MX53 signal: IPU_DI1_PIN4
VGA_VSYNC	X1-81	O	i.MX53 signal: IPU_DI1_PIN6

3.2.12 Serial interfaces

The supported standards, transmission modes and rates of the following interfaces are to be taken from the Freescale Reference Manual (1).

3.2.12.1 CAN

The i.MX537 provides two integrated CAN controller. The signals of both CAN controllers are made available at the module connectors. The drivers have to be integrated on the carrier board. The i.MX535 does not provide CAN. For this reason the CAN functionality is not available in the pin multiplexing.

The following table shows the signals used, as well as their characteristics.

Table 24: CAN1 / CAN2 signals

Signal name	TQMa53 pin	Direction	Remark
CAN1_RXCAN	X2-42	I	–
CAN1_TXCAN	X2-40	O	–
CAN2_RXCAN	X2-41	I	–
CAN2_TXCAN	X2-39	O	–

3.2.12.2 FIRI

The i.MX53 provides a Fast Infrared Interface which is routed to the module connectors.

The following table shows the signals used, as well as their characteristics of the Fast Infrared Interface (FIRI).

Table 25: FIRI signals

Signal name	TQMa53 pin	Direction	Remark
FIRI_RXD	X2-54	I	–
FIRI_TXD	X2-53	O	–

3.2.12.3 I2C

The i.MX53 provides three I²C interfaces. The I²C interfaces I2C2 and I2C3 are available at the module connectors.

The following table shows the signals used, as well as their characteristics.

Table 26: I2C2 signals

Signal name	TQMa53 pin	Direction	Remark
I2C2_SCL	X2-57	I/O _{PU}	4.7 kΩ PU to 3.2 V on TQMa53
I2C2_SDA	X2-55	I/O _{PU}	4.7 kΩ PU to 3.2 V on TQMa53
I2C3_SCL	X2-58	I/O	–
I2C3_SDA	X2-56	I/O	–

The I2C2 bus is also used for components on the TQMa53. The following devices are connected to the I2C2 bus on the TQMa53:

Table 27: I2C2 address distribution

Component	Chosen address
EEPROM (M24C64)	0x50 / 0b1010000
Temperature sensor (LM75A)	0x48 / 0b1001000
PMIC (MC34708VM)	0x08 / 0b0001000

In case more devices are connected to the I2C2 bus on the carrier board, the maximum capacitive bus load accordingly to the I²C standard has to be adhered to. If required additional pull-ups should be provided on the carrier board at the bus.

3.2.12.4 I2S

Signals of the digital audio multiplexer 5 via SSI are available at the module connectors to connect an audio-codec via I²S. The following table shows the signals used by the I²S interface.

Table 28: I2S signals

Signal name	TQMa53 pin	Direction	Remark
I2S_DIN	X2-43	I	AUDMUX signal: AUD5_RXD
I2S_DOUT	X2-46	O	AUDMUX signal: AUD5_TXD
I2S_LRCLK	X2-45	O	AUDMUX signal: AUD5_TXFS
I2S_SCLK	X2-44	O	AUDMUX signal: AUD5_TXC
I2S_MCLK	X2-49	O	CCM signal: SSI_EXT1_CLK

Besides I2S the SSI interface also supports further synchronous modes. Details can be taken from the Freescale Reference Manual of the CPU (1). Asynchronous SSI modes are not supported in the standard pin-multiplexing.

3.2.12.5 1-Wire

The i.MX53 provides a 1-Wire interface which is routed to the module connectors. The following table shows the signal used by the 1-Wire interface.

Table 29: 1-Wire signal

Signal name	TQMa53 pin	Direction	Remark
OWIRE_LINE	X2-62	I/O	–

3.2.12.6 SATA

The i.MX53 provides a SATA controller with integrated PHY. The following table shows the signals used by the SATA interface.

Table 30: SATA signals

Signal name	TQMa53 pin	Direction	Remark
SATA_RXP	X2-72	I	–
SATA_RXM	X2-74	I	–
SATA_TXP	X2-71	O	–
SATA_TXM	X2-73	O	–

- When required, the SATA interface can be configured as a boot device.

3.2.12.7 SPDIF

The i.MX53 provides an SPDIF interface with transmit and receive-functionality. The following table shows the signals used by the SPDIF interface.

Table 31: SPDIF signals

Signal name	TQMa53 pin	Direction	Remark
SPDIF_IN	X2-52	I	–
SPDIF_OUT	X2-50	O	–



3.2.12.8 SPI

The i.MX53 provides a CSPI (Configurable Serial Peripheral Interface) and two ECSPIs (Enhanced Configurable SPI). Primarily CSPI and ECSPi1 are thereof available at the module connectors. Via multiplexing the signals of the ECSPi2 are also available on other signals.

The following table shows the signals used by CSPI interface.

Table 32: CSPI signals

Signal name	TQMa53 pin	Direction	Remark
SPI_SCLK	X2-117	O	Signal i.MX53: CSPI_SCLK
SPI_MOSI	X2-118	O	Signal i.MX53: CSPI_MOSI
SPI_MISO	X2-115	I	Signal i.MX53: CSPI_MISO
SPI_SS[2:0]#	X2-114-116-113	O	Signal i.MX53: CSPI_SS[2:0]#

The following table shows the signals used by the ECSPi interface.

Table 33: ECSPi signals

Signal name	TQMa53 pin	Direction	Remark
ESPI_SCLK	X1-54	O	Signal i.MX53: ECSPi1_SCLK
ESPI_MOSI	X1-45	O	Signal i.MX53: ECSPi1_MOSI
ESPI_MISO	X1-43	I	Signal i.MX53: ECSPi1_MISO
ESPI_SS[3:0]#	X1-50-47-46-48	O	Signal i.MX53: ECSPi1_SS[3:0]#

- When required the port ECSPi1 can be configured as a boot device. Therefore the signal SS1# has to be used as slave select.

3.2.12.9 UART

The i.MX53 provides five UART interfaces. UART1, UART2 and UART3 are available at the module connectors.

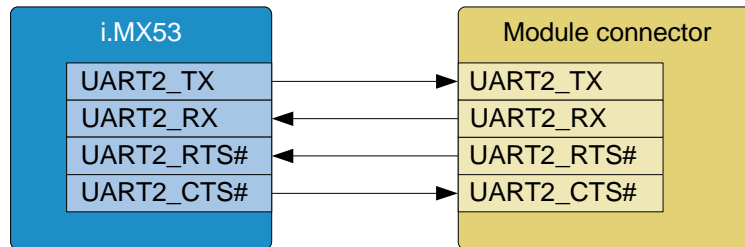


Illustration 9: Block diagram UART2 interface

The following table shows the signals used by the UART1 interface.

Table 34: UART1 signals

Signal name	TQMa53 pin	Direction	Remark
UART1_RXD	X2-30	I	–
UART1_TXD	X2-32	O	–

UART2 also provides handshake signals.

It is to be taken note of that in DTE as well as in DCE mode RTS# is always an input and CTS# is always an output. (See Freescale Reference Manual of the CPU (1).)

The UART2 interface with handshake signals provided by the processor is made available at the module connectors.

The following table shows the signals used by the UART2 interface.

Table 35: UART2 signals

Signal name	TQMa53 pin	Direction	Remark
UART2_RXD	X2-31	I	–
UART2_TXD	X2-29	O	–
UART2_RTS#	X2-33	I	–
UART2_CTS#	X2-35	O	–

The following table shows the signals used by the UART3 interface.

Table 36: UART3 signals

Signal name	TQMa53 pin	Direction	Remark
UART3_RXD	X2-34	I	–
UART3_TXD	X2-36	O	–

- UART4 and UART5 are available if the I²S interface is not used.

3.2.12.10 USB

The i.MX53 CPU provides three USB Host Cores and one USB OTG Core.

The USB-Host1-Core and the USB-OTG-Core have an integrated High-Speed-PHY and are available at the module connectors.

The following table shows the signals used by the USB_H1 interface.

Table 37: USB_H1 signals

Signal name	TQMa53 pin	Direction	Remark
USB_H1_DP	X2-104	I/O	–
USB_H1_DN	X2-102	I/O	–
USB_H1_VBUS	X2-108	AI	Series resistor 100 Ω and capacitor 1 μ F to GND on the TQMa53.
USB_H1_PWR	X2-49 or X1-86	O	Not in Default BSP. Available on I2S_MCLK (X2-49) or DISP1_DAT20 (X1-86).
USB_H1_OC	X2-61 or X1-73	I	Not in Default BSP. Available on GPIO1_GPIO3 (X2-61) or DISP1_DAT21 (X1-73).

The following table shows the signals used by the USB_OTG interface.

Table 38: USB_OTG signals

Signal name	TQMa53 pin	Direction	Remark
USB_OTG_DP	X2-103	I/O	–
USB_OTG_DN	X2-101	I/O	–
USB_OTG_VBUS	X2-109	AI	Series resistor 100 Ω and capacitor 1 μ F to GND on the TQMa53.
USB_OTG_ID	X2-107	I	–
USB_OTG_PWR	X2-41 or X1-33	O	Not in Default BSP. Available on CAN2_RX (X2-41) or GPIO3_GPIO22 (X1-33).
USB_OTG_OC	X2-39 or X1-34	I	Not in Default BSP. Available on CAN2_TX (X2-39) or GPIO3_GPIO21 (X1-34).

- A third USB High-Speed interface can be implemented by connecting USB-Host3 to an ULPI PHY on the carrier board. The USB HOST3 signals are multiplexed with the signals of the Camera Sensor Interface 0 (CSI0). If USB HOST3 is used the CSI0 is not available anymore.

3.2.13 Reset

The following reset inputs or outputs are available at the module connectors of the TQMa53.
The following block diagram shows the wiring of the reset signals.

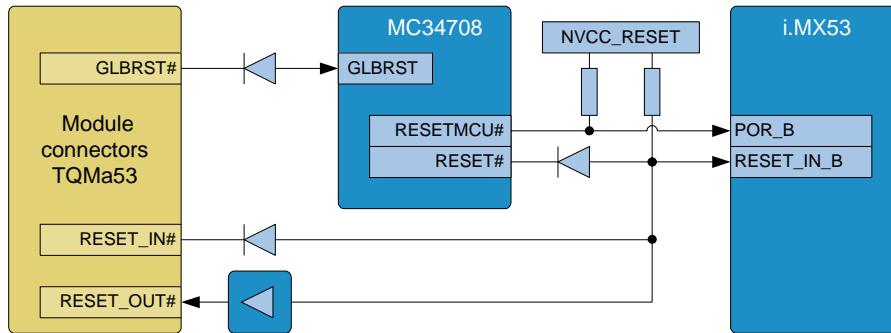


Illustration 10: Reset, block diagram

The following table describes the reset signals which are available at the module connectors.

Table 39: Reset signals

Signal name	TQMa53 pin	Direction	Remark
RESET_IN#	X2-64	I _{PU}	<ul style="list-style-type: none"> Reset input of the i.MX53 System Reset Controller Generates WARM-Reset of the CPU On the module: PU 28 kΩ to 2.775 V Low-active signal
RESET_OUT#	X2-22	O _{OD}	<ul style="list-style-type: none"> Reset output of the PMIC Can be used for reset inputs of external periphery Open Drain, requires pull-up on the carrier board (max. 3.3 V)
GLBRST#	X2-20	I _{PU}	<ul style="list-style-type: none"> Global reset input of the PMIC Generates cold start of the PMIC Internal pull-up to 1.5 V To activate GLBRST apply low level for preset time according to PMIC register GLBRSTTMR[1:0] (see Data sheet PMIC (5))

3.2.14 Supply

3.2.14.1 Overview module supply

The following table shows some technical parameters of the module supply.

The given current consumption has to be seen as an approximate value.

To estimate the power consumption of the system the Freescale Application Note AN4270 (8) should be heeded as the current consumption of the TQMa53 strongly depends on the application, the mode of operation and the operating system.

Table 40: Parameter module supply

Parameter	Value typ.	Remark
Supply voltage V_{IN}	5 V	$\pm 5\%$
Current consumption Linux (idle)	420 mA	CPU 800 MHz / BSP without power management
Current consumption Linux (100 %)	580 mA	CPU 800 MHz / BSP without power management
Switch-on current	5.6 A	Peak current for approximately 1.2 μ s

In principle, the CPU supports besides the Dynamic Voltage Scaling the following Power Modes:

- RUN
- WAIT
- STOP

The implementation of the modes depends on the BSP and is not considered here.

All requirements according to hardware are created by using an intelligent PMIC.

The PMIC itself also has different power modes whose implementation depends on the software.

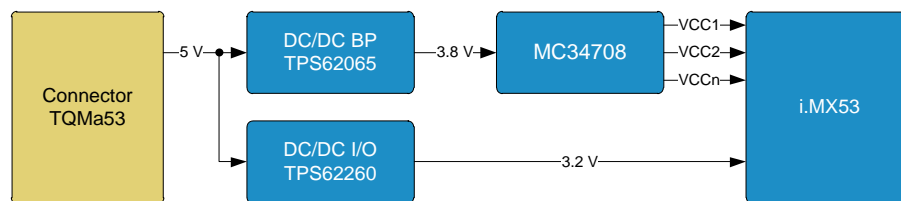


Illustration 11: Power supply, block diagram

In addition to the Freescale PMIC MC34708 two more voltage converters are implemented on the TQMa53. They generate the I/O voltage and the supply voltage for the PMIC.

The following table shows the electric characteristics of both DC/DC converters.

Description	Converter	Power rail	$U_{(min)}$	$U_{(typ)}$	$U_{(max)}$	$I_{(max)}$
DC/DC BP	TPS62065	VCC3V8_BP	3.691 V	3.8 V	3.933 V	1.7 A
DC/DC I/O	TPS62260	VCC3V2	3.145 V	3.2 V	3.348 V	0.6 A

3.2.14.2 Voltage monitoring

An optional supervisor is provided on the TQMa53 to improve the module behaviour and to fix the erratum ER39 of the Freescale-PMIC (voltage drops).

On account of PMIC erratum ER39 modules without supervisor may have restart problems after a brownout.

The supervisor monitors the input voltage VCC5V. The output of the supervisor is connected to the Enable input of the DC/DC BP regulator (see Illustration 11), which supplies the PMIC.

The following block diagram shows how the supervisor is integrated.

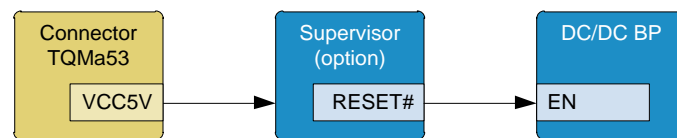


Illustration 12: Optional supervisor, block diagram

The module version with supervisor can only be used in systems, which implement the control of the mainboard regulator as described in section 3.2.14.4, Illustration 13.

The supervisor has the following characteristics:

- Typical threshold voltage: 4,55 V
- Typical delay time: 200 ms

The voltages generated by the PMIC and the DC/DC converters on the TQMa53 are not monitored.

On the TQMa53 the following mechanisms or possibilities to monitor the voltage exist:

- **VCC3V8_BP: PMIC function "BP lower than VBAT_TKRL"** ⇒ switch to Off mode, if BP < 3.0 V (for more information see Data Sheet PMIC (5)).
- **VCC3V8_BP: PMIC ADC channel 2** ⇒ monitoring of undervoltage or overvoltage in software (for more information see Data Sheet PMIC (5)).
- **VCC1V1_SW1 (VDDGP): CPU function "brownout detection"** ⇒ Power_Fail, if VDDGP < 0.8 V (for more information see Reference Manual CPU (1)).
- **VCC2V775:** Voltage is routed to module connector and can be monitored on the carrier board.
- **VCC3V2:** Optional monitoring on the carrier board can be done with an unused I2C3 pin. Therefore the pin has to be configured accordingly and a pull-up resistor has to be assembled on the TQMa53.

3.2.14.3 PMIC signals

The CPU communicates with the PMIC via I²C (I2C2).

- The I²C address of the PMIC is 0x08 / 0b0001000.

The following table shows the signals used by the PMIC, which are made available at the module connectors, as well as the signals, which serve for the communication with the CPU.

Table 41: PMIC signals

Signal name	Description
PWRON	<ul style="list-style-type: none"> – Power on/off button connection 1 to PMIC – Switch to GND – Internal pull-up to 1.5 V
SYSTEM_DOWN#	Indication of imminent system shutdown to processor
PMIC_INT	Interrupt to processor
WDOG#	Watchdog output to PMIC
PMIC_STBY_REQ	Standby output signal to PMIC
PMIC_ON_REQ	Power on/off connection 2 to PMIC

3.2.14.4 Module / carrier board Power-Up sequence

The chronological behaviour of the voltages generated on the carrier board are required for its design because the TQMa53 requires a supply voltage of 5 V, and the 3.2 V I/O voltage of the CPU signals is generated on the TQMa53.

Attention: Power-Up sequence



The following procedure must be adhered to on the base board to enable a correct power-up sequence: The 5 V supply voltage for the TQMa53 is present and the carrier board supply of 3.3 V is activated via module pin VCC2V775. After activation the voltage must be stable within 12 ms.

The following illustration shows the control of a voltage regulator on a carrier board using VCC2V775.

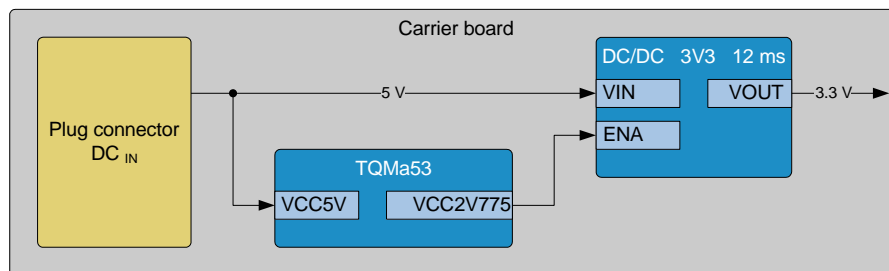


Illustration 13: Block diagram power supply carrier board

With the procedure described above it is certified that the pull-ups on the carrier board are already supplied with voltage when the boot-configuration pins are read.

- In case the LCD bus signals or the matching multiplexed signals representing the boot configurations pins, are not used, the reference voltage VCC2V775 available at the module connector can also be used as a pull-up voltage for the configuration resistors.

Attention: Power-Up sequence



No I/O pins of external components may be driven during the boot-process to avoid cross-supply and errors in the power-up sequence.

3.3 Module interface

3.3.1 Pin assignment

When using the processor signals the multiple pin configurations by different processor-internal function units must be taken note of. The pins assignment listed in sections 3.3.2 and 3.3.3 refer to the corresponding standard BSP of TQ-Systems GmbH. The electrical and pin characteristics are to be taken from the data sheets of CPU (2), (3) and PMIC (5).



3.3.2 Pinout module connector X1

Table 42: Pinout module connector X1

Ball	I/O	Level	Group	Signal	Pin	Signal	Group	Level	I/O	Ball
–	P	0 V	POWER	DGND	1	2	DGND	POWER	0 V	P
P02	I	3.3 V	CSIO	CSIO_HSYNC	3	4	CSIO_PIXCLK	CSIO	3.3 V	I
P04	I	3.3 V	CSIO	CSIO_VSYNC	5	6	DGND	POWER	0 V	P
–	P	0 V	POWER	DGND	7	8	CSIO_DATA_EN	CSIO	3.3 V	I
R01	I	3.3 V	CSIO	CSIO_D4	9	10	CSIO_D5	CSIO	3.3 V	I
R06	I	3.3 V	CSIO	CSIO_D6	11	12	CSIO_D7	CSIO	3.3 V	I
T01	I	3.3 V	CSIO	CSIO_D8	13	14	CSIO_D9	CSIO	3.3 V	I
R05	I	3.3 V	CSIO	CSIO_D10	15	16	CSIO_D11	CSIO	3.3 V	I
T03	I	3.3 V	CSIO	CSIO_D12	17	18	CSIO_D13	CSIO	3.3 V	I
U01	I	3.3 V	CSIO	CSIO_D14	19	20	CSIO_D15	CSIO	3.3 V	I
T04	I	3.3 V	CSIO	CSIO_D16	21	22	CSIO_D17	CSIO	3.3 V	I
U03	I	3.3 V	CSIO	CSIO_D18	23	24	CSIO_D19	CSIO	3.3 V	I
P05	I	3.3 V	CSIO	CSIO_PWDN	25	26	CSIO_MCLK	CSIO	3.3 V	I
P06	I	3.3 V	CSIO	CSIO_RST#	27	28	DGND	POWER	0 V	P
–	P	0 V	POWER	DGND	29	30	GPIO3_GPIO20	GPIO	3.3 V	IO
AA01	IO	3.3 V	GPIO	GPIO3_GPIO28	31	32	GPIO3_GPIO29	GPIO	3.3 V	IO
W02	IO	3.3 V	GPIO	GPIO3_GPIO22	33	34	GPIO3_GPIO21	GPIO	3.3 V	IO
AB04	IO [1]	3.3 V	GPIO	GPIO2_GPIO26	35	36	GPIO2_GPIO27	GPIO	3.3 V	IO [2]
V08	IO [1]	3.3 V	GPIO	GPIO2_GPIO25	37	38	GPIO2_GPIO23	GPIO	3.3 V	IO [1]
AC06	IO	3.3 V	GPIO	GPIO3_GPIO11	39	40	GPIO3_GPIO13	GPIO	3.3 V	IO
AB09	IO [1]	3.3 V	GPIO	GPIO5_GPIO0	41	42	GPIO3_GPIO14	GPIO	3.3 V	IO
U05	I	3.3 V	ESPI	ESPI_MISO	43	44	GPIO3_GPIO12	GPIO	3.3 V	IO
V01	O	3.3 V	ESPI	ESPI_MOSI	45	46	ESPI_SS1#	ECSPI1	3.3 V	O
Y02	O	3.3 V	ESPI	ESPI_SS2#	47	48	ESPI_SS0#	ECSPI1	3.3 V	O
–	P	0 V	POWER	DGND	49	50	ESPI_SS3#	ECSPI1	3.3 V	O
AB07	O	3.3 V	DISP1	DISP1_DRDY_DE	51	52	DGND	POWER	0 V	P
AA08	O	3.3 V	DISP1	DISP1_DAT1	53	54	ESPI_SCLK	ECSPI1	3.3 V	O
Y09	O	3.3 V	DISP1	DISP1_DAT3	55	56	DISP1_CLK	DISP1	3.3 V	O [2]
AB06	O	3.3 V	DISP1	DISP1_DAT5	57	58	DGND	POWER	0 V	P
AA07	O	3.3 V	DISP1	DISP1_DAT7	59	60	DISP1_HSYNC	DISP1	3.3 V	O
Y08	O	3.3 V	DISP1	DISP1_DAT9	61	62	DISP1_VSYNC	DISP1	3.3 V	O
AC03	O [2]	3.3 V	DISP1	DISP1_DAT11	63	64	DGND	POWER	0 V	P
AB03	O [2]	3.3 V	DISP1	DISP1_DAT13	65	66	DISP1_DAT0	DISP1	3.3 V	O
Y06	O [2]	3.3 V	DISP1	DISP1_DAT15	67	68	DISP1_DAT2	DISP1	3.3 V	O
AA03	O [2]	3.3 V	DISP1	DISP1_DAT17	69	70	DISP1_DAT4	DISP1	3.3 V	O
Y05	O [1]	3.3 V	DISP1	DISP1_DAT19	71	72	DISP1_DAT6	DISP1	3.3 V	O
W04	O	3.3 V	DISP1	DISP1_DAT21	73	74	DISP1_DAT8	DISP1	3.3 V	O
V04	O	3.3 V	DISP1	DISP1_DAT23	75	76	DISP1_DAT10	DISP1	3.3 V	O [2]
–	P	0 V	POWER	DGND	77	78	DISP1_DAT12	DISP1	3.3 V	O [2]
AA09	O	3.3 V	VGA	VGA_HSYNC	79	80	DISP1_DAT14	DISP1	3.3 V	O [2]
Y07	O [1]	3.3 V	VGA	VGA_VSYNC	81	82	DISP1_DAT16	DISP1	3.3 V	O [2]
AC19	AO	0.7 V	VGA	TVDAC_IOB	83	84	DISP1_DAT18	DISP1	3.3 V	O [1]
AB20	AO	0.7 V	VGA	TVDAC_I0G	85	86	DISP1_DAT20	DISP1	3.3 V	O
AC21	AO	0.7 V	VGA	TVDAC_I0R	87	88	DISP1_DAT22	DISP1	3.3 V	O
–	P	0 V	POWER	DGND	89	90	DGND	POWER	0 V	P
AC16	O	1.2 V	LVDS0	LVDS0_CLK_P	91	92	LVDS1_CLK_P	LVDS1	1.2 V	O
AB16	O	1.2 V	LVDS0	LVDS0_CLK_N	93	94	LVDS1_CLK_N	LVDS1	1.2 V	O
–	P	0 V	POWER	DGND	95	96	DGND	POWER	0 V	P
AA17	O	1.2 V	LVDS0	LVDS0_TX0_P	97	98	LVDS1_TX0_P	LVDS1	1.2 V	O
Y17	O	1.2 V	LVDS0	LVDS0_TX0_N	99	100	LVDS1_TX0_N	LVDS1	1.2 V	O
–	P	0 V	POWER	DGND	101	102	DGND	POWER	0 V	P
AC17	O	1.2 V	LVDS0	LVDS0_TX1_P	103	104	LVDS1_TX1_P	LVDS1	1.2 V	O
AB17	O	1.2 V	LVDS0	LVDS0_TX1_N	105	106	LVDS1_TX1_N	LVDS1	1.2 V	O
–	P	0 V	POWER	DGND	107	108	DGND	POWER	0 V	P
AA16	O	1.2 V	LVDS0	LVDS0_TX2_P	109	110	LVDS1_TX2_P	LVDS1	1.2 V	O
Y16	O	1.2 V	LVDS0	LVDS0_TX2_N	111	112	LVDS1_TX2_N	LVDS1	1.2 V	O
–	P	0 V	POWER	DGND	113	114	DGND	POWER	0 V	P
AC15	O	1.2 V	LVDS0	LVDS0_TX3_P	115	116	LVDS1_TX3_P	LVDS1	1.2 V	O
AB15	O	1.2 V	LVDS0	LVDS0_TX3_N	117	118	LVDS1_TX3_N	LVDS1	1.2 V	O
–	P	0 V	POWER	DGND	119	120	DGND	POWER	0 V	P

1 Out-Of-Reset: output.

2 During Power-On-Reset: input; Out-of-Reset: output.



3.3.3 Pinout module connector X2

Table 43: Pinout module connector X2

Ball	I/O	Level	Group	Signal	Pin	Signal	Group	Level	I/O	Ball	
–	P	5 V	POWER	VCC5V	1	2	VCC5V	POWER	5 V	P	–
–	P	5 V	POWER	VCC5V	3	4	VCC5V	POWER	5 V	P	–
–	P	5 V	POWER	VCC5V	5	6	VCC5V	POWER	5 V	P	–
–	P	0 V	POWER	DGND	7	8	DGND	POWER	0 V	P	–
–	P	0 V	POWER	DGND	9	10	DGND	POWER	0 V	P	–
–	P	0 V	POWER	DGND	11	12	DGND	POWER	0 V	P	–
K04*	AI	2.4 V	TOUCH	TSX1	13	14	TSY1	TOUCH	2.4 V	AI	J07*
L05*	AI	2.4 V	TOUCH	TSX2	15	16	TSY2	TOUCH	2.4 V	AI	J06*
–	P	0 V	POWER	DGND	17	18	DGND	POWER	0 V	P	–
A11*	P	3.3 V	PMIC	LICELL	19	20	GLBRST#	PMIC	3.3 V	I _{IPU}	G07*
G08*	I _{IPU}	1.5 V	PMIC	PWRON	21	22	RESET_OUT#	PMIC	3.3 V	O _{OD}	–
L03	O	3.3 V	LCD	LCD_BLT_EN	23	24	LCD_PWR_EN	LCD	3.3 V	O	M04
B07	O	3.3 V	LCD	LCD_CONTRAST	25	26	LCD_RESET	LCD	3.3 V	O	L04
–	P	0 V	POWER	DGND	27	28	DGND	POWER	0 V	P	–
J01	O	3.3 V	UART2	UART2_TXD	29	30	UART1_RXD	UART1	3.3 V	I	J02
K04	I	3.3 V	UART2	UART2_RXD	31	32	UART1_TXD	UART1	3.3 V	O	J03
K03	I	3.3 V	UART2	UART2_RTS#	33	34	UART3_RXD	UART3	3.3 V	I	L02
K05	O	3.3 V	UART2	UART2_CTS#	35	36	UART3_TXD	UART3	3.3 V	O	L05
–	P	0 V	POWER	DGND	37	38	DGND	POWER	0 V	P	–
E05	O	3.3 V	CAN2	CAN2_TX	39	40	CAN1_TX	CAN1	3.3 V	O	C04
E06	I	3.3 V	CAN2	CAN2_RX	41	42	CAN1_RX	CAN1	3.3 V	I	D05
D06	I	3.3 V	I2S	I2S_DIN	43	44	I2S_SCLK	I2S	3.3 V	O [3]	C05
E07	O	3.3 V	I2S	I2S_LRCLK	45	46	I2S_DOUT	I2S	3.3 V	O	B03
–	P	0 V	POWER	DGND	47	48	DGND	POWER	0 V	P	–
C08	O	3.3 V	I2S	I2S_MCLK	49	50	SPDIF_OUT	SPDIF	3.3 V	O	A03
–	P	0 V	POWER	DGND	51	52	SPDIF_IN	SPDIF	3.3 V	I	C06
B05	O	3.3 V	FIRI	FIRI_TXD	53	54	FIRI_RXD	FIRI	3.3 V	I	A04
D04	I _{OPU}	3.3 V	I2C2	I2C2_SDA	55	56	I2C3_SDA	I2C3	3.3 V	IO	B06
F06	I _{OPU}	3.3 V	I2C2	I2C2_SCL	57	58	I2C3_SCL	I2C3	3.3 V	IO	A05
–	P	0 V	POWER	DGND	59	60	DGND	POWER	0 V	P	–
A06	I/O	3.3 V	GPIO	GPIO1_GPIO3	61	62	OWIRE	1-WIRE	3.3 V	I/O	D07
A07	O	2.775 V	JTAG	JTAG_TDO	63	64	RESET_IN#	CONFIG	3.3 V	I _{PU}	–
A08	I _{PU}	2.775 V	JTAG	JTAG_TMS	65	66	JTAG_TDI	JTAG	2.775 V	I _{PU}	B08
E09	I _{PU}	2.775 V	JTAG	JTAG_TRST#	67	68	JTAG_TCK	JTAG	2.775 V	I _{PD}	D09
–	P	0 V	POWER	DGND	69	70	DGND	POWER	0 V	P	–
A10	O	[4]	SATA	SATA_TXP	71	72	SATA_RXP	SATA	[4]	I	B12
B10	O	[4]	SATA	SATA_TXM	73	74	SATA_RXM	SATA	[4]	I	A12
–	P	0 V	POWER	DGND	75	76	DGND	POWER	0 V	P	–
M05	I	3.3 V	FEC	FEC_INT#	77	78	FEC_RST#	FEC	3.3 V	O	K06
C10	O	3.3 V	FEC	FEC_TX_EN	79	80	FEC_RXD0	FEC	3.3 V	I	C11
F10	O	3.3 V	FEC	FEC_TXD0	81	82	FEC_RXD1	FEC	3.3 V	I	E11
D10	O	3.3 V	FEC	FEC_TXD1	83	84	FEC_RX_DV	FEC	3.3 V	I	D11
E10	O	3.3 V	FEC	FEC_MDC	85	86	FEC_MDIO	FEC	3.3 V	I _{OPU}	D12
F12	I	3.3 V	FEC	FEC_RX_ER	87	88	FEC_REF_CLK	FEC	3.3 V	I	E12
–	P	0 V	POWER	DGND	89	90	DGND	POWER	0 V	P	–
C07	I	3.3 V	SD	SD_WP	91	92	SD_DAT0	SD	3.3 V	IO	D13
D08	I	3.3 V	SD	SD_CD#	93	94	SD_DAT1	SD	3.3 V	IO	C14
C15	IO	3.3 V	SD	SD_CMD	95	96	SD_DAT2	SD	3.3 V	IO	D14
E14	O	3.3 V	SD	SD_CLK	97	98	SD_DAT3	SD	3.3 V	IO	E13
–	P	0 V	POWER	DGND	99	100	DGND	POWER	0 V	P	–
A19	IO	[5]	USBOTG	USB_OTG_DN	101	102	USB_H1_DN	USBH1	[5]	IO	B17
B19	IO	[5]	USBOTG	USB_OTG_DP	103	104	USB_H1_DP	USBH1	[5]	IO	A17
–	P	0 V	POWER	DGND	105	106	DGND	POWER	0 V	P	–
C16	I	3.3 V	USBOTG	USB_OTG_ID	107	108	USB_H1_VBUS	USBH1	5.0 V	AI	D15
E15	AI	5.0 V	USBOTG	USB_OTG_VBUS	109	110	BOOT_MODE0	CONFIG	2.775 V	I _{PD}	C18
–	P	2.775 V	POWER	VCC2V775	111	112	BOOT_MODE1	CONFIG	2.775 V	I _{PU}	B20
C17	O	3.3 V	SPI	SPI_SS0#	113	114	SPI_SS2#	SPI	3.3 V	O	F16
A20	I	3.3 V	SPI	SPI_MISO	115	116	SPI_SS1#	SPI	3.3 V	O	F17
E16	O	3.3 V	SPI	SPI_SCLK	117	118	SPI_MOSI	SPI	3.3 V	O	F18
–	P	0 V	POWER	DGND	119	120	DGND	POWER	0 V	P	–

* PMIC ball.

3 During Power-On-Reset: output.

4 See Serial ATA Specification 2.6.

5 See USB Specification 2.0.

4. MECHANICS

4.1 Module connectors

The TQMa53 is connected to the carrier board with 240 pins on two module connectors.
The following table shows details of the plug connector used.

Table 44: Plug connector (receptacle) used on the TQMa53

Manufacturer / number	Description	Package
TE Connectivity / 5177985-5	<ul style="list-style-type: none"> 120-pin plug connector (receptacle) 0.8 mm pitch Vertical Plating: Gold (8) 0.2 μm -40 °C to +125 °C 	SMD120

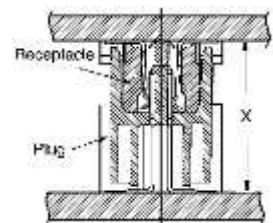
The module is held in the plug connectors with a considerable retention force.

To avoid damaging the modules' plug connectors as well as the carrier board plug connectors while removing the module the use of an extraction tool is strongly recommended. See section 4.3.5 for further information.

The following table shows some suitable mating plug connectors for the carrier board.

Table 45: Suitable carrier board mating plug connectors

Manufacturer / number	Contact Plating	Stack height (X)
TE Connectivity / 5177986-5	0.2 μm Gold	5 mm
TE Connectivity / 5-5177986-5	0.76 μm Gold	5 mm
TE Connectivity / 1-5177986-5	0.2 μm Gold	6 mm
TE Connectivity / 6-5177986-5	0.76 μm Gold	6 mm
TE Connectivity / 2-5177986-5	0.2 μm Gold	7 mm
TE Connectivity / 1-5179030-5	0.76 μm Gold	7 mm
TE Connectivity / 3-5177986-5	0.2 μm Gold	8 mm
TE Connectivity / 6123001-5	0.76 μm Gold	8 mm



4.2 Dimensions

- Board dimensions (L × W) 55.0 × 44.0 mm²
- Stack height⁶ see Illustration 14
- Mass 15 gram ± 1 gram

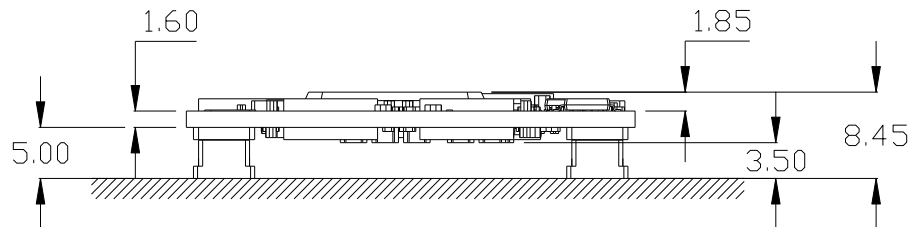


Illustration 14: Stack height

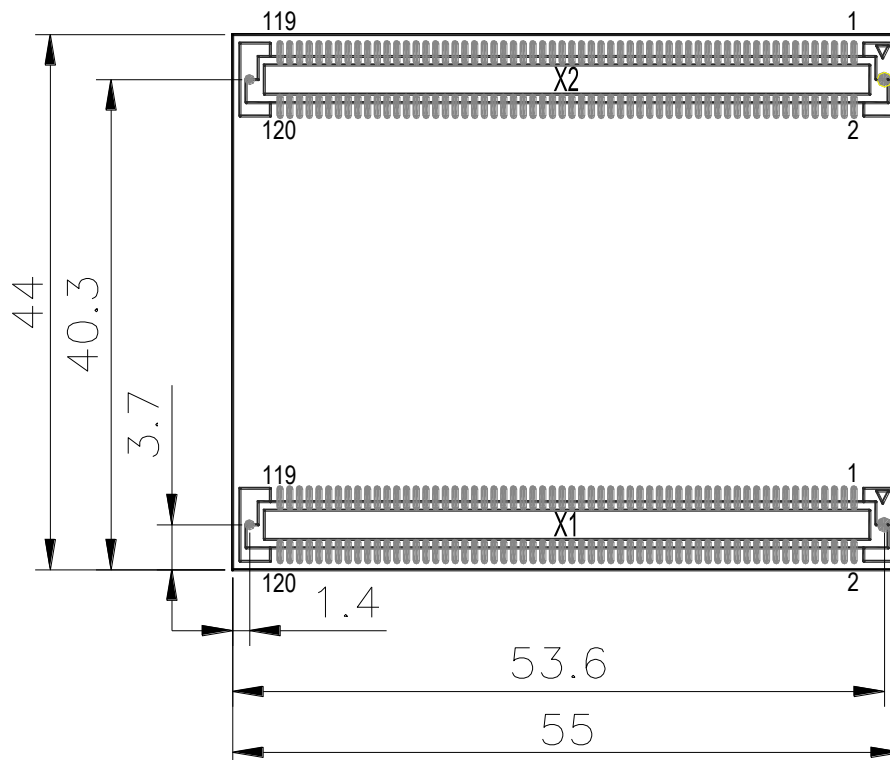


Illustration 15: Overall dimensions (bottom view)

⁶ For 5 mm board to board distance.

4.3 Component placement

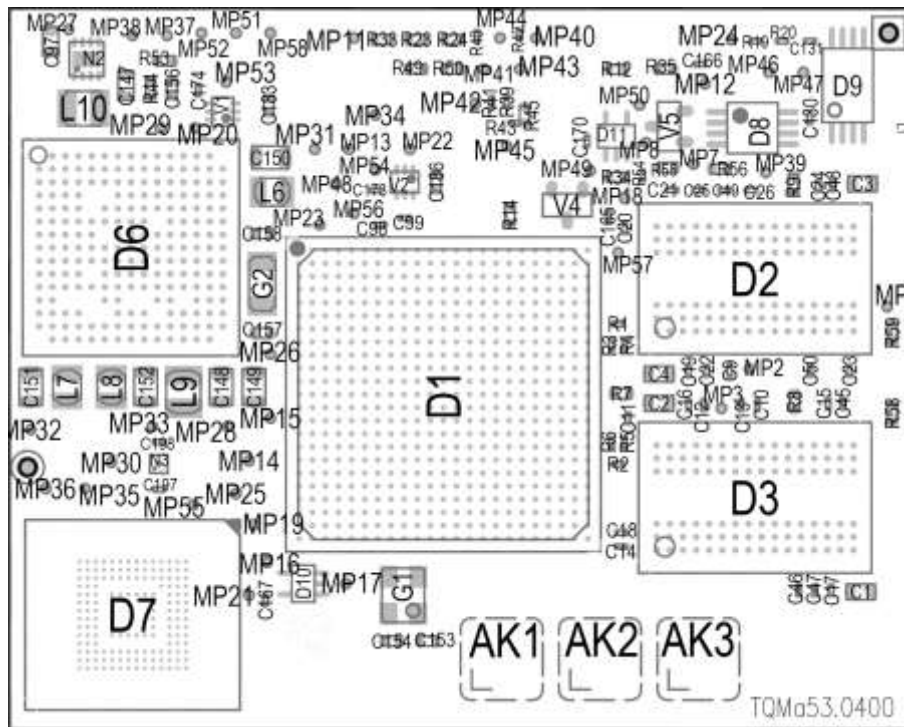


Illustration 16: Component placement top

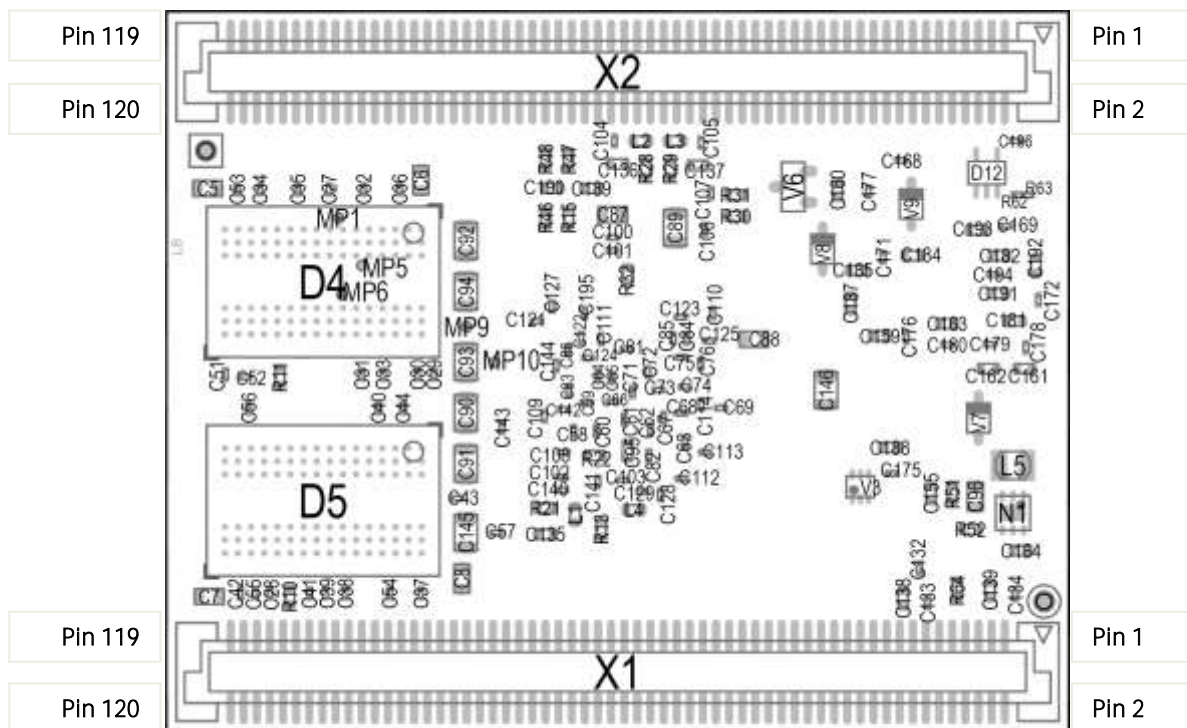


Illustration 17: Component placement bottom

4.3.1 Adaptation to the environment

The overall dimensions (length × width × height) of the Minimodule are 55 × 44 × 6.6 mm³.

The maximum height of the TQMa53 above the carrier board is approximately 8.5 mm see Illustration 14.

4.3.2 Protection against external effects

As an embedded module the TQMa53 is not protected against dust, external impact and contact (IP00).

Adequate protection has to be guaranteed by the surrounding system.

4.3.3 Thermal management

To cool the TQMa53, a maximum of 3 W have to be dissipated, as described in section 3.2.14.1. The power dissipation originates primarily in the processor, the DDR3 SDRAM and the PMIC. The customer is responsible for cooling the TQMa53 in his application. With sufficient airflow a passive cooling should be sufficient in most cases.

4.3.4 Structural requirements

The TQMa53 is held in the module socket by the retention force of the pins (a total of 240). For high requirements with respect to vibration and shock firmness an additional plastic module holder has to be provided in the final product to hold the module in its position. For this purpose TQ-Systems GmbH provides a standard solution. As no heavy and big components are used, no further requirements are given.

Attention: Destruction or malfunction



The CPU belongs to a performance category in which a cooling system may be essential in certain applications. It is the responsibility of the customer to define a suitable cooling method depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software).

4.3.5 Notes of treatment

To avoid damage caused by mechanical stress, the TQMa53 may only be extracted from the carrier board by using the extraction tool MOZI8XXL that can also be obtained separately.

Attention: Note with respect to the component placement of the carrier board



2.5 mm should be kept free on the carrier board, along the longitudinal edges on both sides of the module for the extraction tool.

5. SOFTWARE

The TQMa53 comes with a preinstalled boot loader. The Boot loader and the also available BSP are tailored for the combination of TQMa53 and Starterkit STK-MBa53. More information can be found in the [Support Wiki for the TQMa53](#).

The boot loader contains module specific as well as carrier-board adaptations as for example

- CPU configuration
- PMIC configuration
- RAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strength

These settings have to be adapted if a different boot loader is used. More details can be requested from the TQ-Support.



6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The module was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding besides, take note of not only the frequency, but also the signal rise times
- Filtering of all signals which can be connected externally (also "slow signals" and DC can radiate RF indirectly)

Because the TQMa53 is a module, which is used on an application-specific carrier board, EMC or ESD tests only make sense for the whole device. The TQMa53 is designed to pass the following test:

- EMC-Interference radiation:
Measurement of the electrically radiated emission for standard, residential, commercial and light industrial environments in the range of 30 MHz to 1 GHz according to DIN EN 61000-6-3 respective DIN EN 55022.

6.2 ESD

In order to avoid interspersions on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa53.

Following measures are recommended for a carrier board:

- | | |
|-------------------------|--|
| • Generally applicable: | Shielding of the inputs
(shielding connected well to ground / housing on both ends) |
| • Supply voltages: | Protection by suppressor diode(s) |
| • Slow signal lines: | RC filtering, perhaps Zener diode(s) |
| • Fast signal lines: | Integrated protective devices (e.g., suppressor diode arrays) |

6.3 Operational safety and personal security

Due to the occurring voltages (≤ 5 V DC), tests with respect to the operational and personal safety haven't been carried out.

6.4 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection), hence, no fixed value can be given for the whole assembly. In general, a reliable operation is given when following conditions are met:

Table 2: Climate and operating conditions "Commercial temp. range" 0 °C to +70 °C

Parameter	Range	Remark
Die temperature CPU i.MX535	–40 °C to +105 °C	>95 °C, see (3)
Die temperature CPU i.MX537	–40 °C to +125 °C	>105 °C, see (2)
Die temperature PMIC	–40 °C to +125 °C	–
Housing temperature DDR3 SDRAM	0 °C to +95 °C	–
Housing temperature other ICs	0 °C to +70 °C	–
Permitted storage temperature TQMa53	–40 °C to +85 °C	–
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

Table 3: Climate and operating conditions "Extended temp. range" –25 °C to +85 °C

Parameter	Range	Remark
Die temperature CPU i.MX535	–40 °C to +105 °C	>95 °C, see (3)
Die temperature CPU i.MX537	–40 °C to +125 °C	>105 °C, see (2)
Die temperature PMIC	–40 °C to +125 °C	–
Housing temperature DDR3 SDRAM	–40 °C to +95 °C	–
Housing temperature other ICs	–25 °C to +85 °C	–
Permitted storage temperature TQMa53	–40 °C to +85 °C	–
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

Table 4: Climate and operating conditions "Industrial temp. range" –40 °C to +85 °C

Parameter	Range	Remark
Die temperature CPU i.MX537	–40 °C to +125 °C	>105 °C, see (2)
Die temperature PMIC	–40 °C to +125 °C	–
Housing temperature DDR3 SDRAM	–40 °C to +95 °C	–
Housing temperature other ICs	–40 °C to +85 °C	–
Permitted storage temperature TQMa53	–40 °C to +85 °C	–
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

Detailed information about the thermal characteristics of the CPU are to be taken from the Freescale Data Sheets (2) and (3).

Attention: Destruction or malfunction



The CPU belongs to a performance category in which a cooling system may be essential in certain applications. It is the responsibility of the customer to define a suitable cooling method depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software).



6.5 Reliability and service life

No detailed MTBF calculation has been done for the TQMa53.

The TQMa53 is designed to be insensitive to vibration and impact.

Middle grade connectors, which guarantee at least 100 mating cycles, were used for the module.

6.6 Environment protection

6.6.1 RoHS compliance

The TQMa53 is manufactured RoHS compliant.

- All used components and assemblies are RoHS compliant
- RoHS compliant soldering processes are used

6.6.2 WEEE regulation

The company placing the product on the market is responsible for the observance of the WEEE regulation.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

6.7 Batteries

No batteries are used on the TQMa53.

6.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.

The energy consumption of this subassembly is minimised by suitable measures.

Printed pc-boards are delivered in reusable packaging.

Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.

Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
(source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
(source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
(source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
(source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

7. APPENDIX

7.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 46: Acronyms

Acronym	Meaning
AI	Analog Input
ARM®	Advanced RISC Machine
AXI	Advanced eXtensible Interface (bus)
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
CSI	Camera Sensor Interface
CSPI	Configurable SPI
DC	Direct Current
DDR	Double Data Rate
DISP	Display
DLL	Delay-Locked Loop
eCSPI	enhanced Configurable SPI
EEPROM	Electrically Erasable Programmable Read-only Memory
EIM	External Interface Module
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
eMMC	embedded Multi-Media Card
EN	Europäische Norm
ESD	Electro-Static Discharge
eSD	enhanced Secure Digital
eSDHC	enhanced Multi-Media Card/Secure Digital Host Controller
eSPI	enhanced Serial Peripheral Interface
FEC	Fast Ethernet Controller
FIRI	Fast Infrared Interface
FR4	Flame Retardant 4
GND	Ground
GPIO	General Purpose Input/Output
I/O	Input/Output
IEEE®	Institute of Electrical and Electronics Engineers
IP	Ingress Protection
I²C	Inter-Integrated Circuit
I²S	Inter Integrated Circuit Sound
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LICELL	Lithium Cell
LVDS	Low Voltage Differential Signal
MISO	Master In Slave Out
MMC	Multimedia Card
MMU	Memory Management Unit
MOSI	Master Out Slave In
MOZI	Module extractor (Modulzieher)
MTBF	Mean operating Time Between Failures
NAND	Not-and
NOR	Not-or

Table 46: Acronyms (continued)

Acronym	Meaning
OSC	Oscillator
OTG	On-The-Go
PATA	Parallel ATA
PCB	Printed Circuit Board
PD	Pull-down (resistor)
PHY	Physical (interface)
PMIC	Power Management IC
PU	Pull-up (resistor)
PWM	Pulse Width Modulation
RC	Resistor Capacitor
RF	Radio Frequency
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
SATA	Serial ATA
SCL	Serial Clock
SD	Secure Digital
SDA	Serial Data
SDHC	Secure Digital High Capacity
SDIO	Secure Digital Input/Output
SDRAM	Synchronous Dynamic Random Access Memory
SJC	System JTAG Controller
SMD	Surface-Mounted Device
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SS	Slave Select
SSI	Synchronous Serial Interface
SW	Software
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin count Interface
USB	Universal Serial Bus
USB-HS	Universal Serial Bus - High Speed
USBOTG	USB On-The-Go
UTMI	USB 2.0 Transceiver Macrocell Interface
VGA	Video Graphics Array (640 × 480)
WDI	Watchdog Input
WDOG	Watchdog
WEEE®	Waste Electrical and Electronic Equipment
WEIM	Wireless External Interface Module



7.2 References

Table 47: Further applicable documents

No.	Name	Date	Company
(1)	i.MX53 Multimedia Applications Processor Reference Manual	2.1 / 2012-06	Freescale
(2)	i.MX53 Applications Processors for Industrial Products	6 / 03/2013	Freescale
(3)	i.MX53xD Applications Processors for Consumer Products	6 / 03/2013	Freescale
(4)	Chip Errata for the i.MX53	4 / 06/2013	Freescale
(5)	Power Management Integrated Circuit (PMIC) for i.MX50/53 Families	11.0 / 11/2013	Freescale
(6)	MC34708, Silicon Errata	9.0 / 11/2013	Freescale
(7)	i.MX53 System Development User's Guide	1 / 2011-03	Freescale
(8)	AN4270 Supply Current Measurements	1 / 02/2012	Freescale

