TQMa28
User's Manual

TQMa28 UM 200
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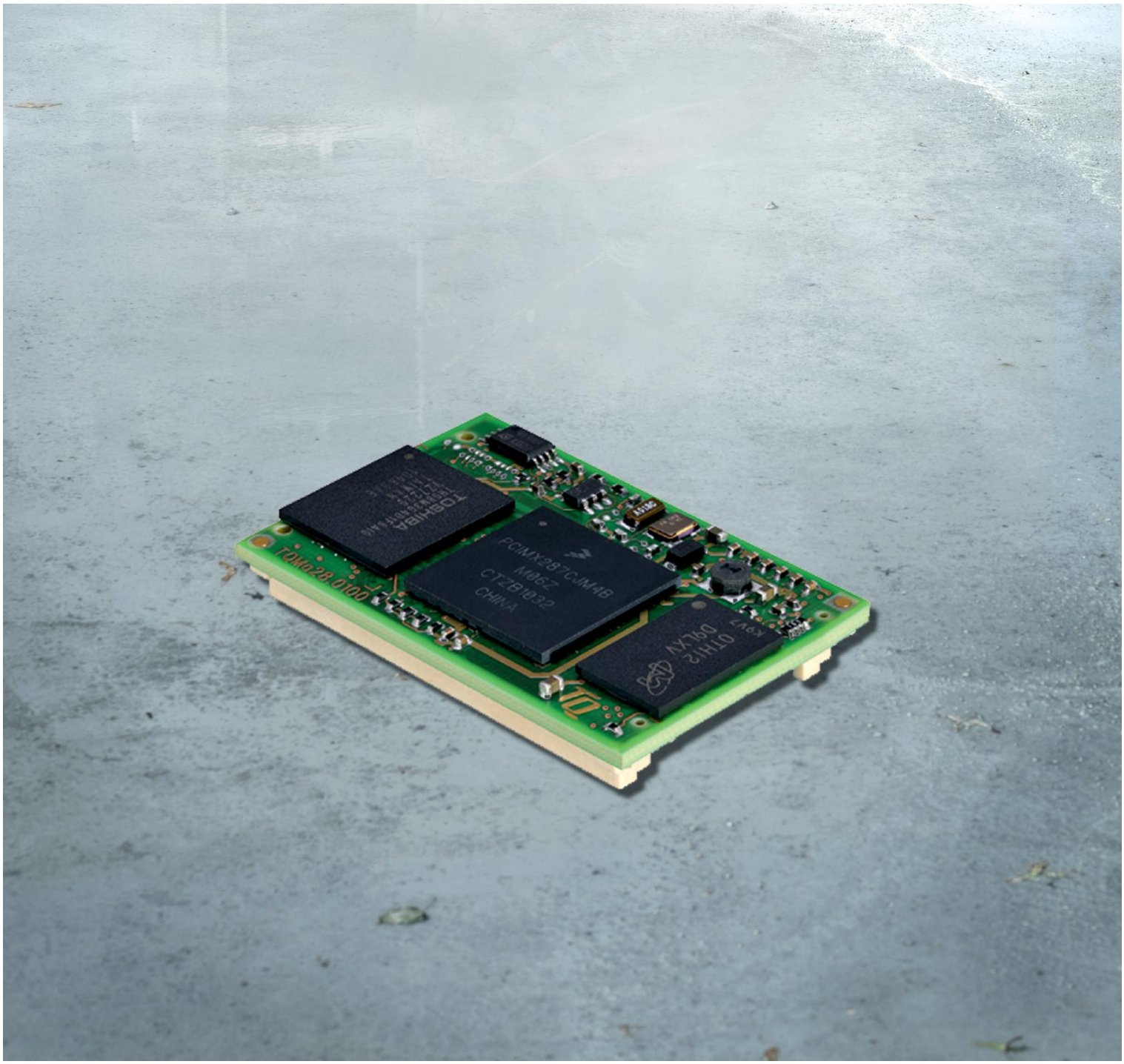

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Revision history

Rev.	Date	Name	Pos.	Modification
003	18.03.2011	Petz		Document created
004	14.07.2011	Petz	Table 6 Illustration 11	Pin assignment revised Replaced
100	25.10.2011	Petz	All	Complete rework
101	03.11.2011	Petz	Table 40	Unit corrected
102	19.12.2011	Petz	All	Expression “Accumulator” replaced with “battery” Expressions containing the word “battery” stated more precisely
103	24.05.2012	Petz	Table 4 Table 6 Table 6 Section 5	Values of plating corrected Typo corrected: LDADC4 ⇨ LRADC4 Negation removed: USB_0_PWR_EN, USB_1_PWR_EN Link to Wiki added
104	28.03.2013	Petz	4.2.6 3.1.2.1 All	Info concerning LAN8720 clarified Max. size of eMMC corrected Signal description of SD_WP and SD_DETECT# corrected
200	11.02.2014	Petz	All	Complete rework

1. ABOUT THIS MANUAL

1.1 Copyright and licence expenses

1.2 Registered trademarks

1.3 Disclaimer

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1.4 Imprint

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1.5 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the module and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

1.10 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 2: Acronyms

Acronym	Meaning
A/D	Analog/Digital
ADC	Analog/Digital Converter
AI	Analog In
ARM®	Advanced RISC Machine
AUART	Application Universal Asynchronous Receiver/Transmitter
BGA	Ball Grid Array
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DC	Direct Current
DDR	Double Data Rate
DUART	Debug Universal Asynchronous Receiver/Transmitter
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electro-Magnetic Compatibility
eMMC	embedded MultiMediaCard (Flash)
ESD	Electrostatic Discharge
GND	Ground
GPIO	General Purpose Input/Output
GPMI	General Purpose Media Interface
I	Input
I/O	Input/Output
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
I^2C	Inter-Integrated Circuit
I^2S	Inter Integrated Circuit Sound
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LL	Lower Left
LR	Lower Right
LVTTL	Low Voltage Transistor Transistor Logic
MOZI	Module extractor (Modulzieher)
MTBF	Mean operating Time Between Failures
NAND	Not-And
O	Output
OTG	On-The-Go
OTP	One-Time Programmable
PD	Pull-Down
PMU	Power Management Unit
PU	Pull-Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
RC	Resistor Capacitor
RGB	Red Green Blue
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
SAIF	Serial Audio Interface
SD	Secure Digital
SD card	Secure Digital Card
SD/MMC	Secure Digital Multimedia Card
SDRAM	Synchronous Dynamic Random Access Memory
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SSP	Synchronous Serial Port
STK	Starterkit
UART	Universal Asynchronous Receiver/Transmitter
UL	Upper Left
UR	Upper Right
USB	Universal Serial Bus
WEEE	Waste Electrical and Electronic Equipment
WP	Write-Protection

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa28 revision 02xx.

This User's Manual does not replace the Reference Manual of the CPU.

The TQMa28 is a universal Minimodule based on the Freescale ARM-CPU i.MX287.
The ARM926EJ-S core works with up to 454 MHz. The module extends the TQ-Systems GmbH product range and provides a well-balanced ratio between computing performance and graphics power.

The module provides the following key functions and characteristics:

- Freescale i.MX287 (ARM9 architecture), 454 MHz
- All functional CPU pins are routed to module connectors
- Up to 16 Gbyte eMMC NAND flash
- Up to 256 Mbyte DDR2 SDRAM
- 64 Kbit EEPROM
- Up to eight 12 bit A/D converter
- PWM
- Various serial interfaces depending on multiplexing (UART, SPI, I^2C, I^2S)
- 2 × CAN
- Temperature sensor
- 2 × USB 2.0 Hi-Speed Host interface with integrated PHY
- Industrial temperature range on request
- Low power consumption (0.11 to 2 W, depending on mode of operation)
- Dimensions: 40 × 26 mm^2
- Long term available
- Power supply: 5 V or Lithium-ion battery

3. TECHNICAL DATA

3.1 System architecture and functionality

3.1.1 TQMa28, block diagram

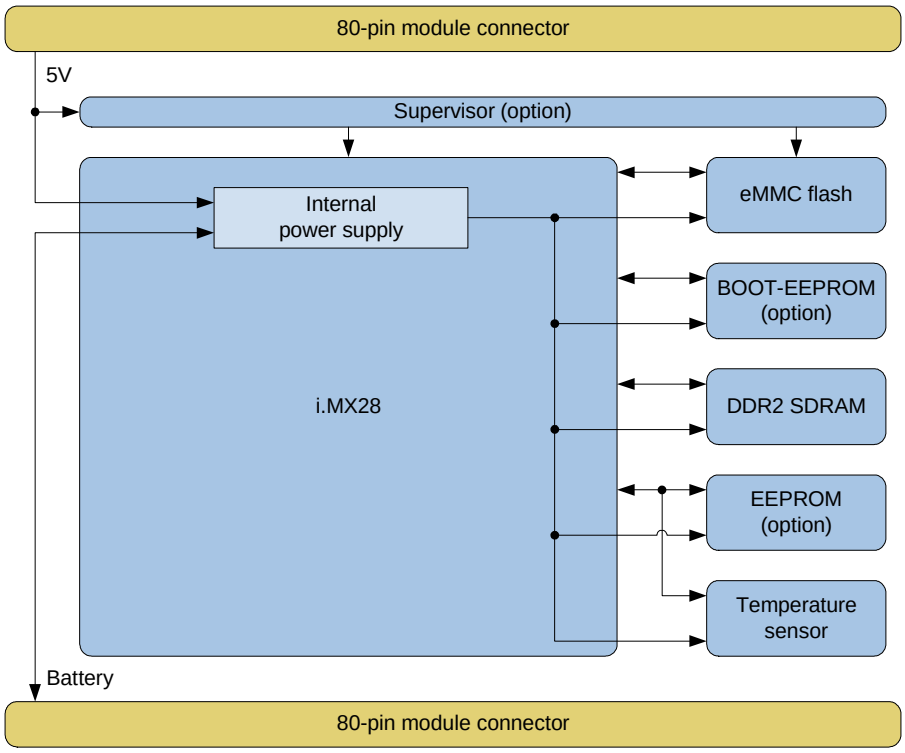


Illustration 1: TQMa28, block diagram

3.1.2 System functionality

The following elements are implemented on the TQMa28:

- i.MX287 CPU
- DDR2 SDRAM
- eMMC NAND flash
- EEPROM
- Temperature sensor
- 2 × 80-pin module connector

The following interfaces are available at the module plug connectors of the TQMa28:

- 1 × parallel display interface
- 1 × SD card
- 5 × UART
- 2 × CAN
- 2 × I^2C
- 1 × I2S
- 1 × SPI
- 2 × Ethernet
- 2 × USB 2.0 Hi-Speed
- JTAG
- ADCs
- PWMs
- GPIOs

4. ELECTRONICS SPECIFICATION

The information in this User's Manual is only valid for the combination of TQMa28 and the especially adapted boot loader, which is preinstalled on every TQMa28 (also see section (5).

4.1 Interfaces to other systems and devices

The TQMa28 is connected to the carrier board with 160 pins on two module connectors.

The module is held in the connectors with a considerable retention force.

To avoid damaging the modules' connectors as well as the carrier board connectors while removing the module the use of an extraction tool is strongly recommended.

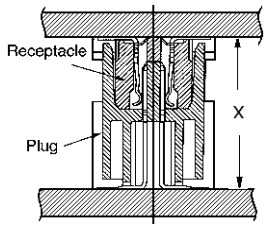
4.1.1 Module connectors

Table 3: TQMa28 module connector

Manufacturer	Order no.	Description
TE Connectivity	5177985-3	80-pin female connector, 0.8 mm pitch, vertical, –40 °C to +85 °C

In the following table applicable carrier board mating connectors are listed.

Table 4: Carrier board connectors

Manufacturer	Order no.	No. of pins	Plating	Stack height (X)	
TE Connectivity	5177984-3	80	0.2 µm Gold	5 mm	
TE Connectivity	5084614-3	80	0.76 µm Gold	5 mm	
TE Connectivity	5179029-3	80	0.2 µm Gold	6 mm	
TE Connectivity	5084615-3	80	0.76 µm Gold	6 mm	
TE Connectivity	5179030-3	80	0.2 µm Gold	7 mm	
TE Connectivity	1-5179030-3	80	0.76 µm Gold	7 mm	
TE Connectivity	5179031-3	80	0.2 µm Gold	8 mm	
TE Connectivity	6123002-3	80	0.76 µm Gold	8 mm	

The board to board distance results from the height of the TQMa28 connector and the connector on the carrier board. The drawings of the TQMa28 can be found in section 6.

When using the processor signals the multiple pin configurations by different processor-internal function units must be taken note of.

The pins of the module connectors are described in detail in the following tables.

In addition to direction, pin name and pin number, external and internal pull-up or-down wirings as well as the references to I/O voltage and processor pin characteristics are listed.

4.1.1.1 Module connector X1

Table 5: Pin assignment module connector X1

PU/PD	I/O	Level	Usage	i.MX28 pin	Name	Pin		Pin	Name	i.MX28 pin	Usage	Level	I/O	PU/PD
		0 V	POWER		GND	1		2	GND		POWER	0 V		
	O	3V3	LCD	N1	LCD_DOTCLK	3		4	LCD_VSYNC	L1	LCD	3V3	O	
		0 V	POWER		GND	5		6	LCD_HSYNC	M1	LCD	3V3	O	
	O	3V3	LCD	K1	LCD_WR_RW#	7		8	GND		POWER	0 V		
	O	3V3	LCD	M6	LCD_RESET	9		10	LCD_RS	M4	LCD	3V3	O	
	O	3V3	LCD	P4	LCD_RD_E	11		12	LCD_ENABLE	N5	LCD	3V3	O	
	O	3V3	LCD	P5	LCD_CS#	13		14	LCD_D00	K2	LCD	3V3	O	10 kΩ ↑
10 kΩ ↓	O	3V3	LCD	K3	LCD_D01	15		16	LCD_D02	L2	LCD	3V3	O	10 kΩ ↓
10 kΩ ↑	O	3V3	LCD	L3	LCD_D03	17		18	LCD_D04	M2	LCD	3V3	O	10 kΩ[1]
	O	3V3	LCD	M3	LCD_D05	19		20	LCD_D06	N2	LCD	3V3	O	
	O	3V3	LCD	P1	LCD_D07	21		22	LCD_D08	P2	LCD	3V3	O	
	O	3V3	LCD	P3	LCD_D09	23		24	LCD_D10	R1	LCD	3V3	O	
	O	3V3	LCD	R2	LCD_D11	25		26	LCD_D12	T1	LCD	3V3	O	
	O	3V3	LCD	T2	LCD_D13	27		28	LCD_D14	U2	LCD	3V3	O	
	O	3V3	LCD	U3	LCD_D15	29		30	LCD_D16	T3	LCD	3V3	O	
	O	3V3	LCD	R3	LCD_D17	31		32	LCD_D18	U4	LCD	3V3	O	
	O	3V3	LCD	T4	LCD_D19	33		34	LCD_D20	R4	LCD	3V3	O	
	O	3V3	LCD	U5	LCD_D21	35		36	LCD_D22	T5	LCD	3V3	O	
	O	3V3	LCD	R5	LCD_D23	37		38	GPIO0_24	R6	GPIO	3V3	I/O	
		5 V	POWER		VCC5V	39		40	GPIO0_6	U6	GPIO	3V3	I/O	
		5 V	POWER		VCC5V	41		42	GPIO0_27	P7	GPIO	3V3	I/O	
		0 V	POWER		GND	43		44	GPIO0_4	T7	GPIO	3V3	I/O	
		0 V	POWER		GND	45		46	GPIO3_6	K5	GPIO	3V3	I/O	
	I/O	3V3	GPIO	N9	GPIO0_17	47		48	GPIO0_26	P6	GPIO	3V3	I/O	
	I/O	3V3	SD_CARD	U8	SD_D0	49		50	GPIO0_7	T6	GPIO	3V3	I/O	
	I/O	3V3	SD_CARD	R8	SD_D2	51		52	GPIO0_16	N7	GPIO	3V3	I/O	
	I/O	3V3	SD_CARD	N8	SD_CMD	53		54	GPIO0_5	R7	GPIO	3V3	I/O	
	I	3v3	SD_CARD	L9	SD_WP	55		56	SD_D1	T8	SD_CARD	3V3	I/O	
	O	3V3	SD_CARD	P8	SD_CLK	57		58	SD_D3	U7	SD_CARD	3V3	I/O	
	I	3V3	UART1	L4	AUART1_RX	59		60	SD_DETECT#	N6	SD_CARD	3V3	I	
	I	3V3	UART3	M5	AUART3_RX	61		62	AUART1_TX	K4	UART1	3V3	O	
	O	3V3	UART3	K6	AUART3_RTS#	63		64	AUART3_TX	L5	UART3	3V3	O	
	I	3V3	CAN1	M9	CAN1_RX	65		66	AUART3_CTS#	L6	UART3	3V3	I	
	O	3V3	CAN1	M7	CAN1_TX	67		68	PWM4	E10	PWM	3V3	O	
	O	3V3	LCD/PWM	K8	LCD_BL_PWM	69		70	PWM3[2]	E9	PWM	3V3	O	
	O	3V3	DUART	L7	DUART_TX	71		72	DUART_RX	K7	DUART	3V3	I	10 kΩ ↑
4.7 kΩ ↑	I/O	3V3	I2C1	H7	I2C1_SDA	73		74	I2C1_SCL	H6	I2C1	3V3	I/O	4.7 kΩ ↑
	I	3V3	UART0	G5	AUART0_RX	75		76	AUART0_TX	H5	UART0	3V3	O	
	O	3V3	UART0	J7	AUART0_RTS#	77		78	AUART0_CTS#	J6	UART0	3V3	I	
		0 V	POWER		GND	79		80	GND		POWER	0 V		

1 Pull-Up or Pull-Down depends on module version. See section 4.2.1.2.

2 Controlled by ROM code pin PWM3 has the function POWER_GATE_GPIO-SD/MMC (output, low) during the boot process. Further information is to be taken from the Reference Manual (1).

4.1.1.2 Module connector X2

Table 6: Pin assignment module connector X2

PU/PD	I/O	Level	Usage	i.MX28 pin	Name	Pin		Pin	Name	i.MX28 pin	Usage	Level	I/O	PU/PD
		0 V	POWER		GND	1		2	GND		POWER	0 V		
	O	3V3	1588	B1	1588_Event2_out	3		4	1588_Event2_in	C1	1588	3V3	I	
	O	3V3	1588	D1	1588_Event3_out	5		6	1588_Event3_in	E1	1588	3V3	I	
	I	3V3	UART	C2	AUART4_RX	7		8	AUART4_TX	A2	UART	3V3	O	
	O	3V3	UART	B2	AUART4_RTS#	9		10	AUART4_CTS#	D2	UART	3V3	I	
	O	3V3	SPI	A3	SSP2_SCK	11		12	SSP2_MISO	B3	SPI	3V3	I	
	O	3V3	SPI	C3	SSP2_MOSI	13		14	SSP2_SS0#	C4	SPI	3V3	O	
	O	3V3	ENET	F3	ENET_RESET#	15		16	DEBUG / (VCC3V3_REF)	B9	CONFIG	3V3	I	10 kΩ ↑
		0 V	POWER		GND	17		18	GND		POWER	0 V		
	O	3V3	ENET	G4	ENET_MDC	19		20	ENET_CLK	E2	ENET	3V3	O	
	I/O	3V3	ENET	H4	ENET_MDIO	21		22	ENET_INT#	E3	ENET	3v3	I	
	I	3V3	ENET0	H1	ENET0_RXD0	23		24	ENET0_TXD0	F1	ENET0	3v3	O	
	I	3V3	ENET0	H2	ENET0_RXD1	25		26	ENET0_TXD1	F2	ENET0	3v3	O	
	I	3V3	ENET0	E4	ENET0_RX_EN	27		28	ENET0_TX_EN	F4	ENET0	3V3	O	
	I	3V3	ENET1	J3	ENET1_RX_EN	29		30	ENET1_TX_EN	J4	ENET1	3V3	O	
	I	3V3	ENET1	J1	ENET1_RXD0	31		32	ENET1_TXD0	G1	ENET1	3V3	O	
	I	3V3	ENET1	J2	ENET1_RXD1	33		34	ENET1_TXD1	G2	ENET1	3V3	O	
		0 V	POWER		GND	35		36	GND		POWER	0 V		
	O	3V3	USB1	F6	USB_1_PWR_EN	37		38	USB_1_DM	B8	USB1	5 V	I/O	
	I	3V3	USB1	D3	USB_1_OC#	39		40	USB_1_DP	A8	USB1	5 V	I/O	
	O	3V3	USB0	F5	USB_0_PWR_EN	41		42	USB_0_DM	A10	USB0	5 V	I/O	
	I	3V3	USB0	D4	USB_0_OC#	43		44	USB_0_DP	B10	USB0	5 V	I/O	
		0 V	POWER		GND	45		46	GND		POWER	0 V		
	I	3V3	USB0	J5	USB_0_ID	47		48	CAN0_RX	L8	CAN0	3V3	I	
	I	3V3	CONFIG	A11	PSWITCH	49		50	CAN0_TX	M8	CAN0	3V3	O	
4.7 kΩ ↑	I/O	3V3	I2C0	C7	I2C0_SCL	51		52	I2C0_SDA	D8	I2C0	3V3	I/O	4.7 kΩ ↑
	O	3V3	SPDIF	D7	SPDIF	53		54	GPIO2_9	D10	GPIO	3V3	I/O	
	O	3V3	I2S/AUDIO	E7	SAIF0_SDATA0	55		56	SAIF1_SDATA0	E8	I2S/AUDIO	3V3	I	
	I/O	3V3	I2S/AUDIO	F7	SAIF0_BITCLK	57		58	SAIF0_LRCLK	G6	I2S/AUDIO	3V3	I/O	
	O	3V3	I2S/AUDIO	G7	SAIF0_MCLK	59		60	RESET#	A14	CONFIG	3V3	I	10 kΩ ↑
		0 V	POWER		GND	61		62	GND		POWER	0 V		
	I	[3]	Touch/ADC	C14	LRADC6	63		64	HSADC0	B14	ADC	[3]	I	
	I	[3]	Touch/ADC	D13	LRADC4	65		66	LRADC5	D15	Touch/ADC	[3]	I	
	I	[3]	Touch/ADC	C8	LRADC2	67		68	LRADC3	D9	Touch/ADC	[3]	I	
	I	[3]	ADC	C15	LRADC0	69		70	LRADC1	C9	ADC	[3]	I	
10 kΩ ↑	I	3V3	JTAG	D12	JTAG_TMS	71		72	JTAG_TCK	E11	JTAG	3V3	I	10 kΩ ↑
10 kΩ ↑	I	3V3	JTAG	E12	JTAG_TDI	73		74	JTAG_TRST#	D14	JTAG	3V3	I	10 kΩ ↑
		4V2	POWER	A15	Battery	75		76	JTAG_RTCK	E14	JTAG	3V3	O	10 kΩ ↑
		4V2	POWER	A15	Battery	77		78	JTAG_TDO	E13	JTAG	3V3	O	
		0 V	POWER		GND	79		80	GND		POWER	0 V		

3 See Freescale datasheet (2).

4.2 System components

4.2.1 Processor

The Freescale processor i.MX28 (MCIMX287CVM4B) based on an ARM926EJ-S™ core is produced in 90 nm technology.
It provides a wide range of functions. Illustration 2 gives an overview.
More information about the i.MX28 processor is provided in the following table.

Table 7: Processor information

Manufacturer	Part number	Temperature range	Package	Silicon revision
Freescale	MCIMX287CVM4B	–40 °C to +85 °C	BGA 289	1.2

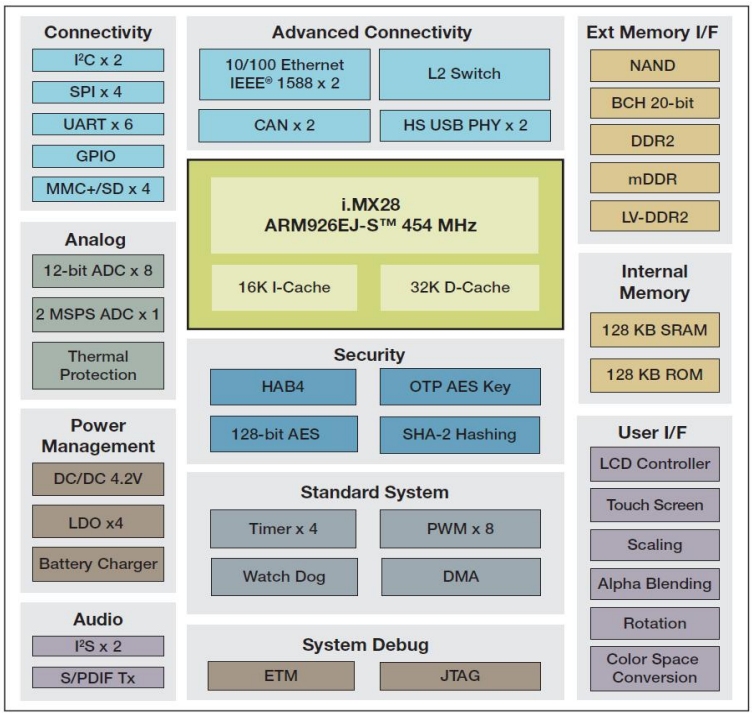


Illustration 2: i.MX28, block diagram
(Source: Freescale)

Other functionality of the processor shown in the block diagram can be looked up in the Freescale Reference Manual (1).
All essential pins of the processor, except the DDR2 SDRAM interface and the eMMC, are routed to the module connectors.

4.2.1.1 Boot modes

The i.MX28 has of a ROM with integrated boot code. When the i.MX28 starts this boot code initializes the hardware and then loads the program image from the selected boot device.

Instead of booting from the integrated eMMC it is also possible to boot from one of the following interfaces:

- USB
- I^2C
- SPI
- SSP
- GPMI

The boot device and its configuration can be defined with several boot mode registers.
For this the i.MX28 offers two possibilities:

- The settings are read from boot mode pins
- The settings are read from internal burnt OTP eFuses

The exact behaviour during the boot process depends on the value of eFuse ENABLE_PIN_BOOT_CHECK and the signal LCD_RS.
The following table shows the possible combinations.

Table 8: Boot configuration

eFuse: ENABLE_PIN_BOOT_CHECK	Pin: LCD_RS	TQMa28 pin	Boot mode	Default
0	**X**	X1_10	**Boot configuration via boot mode pins**	**X**
1	0		Boot configuration via OTP eFuses	–
	1		Boot configuration via boot mode pins	–

4.2.1.2 Boot devices

On account of the Freescale CPU erratum TKT131240 two different boot modes are possible.

This erratum describes an error in the ROM code the CPU which leads to an inverted clock polarity when the boot mode is set to booting from SSP0 (SD card) or SSP1 (eMMC) (see also (3)). This may cause boot errors.

As a workaround the boot device has to be an EEPROM which has to be connected to I2C0 or SPI3. The EEPROM has to contain a binary patch from Freescale, which corrects the clock polarity for one interface (SSP0 or SSP1).

To fix this erratum an optional EEPROM, which is connected to I2C0, is provided on the TQMa28. It corrects the polarity error at SSP0, to enable an error-free boot process from eMMC. Existing designs must be checked whether this option can be used, as address conflicts may appear, or a different multiplexing function than I2C0 was selected.

Optionally an EEPROM can be connected to I2C0 or SPI3 on the carrier board to fix this erratum.

This results in different wirings of the boot mode pins for the TQMa28, which are shown in the following sections:

4.2.1.2.1 TQMa28 with EEPROM at I2C0

The EEPROM with boot patch is preset as the standard boot device (I2C0 MASTER 3V3).
Therefore the boot mode pins on the TQMa28 are connected as follows:

Table 9: Configuration boot mode pins EEPROM

i.MX28 Ball	Pin name	Boot mode name	TQMa28	TQMa28 pin	Boot mode
K2	LCD_D00	BM0	10 kΩ Pull-Up	X1_14	1
K3	LCD_D01	BM1	10 kΩ Pull-Down	X1_15	0
L2	LCD_D02	BM2	10 kΩ Pull-Down	X1_16	0
L3	LCD_D03	BM3	10 kΩ Pull-Down	X1_17	0
M2	LCD_D04	VOLTAGE SELECT	10 kΩ Pull-Down	X1_18	0

4.2.1.2.2 TQMa28 without EEPROM at I2C0

The eMMC is preset as the standard boot device (SD/MMC MASTER ON SSP0 3V3).
Therefore the boot mode pins on the TQMa28 are connected as follows:

Table 10: Configuration boot mode pins eMMC

i.MX28 Ball	Pin name	Boot mode name	TQMa28	TQMa28 pin	Boot mode
K2	LCD_D00	BM0	10 kΩ Pull-Up	X1_14	1
K3	LCD_D01	BM1	10 kΩ Pull-Down	X1_15	0
L2	LCD_D02	BM2	10 kΩ Pull-Down	X1_16	0
L3	LCD_D03	BM3	10 kΩ Pull-Up	X1_17	1
M2	LCD_D04	VOLTAGE SELECT	10 kΩ Pull-Down	X1_18	0

4.2.1.2.3 Other boot modes

To boot from another source rather than the module-internal eMMC, or to use the function ENABLE_PIN_BOOT_CHECK, the default boot mode settings can be changed by resistors of about 1 kΩ at the pins LCD_D[4:0] or LCD_RS.
The necessary settings for other boot device are to be taken from the Freescale Reference Manual (1).

4.2.1.3 Processor clock supply

A crystal oscillator on the TQMa28 supplies the processor with 24 MHz.
A 32.768 kHz crystal oscillator on the TQMa28 supplies the RTC domain with a clock signal.

4.2.1.4 Pin multiplexing

Depending on the configuration, the pin multiplexing enables different pins to have different functions. Freescale provides on their website the program “IOMUXCC”, which supports the selection of the desired options.
The information in this manual corresponds to the signals used on the Starter Kit STK-MBa28 and their support in the BSP.
TQ-Systems GmbH provides an xml file created with the program "IOMUXCC", which shows the pin-multiplexing of the TQMa28. The user can configure specific pin-multiplexing based on this xml file. The xml file can be obtained from TQ-Systems Support.
The accuracy of the generated configuration cannot be guaranteed!
It is the user's responsibility to conscientiously check the generated configuration.

Attention: Destruction or malfunction!	
	Many of the CPU pins can be used in several different ways. Please, notice the notes about the wiring of these pins in the i.MX28 Reference Manual (1) before integration / start-up of your carrier board / Starterkit.

4.2.1.5 CPU errata

Attention: Malfunction!	
	Please pay attention to the latest errata of the Freescale CPU (3).

4.2.2 Memory

4.2.2.1 DDR2 SDRAM

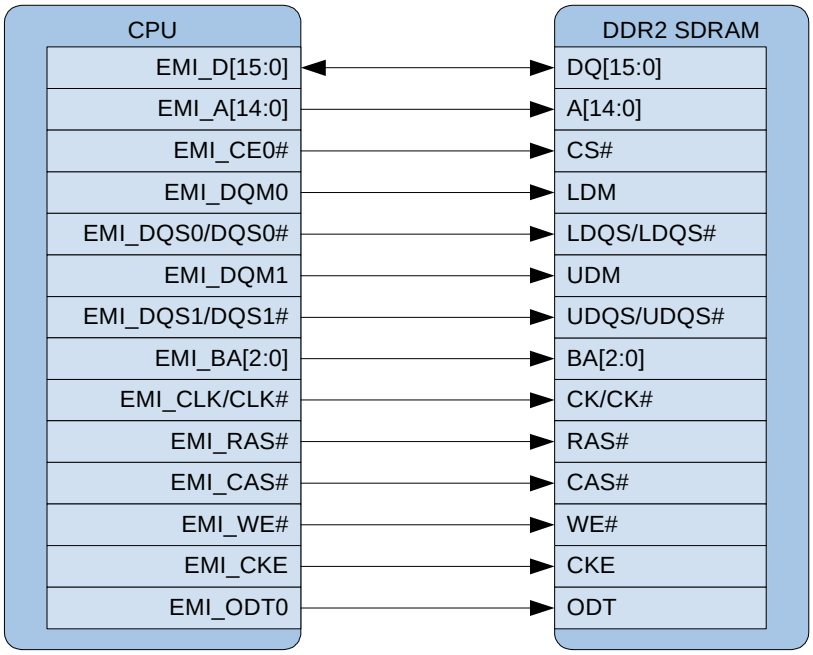


Illustration 3: Interface to DDR2 SDRAM

The following table gives an overview of the possible alternatives.

Table 11: Memory models DDR2 SDRAM

Manufacturer	Manufacturer's number	Type	Capacity	Temp. Range	Remark
Micron	MT47H64M16HR-3IT:H	64M16	128 Mbyte	–40 to +85 °C	–
Micron	**MT47H64M16HR-25EIT:H**	**64M16**	**128 Mbyte**	**–40 to +85 °C**	**Default**
Micron	MT47H128M16RT-25EIT	128M16	256 Mbyte	–40 to +85 °C	–

The memory allocates the following address range:

Table 12: Address configuration DDR2 SDRAM

Start address	Size	Chip Select	Capacity
0x4000_000	0x0800_000	CE0#	128 Mbyte
0x4000_000	0x1000_000	CE0#	256 Mbyte

4.2.2.2 eMMC

The TQMa28 is equipped with an eMMC flash to store programs and data (boot loader and operating system). It is controlled via the SD card controller SSP0 of the i.MX28.

The following illustration shows how the eMMC is connected to the processor.

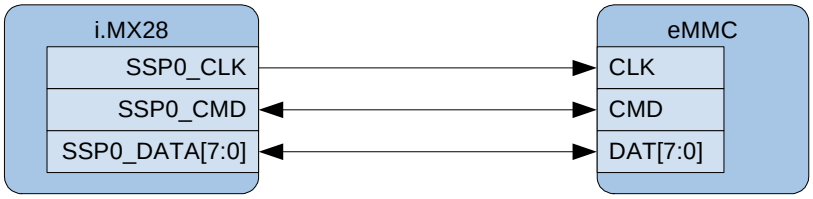


Illustration 4: Interface to eMMC

4.2.2.3 EEPROM

For permanent storage of e.g. module characteristics or customers parameters a serial 64 kbit EEPROM is provided.
The EEPROM is controlled via I^2C bus 1 of the processor.
Detailed information concerning the I^2C-address configuration can be found in section 4.2.8.1.
The writing protection (WP) of the EEPROM is not available.

Table 13: Memory model EEPROM

Manufacturer	Manufacturer's number	Size
ST Microelectronics	M24C64-WDW6TP	64 kbit

In the EEPROM module-specific data is stored. It is, however, not essential for the correct operation of the TQMa28.
The data can be deleted or altered by the user.

In the following table the parameters stored in the EEPROM are shown.

Table 14: EEPROM module specific data

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
0x00	Variable	Variable	32_{10}	Binary	Hard Reset Configuration Word (HRCW), (optional)
0x20	6_{10}	10_{10}	16_{10}	Binary	MAC address
0x30	8_{10}	8_{10}	16_{10}	ASCII	Serial number
0x40	Variable	Variable	64_{10}	ASCII	Module name

4.2.3 RTC

The TQMa28 provides a processor internal RTC. The current consumption of the RTC is approximately 30 µA.
A 32.768 kHz crystal oscillator clocks the RTC.

In the following table the parameters of the crystal oscillator are shown.

Table 15: Parameters of 32.768 kHz crystal oscillator

Parameter	Value	Unit	Remark
Frequency tolerance	±20	ppm	@ 25 °C
Frequency ageing	±3 max.	ppm	First year, @ 25 °C
Parabolic Coefficient	-0.04×10^{-6}	$°C^2$	Additional deviation at temp ≠ 25 °C

When the power supply is switched off the CPU internal RTC has to be buffered by a lithium-ion battery to maintain its function.
As the RTC in the CPU is supplied by the same power plane than the CPU in normal operation the whole system supplies itself from this power plane. For this reason the RTC cannot be buffered with a normal button cell. If the characteristics of the internal RTC are not suitable, the DS1339 is proposed as an external RTC on the carrier board.

4.2.4 Temperature sensor

A National Semiconductor LM73 temperature sensor is provided. The sensor is placed on the topside of the module (see D6 in Illustration 10). The interface of the sensor is shown in section 4.2.8.1.

4.2.5 Graphics interfaces / LCD bus

Parallel displays with a maximum frame size of up to 800 × 480 pixels can be connected to the TQMa28.
The parallel data interface can be up to 24 bits wide. The LCD bus is directly routed to the module connector.

Table 16: Display signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
LCD_D[23:0]	LCD_D[23:0]	X1_[37:14]	O	LCD-Interface RGB-Data
LCD_HSYNC	LCD_HSYNC	X1_06	O	LCD-Interface Horizontal Sync
LCD_VSYNC	LCD_VSYNC	X1_04	O	LCD-Interface Vertical Sync
LCD_ENABLE	LCD_ENABLE	X1_12	O	LCD-Interface Enable
LCD_DOTCLK	LCD_DOTCLK	X1_03	O	LCD-Interface Dotclock
LCD_CS	LCD_CS#	X1_13	O	LCD-Interface Chip Select
LCD_RS	LCD_RS	X1_10	O	LCD-Interface Register Select
LCD_WR_RWN	LCD_WR_RW#	X1_07	O	LCD-Interface 6800 R/W# / 8080 W
LCD_RD_E	LCD_RD_E	X1_11	O	LCD-Interface 6800 Enable / 8080 RD
LCD_RESET	LCD_RESET	X1_09	O	LCD-Interface Reset Out

4.2.6 Ethernet

The i.MX28 provides two built-in Fast Ethernet controllers, which are designed for 10 and 100 Mbps.
Both provided RMII interfaces are available to the user directly at the module connectors.
The Ethernet interface is completed by a PHY on the carrier board.

Table 17: Ethernet signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
ENET0_MDIO	ENET_MDIO	X2_21	I/O	Ethernet Management Data
ENET0_MDC	ENET_MDC	X2_19	O	Ethernet Output Management Data Clock
ENET[0:1]_TXD[0:1]	ENET[0:1]_TXD[0:1]	X2_[24:26_32:34]	O	Ethernet Output Transmit Data
ENET[0:1]_TX_EN	ENET[0:1]_TX_EN	X2_[30_28]	O	Ethernet Output Transmit Enable
ENET[0:1]_RXD[0:1]	ENET[0:1]_RXD[0:1]	X2_[23:25_31:33]	I	Ethernet Input Receive Data
ENET[0:1]_RX_EN	ENET[0:1]_RX_EN	X2_[29_27]	I	Ethernet Data Valid / Carrier Sense
ENET_CLK	ENET_CLK	X2_20	I/O	Reference Clock
GPIO4_5	ENET_INT#	X2_22	I	Ethernet Input Interrupt (GPIO)
GPIO4_13	ENET_RESET#	X2_15	O	Ethernet Output Reset (GPIO)

The processor-internal clock generator of the i.MX28 does not meet the clock jitter values required by most Ethernet PHYs. This may cause Ethernet connection problems during link-up.

It is recommended to provide an external clock generator with suitable precision on the carrier board to generate the clock signal for the input ENET_CLK. This can be achieved by using a quartz crystal or a crystal oscillator.

The CPU supplies additional functions according to IEEE® 1588.

The following signals are available at the module connectors:

Table 18: IEEE1588 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
ENET0_1588_EVENT2_OUT	1588_EVENT2_OUT	X2_03	O	–
ENET0_1588_EVENT2_IN	1588_EVENT2_IN	X2_04	I	–
ENET0_1588_EVENT3_OUT	1588_EVENT3_OUT	X2_05	O	–
ENET0_1588_EVENT3_IN	1588_EVENT3_IN	X2_06	I	–

By turning off pre-set functions and switching on 1588-features, more 1588_Events can be provided.

4.2.7 SD card

The TQMa28 provides an SD card controller (SSP1), whose signals are available at the module connector X1.
The following table shows the signals used for the SD card interface.

Table 19: SD card interface signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
SSP1_SCK	SD_CLK	X1_57	O	SD Card Output Clock
SSP1_CMD	SD_CMD	X1_53	I/O	SD Card Command
SSP1_D[3:0]	SD_D[3:0]	X1_58_51_56_49	I/O	SD Card Data
SSP1_CARD_DETECT	SD_DETECT#	X1_60	I	SD Card Input Card-Detect
GPIO0_28	SD_WP	X1_55	I	SD Card Input Write-Protection

4.2.8 Serial interfaces

The supported standards, transmission modes and transfer rates of the following interfaces are to be taken from the Freescale Reference Manual (1).

4.2.8.1 I²C

The i.MX28 provides two I2C interfaces. Both interfaces are routed to the connectors.
The following table shows the signals used for the I2C interfaces.

Table 20: I2C signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
I2C0_SDA	I2C0_SDA	X2_52	I/O	Pull-Up 4.7 kΩ to 3.3 V on TQMa28
I2C0_SCL	I2C0_SCL	X2_51	O	Pull-Up 4.7 kΩ to 3.3 V on TQMa28
I2C1_SDA	I2C1_SDA	X1_73	I/O	Pull-Up 4.7 kΩ to 3.3 V on TQMa28
I2C1_SCL	I2C1_SCL	X1_74	O	Pull-Up 4.7 kΩ to 3.3 V on TQMa28

The following illustration shows the I²C signals used and how they are connected to the temperature sensor and the EEPROMs.

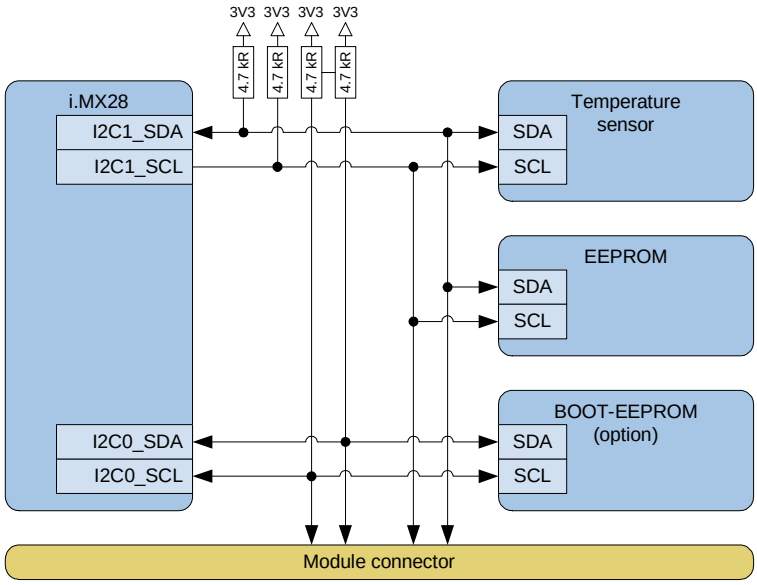


Illustration 5: Interface of the I²C buses

The following table shows the address of the I²C bus 0 used on the TQMa28 in case the version with boot EEPROM was chosen:

Table 21: I2C0 address configuration

Component	Address	
EEPROM	0x50	0b1010000

There are two devices with an I²C interface on the module. Both devices are connected to I²C bus 1:

Table 22: I2C1 address configuration

Component	Address	
Temperature sensor	0x49	0b1001001
EEPROM	0x50	0b1010000

Attention: pull-up resistors	
	Pull-up resistors for the I²C buses are already assembled on the module. If more devices are connected on the carrier board the maximum capacitive bus load according to the I²C standard has to be observed. If necessary additional pull-ups have to be assembled on the carrier board.

4.2.8.2 I2S

To connect an audio-codec via I2S the signals of the Serial Audio Interface (SAIF) are routed to the module plug connectors.
The following table shows the signals used for the SAIF interface.

Table 23: I2S signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
SAIF0_MCLK	SAIF0_MCLK	X2_59	O	System Master Clock
SAIF0_LRCLK	SAIF0_LRCLK	X2_58	I/O	I2S Frame Clock
SAIF0_BITCLK	SAIF0_BITCLK	X2_57	I/O	I2S Bit Clock
SAIF0_SDATA0	SAIF0_SDATA0	X2_55	I	I2S Data Input
SAIF1_SDATA0	SAIF1_SDATA0	X2_56	O	I2S Data Output

The SAIF allows to connect 3, 4 or 5-wire interface, e.g., via I2S. Details are to be taken from the Freescale Reference Manual (1).

4.2.8.3 SPDIF

The i.MX28 provides an SPDIF interface with transmit functionality.
The following table shows the signals used for the SPDIF interface.

Table 24: SPDIF signal

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
SPDIF	SPDIF	X2_53	O	–

4.2.8.4 SPI

The SPI interface of the i.MX28 is named SSP. The SSP2 interface signals are available at the connectors.
In addition to SPI on SSP2, a further SPI interface can be multiplexed on SSP3 as an alternative to AUART4.

Table 25: SPI signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
SSP2_SCK	SSP2_SCK	X2_11	O	–
SSP2_MOSI	SSP2_MOSI	X2_13	O	–
SSP2_MISO	SSP2_MISO	X2_12	I	–
SSP2_SS0	SSP2_SS0#	X2_14	O	–

4.2.8.5 UART

The i.MX28 provides five Application UART interfaces (AUART) and one debug UART (DUART).
AUART0, AUART1, AUART3, AUART4 and DUART signals are available at the module plug connectors.

The following table shows the signals used for the AUART0 interface.

Table 26: AUART0 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
AUART0_TX	AUART0_TX	X1_76	O	–
AUART0_RX	AUART0_RX	X1_75	I	–
AUART0_RTS	AUART0_RTS#	X1_77	O	–
AUART0_CTS	AUART0_CTS#	X1_78	I	–

The following table shows the signals used for the AUART1 interface.

Table 27: AUART1 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
AUART1_TX	AUART1_TX	X1_62	O	–
AUART1_RX	AUART1_RX	X1_59	I	–

The following table shows the signals used for the AUART3 interface.

Table 28: AUART3 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
AUART3_TX	AUART3_TX	X1_64	O	–
AUART3_RX	AUART3_RX	X1_61	I	–
AUART3_RTS	AUART3_RTS#	X1_63	O	–
AUART3_CTS	AUART3_CTS#	X1_66	I	–

The following table shows the signals used for the AUART4 interface.

Table 29: AUART4 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
AUART4_TX	AUART4_TX	X2_08	O	–
AUART4_RX	AUART4_RX	X2_07	I	–
AUART4_RTS	AUART4_RTS#	X2_09	O	–
AUART4_CTS	AUART4_CTS#	X2_10	I	–

The following table shows the signals used for the DUART interface.

Table 30: DUART signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
DUART_TX	DUART_TX	X1_71	O	–
DUART_RX	DUART_RX	X1_72	I	Pull-Up 10 kΩ to 3.3 V on TQMa28

The UART signals are routed to the module connectors as LVTTL signals.
They may need driver's devices on the carrier board to be used as external signals.
In addition, filtering and EMC protection for the UART signals has to be provided on the carrier board.

4.2.8.6 USB

Two USB-High-Speed interfaces are available on the TQMa28. The first (USB0) is OTG capable. The second port exclusively provides a Hi-Speed host. For both ports the PHY is integrated in the i.MX28. The 5 V supply for the USB ports has to be implemented on the carrier board. In addition, filtering and EMC protection for the USB signals has to be provided on the carrier board. Notes are to be found in the USB standard.

The following table shows the signals used for the USB0 interface.

Table 31: USB0 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
USB0DM	USB_0_DM	X2_42	I/O	Negative Data Line
USB0DP	USB_0_DP	X2_44	I/O	Positive Data Line
USB0_ID	USB_0_ID	X2_47	I	Micro-A/-B Identification
GPIO3_9	USB_0_PWR_EN	X2_41	O	Enable Power Distributor (GPIO)
USB0_OVERCURRENT	USB_0_OC#	X2_43	I	Overcurrent Detection

The following table shows the signals used for the USB1 interface.

Table 32: USB1 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
USB1DM	USB_1_DM	X2_38	I/O	Negative Data Line
USB1DP	USB_1_DP	X2_40	I/O	Positive Data Line
GPIO3_8	USB_1_PWR_EN	X2_37	O	Enable Power Distributor (GPIO)
USB1_OVERCURRENT	USB_1_OC#	X2_39	I	Overcurrent Detection

4.2.8.7 CAN

The i.MX28 provides depending on the version one or two integrated CAN controllers.
All four signals are routed to the module connectors. The corresponding drivers have to be provided on the carrier board.
The following table shows the signals used for the CAN interfaces.

Table 33: CAN signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
CAN0_TX	CAN0_TX	X2_50	O	–
CAN0_RX	CAN0_RX	X2_48	I	–
CAN1_TX	CAN1_TX	X1_67	O	–
CAN1_RX	CAN1_RX	X1_65	I	–

4.2.9 PWM

Three of the eight PWM outputs of the i.MX28 are directly available at the module connectors.
More PWMs are available if the pin multiplexing is adapted.
The following table shows the available PWM signals.

Table 34: PWM signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
PWM2	LCD_BL_PWM	X1_69	O	–
PWM3	PWM3	X1_70	O	–
PWM4	PWM4	X1_68	O	–

4.2.10 GPIO

The i.MX28 processor provides GPIO ports as a second or multiple configuration with other function units.
The configuration can be taken from the Freescale Reference Manual (1).
Some of the GPIOs are directly named as GPIO and directly routed to the module connectors.
The following table shows the GPIO signals which can be used.

Table 35: GPIO signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
BANK0_PIN04	GPIO0_4	X1_44	I/O	–
BANK0_PIN05	GPIO0_5	X1_54	I/O	–
BANK0_PIN06	GPIO0_6	X1_40	I/O	–
BANK0_PIN07	GPIO0_7	X1_50	I/O	–
BANK0_PIN16	GPIO0_16	X1_52	I/O	–
BANK0_PIN17	GPIO0_17	X1_47	I/O	–
BANK0_PIN24	GPIO0_24	X1_38	I/O	–
BANK0_PIN26	GPIO0_26	X1_48	I/O	–
BANK0_PIN27	GPIO0_27	X1_42	I/O	–
BANK2_PIN09	GPIO2_9	X2_54	I/O	–
BANK3_PIN06	GPIO3_6	X1_46	I/O	–

4.2.11 JTAG

The i.MX28 provides two JTAG modes. The mode is defined with the signal DEBUG.
To change the JTAG mode, the default can be changed by a pull-down resistor of approximately 1 kΩ at the pin DEBUG.
The following table shows the available modes as well as the default mode used on the TQMa28.

Table 36: JTAG modes

Debug	Default	Name	TQMa28 pin	Remark
0		JTAG interface works for boundary scan	X2_16	–
1	**X**	**JTAG interface works for ARM debugging**		**Pull-Up 10 kΩ to 3.3 V on TQMa28**

The JTAG signals are directly routed from the CPU to the module connector. All necessary pull-up and pull-down resistors are already assembled on the TQMa28.
The following table shows the signals used for the JTAG interface.

Table 37: JTAG signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
JTAG_TCK	JTAG_TCK	X2_72	I	Pull-Up 10 kΩ to 3.3 V on TQMa28
JTAG_TMS	JTAG_TMS	X2_71	I	Pull-Up 10 kΩ to 3.3 V on TQMa28
JTAG_TDI	JTAG_TDI	X2_73	I	Pull-Up 10 kΩ to 3.3 V on TQMa28
JTAG_TDO	JTAG_TDO	X2_78	O	–
JTAG_TRST	JTAG_TRST#	X2_74	I	Pull-Up 10 kΩ to 3.3 V on TQMa28
JTAG_RTCK	JTAG_RTCK	X2_76	O	Pull-Up 10 kΩ to 3.3 V on TQMa28

4.2.12 ADC

The TQMa28 provides eight ADC inputs. All inputs are blocked to GND with 10 nF.
The ADC supports resistive 4- or 5-wire touch screens.
An adequate protection circuit has to be implemented on the carrier board.

Table 38: ADC signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	4-wire touch	5-wire touch	Remark
LRADC0	LRADC0	X2_69	AI			–
LRADC1	LRADC1	X2_70	AI			–
LRADC2	LRADC2	X2_67	AI	Touch Right / X+	UL	–
LRADC3	LRADC3	X2_68	AI	Touch Top / Y+	LL	–
LRADC4	LRADC4	X2_65	AI	Touch Left / X–	UR	–
LRADC5	LRADC5	X2_66	AI	Touch Bottom / Y–	LR	–
LRADC6	LRADC6	X2_63	AI		Common	–
HSADC0	HSADC0	X2_64	AI			High-Speed ADC (not qualified)

4.2.13 Reset

Two sources on the carrier board are possible for a system reset of the CPU:

- Power-on reset
- RESET# (e.g. reset push button)

The following table describes the Reset signal available at the module connector:

Table 39: RESET signal

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
RESETN	RESET#	X2_60	I	- Pull-Up 10 kΩ to 3.3 V on TQMa28 - Minimum required Low-Time: ≥100 ms

To improve the stability in case of voltage drops an optional supervisor is provided on the TQMa28.
The supervisor monitors the input voltage VCC5V. The output of the supervisor is connected to the reset input of the CPU.
The module version with supervisor can only be used with systems which are exclusively supplied with 5 V.
The following illustration shows how the supervisor is connected.

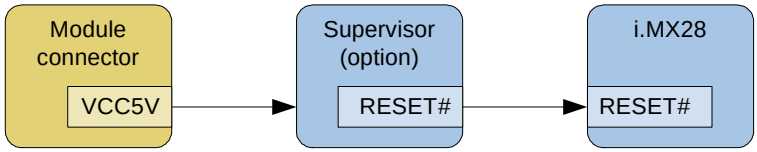


Illustration 6: Optional supervisor, block diagram

The supervisor has the following characteristics:

- Typical threshold voltage: 4.55 V
- Typical delay time: 200 ms

4.2.14 Power supply

4.2.14.1 Module supply

The TQMa28 works with a single supply of 5 V that must be provided by the carrier board.

Alternatively a lithium-ion battery can supply the TQMa28.

If a lithium-ion battery is connected at the BATTERY pin it is charged if the module is supplied with 5 V.
Software settings can be done in the registers HW_LRADC_CONVERSION and HW_POWER_CHARGE.

Attention: Lithium primary batteries and lithium-ion secondary batteries	
	Lithium primary batteries may not be used at the i.MX28 or TQMa28 (pin BATTERY) because of the charging function of the CPU!

The following table shows the permitted ranges of the supply voltages.

Table 40: Supply voltages

Parameter	Min.	Typ.	Max.	Unit
Supply voltage V_{IN} VCC5V	4.75	5.00	5.25	V
Supply voltage V_{IN} BATTERY	3.10	–	4.20	V

The calculated current consumption (worst case) is at most 0.4 A. The current consumption strongly depends on component placement, software and wiring options. The values given are to be seen as indicative values.

Table 41: Current consumption

Parameter	V_{IN}	I_{ITYP}
Current consumption in standby	3.3 V	10 mA
	5.0 V	20 mA
Current consumption in Linux idle mode	3.3 V	140 mA
	5.0 V	130 mA
Current consumption in Linux boot mode	3.3 V	230 mA
	5.0 V	240 mA
Current consumption of internal RTC only	>1.3 V	30 µA
Switch-on current[4]	5.25 V	1.77 A

4 Peak current for approximately 1.2 µs.

4.2.14.2 Power Management Unit

The i.MX28 has an integrated Power Management Unit (PMU). All voltages required on the TQMa28 are generated by the PMU. The following illustration shows the internal structure of the PMU.

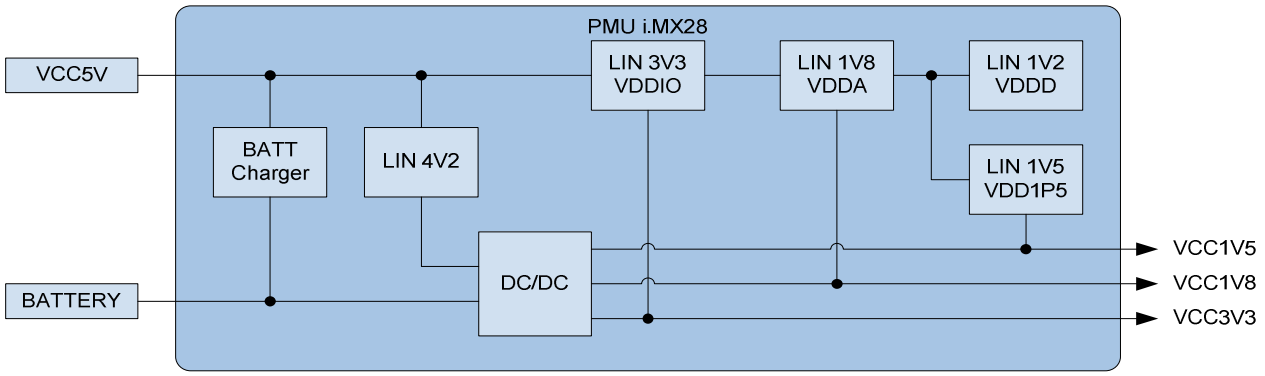


Illustration 7: PMU i.MX28, block diagram

The internal power supply consists of a chain of linear regulators a DC/DC converter and a battery charger.

If the TQMa28 is supplied via VCC5V the processor starts with the voltages generated by its internal linear regulators. During the boot process the linear regulator LIN 4V2 is switched on and supplies the DC/DC converter. From this point the DC/DC converter provides the necessary system voltages instead of the linear regulators. In BATTERY mode the DC/DC converter starts directly.

The i.MX28 provides an extensive set of registers to configure the PMU. Among other things the levels of the output voltages of all voltage regulators, the brown-out level, the start behaviour, the charging currents, the trigger levels, etc. can be configured.

The settings of these registers have to be checked or set for the respective design. Further information is to be taken from the Freescale Reference Manual (1), the i.MX28 data sheet (2) and the Application Note for the power management (4) of the i.MX28.

4.2.14.3 Power-up/down

The start behaviour of the TQMa28 depends on the selected voltage source (VCC5V or BATTERY).

- Module supply with VCC5V: Power-up sequence of the CPU starts immediately
- Module supply with BATTERY: Power-up sequence of the CPU only starts when the pin PSWITCH is supplied with a voltage between 0.65 V and 1.5 V.

The function of the pin PSWITCH depends on the applied voltage (see Freescale Reference Manual (1)).

In case the function "Fast Falling Edge" is not used (which could be used to power-down the CPU) it is recommended to disable this function using the circuitry suggested by Freescale (see Illustration 8).

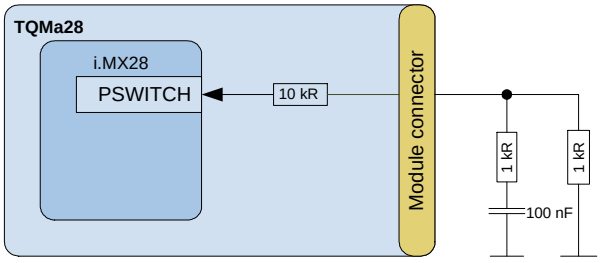


Illustration 8: Wiring of PSWITCH

Attention: Power-up sequence	
	To avoid across supply and errors in the power-up sequence, no I/O pins may be driven by external components during boot-time.

5. SOFTWARE SPECIFICATION

The TQMa28 comes with a preinstalled boot loader. The Boot loader and the also available BSP are tailored for the combination of TQMa28 and Starterkit STK-MBa28. More information can be found in the Support Wiki for the TQMa28.

The boot loader contains module specific as well as carrier-board adaptions as for example

- CPU/PMU configuration
- RAM configuration
- RAM timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strength

These settings have to be adapted if a different boot loader is used. More details can be requested from the TQ-Support.

6. MECHANICS SPECIFICATION

6.1 General information

Dimensions (L x W):	40 × 26 mm²
Maximum stack height:	Max. 1.5 mm (top side) / typ. 3.75 mm (bottom side)
Mounting holes:	None
Board to board distance:	Selectable by different mating plugs (standard: 5 mm), see also Table 4

The dimensions in the drawing are values without tolerances.

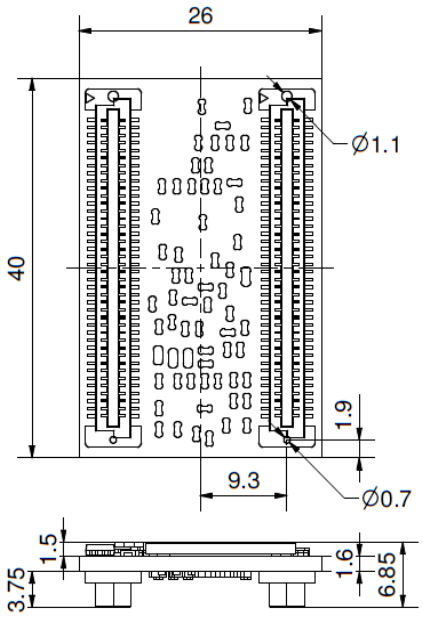


Illustration 9: Overall dimensions (bottom view, side view)

6.2 Notes of treatment

To avoid damages caused by mechanical stress, the TQMa28 may only be extracted from the carrier board by using the extraction tool MOZIa28. It can also be obtained separately.

Attention: Note with respect to the component placement of the carrier board	
	2.5 mm should be kept free on the carrier board, along the longitudinal edges on both sides of the module for the extraction tool MOZIa28.

6.3 Component placement

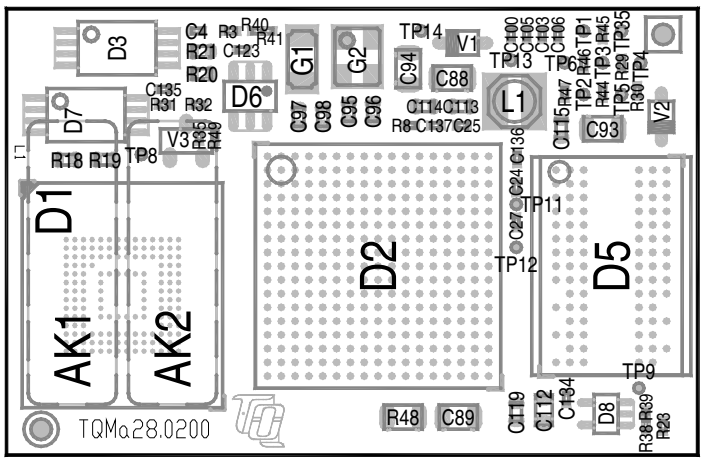


Illustration 10: Component placement top

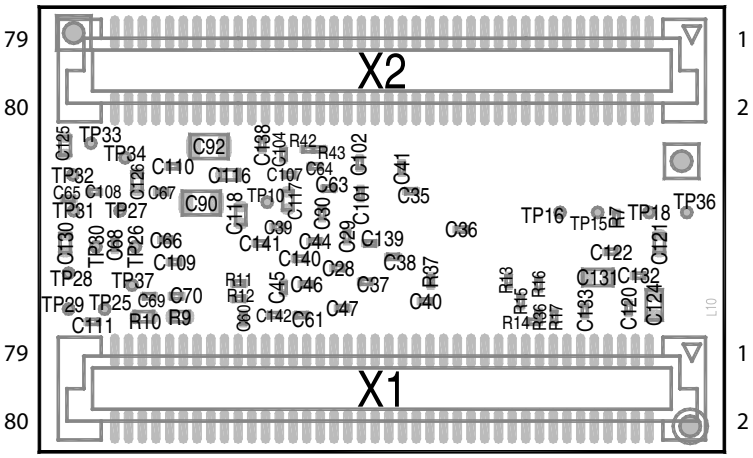


Illustration 11: Component placement bottom

6.4 Requirements for the superior system

6.4.1 Protection against external effects

As an embedded module it is not protected against dust, external impact and contact (IP00).
An adequate protection has to be guaranteed by the surrounding system.

6.4.2 Thermal management

Up to 2 W (worst case) have to be dissipated to cool the TQMa28. The power dissipation originates primarily in the processor and in the DDR2 SDRAM. The thermal resistance of the module is 20 K/W. The user is responsible for the removal of this power dissipation in his application. In most cases a passive cooling should be sufficient.

Attention: Destruction or malfunction!	
	The CPU belongs to a performance category with which in certain applications cooling can become necessary. It is the task of the user, to define a heat sink suitable for the specific case of operation (e.g., by clock frequency, stack height and airflow).

6.4.3 Structural requirements

The TQMa28 is held in the module socket by the retention force of the pins (a total of 160). For high requirements with respect to vibration and shock firmness an additional plastic module holder has to be provided in the final product to hold the module in its position. As no heavy and big components are used, no further requirements are given.

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The module was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short;
  avoid interference of other signals by distance and/or shielding besides,
  notice not only the frequency, but also the signal rise times
- Filtering of all signals which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

7.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system.
As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa28.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of the inputs
  (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, perhaps Zener diode(s)
- Fast signal lines: Integrated protective devices (suppressor diode arrays)

7.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety haven't been carried out.

7.4 Reliability and service life

No detailed MTBF calculation has been done for the TQMa28.

It was designed to be insensitive to vibration and impact.

Product life limiting components like electrolyte capacitors were not used.

Middle grade connectors, which guarantee at least 100 mating cycles, were used for the module.

7.5 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly. In general, a reliable operation is given when following conditions are met:

Table 42: Climate and operating conditions “Commercial temp. range” 0 °C to +70 °C

Parameter	Range	Remark
Die temperature CPU	–40 °C to +105 °C	Environment: –40 °C to +85 °C
Housing temperature DDR2 SDRAM	0 °C to +85 °C	–
Housing temperature other ICs	0 °C to +70 °C	–
Permitted storage temperature TQMa28	–40 °C to +85 °C	–
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

Table 43: Climate and operating conditions “Extended temp. range” –25 °C to +85 °C

Parameter	Range	Remark
Die temperature CPU	–40 °C to +105 °C	Environment: –40 °C to +85 °C
Housing temperature DDR2 SDRAM	–40 °C to +95 °C	–
Housing temperature other ICs	–25 °C to +85 °C	–
Permitted storage temperature TQMa28	–40 °C to +85 °C	–
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

Table 44: Climate and operating conditions “Industrial temp. range” –40 °C to +85 °C

Parameter	Range	Remark
Die temperature CPU	–40 °C to +105 °C	Environment: –40 °C to +85 °C
Housing temperature DDR2 SDRAM	–40 °C to +95 °C	Environment: –40 °C to +85 °C
Housing temperature other ICs	–40 °C to +85 °C	–
Permitted storage temperature TQMa28	–40 °C to +85 °C	–
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

7.6 Environment protection

7.6.1 RoHS compliance

The TQMa28 is manufactured RoHS compliant.

- All components used and assemblies are RoHS compliant
- RoHS compliant soldering processes are used

7.6.2 WEEE regulation

The company placing the product on the market is responsible for the observance of the WEEE regulation.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

7.6.3 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.

8. APPENDIX

8.1 References

Table 45: Further applicable documents

No.	Description	Rev. / Date	Company
(1)	i.MX28 Applications Processor Reference Manual	Rev. 2, 08/2013	Freescale
(2)	Datasheet i.MX28 Applications Processors for Consumer Products	Rev. 3, 07/2012	Freescale
(3)	Chip Errata for the i.MX28	Rev. 2, 09/2012	Freescale
(4)	Application Note AN4199	Rev. 1, 03/2013	Freescale
(5)	TQMa28.IOMuxDesign_2.0.27	Rev. 0102	TQ-Systems
(6)	TQMa28-MBa28 Tech Note	Rev. 0101	TQ-Systems

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