



## **ETX<sup>®</sup> conga-EAF**

***AMD<sup>®</sup> Embedded G-Series processors and AMD A55E  
controller hub***

***User's Guide***

***Revision 1.4***

## Revision History

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Revision	Date (yyyy.mm.dd)	Author	Changes
1.0	2011.07.29	GDA	Official release
1.1	2011.08.09	GDA	Corrected TDP values for AMD G-T40E 1.0 GHz Dual Core and AMD G-T40R 1.0 GHz Single Core in the conga-EAF Options Information table on page 8. Corrected "100% workload" value in section 1.5.6, should be 10.0 W, not 5.0 W.
1.2	2011.10.18	GDA	Removed information from section 6.3 about limiting the maximum processor frequency via BIOS setup node, this feature is not available. Added note throughout about Native and Compatible IDE support. Added ISA limitations to section 4.2. Added information about Native and Compatible option in section 6. Updated BIOS section.
1.3	2012.07.13	GDA	Added maximum memory speed to Options Information table and Feature List table 1. Added section 6.8 "HDMI/DisplayPort (DP) Audio Support." Updated section 9 "BIOS Setup Description."
1.4	2013.06.14	AEM	Changed maximum torque rating for heatspreader screws in section 3.1 "Heatspreader Dimensions" and added a caution statement. Added section 7.9 "Boot Strap Signals". Updated section 9 "BIOS Setup Description". Added a warning note regarding the flat foil cable in section 7.8 "DDI connector X6". Updated the whole document.

## Preface

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This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-EAF. It is one of three documents that should be referred to when designing an ETX® application. The other reference documents that should be used include the following:

- ETX® Design Guide
- ETX® Specification

The links to these documents can be found on the congatec AG website at [www.congatec.com](http://www.congatec.com)

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## Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

## Symbols

The following symbols are used in this user's guide:



### **Warning**

*Warnings indicate conditions that, if not observed, can cause personal injury.*



### **Caution**

*Cautions warn the user about how to prevent damage to hardware or loss of data.*



### **Note**

*Notes call attention to important information that should be observed.*

## Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHz	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
T.O.M.	Top of memory = max. DRAM installed
TDP	Thermal Design Power
SATA	Serial ATA
PATA	Parallel ATA
HDA	High Definition Audio
APU	Accelerated Processor Unit
CH	Controller Hub
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

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## ETX<sup>®</sup> Concept

The ETX<sup>®</sup> concept is an off the shelf, multi-vendor, single-board computer that integrates all the core components of a common PC and is mounted onto an application specific baseboard. ETX<sup>®</sup> modules have a standardized form factor of just 95mm x 114mm and have identical pinouts on the four system connectors. The ETX<sup>®</sup> module provides most of the functional requirements for any application. These functions include, but are not limited to graphics, sound, keyboard/mouse, IDE, Ethernet, parallel, serial and USB ports. Four ruggedized connectors provide the baseboard interface and carry all the I/O signals to and from the ETX<sup>®</sup> module.

Baseboard designers can use as little or as many of the I/O interfaces as deemed necessary. The baseboard therefore can provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly ETX<sup>®</sup> applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class ETX<sup>®</sup> modules. Simply unplug one module and replace it with another, no redesign is necessary.

## Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

## Electrostatic Sensitive Device



All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

## conga-EAF Options Information

The conga-EAF is available in seven variants. This user's guide describes all of these options. The tables below show the different configurations that are currently offered by congatec AG. Check the table for the Part no. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Part-No.	041071	041074	041072	041075
<b>CPU</b>	AMD G-T56N 1.6 GHz Dual Core	AMD G-T52R 1.5 GHz Single Core	AMD G-T48N 1.4 GHz Dual Core	AMD G-T44R 1.2 GHz Single Core
<b>DDR3 Speed</b>	DDR3-1333	DDR3-1333	DDR3-1066	DDR3-1066
<b>Cache</b>	512kB x 2	512kB	512kB x 2	512kB
<b>LVDS</b>	Yes	Yes	Yes	Yes
<b>Graphic</b>	Radeon™ HD 6320	Radeon™ HD 6310	Radeon™ HD 6310	Radeon™ HD 6250
<b>DisplayPort (DP)</b>	Yes (shared with HDMI)	Yes (shared with HDMI)	Yes (shared with HDMI)	Yes (shared with HDMI)
<b>HDMI</b>	Yes (shared with DP)	Yes (shared with DP)	Yes (shared with DP)	Yes (shared with DP)
<b>SATA</b>	x 2	x 2	x 2	x 2
<b>TDP</b>	18W	18W	18W	9W
<b>Suspend to RAM (S3)</b>	Yes	Yes	Yes	Yes

Part-No.	041073	041077	041076
<b>CPU</b>	AMD G-T40N 1.0 GHz Dual Core	AMD G-T40E 1.0 GHz Dual Core	AMD G-T40R 1.0 GHz Single Core
<b>DDR3 Speed</b>	DDR3-1066	DDR3-1066	DDR3-1066
<b>Cache</b>	512kB x 2	512kB x 2	512kB
<b>LVDS</b>	Yes	Yes	Yes
<b>Graphic</b>	Radeon™ HD 6290	Radeon™ HD 6250	Radeon™ HD 6250
<b>DisplayPort (DP)</b>	Yes (shared with HDMI)	Yes (shared with HDMI)	Yes (shared with HDMI)
<b>HDMI</b>	Yes (shared with DP)	Yes (shared with DP)	Yes (shared with DP)
<b>SATA</b>	x 2	x 2	x 2
<b>TDP</b>	9W	6.4W	5.5W
<b>Suspend to RAM (S3)</b>	Yes	Yes	Yes

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# 1 Specifications

## 1.1 Feature List

**Table 1 Feature Summary**

<b>Form Factor</b>	ETX® standard (Rev. 3.02)	
<b>Processor</b>	AMD G-T56N 1.6 GHz Dual Core with L2 cache 512kB x2 AMD G-T48N 1.4 GHz Dual Core with L2 cache 512kB x2 AMD G-T40N 1.0 GHz Dual Core with L2 cache 512kB x2 AMD G-T40E 1.0 GHz Dual Core with L2 cache 512kB x2 AMD G-T52R 1.5 GHz Single Core with L2 cache 512kB AMD G-T44R 1.2 GHz Single Core with L2 cache 512kB AMD G-T40R 1.0 GHz Single Core with L2 cache 512kB	
<b>Memory</b>	DDR3 SO-DIMM memory 1333 MT/s (666MHz) and 1066 MT/s (533 MHz) up to 4-GByte	
<b>Chipset</b>	AMD A55E Controller Hub	
<b>Audio</b>	Realtek ALC 262 HDA (High Definition Audio) codec	
<b>Ethernet</b>	Realtek RTL8105E	
<b>Graphics Options</b>	Integrated High Performance Video AMD Radeon™ HD 6310 or AMD Radeon™ HD 6250, DirectX®11 graphics with UVD 3.0, Integrated VGA DAC, Dual Simultaneous Display Support	
	<ul style="list-style-type: none"> <li>CRT Interface 400 MHz RAMDAC, Resolutions up to 1920x1200 @ 60Hz (WUXGA)</li> <li>2x DisplayPort 1.1a, Resolutions up to 1920x1200. Shared with HDMI port provided on flat-foil connector</li> <li>2x HDMI 1.3a Port, Resolutions up to 1920x1080. Shared with DisplayPort provided on flat-foil connector</li> <li>1x DisplayPort/HDMI port is used for LVDS if module supports LVDS</li> </ul>	<ul style="list-style-type: none"> <li>Flat panel Interface (provided by Analogix ANX3110 DisplayPort to LVDS converter)</li> <li>Single-channel LVDS interface support: 1 x 18 bpp or 1 x 24 bpp</li> <li>Dual-channel LVDS interface support: 2 x 18 bpp or 2 x 24 bpp panel. Supports VESA standard or JEDIA data mapping</li> <li>Automatic Panel Detection via EDID/EPI (Embedded Panel Interface based on VESA EDID™ 1.3). Resolutions up to 1900x1200 (WUXGA) @ 60 Hz</li> </ul>
<b>Super I/O</b>	Winbond 83627DHG	
<b>Peripheral Interfaces</b>	<ul style="list-style-type: none"> <li>PS/2 Keyboard, Mouse</li> <li>PCI Bus Rev. 2.3</li> <li>ISA Bus</li> <li>2x EIDE (UDMA-66/100)</li> <li>2x Serial ATA® with RAID 0,1 support. Connectors placed according to ETX specification 3.02</li> </ul>	<ul style="list-style-type: none"> <li>4x USB 2.0 (EHCI)</li> <li>I²C Bus, Fast Mode (400 kHz)</li> <li>Floppy (shared with LPT)</li> <li>LPT (EEP/ECP, shared with floppy)</li> <li>2 x COM Ports, TTL Level</li> <li>1 x IrDA Port</li> </ul>
<b>BIOS</b>	AMI Aptio® UEFI 2.x firmware, 4MByte serial SPI with congatec Embedded BIOS features	
<b>Power Management</b>	ACPI 3.0 compliant. Also supports Suspend to RAM (S3).	

### Note

*Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 8 of this user's guide to determine what options are available on your particular module.*

## 1.2 Supported Operating Systems

The conga-EAF supports the following operating systems.

- Microsoft® Windows® 7 (32 and 64 bit)
- Microsoft® Windows® 7 Embedded
- Microsoft® Windows® XP
- Microsoft® Windows® XP Embedded
- Linux



### Note

*The IDE interface on the conga-EAF can only be used in Native IDE mode (no compatible/legacy mode support). This means that any OS that is booted from the IDE interface must support Native IDE mode.*

## 1.3 Mechanical Dimensions

- 95.0 mm x 114.0 mm (3.75" x 4.5")
- Height approx. 12mm (0.4")

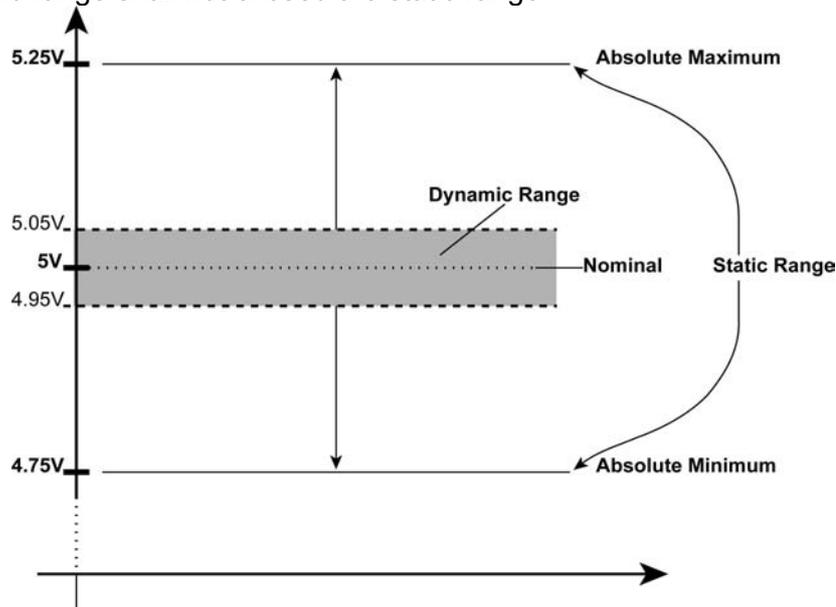
## 1.4 Electrical Characteristics

Characteristics			Min	Type	Max	Units	Comment
5V	Voltage	+/-5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	100	mV <sub>pp</sub>	0-20MHz
	Current	See section 1.5 'Power Consumption' for supply current information.					
5V_SB	Voltage	+/-5%	4.75	5.00	5.25	Vdc	
	Current			TBD	TBD	mA	

### 1.4.1 Supply Voltage Ripple

- 5V DC  $\pm$  5%
- Maximum 100mV peak to peak over a frequency band of 10Hz to 20MHz.

The dynamic range shall not exceed the static range.



### 1.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

## 1.5 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The ETX<sup>®</sup> module was mounted onto a special baseboard. This baseboard has two Hirose connectors that connect to the corresponding X3 and X4 connectors on the module. The special baseboard does not have any power consuming components mounted on it. It provides one connector for a CRT monitor connection, a PS2 keyboard and mouse connection, and an IDE device connection. The baseboard is powered by a direct current (DC) power supply that is set to output 5 volts and is connected directly to the special baseboard. Additionally, positive and negative sense lines are connected to the baseboard in order to measure the current consumption of the module. This current consumption value is displayed by the DC power supply's readout and this is the value that is recorded as the power consumption measurement. All recorded values are approximate.

All external peripheral devices such as the hard drive, are externally powered so that they do not influence the power consumption value that is measured for the module. This ensures the value measured reflects the true power consumption of the module and only the module. A keyboard is used to configure the module and then it is

disconnected before the measurement is recorded. If the keyboard remained connected, an additional current consumption of approximately 10 mA is noticed.

Each module was measured while running Windows XP Professional with SP3 (service pack 3) and the “Power Scheme” set to “Portable/Laptop”. This setting ensures that processor core is running in LFM (lowest frequency mode) with minimal core voltage during desktop idle. Each conga-EAF variant was tested with 2GB memory module. Using different sizes of RAM will cause slight variances in the measured results.

Power consumption values were recorded during the following stages:

#### Windows XP Professional SP2

- Desktop Idle
- 100% CPU workload (*see note below*)
- Windows Standby (*see note below*)



#### Note

*A software tool was used to stress the CPU to max. frequency.*

*ACPI OS Standby = S1 = POS (Power On Suspend) = CPU is in sleep mode (internal clocks stopped, no snoops)*

### 1.5.1 conga-EAF AMD G-T56N 1.6 GHz Dual Core

With 2GB memory installed

conga-EAF Article No. 041071	AMD T56N 1.6 GHz Dual Core with L2 cache 512kB x2 40nm Layout Rev. EBRALA0 /BIOS Rev. EBRA007		
Memory Size	2GB		
Operating System	Windows XP Professional SP3		
Power State	Desktop Idle	100% workload	Standby
Power consumption (measured in Amperes/Watts)	1.4 A/7.0 W	3.0 A/15.0 W	0.06 A/0.3 W

## 1.5.2 conga-EAF AMD G-T48N 1.4 GHz Dual Core

With 2GB memory installed

conga-EAF Article No. 041072	AMD T48N 1.4 GHz Dual Core with L2 cache 512kB x2 40nm Layout Rev. EBRALA0 /BIOS Rev. EBRA007		
Memory Size	2GB		
Operating System	Windows XP Professional SP3		
Power State	Desktop Idle	100% workload	Standby
Power consumption (measured in Amperes/Watts)	TBD A/TBD W	TBD A/TBD W	TBD A/TBD W

## 1.5.3 conga-EAF AMD G-T40N 1.0 GHz Dual Core

With 2GB memory installed

conga-EAF Article No. 041073	AMD T40N 1.0 GHz Dual Core with L2 cache 512kB x2 40nm Layout Rev. EBRALA0 /BIOS Rev. EBRA007		
Memory Size	2GB		
Operating System	Windows XP Professional SP3		
Power State	Desktop Idle	100% workload	Standby
Power consumption (measured in Amperes/Watts)	1.3 A/6.5 W	2.3 A/11.5 W	0.06 A/0.3 W

## 1.5.4 conga-EAF AMD G-T40E 1.0 GHz Dual Core

With 2GB memory installed

conga-EAF Article No. 041077	AMD T40E 1.0 GHz Dual Core with L2 cache 512kB 40nm Layout Rev. EBRALA0 /BIOS Rev. EBRA007		
Memory Size	2GB		
Operating System	Windows XP Professional SP3		
Power State	Desktop Idle	100% workload	Standby
Power consumption (measured in Amperes/Watts)	TBD A/W	TBD A/TBD W	TBD A/TBD W

### 1.5.5 conga-EAF AMD G-T52R 1.5 GHz Single Core

With 2GB memory installed

conga-EAF Article No. 041074	AMD T52R 1.5 GHz Single Core with L2 cache 512kB 40nm Layout Rev. EBRALA0 /BIOS Rev. EBRA007		
Memory Size	2GB		
Operating System	Windows XP Professional SP3		
Power State	Desktop Idle	100% workload	Standby
Power consumption (measured in Amperes/Watts)	1.3 A/6.5 W	2.1 A/10.5 W	0.06 A/0.3 W

### 1.5.6 conga-EAF AMD G-T44R 1.2 GHz Single Core

With 2GB memory installed

conga-EAF Article No. 041075	AMD T44R 1.2 GHz Single Core with L2 cache 512kB 40nm Layout Rev. EBRALA0 /BIOS Rev. EBRA007		
Memory Size	2GB		
Operating System	Windows XP Professional SP3		
Power State	Desktop Idle	100% workload	Standby
Power consumption (measured in Amperes/Watts)	1.3 A/6.5 W	2.0 A/10.0 W	0.06 A/0.3 W

### 1.5.7 conga-EAF AMD G-T40R 1.0 GHz Single Core

With 2GB memory installed

conga-EAF Article No. 041076	AMD T40R 1.0 GHz Single Core with L2 cache 512kB 40nm Layout Rev. EBRALA0 /BIOS Rev. EBRA007		
Memory Size	2GB		
Operating System	Windows XP Professional SP3		
Power State	Desktop Idle	100% workload	Standby
Power consumption (measured in Amperes/Watts)	TBD A/TBD W	TBD A/TBD W	TBD A/TBD W

#### Note

*All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Power consumption results will vary depending on the workload of components such as graphics engine, memory, etc.*

## 1.6 Supply Voltage Battery Power

- 2.0V-3.6V DC
- Typical 3.0V DC

### 1.6.1 CMOS Battery Power Consumption

RTC @ 20°C	Voltage	Current
Integrated in the AMD A55E FCH	3.0V	2.04 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9\_RTC\_Battery\_Lifetime.pdf, which can be found on the congatec AG website at [www.congatec.com](http://www.congatec.com).

## 1.7 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%



### Caution

*The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface.*

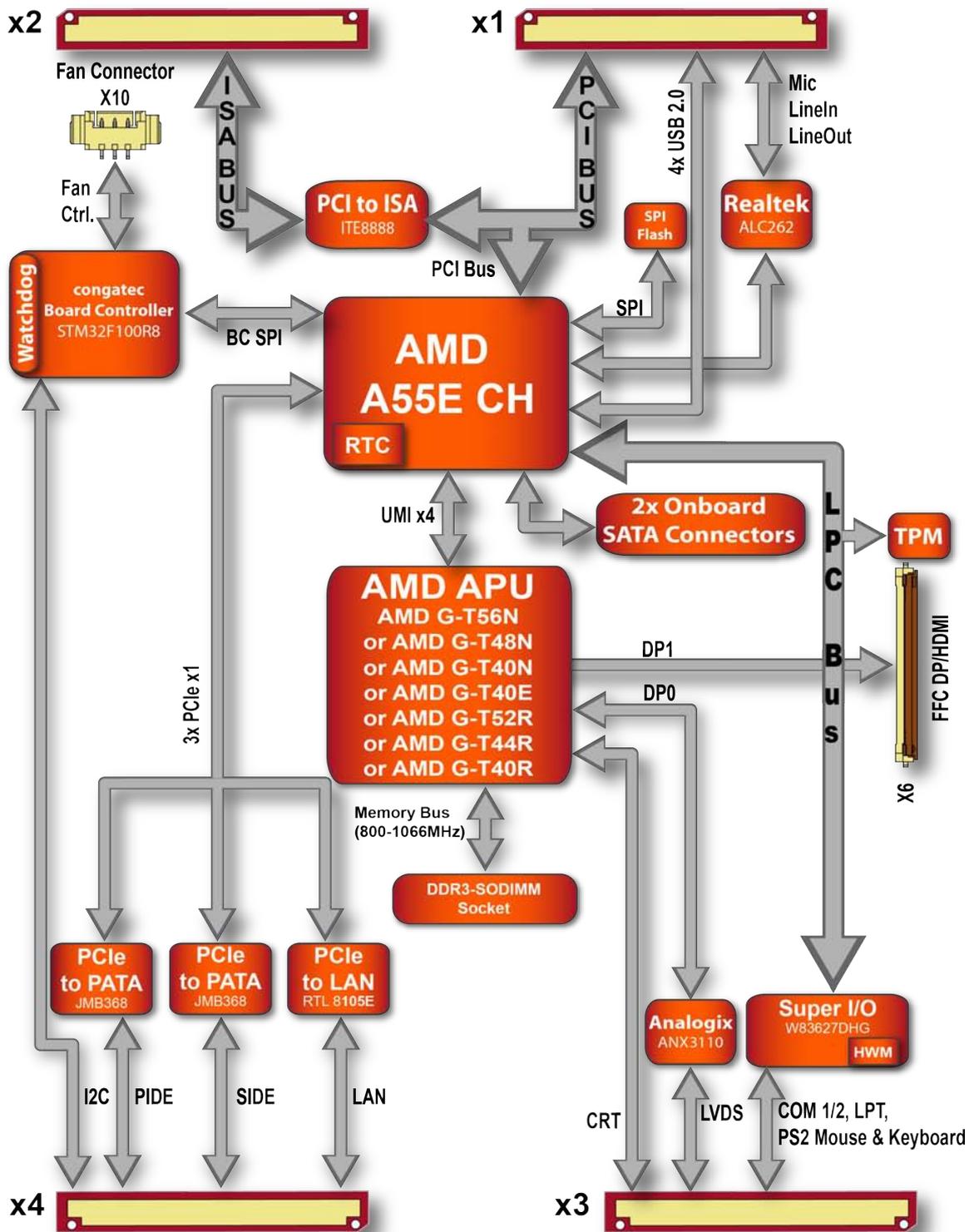
*congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.*

*If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.*

*For more information about operating a congatec module without heatspreader contact congatec technical support.*

*Humidity specifications are for non-condensing conditions.*

## 2 Block Diagram



## 3 Heatspreader

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An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module and its aluminum plate is 2mm thick.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis thereby using the whole chassis as a heat dissipator.



### Caution

*There are mounting holes on the heatspreader designed to attach the heatspreader to the module. These mounting holes must be used to ensure that all components that are required to make contact with heatspreader do so. Failure to utilize these mounting holes will result in improper contact between these components and heatspreader thereby reducing heat dissipation efficiency.*

*Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.*

*For more information about this subject refer to Application Note AN14\_ETX\_XTX\_Mounting\_Solutions.pdf that can be found on the congatec website.*

*Only heatspreaders that feature micro pins that secure the thermal stacks should be used for applications that require the heatspreader to be mounted vertically. It cannot be guaranteed that the thermal stacks will not move if a heatspreader that does not have the pilot pin feature is used in vertically mounted applications.*

*Additionally, the gap pad material used on all heatspreaders contains silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

*For more information about heatspreader mounting refer to Application Note AN14\_ETX\_XTX\_Mounting\_Solutions.pdf that can be found on the congatec website.*

## 3.1 Heatspreader Dimensions

### Note

*All measurements are in millimeters. Torque specification for heatspreader screws is 0.3 Nm.*



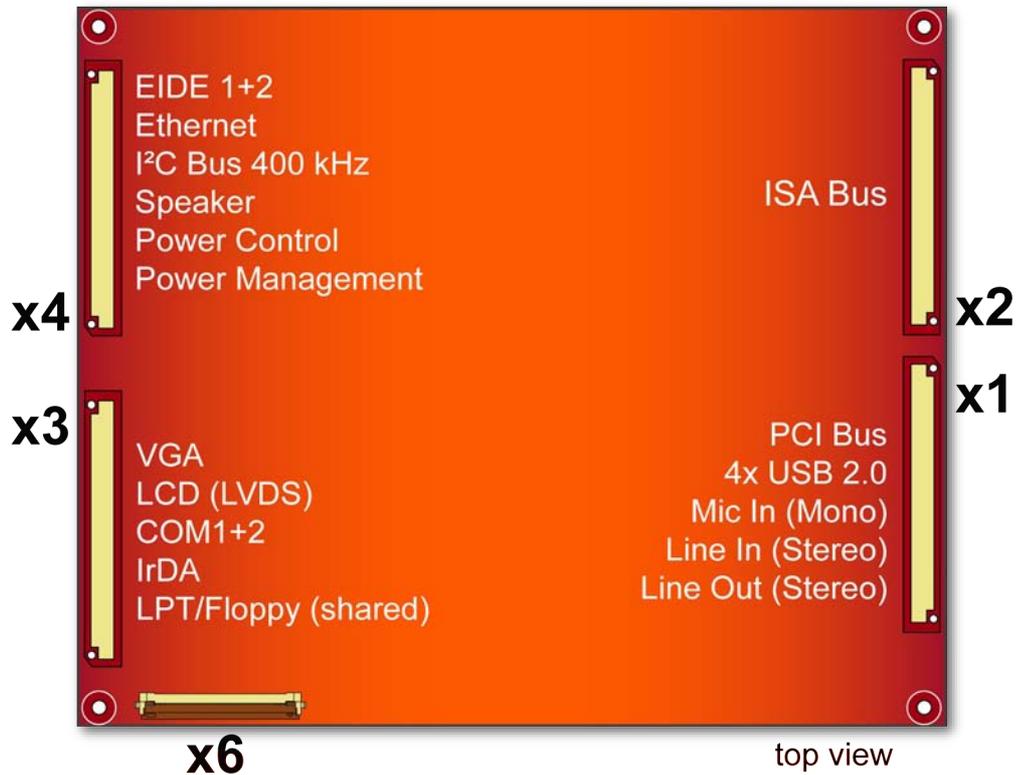
### Caution



*When using the heatspreader in a high shock and/or vibration environment, congatec recommends the use of a thread-locking fluid on the heatspreader screws to ensure the above mentioned torque specification is maintained.*

## 4 Connector Subsystems

### X connector Subsystems (top view)



In this view the connectors are seen “through” the module.

### 4.1 Connector X1

The following subsystems can be found on connector X1.

#### 4.1.1 PCI Bus

The implementation of the PCI bus complies with PCI specification Rev. 2.3 and ETX<sup>®</sup> specification Rev. 3.02. It provides a 32bit parallel PCI Bus that is capable of operating at 33MHz.

#### Note

*The PCI interface is specified to be +5V tolerant, with +3.3V signaling.*

## 4.1.2 USB 2.0

The conga-EAF offers 4 USB host ports via the AMD A55E FCH. These ports comply with USB standard 1.1 and 2.0 and they are located on the X1 connector. Each port is capable of supporting USB 1.1 and 2.0 compliant devices.



### Note

*The USB controller is a PCI bus device. The BIOS allocates the necessary system resources when configuring the PCI devices.*

## 4.1.3 Audio

The conga-EAF is equipped with a Realtek ALC262 HDA (High Definition Audio) codec onboard.

## 4.1.4 Onboard Generated Supply Voltage

Pins 12, 16 and 24 on the X1 connector provide the ability to connect external devices to the supply voltage (3.3V±5%) generated onboard the module. 3.3V external devices can be connected to these pins but must not exceed a maximum external load of 500mA. For more information about this feature contact congatec AG technical support.



### Caution

*Do not connect pins 12, 16 and 24 to a 3.3V external power supply. This will cause a current cross-flow and may result in either a system malfunction and/or damage to the external power supply and the module.*

## 4.2 Connector X2 (ISA Bus)

The AMD chipset used on conga-EAF does not offer native support for the ISA bus. The ISA bus is provided by an ITE8888 PCI to ISA bridge. The combination of the chipset, the PCI to ISA bridge and the UEFI firmware running on the conga-EAF does not offer a 100% compatible ISA bus.

### 4.2.1 ISA Bus Limitations

#### 4.2.1.1 IRQs that can be used for ISA (3 in total)

IRQ5 is unconditionally reserved for ISA bus only

Two additional IRQs (3, 4, 6, 7, 10, 11, 14 or 15) can be made available for the ISA bus via BIOS setup nodes. See section "PCI Configuration Submenu" in the conga-EAF user's guide. The selection of these two additional ISA IRQs is only available in BIOS version EBRAR010 and later.

When using IRQ3, IRQ4 or IRQ7, the respective onboard Super I/O device (COM1, COM2, LPT) must be disabled.

IRQ14 and IRQ15 are only available for the ISA bus as long as the internal SATA controller is not set to legacy mode (default is native mode).

#### **4.2.1.2 No ISA DMA support**

Due to this limitation, there is no support for ISA sound cards and SCSI cards since these cards require ISA DMA transfers.

#### **4.2.1.3 No support for ISA VGA cards**

ISA graphic cards are not supported.

#### **4.2.1.4 ISA memory support limitations**

ISA memory can only be accessed in the D0000h to DFFFFh range. There is no 15-16MB memory hole support. ISA OptionROMs are not executed by the UEFI firmware.

#### **4.2.1.5 ISA I/O support limitations**

I/O addresses 2F8h-2FFh, 3F8h-3FFh, 378h-37fh, 778h-77Fh and A00h-A0Fh are unconditionally routed to LPC. This means they are not available for ISA.

All other I/O addresses above 100h are available as long as they are not used by PCI/PCIe Express or chipset internal devices.

#### **4.2.1.6 No support for ISA PnP**

The UEFI does not offer any support for Plug & Play and therefore there is no support for ISA Plug & Play. This means that a PnP ISA card cannot be expected to work. No ISA PnP configuration cycle will be executed by the UEFI. The card will usually resort back to its default configuration. Since no PnP memory structures will be added by the UEFI, there is the possibility that the device drivers will not work after loading the OS.

## **4.3 Connector X3**

The following subsystems can be found on connector X3. The implementation of all the subsystems comply with ETX<sup>®</sup> specification 3.02. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Check the BIOS Setup Description section for more information about how to configure a particular subsystem.

### **4.3.1 Graphics**

The conga-EAF features integrated high performance video within the AMD APU. Either AMD Radeon™ HD 6310 (18W APU) or AMD Radeon™ HD 6250 (9W APU) is integrated in the AMD processor. It supports DirectX®11 graphics with UVD 3.0, integrated VGA DAC, and dual simultaneous display.

### **4.3.2 LCD**

The conga-EAF offers a dual channel LVDS interface. This interface is provided through the use of Analogix ANX3110 attached to one of the two APU DisplayPort interfaces. ANX3110 is a high quality DisplayPort™ to LVDS converter offering up to 24 bits per pixel and single/dual channel LVDS output support.

### **4.3.3 Serial Ports (1 and 2)**

The conga-EAF offers two serial interfaces (TTL level) via the Winbond W83627DHG super I/O controller located on the conga-EAF.

### **4.3.4 Serial Infrared Interface**

Serial port 2 can be configured as a serial infrared interface. The Infrared (IrDA) function provides point-to-point (or multi-point to multi-point) wireless communication, which can operate under various transmission protocols including IrDA SIR. This feature is also implemented by the onboard Winbond W83627DHG super I/O.

### **4.3.5 Parallel Port**

The multi-mode parallel port can be configured as either a conventional LPT parallel port, an Enhanced Parallel Port (EPP) or an Extended Capabilities Parallel Port (ECP). This is software implemented and can be configured in the BIOS setup program. See section 9.4.12 of this document for information about configuring the parallel port.

### **4.3.6 Keyboard/Mouse**

The implementation of these subsystems comply with ETX<sup>®</sup> specification 3.02.

## 4.4 Connector X4

The following subsystems can be found on connector X4. The implementation of all the subsystems comply with ETX<sup>®</sup> specification 3.02. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Check the BIOS Setup Description section for more information about how to configure a particular subsystem.

### 4.4.1 IDE

The conga-EAF supports an IDE interface that is capable of UDMA-33/66/100 operation. This interface is implemented by converting PCI Express to parallel ATA channels using JMicron's JMB368 chip. IDE provides the connection of two channels (master/slave) that are available as primary and secondary devices at any given moment.



#### Note

*The IDE interface on the conga-EAF can only be used in Native IDE mode (no compatible/legacy IDE mode support).*

### 4.4.2 Ethernet

Ethernet interface is provided by a Realtek RTL8105E Fast Ethernet NIC controller. The controller is IEEE 802.3u, 10/100Base-Tx fast Ethernet compatible. The interface provides single-ended differential signals that have to be routed through an Ethernet transformer to the 10/100 BaseT RJ45 connector placed on the carrier board.

### 4.4.3 I<sup>2</sup>C Bus 400kHz

The I<sup>2</sup>C bus is implemented through the use of STMicroelectronics STM32F100R8 microcontroller. It provides a Fast Mode (400kHz max.) multi-master I<sup>2</sup>C Bus that has maximum I<sup>2</sup>C bandwidth.

## 4.4.4 Power Control

### PWGIN

PWGIN (pin 4 on the X4 connector) can be connected to an external power good circuit or it may also be utilized as a manual reset input. In order to use PWGIN as a manual reset the pin must be grounded through the use of a momentary-contact pushbutton switch. When external circuitry asserts this signal, it's necessary that an open-drain driver drives this signal causing it to be held low for a minimum of 15ms to initiate a reset. Using this input is optional. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies, the conga-EAF module is capable of generating its own power-on reset.

The conga-EAF provides support for controlling ATX-style power supplies. In order to do this, the power supply must provide a constant source of 5V power. When not using an ATX power supply then the conga-EAF's pins PS\_ON, 5V\_SB, and PWRBTN# should be left unconnected.

### PS\_ON#

The PS\_ON (pin 5 on the X4 connector) signal is an active-low output that turns on the main outputs of an ATX-style power supply. This open-collector signal can be pulled up to the 5V\_SB supply voltage through the use of a 1K resistor. Usually there is a pull-up resistor internally implemented in the power supply yet it is also good practice to implement a footprint for the pull-up resistor in the baseboard circuitry.

### PWRBTN#

When using ATX-style power supplies, PWRBTN# (pin 7 on the X4 connector) is used to connect to a momentary-contact, active-low pushbutton input while the other terminal on the pushbutton must be connected to ground. This signal is ETX<sup>®</sup> internally pulled up to 5V\_SB using a 4k7 resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in the BIOS settings or by system software.

## Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-EAF. The remaining necessary voltages are internally generated on the module using onboard power supplies. A baseboard designer should be aware of the following important information when designing a power supply for a conga-EAF application:

- As mentioned earlier in section 4.1.4 the conga-EAF is capable of generating an onboard 3.3V supply with an output current that is limited to 500mA. If an external device requires more than this 500mA limit then it's necessary to design a 3.3V supply into the baseboard.



### Caution

*It is not possible to connect an external 3.3V supply to the onboard generated 3.3V supply pins on the conga-EAF module. This will cause a current cross-flow and may result in either a system malfunction and/or damage to the external power supply and the module.*

- Sometimes when designing baseboards, baseboard designers choose to fuse power to some external devices such as keyboards or USB devices by using solid-state or polyswitch overcurrent protection devices. This results in the protective devices typically only opening after they pass their rated current several times for long periods of time. When the application power supply is incapable of generating the necessary current needed to open these protective devices, it is possible that the application crashes as a result of an external fault and therefore will reduce the reliability of the application as well as make fault diagnosis difficult.
- It has also been noticed that on some occasions, problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) generates their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase, thereby ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit [www.formfactors.org](http://www.formfactors.org) and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

#### 4.4.5 Power Management

APM 1.2 compliant. ACPI 3.0. Also supports Suspend to RAM (S3).

#### 4.5 Connector X6

Flat foil connector X6 provides a Digital Display Interface (DDI), that can be configured to be a DisplayPort or HDMI/DVI Interface.

#### 4.6 Connectors X8 and X9

In accordance to ETX Specification 3.02, SATA interfaces are supported on the conga-EAF via two right angle SATA connectors placed on the topside of the module. Connector X8 provides SATA0, connector X9 provides SATA1.

#### 4.7 Fan Connector X10

A 3pin fan connector is provided on conga-EAF via connector X10 to support active cooling. See section 6.5 for more details.

## 5 Additional Features

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### 5.1 Watchdog

The conga-EAF is equipped with a multi stage watchdog. This solution can be triggered by software and external OEM hardware (input pin is pin 48 on the X2 connector called WDTRG#). For more information about the Watchdog feature see the BIOS setup description section 9.4.2 of this document and application note AN3\_Watchdog.pdf on the congatec AG website at [www.congatec.com](http://www.congatec.com).

### 5.2 Onboard Microcontroller

The conga-EAF is equipped with a STMicroelectronics STM32F100R8 microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I<sup>2</sup>C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability even when the x86 processor is in a low power mode.

### 5.3 Embedded BIOS

The conga-EAF is equipped with congatec Embedded BIOS and has the following features:

- ACPI Power Management
- ACPI Battery Support
- Supports Customer Specific CMOS Defaults
- Multistage Watchdog
- User Data Storage
- Manufacturing Data and Board Information
- OEM Splash Screen
- Flat Panel Auto Detection and Backlight Control
- BIOS Setup Data Backup
- Fast Mode I<sup>2</sup>C Bus
- Real Headless Operation
- Console Redirection via Serial Port

## 5.4 Security Features

The conga-EAF can be equipped optionally with a “Trusted Platform Module“ (TPM 1.2). This TPM 1.2 includes coprocessors to calculate efficient hash and RSA algorithms with key lengths up to 2,048 bits as well as a real random number generator. Security sensitive applications like gaming and e-commerce will benefit also with improved authentication, integrity and confidence levels.

## 5.5 Suspend to RAM

The Suspend to RAM feature is supported on the conga-EAF.

## 5.6 DDI

The conga-EAF provides one Digital Display Interface (DDI), which is implemented by the AMD APU. This interface is available via X6 connector located on the bottom side of conga-EAF. DDI can be configured to support DisplayPort or TMDS signals used by HDMI or DVI. The DisplayPort is compliant with DisplayPort Standard Version 1.1a; HDMI is compliant with High-Definition Multimedia Interface Specification Version 1.3a; DVI is compliant with Digital Visual Interface Revision 1.0. For information about the pinout of the X6 connector see section 7.8 .

## 5.7 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for additional modifications to the system BIOS.

The conga-EAF BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM<sup>2</sup> User's Guide

## 6 conga Tech Notes

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The conga-EAF has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

### 6.1 Native vs. Compatible IDE mode

#### 6.1.1 Compatible Mode

When operating in compatible mode, the SATA controller needs two legacy IRQs (14 and 15) and is unable to share these IRQs with other devices. This is because the SATA controller emulates the primary and secondary legacy IDE controllers. The two PATA controllers on conga-EAF do not support compatible IDE mode. The SATA controller defaults to native IDE mode but can be set to Compatible/Legacy IDE mode in the "SATA/PATA Configuration Submenu" in the BIOS setup program. See section 9.4.10 of this user's guide for more information about this.

#### 6.1.2 Native Mode

Native mode allows the SATA controller and PATA controllers to operate as true PCI devices and therefore do not need dedicated legacy resources. This means they can be configured anywhere within the system. When either controller runs in native mode, it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system. Running the SATA controller in native mode frees up IRQs 14 and 15 to be used for the ISA bus and decreases the chance that there may be a shortage of interrupts when installing devices.

#### Note

*If your operating system supports native mode then congatec AG recommends you enable it. Only operating systems supporting native IDE mode can be booted from the PATA interface.*

### 6.2 Thermal Monitor and Catastrophic Thermal Protection

G-Series processors provide a side-band thermal sensor interface (SB-TSI) to read the die temperature. The thermal diode is not supported on G-Series processors. SB-TSI is an on-die temperature sensing interface that accesses the internal digital temperature sensor. SB-TSI uses SMBus protocol, which allows use of an embedded controller. Additionally on G-Series processors, SB-TSI can set a P-state limit to limit the CPU power consumption.

#### Note

*The maximum operating temperature for G-Series processors is 100°C.*

## 6.3 Processor Thermal Management

G-Series processors provide hardware thermal control (HTC), local hardware thermal control (LHTC), PROCHOT\_L pin, and THERMTRIP to ensure that the processor is within its functional temperature limits.

- HTC is a hardware mechanism activated internally by the processor to reduce its power consumption.
- LHTC provides an additional layer of thermal protection. When the LHTC temperature threshold is exceeded, the processor limits the maximum P-state of all cores to reduce power consumption. Typically, the LHTC temperature threshold is few degrees below the HTC temperature threshold. Also, the LHTC limits the processor to a higher P-state than HTC, i.e., the reduction in power with LHTC is less than that with HTC.
- The PROCHOT\_L pin, as a bidirectional pin, provides a mechanism for hardware (e.g. an embedded controller or external temperature sensor) to activate HTC. It is useful for current limiting under battery control and system thermal management.
- THERMTRIP is a hardware-enforced thermal protection mechanism activated by the processor. The processor clocks are gated off and a low voltage VID is sent to the voltage regulator. THERMTRIP activates only when the processor temperature is much greater than the specified maximum temperature (approximately at 125°C).

## 6.4 Processor Performance Control

G-Series processors run at different voltage/frequency states (performance states) referred to as P-State technology. Operating systems that support performance control take advantage of microprocessors that use several performance states in order to efficiently operate the processor when it's not being fully utilized. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting found in the control panel option applet.

### Note

*If the "Home/Office" or "Always On" power scheme is selected when using Windows operating systems then the processor will always run at the highest performance state. For more information about this subject see chapter 8 of the ACPI Specification Revision 2.0c, which can be found at [www.acpi.info](http://www.acpi.info). Also visit Microsoft's website and search for the document called "Windows Native Processor Performance Control".*

## 6.5 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

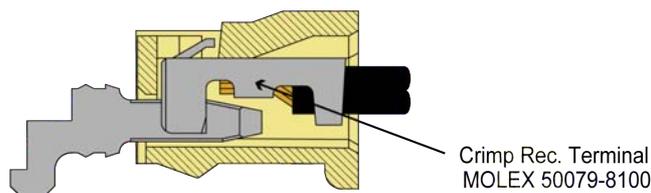
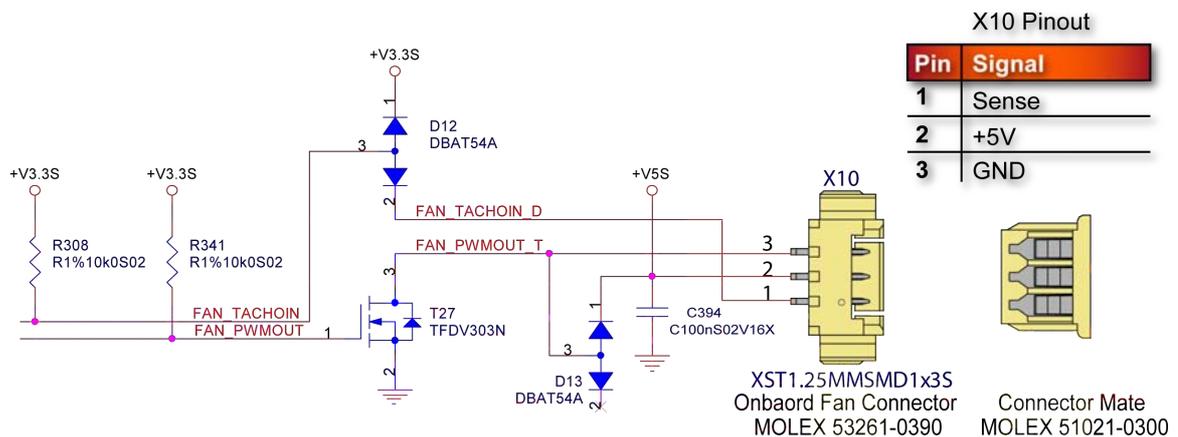
The conga-EAF ACPI thermal solution offers three different cooling policies.

- Passive Cooling

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- Active Cooling

The conga-EAF is equipped with an onboard fan connector that is described in the diagram below. During an active cooling policy the operating system turns the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the "active cooling trip point" setup node in the BIOS setup description section 9.4.1 to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).



- Critical Trip Point

If the temperature in the thermal zone reaches a critical point then the operating system performs a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the “critical trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.


**Notes**

*The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points. If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled.*

## 6.6 ACPI Suspend Modes and Resume Events

conga-EAF supports the S3 (STR= Suspend to RAM) state. For more information about S3 wake events see section 9.4.4 “ACPI Configuration Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4\_BIOS) but it is supported by the following operating systems (S4\_OS= Hibernate):

- Windows 7/Vista/XP/2K
- Linux

This table lists the “Wake Events” that resume the system from S3 unless otherwise stated in the “Conditions/Remarks” column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.


**Note**

*The above list has been verified using a Windows XP SP3 ACPI enabled installation.*

## 6.7 USB 2.0 EHCI Host Controller Support

The 4 USB ports are shared between the 3 EHCI host controller and the 3 OHCI host controllers. Within the EHC functionality, there is a port-routing logic that executes the muxing between the two different types of host controllers (EHCI and OHCI). This means that when a USB device is connected, the routing logic determines who owns the port. If the device is not USB 2.0 compliant or if the software drivers for EHCI support are not installed, then the OHCI controller owns the ports.

## 6.8 HDMI/DisplayPort (DP) Audio Support

In order to support HDMI/DP audio on the X6 connector, the system must be configured as follows:

- BIOS default settings (HDA Controller ENABLED, HDMI/DP Audio Support ENABLED)
- Installation of AMD chipset drivers include HDMI/DP audio support
- Installation of Realtek HDA codec driver

HDMI/DP audio and native HDA audio can only work one at a time, not both at the same time. The desired audio output must be selected in the audio device driver and/or OS setting.

congatec has validated the HDMI/DP audio functionality within Windows XP SP3 by using the following test procedures and settings.

Play wma/mp3 (video/audio) file with Microsoft Windows media player:

- Audio functions on one output only (either HDMI/DP or HDA):
- Connect headphones to HDMI/DP monitor -> validate that this is functioning.
- Next step (while audio is still present) connect another speaker to the native audio output of the conga-EAF -> validate that no audio is present.
- Change the default "Sound Playback device" in the "Sound and Audio Device Properties" menu (see below) to "Realtek HD Audio output".



After this change the audio is no longer present in the headphones connected to the HDMI/DP monitor but the audio is now present on the native audio output of the conga-EAF.

## 7 Signal Descriptions and Pinout Tables

The following section describes the signals found on the four X connectors located on the bottom of the module.

This table describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if an ETX<sup>®</sup> internal pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented.

The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.

**Table 2 Signal Tables Terminology Descriptions**

Term	Description
PU	ETX <sup>®</sup> Internally implemented Pull up resistor
PD	ETX <sup>®</sup> Internally implemented Pull down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
P	Power Input/Output
DDC	Display Data Channel
LVDS	Low Voltage Differential Signal-350mV nominal; 450mV maximum differential signal

### 7.1 X1 Connector Signal Descriptions

**Table 3 Signal Descriptions**

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC ±5%	P		External supply
GND	Power Ground	P		External supply
3V	Power Supply +3.3VDC	P		See section 4.1.4
N.C.	Not Connected or internally connected	N.A.		Do not connect on baseboard
SERRIRQ	Serial Interrupt request	I 3.3V		Used in conjunction with LPC bus

**Table 4 PCI Signal Descriptions**

Signal	Description of PCI Bus Signals	I/O	PU/PD	Comment
PCICLK1..4.	Clock output	O 3.3V		
REQ0..3#	Bus request	I 3.3V		5V tolerant
GNT0..3#	Bus grant	O 3.3V		
AD0..31	Address/Data bus lines	I/O 3.3V		5V tolerant
CBE0..3#	Bus command/byte enables	I/O 3.3V		5V tolerant
PAR	Bus parity	I/O 3.3V		5V tolerant
SERR#	Bus system error	I/O 3.3V		5V tolerant
GPERR#	Bus grant parity error	I/O 3.3V		5V tolerant
PME#	Bus power management event	I/O 3.3V		5V tolerant
LOCK#	Bus lock	I/O 3.3V		5V tolerant
DEVSEL#	Bus device select	I/O 3.3V		5V tolerant
TRDY#	Bus target ready	I/O 3.3V		5V tolerant
IRDY#	Bus initiator ready	I/O 3.3V		5V tolerant
STOP#	Bus stop	I/O 3.3V		5V tolerant
FRAME#	Bus frame	I/O 3.3V		5V tolerant
PCIRST#	Bus reset	O 3.3V		
INTA#	Bus interrupt A	I 3.3V		5V tolerant
INTB#	Bus interrupt B	I 3.3V		5V tolerant
INTC#	Bus interrupt C	I 3.3V		5V tolerant
INTD#	Bus interrupt D	I 3.3V		5V tolerant

**Table 5 USB Signal Descriptions**

Signal	Description of USB Signals	I/O	PU/PD	Comment
USB0	USB Port 0, data + or D+	I/O 3.3V		Differential Pair, USB 2.0 compliant and backwards compatible to USB 1.1
USB0#	USB Port 0, data - or D-	I/O 3.3V		
USB1	USB Port 1, data + or D+	I/O 3.3V		Differential Pair, USB 2.0 compliant and backwards compatible to USB 1.1
USB1#	USB Port 1, data - or D-	I/O 3.3V		
USB2	USB Port 2, data + or D+	I/O 3.3V		Differential Pair, USB 2.0 compliant and backwards compatible to USB 1.1
USB2#	USB Port 2, data - or D-	I/O 3.3V		
USB3	USB Port 3, data + or D+	I/O 3.3V		Differential Pair, USB 2.0 compliant and backwards compatible to USB 1.1
USB3#	USB Port 3, data - or D-	I/O 3.3V		

**Table 6 Audio Signal Descriptions**

Signal	Description of Audio Signals	I/O	PU/PD	Comment
SNDL	Line-Level stereo output left	O		Analog output (1 Vrms)
SNDR	Line-Level stereo output right	O		Analog output (1 Vrms)
AUXAL	Auxiliary input A left	I		Analog input (1 Vrms)
AUXAR	Auxiliary input A right	I		Analog input (1 Vrms)
MIC	Microphone input	I		Analog input (1 Vrms)
ASGND	Analog ground of sound controller	P		
ASVCC	Analog supply of sound controller	P		Internally connected to +3.3 audio voltage for reference, max. 10mA

## 7.2 Connector X1 Pinout

**Table 7 X1 Connector Pinout**

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	PCICLK3	4	PCICLK4	53	PAR	54	SERR#
5	GND	6	GND	55	GPERR#	56	Reserved
7	PCICLK1	8	PCICLK2	57	PME#	58	USB2#
9	REQ3#	10	GNT3#	59	LOCK#	60	DEVSEL#
11	GNT2#	12	3V	61	TRDY#	62	USB3#
13	REQ2#	14	GNT1#	63	IRDY#	64	STOP#
15	REQ1#	16	3V	65	FRAME#	66	USB2
17	GNT0#	18	RESERVED	67	GND	68	GND
19	VCC	20	VCC	69	AD16	70	CBE2#
21	SERIRQ	22	REQ0#	71	AD17	72	USB3
23	AD0	24	3V	73	AD19	74	AD18
25	AD1	26	AD2	75	AD20	76	USB0#
27	AD4	28	AD3	77	AD22	78	AD21
29	AD6	30	AD5	79	AD23	80	USB1#
31	CBE0#	32	AD7	81	AD24	82	CBE3#
33	AD8	34	AD9	83	VCC	84	VCC
35	GND	36	GND	85	AD25	86	AD26
37	AD10	38	AUXAL	87	AD28	88	USB0
39	AD11	40	MIC	89	AD27	90	AD29
41	AD12	42	AUXAR	91	AD30	92	USB1
43	AD13	44	ASVCC	93	PCIRST#	94	AD31
45	AD14	46	SNDL	95	INTC#	96	INTD#
47	AD15	48	ASGND	97	INTA#	98	INTB#
49	CBE1#	50	SNDR	99	GND	100	GND

## 7.3 X2 Connector Signal Descriptions

**Table 8 Signal Descriptions**

Signal	Description	I/O	Comment
VCC	Power Supply +5VDC, ±5%	I	External supply
GND	Power Ground	I	External supply
N.C.	Not connected	N.A.	Do not connect

**Table 9 ISA Bus Signal Descriptions**

Signal	Description of ISA Bus Signals	I/O	PU/PD	Comment
SD0..15	ISA Data bus	I/O 5V		
SA0..19, LA17..20	ISA Address bus	O 5V		
SBHE#	ISA Byte High Enable	O 5V		
BALE	ISA Address Latch Enable	O 5V		
AEN	ISA Address Enable	O 5V		
MEMR#	ISA memory read	O 5V		
SMEMR#	ISA memory read in lowest 1MB address range	O 5V		
MEMW#	ISA memory write	O 5V		
SMEMW#	ISA memory write in lowest 1MB address range	O 5V		
IOR#	ISA IO read	O 5V		
IOW#	ISA IO write	O 5V		
IOCHK#	ISA IO check	I 5V		
IOCHRDY	ISA IO channel ready	I 5V		
M16#	ISA 16Bit memory device	I 5V		
IO16#	ISA 16Bit IO device	I 5V		
REFSH#	ISA memory refresh cycle pending	O 5V		
NOWS#	ISA No wait states	I 5V		
MASTER#	ISA Master	I 5V		
SYSCLK	ISA System clock (8 MHz)	O 5V		
OSC	ISA Oscillator (14,31818 MHz)	O 5V		
RSTDRV	ISA Reset signal	O 5V		
DREQ [0,1,2,3,5,6,7]	ISA DMA request	I 5V		
DACK# [0,1,2,3,5,6,7]	ISA DMA acknowledge	O 5V		
TC	ISA DMA end	O 5V		
IRQ [3..7, 9..15]	ISA Interrupt request	I/O 5V		

## 7.4 X2 Connector Pinout

**Table 10 Connector X2 Pinout**

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	SD14	4	SD15	53	SA6	54	IRQ5
5	SD13	6	MASTER#	55	SA7	56	IRQ6
7	SD12	8	DREQ7	57	SA8	58	IRQ7
9	SD11	10	DACK7#	59	SA9	60	SYSCLK
11	SD10	12	DREQ6	61	SA10	62	REFSH#
13	SD9	14	DACK6#	63	SA11	64	DREQ1
15	SD8	16	DREQ5	65	SA12	66	DACK1#
17	MEMW#	18	DACK5#	67	GND	68	GND
19	MEMR#	20	DREQ0	69	SA13	70	DREQ3
21	LA17	22	DACK0#	71	SA14	72	DACK3#
23	LA18	24	IRQ14	73	SA15	74	IOR#
25	LA19	26	IRQ15	75	SA16	76	IOW#
27	LA20	28	IRQ12	77	SA18	78	SA17
29	LA21	30	IRQ11	79	SA19	80	SMEMR#
31	LA22	32	IRQ10	81	IOCHRDY	82	AEN
33	LA23	34	IO16#	83	VCC	84	VCC
35	GND	36	GND	85	SD0	86	SMEMW#
37	SBHE#	38	M16#	87	SD2	88	SD1
39	SA0	40	OSC	89	SD3	90	NOWS#
41	SA1	42	BALE	91	DREQ2	92	SD4
43	SA2	44	TC	93	SD5	94	IRQ9
45	SA3	46	DACK2#	95	SD6	96	SD7
47	SA4	48	IRQ3	97	IOCHK#	98	RSTDRV
49	SA5	50	IRQ4	99	GND	100	GND

## 7.5 X3 Connector Signal Descriptions

**Table 11 Signal Descriptions**

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC, $\pm 5\%$	P		External supply
GND	Power Ground	P		External supply
N.C.	Not connected	N.A.		Do not connect
LTGIO0	General Purpose I O	N.C.		Not supported

**Table 12 CRT Signal Descriptions**

Signal	Description of CRT signals	I/O	PU/PD	Comment
HSY	Horizontal Synchronization Pulse	O 5V		
VSY	Vertical Synchronization Pulse	O 5V		
R	Red channel RGB Analog Video Output	O		Analog output
G	Green channel RGB Analog Video Output	O		Analog output
B	Blue channel RGB Analog Video Output	O		Analog output
DDCK	Display Data Channel Clock	I/O 5V		
DDDA	Display Data Channel Data	I/O 5V		

**Table 13 COM Signal Descriptions**

Signal	Description of COM signals	I/O	PU/PD	Comment
DTR1#	Data terminal ready for COM1	O 3.3V		
DTR2#	Data terminal ready for COM2	O 3.3V		
RI1#, RI2#	Ring indicator for COM1/COM2	I 3.3V	PU 100K	5V tolerant input
TXD1	Data transmit for COM1	O 3.3V		
TXD2	Data transmit for COM2	O 3.3V		
RXD1, RXD2	Data receive for COM1/COM2	I 3.3V	PU 100K	5V tolerant input
CTS1#, CTS2#	Clear to send for COM1/COM2	I 3.3V	PU 100K	5V tolerant input
RTS1#, RTS2#	Request to send for COM1/COM2	O 3.3V		
DCD1#, DCD2#	Data carrier detect for COM1/COM2	I 3.3V	PU 100K	5V tolerant input
DSR1#, DSR2#	Data set ready for COM1/COM2	I 3.3V	PU 100K	5V tolerant input

**Table 14 Keyboard and Infrared Signal Descriptions**

Signal	Description of keyboard and infrared signals	I/O	PU/PD	Comment
KBDAT	Keyboard Data	I/O 5V	PU 4K7	
KBCLK	Keyboard Clock	O 5V	PU 4K7	
MSDAT	Mouse Data	I/O 5V	PU 4K7	
MSCLK	Mouse Clock	O 5V	PU 4K7	
IRTX	Infrared Transmit	O 5V	PU 100K	
IRRX	Infrared Receive	I 5V	PU 100K	

**Table 15 LVDS Flat Panel Signals**

Signal	Description of LVDS Flat Panel signals	I/O	PU/PD	Comment
BIASON	Controls display contrast voltage ON	O 3.3V		
DIGON	Controls display Power ON	O 3.3V		
BLON#	Controls display Backlight ON	O 3.3V		
LCDD00..19	LVDS channel data 0..19	O LVDS		
DETECT#	Panel hot-plug detection	N.C.		
FPDDC_CLK	DDC lines used for flat panel detection and control.	O 3.3V		
FPDDC_DAT	DDC lines used for flat panel detection and control.	I/O 3.3V		

**Table 16 LVDS Interface Pinout**

Pin	Signal Name	Signal Mapping	Pin	Signal Name	Signal Mapping
1	GND		2	GND	
3	R		4	B	
5	HSY		6	G	
7	VSY		8	DDCK	
9	DETECT# (*)		10	DDDA	
11	LCDDO[16]	TX2OUTCLK-	12	LCDDO[18]	TX2OUT3-
13	LCDDO[17]	TX2OUTCLK+	14	LCDDO[19]	TX2OUT3+
15	GND		16	GND	
17	LCDDO[13]	TX2OUT1+	18	LCDDO[15]	TX2OUT2+
19	LCDDO[12]	TX2OUT1-	20	LCDDO[14]	TX2OUT2-
21	GND		22	GND	
23	LCDDO[8]	TX1OUT3-	24	LCDDO[11]	TX2OUT0+
25	LCDDO[9]	TX1OUT3+	26	LCDDO[10]	TX2OUT0-
27	GND		28	GND	
29	LCDDO[4]	TX1OUT2-	30	LCDDO[7]	TX1OUTCLK+
31	LCDDO[5]	TX1OUT2+	32	LCDDO[6]	TX1OUTCLK-
33	GND		34	GND	
35	LCDDO[1]	TX1OUT0+	36	LCDDO[3]	TX1OUT1+
37	LCDDO[0]	TX1OUT0-	38	LCDDO[2]	TX1OUT1-
39	VCC		40	VCC	
41	FPDDC_DAT		42	LTGIO0	
43	FPDDC_CLK		44	BLON#	
45	BIASON		46	DIGON	
47	COMP (*)		48	Y (*)	
49	SYNC (*)		50	C (*)	

TX1= Channel 1 transmit  
 TX2= Channel 2 transmit

 **Note**

*The signals marked with an asterisk symbol (\*) are not supported on the conga-EAF.*

**Table 17 FDC Signal Descriptions (not supported)**

Signal	Description of FDC signals (shared with LPT)	I/O	PU/PD	Comment
FLPY#	Floppy Interface configuration input	I 3.3V	10K	Not supported
RES	N.C.	N.A.		Not available
DENSEL	Density select: low = 250/300Kb/s high = 500/1000Kb/s	O 5V		
INDEX#	Index signal	I 5V		
TRK0#	Track signal	I 5V		
WP#	Write protect signal	I 5V		
RDATA#	Raw data read	I 5V		
DSKCHG#	Disk change	I 5V		
HDSEL#	Head select	O 5V		
DIR#	Direction	O 5V		
STEP#	Motor step	O 5V		
DRV	Drive select	O 5V		
MOT#	Motor select	O 5V		
WDATA#	Raw write data	O 5V		
WGATE#	Write enable	O 5V		

**Table 18 Floppy Support Mode Pinout (not supported)**

Floppy Support Mode Pinout			
Pin	Signal	Pin	Signal
51	N.A.	52	RESERVED
53	VCC	54	GND
55	RESERVED	56	DENSEL
57	RESERVED	58	RESERVED
59	IRRX	60	HDSEL#
61	IRTX	62	RESERVED
63	RXD2	64	DIR#
65	GND	66	GND
67	RTS2#	68	RESERVED
69	DTR2#	70	STEP#
71	DCD2#	72	DSKCHG#
73	DSR2#	74	RDATA#
75	CTS2#	76	WP#
77	TXD2	78	TRK0#
79	RI2#	80	INDEX#
81	VCC	82	VCC
83	RXD1	84	DRV
85	RTS1#	86	MOT
87	DTR1#	88	WDATA#
89	DCD1#	90	WGATE#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

**Table 19 LPT Signal Descriptions**

Signal	Description of LPT signals (shared with FDC)	I/O	PU/PD	Comment
LPT	LPT Interface configuration input	I 3.3V	PU 10K	Not supported
STB#	Strobe signal	O 3.3V	PU 100K	
AFD#	Automatic feed	O 3.3V	PU 100K	
PD0	Data bus D0	I/O 3.3V	PU 100K	5V tolerant input
PD1	Data bus D1	I/O 3.3V	PU 100K	5V tolerant input
PD2	Data bus D2	I/O 3.3V	PU 100K	5V tolerant input
PD3	Data bus D3	I/O 3.3V	PU 100K	5V tolerant input
PD4	Data bus D4	I/O 3.3V	PU 100K	5V tolerant input
PD5	Data bus D5	I/O 3.3V	PU 100K	5V tolerant input
PD6	Data bus D6	I/O 3.3V	PU 100K	5V tolerant input
PD7	Data bus D7	I/O 3.3V	PU 100K	5V tolerant input
ERR#	LPT error	I 3.3V	PU 100K	5V tolerant input
INIT#	Initiate	O 3.3V	PU 100K	
SLIN#	Select	O 3.3V	PU 100K	
ACK#	Acknowledge	I 3.3V	PU 100K	5V tolerant input
BUSY	Busy	I 3.3V	PU 100K	5V tolerant input
PE	Paper empty	I 3.3V	PU 100K	5V tolerant input
SLCT	Power On	I 3.3V	PU 100K	5V tolerant input

**Table 20 LPT Support Mode Pinout**

Parallel Port Mode Pinout			
Pin	Signal	Pin	Signal
51	N.A.	52	RESERVED
53	VCC	54	GND
55	STB#	56	AFD#
57	RESERVED	58	PD7
59	IRRX	60	ERR#
61	IRTX	62	PD6
63	RXD2	64	INIT#
65	GND	66	GND
67	RTS2#	68	PD5
69	DTR2#	70	SLIN#
71	DCD2#	72	PD4
73	DSR2#	74	PD3
75	CTS2#	76	PD2
77	TXD2	78	PD1
79	RI2#	80	PD0
81	VCC	82	VCC
83	RXD1	84	ACK#
85	RTS1#	86	BUSY
87	DTR1#	88	PE
89	DCD1#	90	SLCT
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

## 7.6 X4 Connector Signal Descriptions

**Table 21 Signal Descriptions**

Signal	Description	I/O	Comment
VCC	Power Supply +5VDC, ±5%	I	external supply
GND	Power Ground	I	external supply
N.C.	Not connected	N.A.	Do not connect
PIDE	Refers to Primary IDE channel	I/O	
SIDE	Refers to Secondary IDE channel	I/O	

**Table 22 IDE Signal Descriptions**

Signal	Description of IDE signals	I/O	PU/PD	Comment
PIDE_D0..15	Primary IDE Data bus	I/O 3.3V		5V tolerant
PIDE_A0..2	Primary IDE Address bus	O 3.3V		
PIDE_CS1#	Primary IDE chip select channel 0	O 3.3V		
PIDE_CS3#	Primary IDE chip select channel 1	O 3.3V		
PIDE_DRQ	Primary IDE DMA request	I 3.3V		5V tolerant
PIDED_AK#	Primary IDE DMA acknowledge	O 3.3V		
PIDE_RDY	Primary IDE ready	I 3.3V		5V tolerant
PIDE_IOR#	Primary IDE IO read	O 3.3V		
PIDE_IOW#	Primary IDE IO write	O 3.3V		
PIDE_INTRQ	Primary IDE interrupt request	I 3.3V		5V tolerant
SIDE_D0..15	Secondary IDE Data bus	I/O 3.3V		5V tolerant
SIDE_A0..2	Secondary IDE Address bus	O 3.3V		
SIDE_CS1#	Secondary IDE chip select channel0	O 3.3V		
SIDE_CS3#	Secondary IDE chip select channel1	O 3.3V		
SIDE_DRQ	Secondary IDE DMA request	I 3.3V		5V tolerant
SIDED_AK#	Secondary IDE DMA acknowledge	O 3.3V		
SIDE_RDY	Secondary IDE ready	I 3.3V		5V tolerant
SIDE_IOR#	Secondary IDE IO read	O 3.3V		
SIDE_IOW#	Secondary IDE IO write	O 3.3V		
SIDE_INTRQ	Secondary IDE interrupt request	I 3.3V		5V tolerant
DASP_S	Secondary IDE Drive active	O 3.3V		
PDIAG_S	Secondary IDE 80 pin cable detect	I 3.3V		5V tolerant
HDRST#	Hard Drive reset	O 3.3V		
CBLID_P#	Primary IDE 80pin cable detect	I 3.3V		5V tolerant

**Table 23 Ethernet Signal Descriptions**

Signal	Description of Ethernet signals	I/O	PU/PD	Comment
TXD#, TXD	Ethernet transmit signal pair	O		Signals for external transformer
RXD#, RXD	Ethernet receive signal pair	I		Signals for external transformer
ACTLED#	Ethernet activity LED	O 3.3V		
LILED#	Ethernet link LED	O 3.3V		
SPEEDLED#	Ethernet speed LED, ON at 100Mb/s	O 3.3V		

**Table 24 Power Control Signals**

Signal	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	Power good input	I		Also usable as reset input, make low with O.C. to cause reset.
5V_SB	Supply of internal suspend circuit	P		
PS_ON#	ATX Power On	O		
PWRBTN#	Power Button	I		Pull low to switch ATX on

**Table 25 Power Management Signals**

Signal	Description of Power Management signals	I/O	PU/PD	Comment
RSMRST#	Standby voltage control	I/O 3.3V		Normally leave open
SMBALRT#	System management bus alert input	I 3.3V		
BATLOW#	Battery low input	I 3.3V		
GPE1#	General purpose power management event input 1	I 3.3V		
GPE2#	General purpose power management event input 2	I 3.3V		Ring indicator wake-up
EXTSMI#	System management interrupt input	I 3.3V		

**Table 26 Miscellaneous Signal Descriptions**

Signal	Description of Miscellaneous signals	I/O	PU/PD	Comment
SPEAKER	Speaker output	O 3.3V		
BATT	Battery supply	I (2.0 ... 3.6 V)		Power for RTC
I <sup>2</sup> CLK	I <sup>2</sup> C Bus clock	I/O 5V		
I <sup>2</sup> DAT	I <sup>2</sup> C Bus Data	I/O 5V		
SMBCLK	SM Bus clock	I/O 3.3V		
SMBDATA	SM Bus Data	I/O 3.3V		
KBINH#	Keyboard inhibit	N.A.		Not available
OVCR#	Over current detect for USB	I 3.3V	PU 10K	Pull low to generate USB over current event for OS
ROMKBCS#	Do not connect	N.A.		Not available
EXT_PRG	Do not connect	N.A.		Not available
GPCS#	General purpose chip select	N.A.		Not available

## 7.7 X4 Connector Pinout

**Table 27 Connector X4 Pinout**

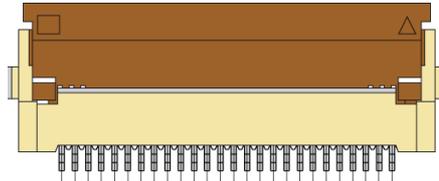
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	SIDE_IOW#	52	PIDE_IOR#
3	5V_SB	4	PWGIN	53	SIDE_DRQ	54	PIDE_IOW#
5	PS_ON#	6	SPEAKER	55	SIDE_D15	56	PIDE_DRQ
7	PWRBTN#	8	BATT	57	SIDE_D0	58	PIDE_D15
9	KBINH# (*)	10	LILED#	59	SIDE_D14	60	PIDE_D0
11	RSMRST#	12	ACTLED#	61	SIDE_D1	62	PIDE_D14
13	ROMKBCS# (*)	14	SPEEDLED#	63	SIDE_D13	64	PIDE_D1
15	EXT_PRG (*)	16	I2CLK	65	GND	66	GND
17	VCC	18	VCC	67	SIDE_D2	68	PIDE_D13
19	OVCR#	20	GPCS# (*)	69	SIDE_D12	70	PIDE_D2
21	EXTSMI#	22	I2DAT	71	SIDE_D3	72	PIDE_D12
23	SMBCLK	24	SMBDATA	73	SIDE_D11	74	PIDE_D3
25	SIDE_CS3#	26	SMBALRT#	75	SIDE_D4	76	PIDE_D11
27	SIDE_CS1#	28	DASP_S (*)	77	SIDE_D10	78	PIDE_D4
29	SIDE_A2	30	PIDE_CS3#	79	SIDE_D5	80	PIDE_D10
31	SIDE_A0	32	PIDE_CS1#	81	VCC	82	VCC
33	GND	34	GND	83	SIDE_D9	84	PIDE_D5
35	PDIAG_S	36	PIDE_A2	85	SIDE_D6	86	PIDE_D9
37	SIDE_A1	38	PIDE_A0	87	SIDE_D8	88	PIDE_D6
39	SIDE_INTRQ	40	PIDE_A1	89	GPE2#	90	CBLID_P#
41	BATLOW#	42	GPE1#	91	RXD#	92	PIDE_D8
43	SIDE_AK#	44	PIDE_INTRQ	93	RXD	94	SIDE_D7
45	SIDE_RDY	46	PIDE_AK#	95	TXD#	96	PIDE_D7
47	SIDE_IOR#	48	PIDE_RDY	97	TXD	98	HDRST#
49	VCC	50	VCC	99	GND	100	GND

 **Note**

*The signals marked with an asterisk symbol (\*) are not supported on the conga-EAF.*

## 7.8 DDI Connector X6

Connector and flat foil cable information for the DDI connector (X6) located on the bottom side of the conga-EAF.



- Connector type      Hirose 0.5mm Pitch Bottom Contact Type  
Order no.              FH12-26S-0.5SH
- FFC type              26 positions, 30cm length, 0.5mm pitch both ends opposite sides  
Manufacturer          YOUNGSHIN  
Order No.              MCAB26x300B05



*The fan2 connector on the conga-EEVAL Evaluation Board revision A1.1 obstructs and compresses the conga-EBRA Revision B.3 flat foil cable when the module is mounted on the Evaluation Board. This compression may bend, expose or possibly damage the flat foil cable.*

*congatec therefore recommends the use of the latest conga-EEVAL board revision A.1 (Part No. : 033269) or to alternatively remove the fan2 connector on the conga-EEVAL board revision A1.1.*

**Table 28      DDI Pinout Description**

Pin	Signal	Description	DP Mode	HDMI Mode
1	GND	Ground	Ground	Ground
2	DDI_TX0P	DDI Transmitter 0 Positive	ML_Lane 0(p)	TMDS Data 2+
3	DDI_TX0N	DDI Transmitter 0 Negative	ML_Lane 0(p)	TMDS Data 2-
4	GND	Ground	Ground	Ground
5	DDI_TX1P	DDI Transmitter 1 Positive	ML_Lane 1(p)	TMDS Data 1+
6	DDI_TX1N	DDI Transmitter 1 Negative	ML_Lane 1(p)	TMDS Data 1-
7	GND	Ground	Ground	Ground
8	DDI_TX2P	DDI Transmitter 2 Positive	ML_Lane 2(p)	TMDS Data 0+
9	DDI_TX2N	DDI Transmitter 2 Negative	ML_Lane 2(p)	TMDS Data 0-
10	GND	Ground	Ground	Ground
11	DDI_TX3P	DDI Transmitter 3 Positive	ML_Lane 3(p)	TMDS Clock+
12	DDI_TX3N	DDI Transmitter 3 Negative	ML_Lane 3(p)	TMDS Clock-
13	GND	Ground	Ground	Ground

Pin	Signal	Description	DP Mode	HDMI Mode
14	NC	Not connect	Not connect	Not connect
15	DDI_AUXP	DDI Auxiliary Transmitter Positive	AUX ch(p)	DDC Clock (SCL)
16	DDI_AUXN	DDI Auxiliary Transmitter Negative	AUX ch(n)	DDC Data (SDA)
17	GND	Ground	Ground	Ground
18	DDI_HPD	DDI Hot Plug Detect	Hot Plug Detect	Hot Plug Detect
19	SMB_DAT	SM Bus Data	SM Bus Data	SM Bus Data
20	SMB_CLK	SM Bus Clock	SM Bus Clock	SM Bus Clock
21	GND	Ground	Ground	Ground
22	GND	Ground	Ground	Ground
23	GND	Ground	Ground	Ground
24	VCC_3V3	Supply Voltage 3.3V	Supply Voltage 3.3V	Supply Voltage 3.3V
25	VCC_3V3	Supply Voltage 3.3V	Supply Voltage 3.3V	Supply Voltage 3.3V
26	VCC_5V0	Supply Voltage 5.0V	Supply Voltage 5.0V	Supply Voltage 5.0V

 **Note**

See section 9.4.1 how to configure appropriate mode of DDI (Digital Display Channel 1) supported on the conga-EAF.

## 7.9 Boot Strap Signals

**Table 29 Signal Descriptions**

Signal	Pin	Description of Boot Strap Signals	I/O	PU/PD	Comment
PCICLK2	X1_8	Clock output	O 3.3V	PU 10K 3.3V	
AEN	X2_82	ISA Address Enable	O 5V	PD 4.7K	
BALE	X2_42	ISA Address Latch Enable	O 5V	PD 4.7K	
TC	X2_44	ISA DMA end	O 5V	PD 4.7K	
TXD1	X3_95	Data transmit for COM1	O 3.3V	PU 1K 3.3V	
RTS1#	X3_85	Request to send for COM1	O 3.3V	PD 1K	
TXD2	X3_77	Data transmit for COM2	O 3.3V	PU 1K 3.3V	

 **Note**

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the module to malfunction and/or cause irreparable damage to the module.

## 8 System Resources

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### 8.1 I/O Address Assignment

The I/O address assignment of the conga-EAF module is functionally identical with a standard PC/AT.

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

#### 8.1.1 Onboard LPC Bus and External ISA Bus

On the conga-EAF the ISA Bus acts as the main subtractive decoding agent. All I/O cycles that are not positively decoded by PCI devices or onboard PCI Express devices are forwarded to the ISA Bus. However, specified I/O ranges are forwarded to the onboard LPC Bus only. In the congatec Embedded BIOS the following I/O address ranges are sent to the onboard LPC Bus and are thus not available on the ISA bus:

2Eh – 2Fh

4Eh – 4Fh

60h, 64h

2F8h -2FFh

378h – 37Fh

3F8h – 3FFh

778h – 77Fh

A00h – BFFh

## 8.2 Interrupt Request (IRQ) Lines

**Table 30** IRQ Lines in PIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Note 2	Serial Port 1 (COM2)	ISA IRQ3
4	Note 2	Serial Port 0 (COM1)	ISA IRQ4
5	Yes		ISA IRQ5
6	Yes		ISA IRQ6
7	Note 2	Parallel Port 1 (LPT1)	ISA IRQ7, PCI BUS INTx
8	No	Real-time Clock	Not applicable
9	No	SCI	Not applicable
10	Yes		ISA IRQ10, PCI BUS INTx
11	Yes		ISA IRQ11, PCI BUS INTx
12	No	PS/2 Mouse	Not applicable
13	No	Math processor	Not applicable
14	Note 1	IDE Controller 0 (IDE0) / Generic	ISA IRQ14, PCI BUS INTx
15	Note 1	IDE Controller 1 (IDE1) / Generic	ISA IRQ15, PCI BUS INTx

### Note

1. If the SATA interface mode configuration in BIOS setup is NOT set to legacy IDE mode IRQ14 and 15 are free for ISA bus.
2. If the respective onboard Super I/O device is disabled in BIOS, the interrupt can be used for ISA bus.

**Table 31 IRQ Lines in APIC mode**

IRQ#	Available	Typical Interrupt Source	Connected to Pin / Function
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Note 2	Serial Port 1 (COM2)	ISA IRQ3
4	Note 2	Serial Port 0 (COM1)	ISA IRQ4
5	Yes		ISA IRQ5
6	Yes		ISA IRQ6
7	Note 2	Parallel Port 1 (LPT1)	ISA IRQ7
8	No	Real-time Clock	Not applicable
9	No	SCI	Not applicable
10	Yes		ISA IRQ10
11	Yes		ISA IRQ11
12	No	PS/2 Mouse	Not applicable
13	No	Math processor	Not applicable
14	Note 1	IDE Controller 0 (IDE0) / Generic	ISA IRQ14
15	Note 1	IDE Controller 1 (IDE1) / Generic	ISA IRQ15
16	No		PIRQA, PCI Express Root Port 0/4/5/6, onboard LAN Controller, PCI Express Port 0 (see Note 2), Main High Definition Audio Controller
17	No		PIRQB, Addon PATA Controller 0, EHCI Host Controller 0, Chipset IDE Controller 1 (unused)
18	No		PIRQC, Addon PATA Controller 1, OHCI Host Controller 0, Integrated Graphics Controller
19	No		PIRQD, Chipset IDE Controller 0 (SATA), HDMI / DisplayPort HDA Controller (for HDMI/DisplayPort integrated audio only)
20	Yes		PIRQE, PCI BUS INTA
21	Yes		PIRQF, PCI BUS INTB
22	Yes		PIRQG, PCI BUS INTC
23	Yes		PIRQH, PCI BUS INTD

In APIC mode, the PCI bus interrupt lines are connected with IRQ 20, 21, 22 and 23.

 **Note**

1. If the SATA interface mode configuration in BIOS setup is NOT set to legacy IDE mode, then IRQs 14 and 15 are free for ISA bus.
2. If the respective onboard Super I/O device is disabled in BIOS, the interrupt can be used for ISA bus.

## 8.3 PCI Configuration Space Map

**Table 32 PCI Configuration Space Map**

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	01h	00h	Internal	Integrated Graphics Controller (VGA)
00h	01h	01h	Internal	HDMI / Display Port HDA Controller (for HDMI/Display Port integrated audio only)
00h	04h	00h	Internal	PCI Express Root Port 0
00h	11h	00h	Internal	Chipset IDE Controller 0 (SATA)
00h	12h	00h	Internal	OHCI Host Controller 0
00h	12h	02h	Internal	EHCI Host Controller 0
00h	14h	00h	N.A.	SMBus Host Controller
00h	14h	01h	Internal	Chipset IDE Controller 1 (unused)
00h	14h	02h	Internal	High Definition Audio Controller
00h	14h	03h	N.A.	PCI to LPC Bridge
00h	14h	04h	N.A.	PCI to PCI Bridge
00h	15h	00h	Internal	PCI Express Root Port 4
00h	15h	01h	Internal	PCI Express Root Port 5
00h	15h	02h	Internal	PCI Express Root Port 6
00h	18h	00h	N.A.	Chipset Configuration Registers
00h	18h	01h	N.A.	Chipset Configuration Registers
00h	18h	02h	N.A.	Chipset Configuration Registers
00h	18h	03h	N.A.	Chipset Configuration Registers
00h	18h	04h	N.A.	Chipset Configuration Registers
00h	18h	05h	N.A.	Chipset Configuration Registers
00h	18h	06h	N.A.	Chipset Configuration Registers
00h	18h	07h	N.A.	Chipset Configuration Registers
01h	02h	00h	N.A.	PCI to ISA Bridge
01h	03h	00h	INTA-INTD	PCI Bus Slot 1
01h	04h	00h	INTA-INTD	PCI Bus Slot 2
01h	05h	00h	INTA-INTD	PCI Bus Slot 3
01h	06h	00h	INTA-INTD	PCI Bus Slot 4
02h	00h	00h	Internal	Onboard LAN Controller
03h	00h	00h	Internal	Addon PATA Controller 0
04h	00h	00h	Internal	Addon PATA Controller 1

## 8.4 PCI Interrupt Routing Map

**Table 33 PCI Interrupt Routing Map**

PIRQ	PCI BUS INT Line <sup>1</sup>	APIC Mode IRQ	VGA	HDA (HDMI / DP)	OHCIO	EHCIO	IDE0 (SATA)	IDE1 (not used)	HDA (Main)
A		16							X
B		17				X		X	
C		18	X		X				
D		19		X			X		
E	INTA	20							
F	INTB	21							
G	INTC	22							
H	INTD	23							

**Table 34 PCI Interrupt Routing Map (continued)**

PIRQ	PCI-EX Root Port 0	PCI-EX Root Port 4	PCI-EX Root Port 5	PCI-EX Root Port 6	LAN	PATA0	PATA1
A	X	X	X	X	X		
B						X	
C							X
D							
E							
F							
G							
H							

 **Note**

<sup>1</sup> These interrupts are available for external devices/slots via the X1 connector.

## 8.5 PCI Bus Masters

The conga-EAF supports 4 external PCI Bus Masters. There are no limitations in connecting bus master PCI devices.

 **Note**

*If there are two devices connected to the same PCI REQ/GNT pair and they are transferring data at the same time then the latency time of these shared PCI devices can not be guaranteed.*

## **8.6 I<sup>2</sup>C Bus**

There are no onboard resources connected to the I<sup>2</sup>C bus. Address 16h is reserved for congatec Battery Management solutions.

## **8.7 SM Bus**

System Management (SM) bus signals are connected to the AMD Chipset and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

## 9 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

### 9.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <F2> key during POST.

#### 9.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used, a selection will be displayed immediately after POST allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

### 9.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:



#### Note

*Entries in the option column that are displayed in bold print indicate BIOS default values.*

Main	Advanced	Boot	Security	Save & Exit
------	----------	------	----------	-------------

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

## 9.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab.

The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
<b>BIOS Information</b>		
Main BIOS Version	no option	Displays the main BIOS version.
OEM BIOS Version	no option	Displays the additional OEM BIOS version.
Build Date	no option	Displays the date the BIOS was built
<b>Board Information</b>		
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
Running Time	no option	Displays the time the board is running [in hours max. 65535].
<b>Memory Information</b>		
Total Memory	no option	Displays amount of installed memory.
Memory Clock	no option	Displays current memory clock.
<b>CPU Information</b>		
	no option	Displays CPU type and feature information.
System Date	Day of week, month/day/year	Specifies the current system date. <i>Note: The date is in month-day-year format.</i>
System Time	Hour:Minute:Second	Specifies the current system time. <i>Note: The time is in 24-hour format.</i>

## 9.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Boot	Security	Save & Exit
	Graphics Configuration			
	Watchdog Configuration			
	PCI Configuration			
	ACPI Configuration			
	RTC Wake Settings			
	Trusted Computing Configuration			
	CPU Configuration			
	Chipset Configuration			
	Hardware Health Monitoring			
	SATA/PATA Configuration			
	USB Configuration			
	Super I/O Configuration			
	Serial Port Console Redirection			
	ISA Configuration			

## 9.4.1 Graphics Configuration Submenu

Feature	Options	Description
Primary Graphics Device	IGD <b>PCI</b>	Select primary graphics adapter to be used during boot up. IGD: Internal Graphics Device PCI: Try to use external standard PCI Graphics Device. If not present, IGD is used.
Integrated Graphics Device	<b>Auto Configuration</b> Disabled Manual Configuration	Deactivate IGD or select frame buffer configuration mode. In auto mode, the frame buffer size will be defined based on the amount of physical memory present.
IGD Frame buffer Size	32M 64M 128M <b>256M</b> 512M	Only visible if IGD is set to manual configuration. Set fixed graphics frame buffer size for IGD. The graphics driver might allocate additional memory.
Display Channel 0 Output	<b>LVDS</b> Disabled	Define output mode and connection of the integrated digital display channel 0.
Display Channel 1 Output	<b>Display Port</b> HDMI Disabled	Define output mode and connection of the integrated digital display channel 1. <i>Note: The different output options require different, additional hardware support. Thus not all options are available on all board variants.</i>
IGD Boot Display Device	<b>Auto</b> CRT Only Display Channel 0 Display Channel 1 CRT + Display Channel 0 CRT + Display Channel 1 Display Channel 0 + 1	Select the IGD display device(s) used for boot up.
Always Try Auto Panel Detect	<b>No</b> Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the LVDS flat panel output. Only if no external EDID data set can be found, the data set selected under 'Local Flat Panel Type' will be used as fallback data set.
Local Flat Panel Type	<b>Auto</b> VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 2x24 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I <sup>2</sup> C bus. The number in brackets specifies the congatec internal number of the respective panel data set. <i>Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.</i>
Backlight Inverter Type	<b>None</b> PWM I2C PWM (no ACPI)	Select the type of backlight inverter used. PWM = Use IGD PWM signal. I2C = Use I2C backlight inverter device connected to the video I <sup>2</sup> C bus.

Feature	Options	Description
		PWM (no ACPI) = Use IGD PWM signal; no ACPI interface provided.
PWM Inverter Frequency (Hz)	<b>200-40000</b>	Only visible if backlight Inverter Type is set to PWM. Set the PWM inverter frequency in Hertz.
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, <b>100%</b>	Actual backlight value in percent of the maximum setting.
Inhibit Backlight	<b>No</b> Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Setting	<b>No</b> Yes	Allow to invert backlight setting values if required for the actual backlight hardware controller.
LVDS SSC	<b>Disabled</b> Enabled	Enable or disable LVDS spread spectrum clock modulation.
SSC Modulation Frequency	<b>30kHz</b> 35kHz 40kHz	Select the LVDS SSC modulation frequency.
SSC Modulation Percentage	<b>0.25%</b> , 0.50%, 0.75%, 1.00%, 1.25%, 1.50%, 1.75%	Select the LVDS SSC modulation percentage.

## 9.4.2 Watchdog Configuration Submenu

Feature	Options	Description
POST Watchdog	<b>Disabled</b> 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog.  The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset..
Stop Watchdog For User Interaction	No <b>Yes</b>	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	<b>Disabled</b> One-time Trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to ' <i>One-time Trigger</i> ' the watchdog will be disabled after the first trigger. If set to ' <i>Single Event</i> ', every stage will be executed only once, then the watchdog will be disabled. If set to ' <i>Repeated Event</i> ' the last stage will be executed repeatedly until a reset occurs.
Delay	<b>Disabled</b> 10sec 30sec 1min 2min 5min 10min 30min	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	NMI ACPI Event <b>Reset</b> Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about <i>ACPI Event</i> see note below.
Event 2	<b>Disabled</b> NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	<b>Disabled</b> NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	1sec 2sec 5sec 10sec <b>30sec</b> 1min 2min 5min 10min 30min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.
Watchdog ACPI Event	<b>Shutdown</b> Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

## Note



In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

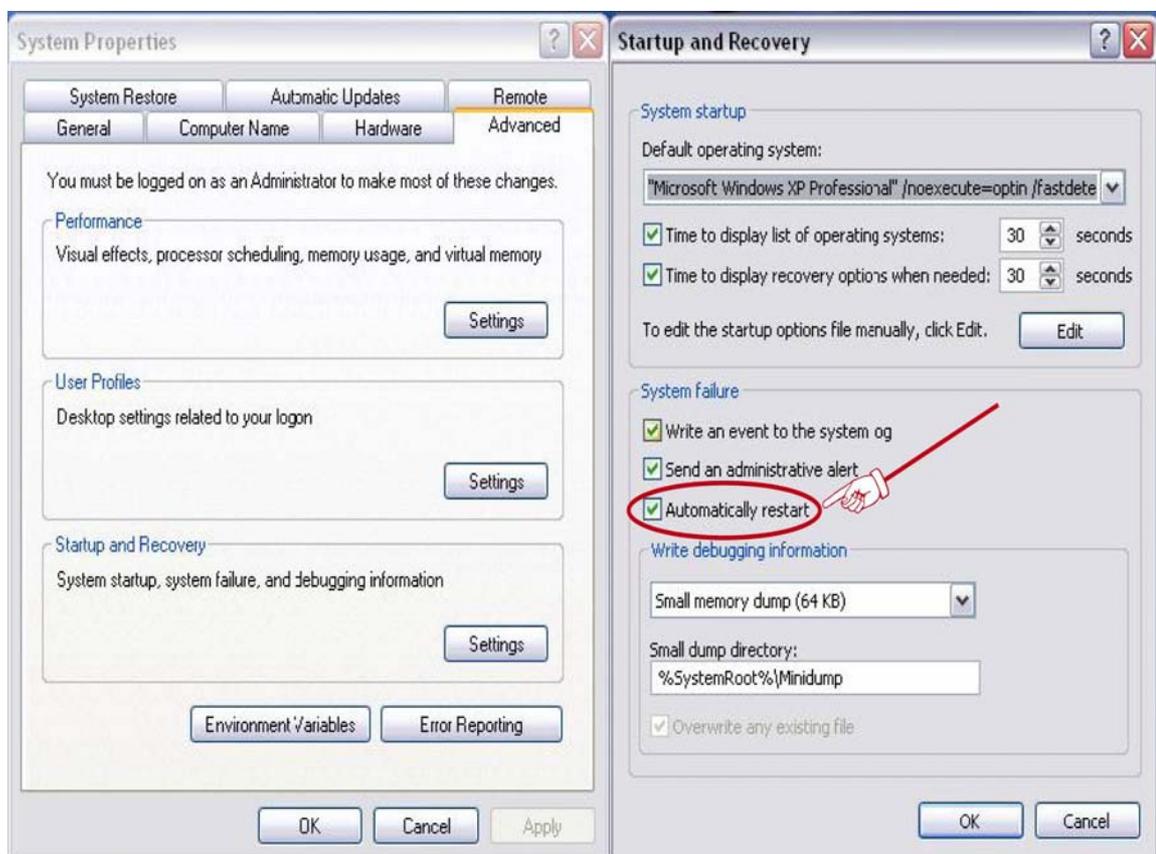
*For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.*

*For Restart: An ACPI fatal error is reported to the OS.*

*It depends on your particular OS as to how this reported fatal error will be handled when the Restart function is selected. If you are using Windows XP/2000 there is a setting that can be enabled to ensure that the OS will perform a restart when a fatal error is detected. After a very brief blue-screen the system will restart.*

*You can enable this setting by going to the "System Properties" dialog box and choosing the "Advanced" tab. Once there choose the "Settings" button for the "Startup and Recovery" section. This will open the "Startup and Recovery" dialog box. In this dialog box under "System failure" there are three check boxes that define what Windows will do when a fatal error has been detected. In order to ensure that the system restarts after a 'Watchdog ACPI Event' that is set to 'Restart', you must make sure that the check box for the selection "Automatically restart" has been checked. If this option is not selected then Windows will remain at a blue-screen after a 'Watchdog ACPI Event' that has been configured for 'Restart' has been generated. Below is a Windows screen-shot showing the proper configuration.*

## Win XP Watchdog ACPI Event restart configuration



### 9.4.3 PCI Configuration Submenu

Feature	Options	Description
PCI ROM Priority	Legacy ROM <b>EFI Compatible ROM</b>	Specify which PCI option ROM to launch in case that multiple option ROMs (legacy and EFI compatible) are present.
Launch PXE Option ROM	<b>Disabled</b> Enabled	Enable or disable start of PXE option ROMs for external legacy network devices.
Launch Storage Option ROM	Disabled <b>Enabled</b>	Enable or disable start of option ROMs for legacy mass storage devices.
<b>PCI Settings</b>		
PCI Latency Timer	<b>32</b> , 64, 96, 128, 160, 192, 224, 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
VGA Palette Snoop	<b>Disabled</b> Enabled	Enable or disable VGA palette registers snooping.
PERR# Generation	<b>Disabled</b> Enabled	Enable or disable PCI device SERR# generation.
SERR# Generation	<b>Disabled</b> Enabled	Enable or disable PCI device SERR# generation.
► PIRQ Routing	submenu	Opens the PIRQ routing submenu

#### 9.4.3.1 PIRQ Routing Submenu

Feature	Options	Description
PIRQA	<b>Auto</b> IRQ3 IRQ4 IRQ6 IRQ7 IRQ10 IRQ11 IRQ14 IRQ15	Set interrupt for selected PIRQ. Refer to board's resource list of devices connected to the respective PIRQ. <i>Note: These settings will only be effective while operating in PIC (non IOAPIC) interrupt mode.</i>
PIRQB	See above	See above
PIRQC	See above	See above
PIRQD	See above	See above
PIRQE (PCI INTA)	See above	See above
PIRQF (PCI INTA)	See above	See above
PIRQG (PCI INTA)	See above	See above
PIRQH (PCI INTA)	See above	See above

## 9.4.4 ACPI Configuration Submenu

Feature	Options	Description
Hibernation Support	Disabled <b>Enabled</b>	Enable or disable system ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled <b>S3 (Suspend to RAM)</b>	Select the state used for ACPI system sleep/suspend.
S3 Video Repost	<b>Disabled</b> Enabled	Enable or disable video BIOS re-post on S3 resume. Required by some operating systems.
USB Device Wake up From S3 or S4	Disabled <b>Enabled</b>	Enable or disable USB device wake up support from S3 or S4. Additional operating systems may be required as well.
Active Trip Point	Disabled, 20, 30, 40, 50, <b>60, 70, 80, 90, 95°C</b>	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Trip Point	Disabled, 60, 70, 80, 90, <b>95°C</b>	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.

## 9.4.5 RTC Wake Settings Submenu

Feature	Options	Description
Wake System At Fixed Time	<b>Disabled</b> Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour		Specify wake up hour.
Wake up minute		Specify wake up minute.
Wake up second		Specify wake up second.

## 9.4.6 Trusted Computing Configuration Submenu

Feature	Options	Description
TPM Support	<b>Disabled</b> Enabled	Enable or disable TPM support. System reset is required after change.
TPM State	<b>Disabled</b> Enabled	Enable or disable TPM chip. Note: System might restart several times during POST to acquire target state.
Pending TPM Operation	<b>None,</b> Enable Take Ownership, Disable Take Ownership, TPM Clear	Perform selected TPM chip operation. Note: System might restart several times during POST to perform selected operation.

### Note

*This setup menu only available if module is equipped with TPM chip.*

## 9.4.7 CPU Configuration Submenu

Feature	Options	Description
Limit CPUID Maximum	<b>Disabled</b> Enabled	When <b>enabled</b> , the processor will limit the maximum CPUID input value to <b>03h</b> when queried, even if the processor supports a higher CPUID input value. When <b>disabled</b> , the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
AMD PowerNow! Support	Disabled <b>Enabled</b>	Enable or disable support for AMD PowerNow! Technology. Allows operatins systems to control CPU performance states.
Maximum OS P-State	<b>P-State 0</b> P-State 1 P-State 2 P-State 3 P-State 4	Select the maximum CPU performance state the operating system should support. Higher numbers mean lower performance. P-state 0 is the highest performance state.
Maximum Power Up P-State	<b>P-State 0</b> P-State 1 P-State 2 P-State 3 P-State 4	Select the maximum CPU performance state to be set at power up. Higher numbers mean lower performance. P-State 0 is the highe
NX Mode	Disabled <b>Enabled</b>	Enable or disable the 'no-execute' page protection function.
Virtualization Technology	Disabled <b>Enabled</b>	When enabled, a Virtual Machine Manager (VMM) can utilize the integrated hardware virtualization support.
C6 Support	<b>Disabled</b> Enabled	Enable or disable CPU C6 low power state support.
Core Performance Boost	<b>Auto</b> Disabled	Controls usage of boosted CPU P-states, i.e. P-states above the standard CPU P-state limit. Availability of boosted P-states depends on CPU type and revision, actual usage on total CPU/GPU power consumption.

## 9.4.8 Chipset Configuration Submenu

Feature	Options	Description
Memory Bank Interleaving	<b>Disabled</b> Enabled	Enable or disable memory bank interleaving.
Memory Bus Clock	<b>Auto</b> 400MHz (DDR3-800) 533MHz (DDR3-1066)	Select or limit memory frequency.
HDA Controller	Auto Disabled <b>Enabled</b>	Control activation of the High Definition Audio controller.
HDMI/DP Audio Support	Disabled <b>Enabled</b>	Enable or disable HDMI/DisplayPort integrated audio support.
Onboard LAN	Disabled <b>Enabled</b>	Enable or disable the onboard Ethernet controller.
Launch Onboard LAN PXE ROM	<b>Disabled</b> Enabled	Enable or disable PXE option ROM execution of the onboard Ethernet controller.
UMI (NB to SB) PCIe Gen2 Support	Disabled <b>Enabled</b>	Enable or disable PCI Express generation 2 link speed for the UMI chipset interface.

## 9.4.9 Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	no option	Current CPU temperature.
Southbridge Temperature	no option	Current southbridge temperature.
Board Temperature	no option	Current board temperature.
DIMM Env. Temperature	no option	Current DIMM environment temperature.
5V Standard	no option	Current 5V input reading.
5V Standby	no option	Current 5V standby input reading.
Memory Voltage	no option	Current memory voltage reading.
CPU Fan Speed	no option	Current CPU fan speed reading.

## 9.4.10 SATA/PATA Configuration Submenu

Feature	Options	Description
SATA Controller	Disabled <b>Enabled</b>	Enable or disable the onboard SATA controller.
SATA Interface Mode	<b>Native IDE</b> RAID AHCI Legacy IDE	Select onboard SATA controller interface mode.
SATA Port 0	<b>Enabled</b> Disabled	Enable or disable selected port.
Port Speed	<b>Auto</b> Gen1 Gen2	Select SATA speed generation for the selected port.
SATA Port 1	<b>Enabled</b> Disabled	Enable or disable selected port.
Port Speed	<b>Auto</b> Gen1 Gen2	Select SATA speed generation for the selected port.
Primary PATA Controller	Disabled <b>Enabled</b>	Enable or disable the primary onboard PATA controller.
Maximum UDMA Mode	UDMA0 UDMA1 UDMA2 UDMA3 UDMA4 UDMA5 UDMA6	Allows to limit the UDMA mode that should be supported for drives connected to this controller.
Secondary PATA Controller	Disabled <b>Enabled</b>	Enable or disable the secondary onboard PATA controller.
Maximum UDMA Mode	UDMA0 UDMA1 UDMA2 UDMA3 UDMA4 UDMA5 UDMA6	Allows to limit the UDMA mode that should be supported for drives connected to this controller.

## 9.4.11 USB Configuration Submenu

Feature	Options	Description
USB Port 0	Disabled <b>Enabled</b>	Enable or disable selected port.
USB Port 1	Disabled <b>Enabled</b>	Enable or disable selected port.
USB Port 2	Disabled <b>Enabled</b>	Enable or disable selected port.
USB Port 3	Disabled <b>Enabled</b>	Enable or disable selected port.
USB Overcurrent Reporting	Disabled <b>Enabled</b>	Select whether activation of the USB overcurrent signals results in USB overcurrent register reporting and software event handling as well.
Legacy USB Support	<b>Enabled</b> Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
EHCI Hand-off	Disabled <b>Enabled</b>	This is a workaround for OSES without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
► Per-Port Legacy USB Support Control	submenu	Opens the Per-Port Legacy USB Support Control submenu
USB Transfer Timeout	1 sec 5sec 10 sec <b>20 sec</b>	Timeout value for legacy USB control, bulk and interrupt transfers.
Device Reset Timeout	10 sec <b>20 sec</b> 30 sec 40 sec	USB legacy mass storage device start unit command timeout.
Device Power-Up Delay Selection	<b>Auto</b> Manual	Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.
Device Power-Up Delay Value	<b>5</b> 1-40	Actual power-up delay value in seconds.
<i>USB Mass Storage Device Name</i>  <i>(Auto detected USB mass storage devices are listed here dynamically)</i>	<b>Auto</b> Floppy Forced FDD Hard Disk CD-ROM	Every USB mass storage device that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. <i>Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.</i> Select <i>AUTO</i> to let the BIOS auto detect the current formatted media. If <i>Floppy</i> is selected then the device will be emulated as a floppy drive. <i>Forced FDD</i> allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. <i>Hard Disk</i> allows the device to be emulated as hard disk. <i>CDROM</i> assumes the CD.ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

### 9.4.11.1 Per-Port Legacy USB Support Control Submenu

Feature	Options	Description
USB0 Port Legacy Support	Disabled <b>Enabled</b>	Enable or disable legacy USB support for this port. Enabled is only effective if the port is not disabled by another setting in the USB configuration menu.
USB1 Port Legacy Support	See above	See above
USB2 Port Legacy Support	See above	See above
USB3 Port Legacy Support	See above	See above

### 9.4.12 Super I/O Configuration Submenu

Feature	Options	Description
<b>Onboard Super I/O Configuration</b>		
Serial Port 0	Disabled <b>Enabled</b>	Enable or disable serial port 0.
<i>Device Settings</i>	<i>IO=3F8h; IRQ=4;</i>	<i>Fixed configuration of serial port 0 if enabled.</i>
Serial Port 1	Disabled <b>Enabled</b>	Enable or disable serial port 1.
<i>Device Settings</i>	<i>IO=2F8h; IRQ=3;</i>	<i>Fixed configuration of serial port 1 if enabled.</i>
Parallel Port	Disabled <b>Enabled</b>	Enable or disable parallel port.
<i>Device Settings</i>	<i>IO=378h; IRQ=7;</i>	<i>Fixed configuration of the parallel port if enabled.</i>
Device Mode	<b>Standard Parallel Mode</b> EPP Mode ECP Mode EPP Mode & ECP Mode	Set the parallel port mode.
<b>External Super IO Configuration (ISA bus Super IO SMSC 37C669)</b>		
Serial Port 0	<b>Disabled</b> Enabled	Enable or disable serial port 0.
<i>Device Settings</i>	<i>IO=3E8h; IRQ=10;</i>	<i>Fixed configuration of serial port 0 if enabled.</i>
Serial Port 1	<b>Disabled</b> Enabled	Enable or disable serial port 1.
<i>Device Settings</i>	<i>IO=2E8h; IRQ=11;</i>	<i>Fixed configuration of serial port 1 if enabled.</i>
Parallel Port	<b>Disabled</b> Enabled	Enable or disable parallel port.
<i>Device Settings</i>	<i>IO=278h; IRQ=5;</i>	<i>Fixed configuration of the parallel port if enabled.</i>
Device Mode	<b>Normal/Printer Mode</b> Bi-Directional Mode EPP Mode	Set the parallel port mode.

### 9.4.13 Serial Port Console Redirection

Feature	Options	Description
COM0 Console Redirection	<b>Disabled</b> Enabled	Enable or disable serial port 0 console redirection.
▶ Console Redirection Settings	submenu	Opens console redirection configuration sub menu.
COM1 Console Redirection	<b>Disabled</b> Enabled	Enable or disable serial port 0 console redirection.
▶ Console Redirection Settings	submenu	Opens console redirection configuration sub menu.

#### 9.4.13.1 Console Redirection Settings Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 <b>ANSI</b>	Select terminal type.
Baudrate	9600, 19200, 38400, 57600, <b>115200</b>	Select baudrate.
Data Bits	7, <b>8</b>	Set number of data bits.
Parity	<b>None</b> Even Odd Mark Space	Select parity.
Stop Bits	<b>1</b> 2	Set number of stop bits.
Flow Control	<b>None</b> Hardware RTS/CTS	Select flow control.
Recorder Mode	<b>Disabled</b> Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	<b>Disabled</b> Enabled	Enables or disables extended terminal resolution in UEFI environment.
Legacy OS Redirection Resolution	<b>80x24</b> 80x25	Number of rows and columns supported for legacy OS redirection.

## 9.4.14 ISA Configuration Submenu

Feature	Options	Description
ISA Decoding	<b>Subtractive Decoding</b> Positive Decoding	Select address decoding type of the onboard PCI-ISA bridge.
ISA Memory Hole 15MB-16MB	<b>Disabled</b> Enabled	Enable or disable the ISA memory hole between 15MB and 16MB.
▶ Distributed DMA Channels	submenu	Opens the distributed DMA configuration submenu
▶ ISA I/O Range Decoding	submenu	Opens the ISA I/O range configuration submenu (Only available when positive ISA decoding is selected.)
▶ ISA Memory Range Decoding	submenu	Opens the ISA memory range configuration submenu (Only available when positive ISA decoding is selected.)
Additional ISA Interrupt 1	None IRQ3 IRQ4 IRQ6 IRQ7 IRQ10 IRQ11 IRQ14 IRQ15	Reserve additional IRQ for ISA bus. IRQ5 is always available for ISA, IRQ9 never. IRQ3, IRQ4 and IRQ7 may only be used for ISA when the onboard Super I/O devices are disabled.
Additional ISA Interrupt 2	None IRQ3 IRQ4 IRQ6 IRQ7 IRQ10 IRQ11 IRQ14 IRQ15	Reserve additional IRQ for ISA bus. IRQ5 is always available for ISA, IRQ9 never. IRQ3, IRQ4 and IRQ7 may only be used for ISA when the onboard Super I/O devices are disabled.
Additional ISA Interrupt 3	None IRQ3 IRQ4 IRQ6 IRQ7 IRQ10 IRQ11 IRQ14 IRQ15	Reserve additional IRQ for ISA bus. IRQ5 is always available for ISA, IRQ9 never. IRQ3, IRQ4 and IRQ7 may only be used for ISA when the onboard Super I/O devices are disabled.

### 9.4.14.1 Distributed DMA Channels Submenu

Feature	Options	Description
DDMA Support	<b>Disabled</b> Enabled	Enable or disable Distributed DMA (DDMA) support. The DDMA implementation uses SMIs to emulate ISA DMA. This might not be adequate for real time systems !
DDMA Slave Channel 0	Disabled <b>Enabled</b>	Enable or disable DMA channel 0 emulation.
DDMA Slave Channel 1	Disabled <b>Enabled</b>	Enable or disable DMA channel 1 emulation.
DDMA Slave Channel 2	Disabled <b>Enabled</b>	Enable or disable DMA channel 2 emulation.
DDMA Slave Channel 3	Disabled <b>Enabled</b>	Enable or disable DMA channel 3 emulation.
DDMA Slave Channel 4	Disabled <b>Enabled</b>	Enable or disable DMA channel 4 emulation.
DDMA Slave Channel 5	Disabled <b>Enabled</b>	Enable or disable DMA channel 5 emulation.
DDMA Slave Channel 6	Disabled <b>Enabled</b>	Enable or disable DMA channel 6 emulation.
DDMA Slave Channel 7	Disabled <b>Enabled</b>	Enable or disable DMA channel 7 emulation.

### 9.4.14.2 ISA I/O Range Decoding Submenu

Feature	Options	Description
I/O Range 0	Disabled <b>Enabled</b>	Enable postive ISA bus decoding of I/O range 0.
I/O Decoding Speed	Subtractive Speed Slow Speed <b>Medium Speed</b> Fast Speed	Select decoding speed for this I/O range.
I/O Decoding Base Address	<b>100</b> (0-FFFFh)	Select hexadecimal base address of this I/O range.
I/O Decoding Size	1, 2, 4, 8, 16, 32, 64, <b>128</b> Byte	Select size of this I/O range.
I/O Range 1	Disabled <b>Enabled</b>	Enable postive ISA bus decoding of I/O range 1.
I/O Decoding Speed	Subtractive Speed Slow Speed <b>Medium Speed</b> Fast Speed	Select decoding speed for this I/O range.
I/O Decoding Base Address	<b>180</b> (0-FFFFh)	Select hexadecimal base address of this I/O range.
I/O Decoding Size	1, 2, 4, 8, 16, 32, <b>64</b> , 128 Byte	Select size of this I/O range.
I/O Range 2	Disabled	Enable postive ISA bus decoding of I/O range 2.

Feature	Options	Description
	<b>Enabled</b>	
I/O Decoding Speed	Subtractive Speed Slow Speed <b>Medium Speed</b> Fast Speed	Select decoding speed for this I/O range.
I/O Decoding Base Address	<b>1C0</b> (0-FFFFh)	Select hexadecimal base address of this I/O range.
I/O Decoding Size	1, 2, 4, 8, 16, <b>32</b> , 64, 128 Byte	Select size of this I/O range.
I/O Range 3	Disabled <b>Enabled</b>	Enable postive ISA bus decoding of I/O range 3.
I/O Decoding Speed	Subtractive Speed Slow Speed <b>Medium Speed</b> Fast Speed	Select decoding speed for this I/O range.
I/O Decoding Base Address	<b>200</b> (0-FFFFh)	Select hexadecimal base address of this I/O range.
I/O Decoding Size	1, 2, 4, 8, 16, 32, 64, <b>128</b> Byte	Select size of this I/O range.
I/O Range 4	Disabled <b>Enabled</b>	Enable postive ISA bus decoding of I/O range 4.
I/O Decoding Speed	Subtractive Speed Slow Speed <b>Medium Speed</b> Fast Speed	Select decoding speed for this I/O range.
I/O Decoding Base Address	<b>300</b> (0-FFFFh)	Select hexadecimal base address of this I/O range.
I/O Decoding Size	1, 2, 4, 8, 16, 32, <b>64</b> , 128 Byte	Select size of this I/O range.
I/O Range 5	Disabled <b>Enabled</b>	Enable postive ISA bus decoding of I/O range 5.
I/O Decoding Speed	Subtractive Speed Slow Speed <b>Medium Speed</b> Fast Speed	Select decoding speed for this I/O range.
I/O Decoding Base Address	<b>340</b> (0-FFFFh)	Select hexadecimal base address of this I/O range.
I/O Decoding Size	1, 2, 4, 8, 16, <b>32</b> , 64, 128 Byte	Select size of this I/O range.

### 9.4.14.3 ISA Memory Range Decoding Submenu

Feature	Options	Description
Memory Range 0	Disabled <b>Enabled</b>	Enable positive ISA bus decoding of memory range 0.
Memory Decoding Speed	Subtractive Speed Slow Speed <b>Medium Speed</b> Fast Speed	Select decoding speed for this memory range.
Memory Decoding Base Address	<b>D00</b> (0-FFFFh)	Select hexadecimal memory range decoding base address address bits [23:8].
Memory Decoding Size	16 KB, 32 KB, <b>64 KB</b> , 128 KB, 256 KB, 512 KB, 1 MB, 2 MB	Select size of this memory range.
Memory Range 1	<b>Disabled</b> Enabled	Enable positive ISA bus decoding of memory range 1.
Memory Decoding Speed	Subtractive Speed Slow Speed <b>Medium Speed</b> Fast Speed	Select decoding speed for this memory range.
Memory Decoding Base Address	<b>0</b> (0-FFFFh)	Select hexadecimal memory range decoding base address address bits [23:8].
Memory Decoding Size	16 KB, <b>32 KB</b> , 64 KB, 128 KB, 256 KB, 512 KB, 1 MB, 2 MB	Select size of this memory range.
Memory Range 2	<b>Disabled</b> Enabled	Enable positive ISA bus decoding of memory range 2.
Memory Decoding Speed	Subtractive Speed Slow Speed <b>Medium Speed</b> Fast Speed	Select decoding speed for this memory range.
Memory Decoding Base Address	<b>0</b> (0-FFFFh)	Select hexadecimal memory range decoding base address address bits [23:8].
Memory Decoding Size	16 KB, <b>32 KB</b> , 64 KB, 128 KB, 256 KB, 512 KB, 1 MB, 2 MB	Select size of this memory range.
Memory Range 3	<b>Disabled</b> Enabled	Enable positive ISA bus decoding of memory range 3.
Memory Decoding Speed	Subtractive Speed Slow Speed <b>Medium Speed</b> Fast Speed	Select decoding speed for this memory range.
Memory Decoding Base Address	<b>0</b> (0-FFFFh)	Select hexadecimal memory range decoding base address address bits [23:8].
Memory Decoding Size	16 KB, <b>32 KB</b> , 64 KB, 128 KB, 256 KB, 512 KB, 1 MB, 2 MB	Select size of this memory range.

## 9.5 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

### 9.5.1 Boot Settings Configuration

Feature	Options	Description
Quiet Boot	<b>Disabled</b> Enabled	<i>Disabled</i> displays normal POST diagnostic messages. <i>Enabled</i> displays OEM logo instead of POST messages. <i>Note: The default OEM logo is a dark screen.</i>
Setup Prompt Timeout	<b>1</b> 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot, 65535 means infinite wait.
POST/Setup VGA Support	<b>Disabled</b> Enabled	Select VGA mode for setup and POST screen. Enables setup and POST screen output support for VGA and WVGA display resolutions.
Bootup NumLock State	<b>On</b> Off	Select the keyboard numlock state.
Enter Setup If No Boot Device	No <b>Yes</b>	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No <b>Yes</b>	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based <b>Type Based</b>	Select between device and type based boot priority lists. The "Device Based" boot priority list allows you to select from a list of currently detected devices only. The "Type Based" boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the "Device Based" boot priority list might change dynamically in cases when devices are physically removed or added to the system. The "Type Based" boot menu is static and can only be changed by the user.
1st, 2nd, 3rd, ... Boot Device  (Up to 12 boot devices can be prioritized if device based priority list control is selected. If "Type Based" priority list control is enabled only 8 boot devices can be prioritized.)	Disabled SATA 0 Drive SATA 1 Drive Primary PATA Master Primary PATA Slave Secondary PATA Master Secondary PATA Slave USB Floppy USB Hard disk USB CDROM Onboard LAN External LAN Other BEV Device OEM BEV Device	This view is only available when in the default "Type Based" mode.  When in "Device Based" mode you will only see the devices that are currently connected to the system.
Power Loss Control	<b>Remain Off</b> Turn On Last State	Specifies the mode of operation if an AC power loss occurs. <i>Remain Off</i> keeps the power off until the power button is pressed. <i>Turn On</i> restores power to the computer. <i>Last State</i> restores the previous power state before power loss occurred. <i>Note: Only works with an ATX type power supply.</i>
AT Shutdown Mode	<b>System Reboot</b> Hot S5	Determines the behavior of an AT-powered system after a shutdown.
System Off Mode	<b>G3/Mech Off</b> S5/Soft Off	Define system state after shutdown when a battery system is present.
GateA20 Active	<b>Upon Request</b> Always	Gate A20 control. Upon Request = Gate A20 can be disabled using BIOS services. Always = Do not allow disabling Gate A20

Feature	Options	Description
Option ROM Messages	<b>Force BIOS</b> Keep Current	Set display mode for option ROMs.
Interrupt 19 Capture	<b>Disabled</b> Enabled	Defines whether option ROMs may trap the INT19h legacy boot vector.

### Note

1. The term 'AC power loss' stands for the state when the module loses the standby voltage on the 5V<sub>SB</sub> pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.
2. Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS\_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.

## 9.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

### 9.6.1 Security Settings

Feature	Options	Description
Administrator Password	enter password	Specifies the setup administrator password.
<b>HDD Security Configuration</b>		
List of all detected harddisks supporting the security feature set	Select device to open device security configuration submenu	

### 9.6.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

### 9.6.3 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen.

You can display an Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
<b>Save Options</b>	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.
<b>Boot Override</b>	
<i>List of all boot devices currently detected</i>	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to "Device Based".

## 10 Additional BIOS Features

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The conga-EAF uses a congatec/AMI Aptio UEFI firmware that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as EBRA1xx where EBRA is the congatec internal project name, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

### 10.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” please refer to the user's guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at [www.congatec.com](http://www.congatec.com).

### 10.2 BIOS Security Features

The BIOS provides a setup administrator password that limits access to the BIOS setup menu.

### 10.3 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to 'lock' and 'unlock' drives using the security password. A 'locked' drive will be detected by the system, but no data can be accessed. Accessing data on a 'locked' drive requires the proper password to 'unlock' the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within five attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA

security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

## 11 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
ETX® Specification Rev. 3.02	<a href="http://www.etx-ig.de/specs/specs.php">http://www.etx-ig.de/specs/specs.php</a>
Audio Codec '97 Component Specification, Version 2.3 (AC '97)	<a href="http://www.intel.com/design/chipsets/audio/">http://www.intel.com/design/chipsets/audio/</a>
Low Pin Count Interface Specification, Revision 1.0 (LPC)	<a href="http://developer.intel.com/design/chipsets/industry/lpc.htm">http://developer.intel.com/design/chipsets/industry/lpc.htm</a>
Universal Serial Bus (USB) Specification, Revision 2.0	<a href="http://www.usb.org/home">http://www.usb.org/home</a>
PCI Specification, Revision 2.2	<a href="http://www.pcisig.com/specifications">http://www.pcisig.com/specifications</a>
Serial ATA Specification, Revision 1.0a	<a href="http://www.serialata.org">http://www.serialata.org</a>
Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003	<a href="http://www.acpi.info">http://www.acpi.info</a>
Information Technology AT Attachment with Packet Interface -5 (ATA/ATAPI-5) Revision 3, February 29, 2000	<a href="http://www.t13.org">http://www.t13.org</a>